MA009A

24-bit I/O extender with interrupt function

Features

- Operation voltage: 2.0V to 5.7V
- Low standby current (1uA, typ.)
- 2 Mbps, 3-wire serial interface
- 8 chip addresses are provided
- 24 input/output pins
- 16 input pins with pull-high disable/enable and interrupt function
- 16 output pins with CMOS/NMOS, large/small sink capability

Selection Information

	MA009AH	MA009AP	MA009AD	MA009AF
Package / Dice	Dice	44-PLCC	48-LQFP	44-PQFP
Parallel Input	8 pins			
Parallel Output	8 pins			
Parallel I/O	8 pins			
Max. Sink Current	20mA			

Application Field

System I/O port

LED status indicator

2006/09 version A1

MEGAWIN

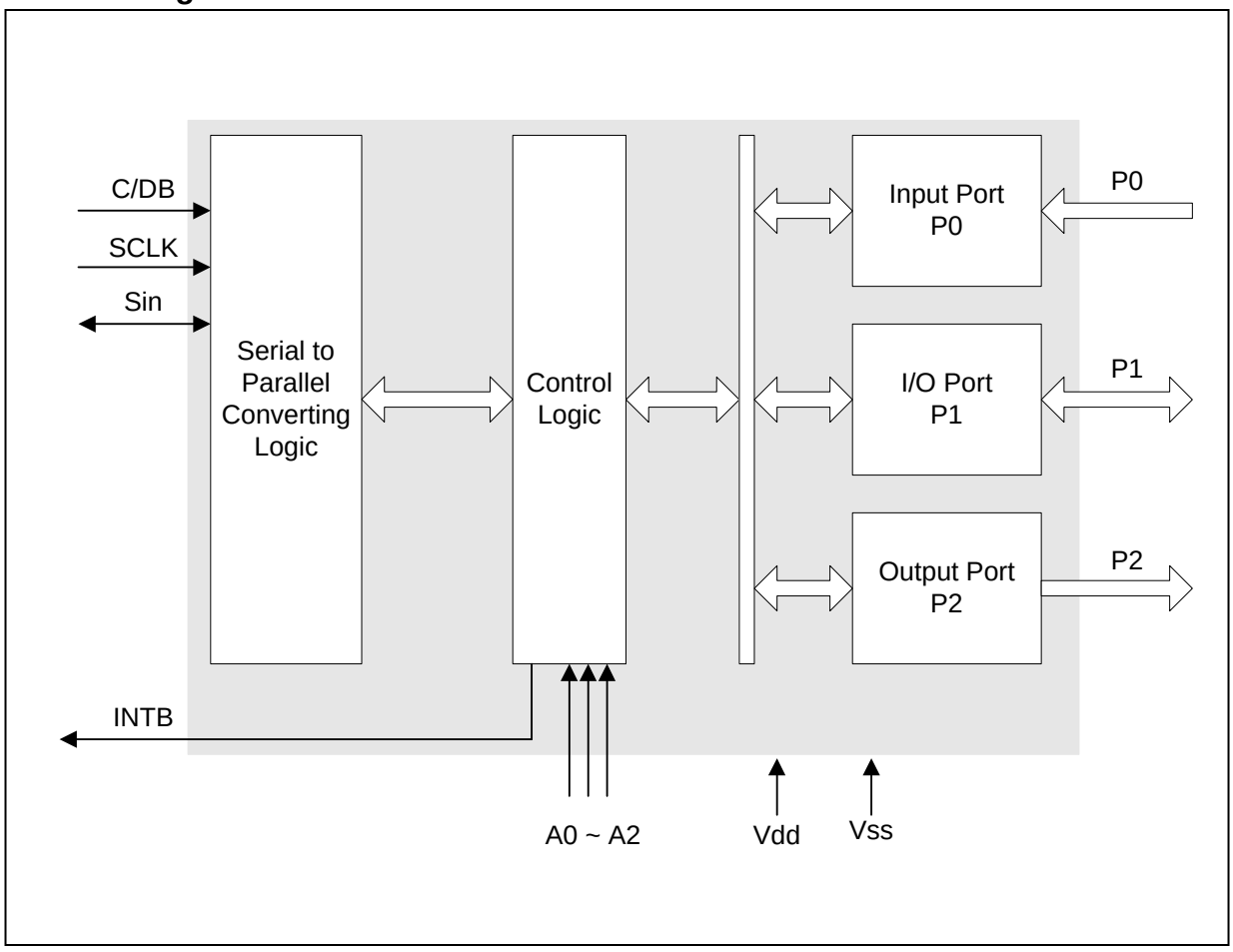
General Description

The MA009 is high-speed Si-gate CMOS devices that provide a general purpose I/O peripheral. The MA009 provides microcontroller eight input pins plus eight I/O pins and eight output pins. Each input pin can be configured as interrupt source and output pin can be configured as CMOS/NMOS output. The MA009 is controlled through a 3-wire serial interface, and can be set as one of eight chip addresses by pin option. The device is optimized for use in many commercial and industrial applications where high density, low pin count, low voltage, and low power are essential.

Pad Description

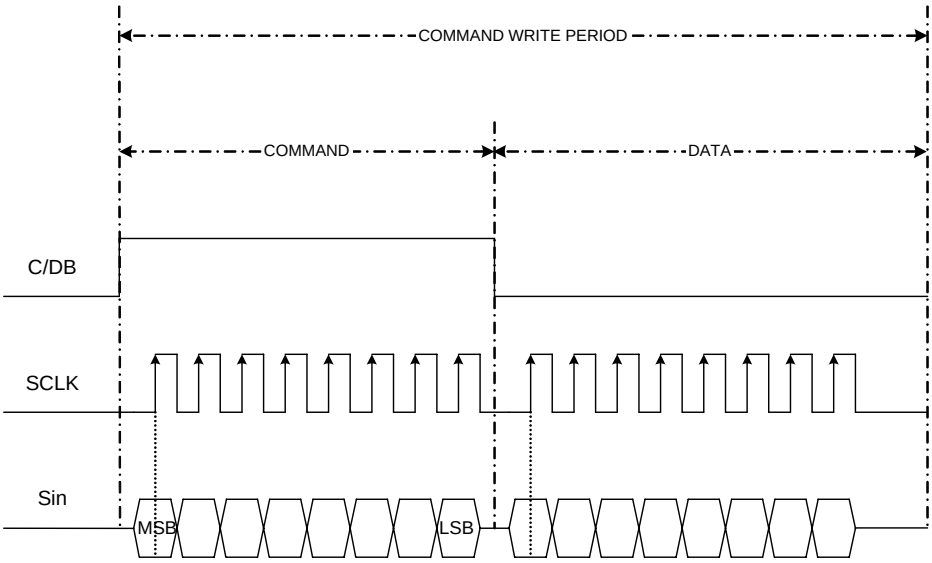
Pad No.	Pad Name	I/O	Description
1, 8, 9	NC	I	No connection
2, 3, 4	A0, A1, A2	I	Chip Address bit0, bit1, bit2
5	C/DB	I	Serial interface, command/data selector
6	SCLK	I	Serial interface, serial clock
7	Sin	I	Serial interface, serial command/data input
10	INTB	O	Input port interrupt event indicator
20 to 13	P_{20} to P_{27}	O	Output Port 2
29 to 22	P_{10} to P_{17}	O	Input/Output Port 1
38 to 31	P_{00} to P_{07}	O	Input Port 0
12, 30, 40, 41	V_{CC}	P	Positive supply voltage
11, 21, 39	GND	P	Power ground (0 V)

Block Diagram

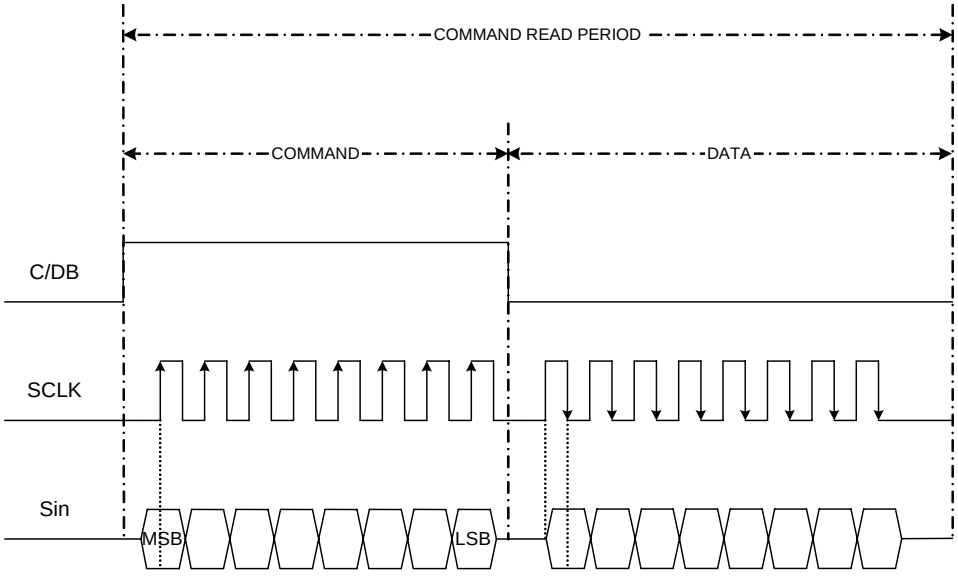


Function Description

There are three 8-bit I/O ports (P0 is pure input port, P1 is I/O port and P2 is pure output port) and one interrupt output pin (INTB) in MA009. The MA009 operates as a slave that sends and receives data through a 3-wire interface. The interface uses a command/data select line (C/DB); serial command/data line (Sin) and a serial clock line (SCLK) to achieve bidirectional communication between master(s) and slave(s). The master (such as microcontroller) should send serial clock and serial command to configure or to get data from MA009. The serial communication waveform are shown as below:



Command Write Period Waveform (command should be ready in rising edge)



Command Read Period Waveform (master can get data in falling edge)

Control Registers Definition

The default value of all the control register is 0 after power on.

Chip Address

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
C_ADDR	-	-	-	-	-	A02	A01	A00

Chip address register.

Only the contents of chip address register are same as chip address pin A2, A1 and A0, all command could be enabled. This function will make the master to connect more than one MA009 easily.

Input Port 0

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P0	P07	P06	P05	P04	P03	P02	P01	P00

Port P0 input status register.

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P0PR	-	-	-	-	-	-	PR01	PR00

Port P0 pull high control register.

P0PR.0: P0.0 ~ P0.3 pull high control, 0: enable (large resistance, 350K), 1: disable

P0PR.1: P0.4 ~ P0.7 pull high control, 0: enable (large resistance, 350K), 1: disable

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P0PSR	-	-	-	-	-	-	PS01	PS00

Port P0 strong pull high selection register.

P0PSR.0: P0.0 ~ P0.3 strong pull high selection, 0: disable, 1: enable (small resistance, 50K)

P0PSR.1: P0.4 ~ P0.7 strong pull high selection, 0: disable, 1: enable (small resistance, 50K)

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P0IEN	IE07	IE06	IE05	IE04	IE03	IE02	IE01	IE00

Port P0 interrupts enable register.

P0IEN.0 ~ P0IEN.7: P0.0 ~ P0.7 falling edge interrupts control, 0: disable, 1: enable

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P0EVT	ST07	ST06	ST05	ST04	ST03	ST02	ST01	ST00

Port P0 interrupts events status register.

When a falling edge signal is occurs in any interrupt enabled (the bit 0 or bit 1 of P0IEN is set to 1) pins of port P0, the corresponding bit of P0EVT will be set to 1. The interrupt will be generated from the INTB (1→0) pin in this condition, and the mater (for example, a microcontroller) can read the interrupt status from P0EVT. The master can send EVTCLR (13H) command to MA009 to clear the P0EVT after the interrupt event is processed. This

function will make the mater to expand interrupt pins very easily.

I/O Port 1

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P1	P17	P16	P15	P14	P13	P12	P11	P10

Port P1 input or output status register.

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P1CR	-	-	-	-	-	-	CR11	CR10

Port P1 I/O control register.

P1CR.0: P1.0 ~ P1.3 is input or output, 0: input, 1: output

P1CR.1: P1.4 ~ P1.7 is input or output, 0: input, 1: output

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P1POR	-	-	-	-	-	-	PO11	PO10

Port P1 pull high/output mode control register.

If P1CR.x == 0 (input mode)

P1POR.0: P1.0 ~ P1.3 pull high control, 0: enable (large resistance, 350K), 1: disable

P1POR.1: P1.4 ~ P1.7 pull high control, 0: enable (large resistance, 350K), 1: disable

If P1CR.x == 1 (output mode)

P1POR.0: P1.0 ~ P1.3 CMOS/NMOS selector, 0: CMOS, 1: NMOS

P1POR.1: P1.4 ~ P1.7 CMOS/NMOS selector, 0: CMOS, 1: NMOS

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P1PSR	-	-	-	-	-	-	PS11	PS10

Port P1 strong pull high selection register.

If P1CR.x == 0 (input mode)

P1PSR.0: P1.0 ~ P1.3 strong pull high control, 0: disable, 1: enable (small resistance, 50K)

P1PSR.1: P1.4 ~ P1.7 strong pull high control, 0: disable, 1: enable (small resistance, 50K)

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P1SCR	-	-	-	-	-	-	SC11	SC10

Port P1 sink control register.

If P1CR.x == 1 (output mode)

P1SCR.0: P1.0 ~ P1.3 output sink ability control, 0: weak, 1: strong (large sink current)

P1SCR.1: P1.4 ~ P1.7 output sink ability control, 0: weak, 1: strong (large sink current)

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P1IEN	IE17	IE16	IE15	IE14	IE13	IE12	IE11	IE10

Port P1 interrupts enable register.

If P1CR.x == 0 (input mode)

P1IEN.0 ~ P1IEN.7: P1.0 ~ P1.7 falling edge interrupts control, 0: disable, 1: enable

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P1EVT	ST17	ST16	ST15	ST14	ST13	ST12	ST11	ST10

Port P1 interrupts events status register.

This function is same as port P0. When a falling edge signal is occurs in any interrupt enabled (the bit 0 or bit 1 of P1IEN is set to 1) pins of port P1, the corresponding bit of P1EVT will be set to 1. The interrupt will be generated from the INTB (1→0) pin in this condition, and the mater (for example, a microcontroller) can read the interrupt status from P1EVT. The master can send EVTCLR (13H) command to MA009 to clear the P1EVT after the interrupt event is processed.

Output Port 2

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P2	P27	P26	P25	P24	P23	P22	P21	P20

Port P2 output status register.

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P2OR	-	-	-	-	-	-	OR21	OR20

Port P2 output mode control register

P2OR.0: P2.0 ~ P2.3 CMOS/NMOS selector, 0: CMOS, 1: NMOS

P2OR.1: P2.4 ~ P2.7 CMOS/NMOS selector, 0: CMOS, 1: NMOS

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P2SCR	-	-	-	-	-	-	SC21	SC20

Port P2 sink control register.

P2SCR.0: P2.0 ~ P2.3 output sink ability control, 0: weak, 1: strong (large sink current)

P2SCR.1: P2.4 ~ P2.7 output sink ability control, 0: weak, 1: strong (large sink current)

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P2PR	-	-	-	-	-	-	PR21	PR20

Port P2 pull high control register.

P2PR.0: P2.0 ~ P2.3 pull high control, 0: enable (large resistance, 350K), 1: disable

P2PR.1: P2.4 ~ P2.7 pull high control, 0: enable (large resistance), 1: disable

Command Definition

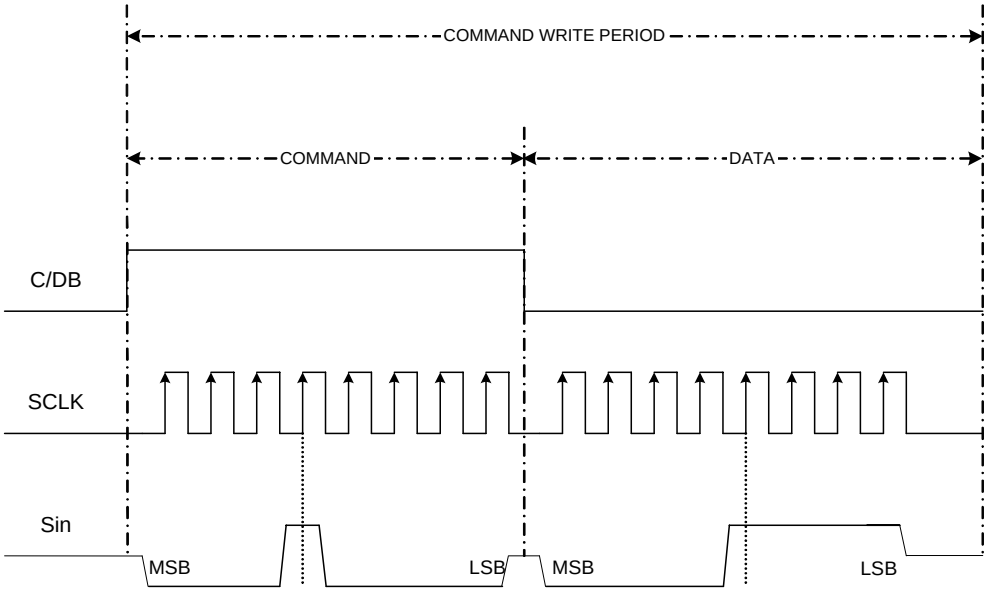
Instruction	OPCODE	Operand1	Data	Comments
C_RES	FEFFH			Software chip reset, all register value will be reset to 0 (default value).
C_EVTCLR	13H			Clear all event, P0EVT and P1EVT will be cleared.
W_ADDR	FDH	8-bit data		Write chip address, must match the pin status of A2 ~A0 to enable MA009.
Input port P0				
W_P0PR	04H	8-bit data		Write P0PR (pull high control register)
W_P0PSR	0AH	8-bit data		Write P0PSR (strong pull high selection register)
W_P0IEN	10H	8-bit data		Write P0IEN (interrupts enable register)
R_P0	3DH		8-bit data (R)	Read P0
R_P0PR	34H		8-bit data (R)	Read P0PR
R_P0PSR	3AH		8-bit data (R)	Read P0PSR
R_P0EVT	43H		8-bit data (R)	Read P0EVT (interrupts events status register)
I/O port P1				
W_P1	0EH	8-bit data		Write P1
W_P1CR	02H	8-bit data		Write P1CR (I/O control register)
W_P1POR	05H	8-bit data		Write P1POR (pull high/output mode control register)
W_P1PSR	0BH	8-bit data		Write P1PSR
W_P1SCR	08H	8-bit data		Write P1SCR (sink control register)
W_P1IEN	11H	8-bit data		Write P1IEN
R_P1	3EH		8-bit data (R)	Read P1
R_P1CR	32H		8-bit data (R)	Read P1CR
R_P1POR	35H		8-bit data (R)	Read P1POR
R_P1PSR	3BH		8-bit data (R)	Read P1PSR
R_P1SCR	38H		8-bit data (R)	Read P1SCR
R_P1EVT	44H		8-bit data (R)	Read P1EVT
Output port P2				
W_P2	0FH	8-bit data		Write P2
W_P2OR	06H	8-bit data		Write P2OR (output mode control register)
W_P2SCR	09H	8-bit data		Write P2SCR
W_P2PR	0CH	8-bit data		Write P2PR
R_P2OR	36H		8-bit data (R)	Read P2OR
R_P2SCR	39H		8-bit data (R)	Read P2SCR
R_P2PR	3CH		8-bit data (R)	Read P2PR

The command should be sent from MSB to LSB, and the signal must be stable in clock rising edge.

Command waveform example:

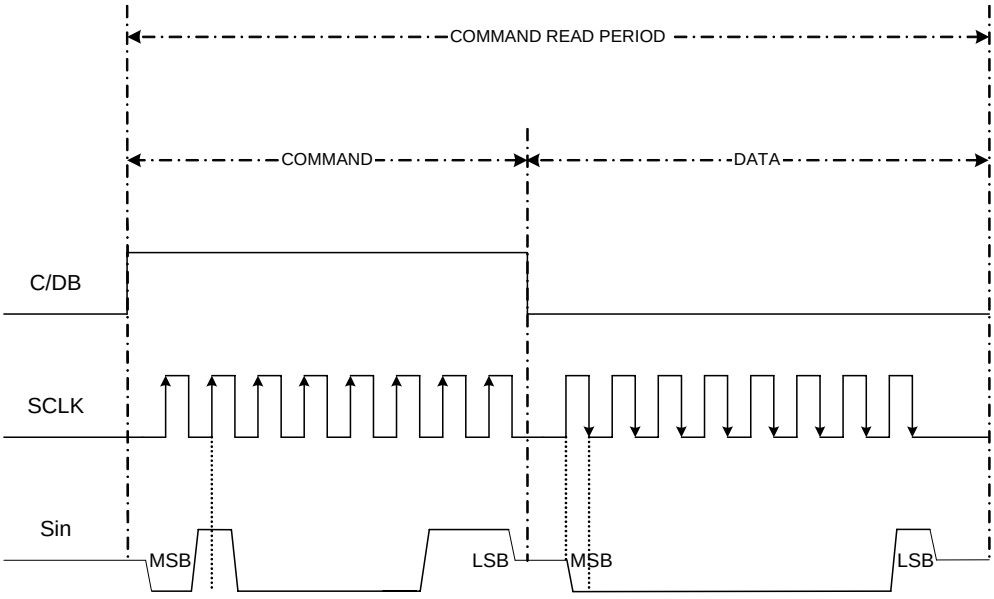
If we want to set the P0.0~P0.3 as interrupt source, then we can write 0FH into P0IEN register.

All the signals are sent MA009 by master(s) in this case.

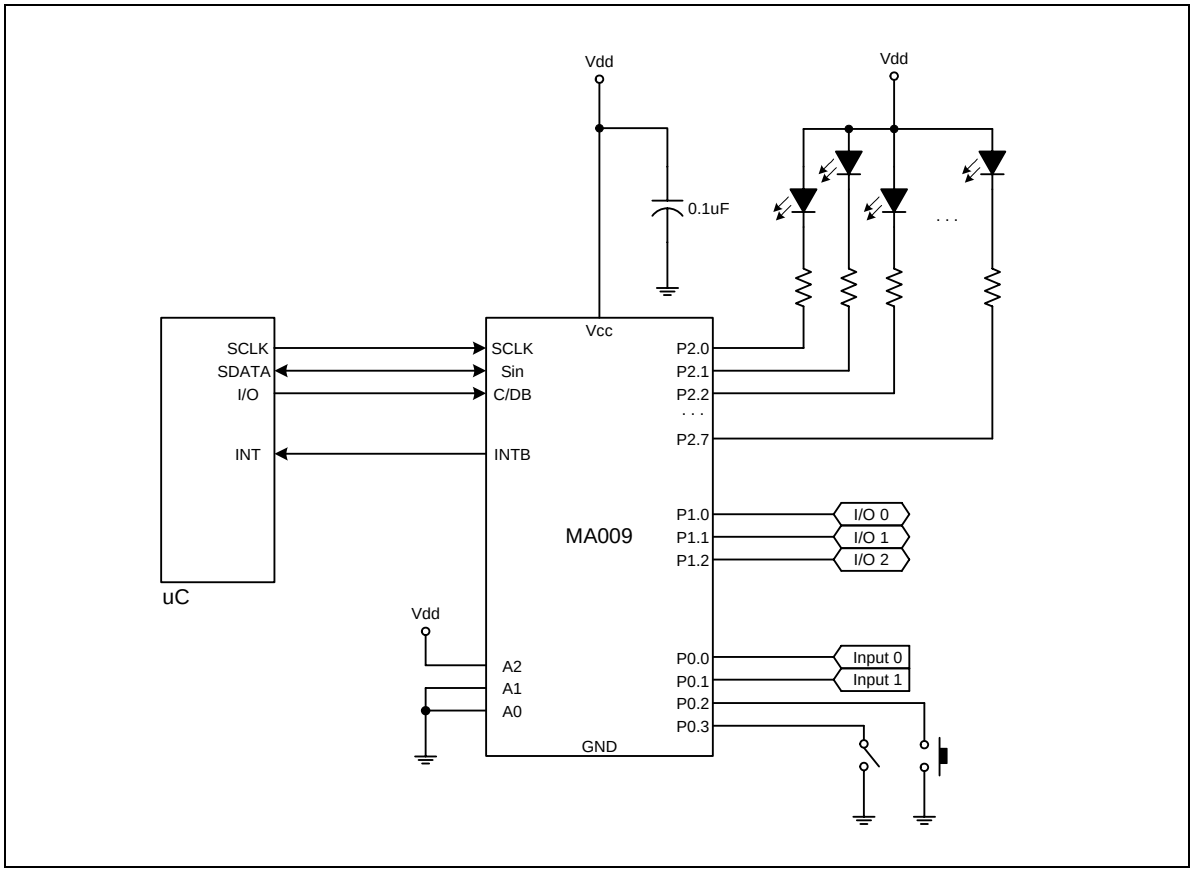


If we want to read the interrupt status, then we can send 43H to MA009.

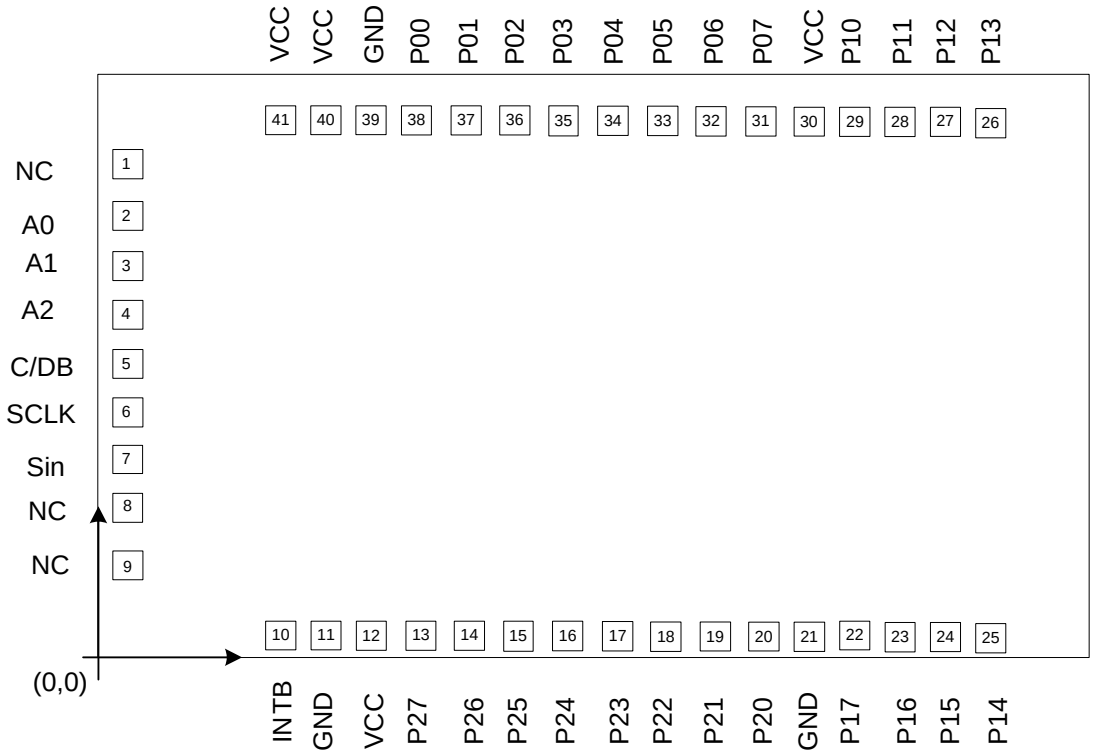
The last 8-bit data is sent by MA009 in this case.



Application Circuit



Pad Assignment



Absolute Maximum Rating

PARAMETER	RATING	UNIT
Supply Voltage to Ground Potential	-0.3 to +6.0	V
Applied Input / Output Voltage	-0.3 to +6.0	V
Power Dissipation	500	mW
Ambient Operating Temperature	0 to +70	°C
Storage Temperature	-55 to +150	°C

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

DC Characteristics

(V_{CC}-GND = 5.0V, Ta = 25° C; unless otherwise specified)

PARAMETER	SYM.	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Op. Voltage	V_{CC}	-	2.0	5.0	6.0	V
Op. Current	I_{OP}	No load (Ext.-V)	-	4.0	16.0	μA
Standby Current	I_{STB}	No load (Ext.-V)	-	0.5	2.0	μA
Input High Voltage	V_{IH}	-	0.7 V_{DD}	-	V_{DD}	V
Input Low Voltage	V_{IL}	-	0	-	0.3V_{DD}	V
$P_{1.0}$ to $P_{2.7}$, INTB normal sink current	I_{OL0}	V_{OL} = 0.4V	-	3.0	4.5	mA
INTB drive current	I_{OH0}	V_{OH} = 4.5V	-	1.5	2.5	mA
$P_{1.0}$ to $P_{2.7}$ large sink current	I_{OL1}	V_{OL} = 0.4V	-	18	27	mA
		V_{OL} = 0.4V, V_{CC} = 6.0V	-	20	32	mA
$P_{1.0}$ to $P_{2.7}$ drive current	I_{OH1}	V_{OH} = 4.5V	-	2.7	3.5	mA
		V_{OH} = 5.4V, V_{CC} = 6.0V	-	3.0	5.5	mA
All output ($P_{1.0}$ to $P_{2.7}$) large sink current	I_{OL2}	V_{OL} = 0.4V	-	16	24	mA
All output ($P_{1.0}$ to $P_{2.7}$) drive current	I_{OH2}	V_{OH} = 4.5V	-	8	12	mA
Total output large sink current	I_{OL3}	V_{OL} = 0.4V	-	256	384	mA
Total output drive current	I_{OH3}	V_{OH} = 4.5V	-	128	192	mA
Internal Pull-high Resistor (L)	R_{PH0}	Weak pull high	-	350K	-	Ω
Internal Pull-high Resistor (S)	R_{PH1}	Strong pull high, P0, P1 only	-	50K	-	Ω

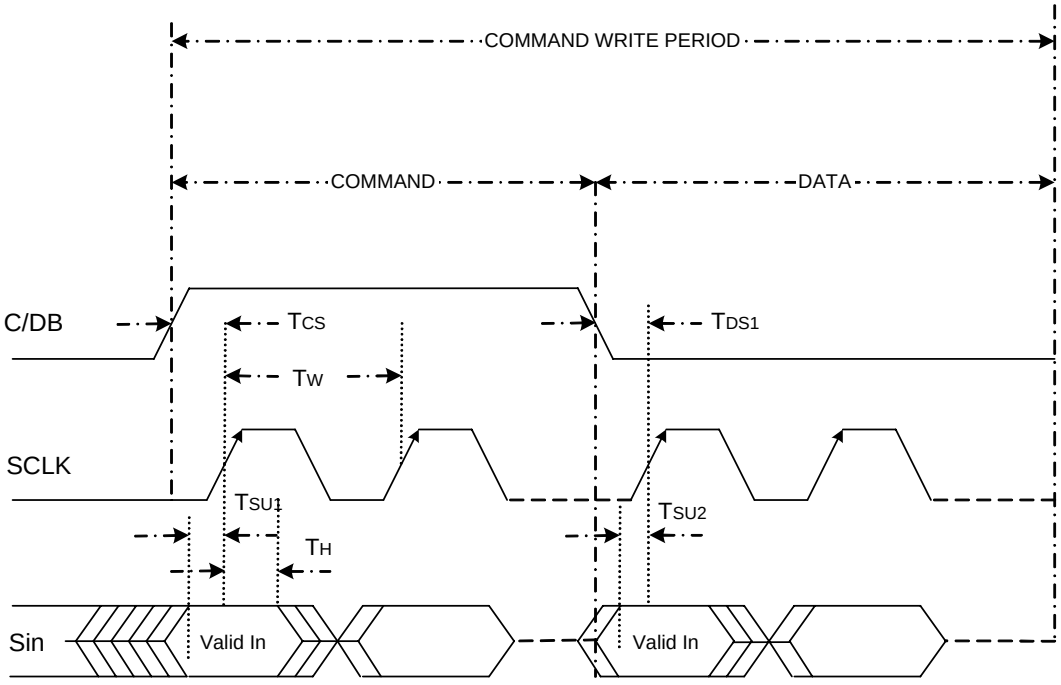
AC Characteristics

(VCC-GND = 5.0V, Ta = 25° C; unless otherwise specified)

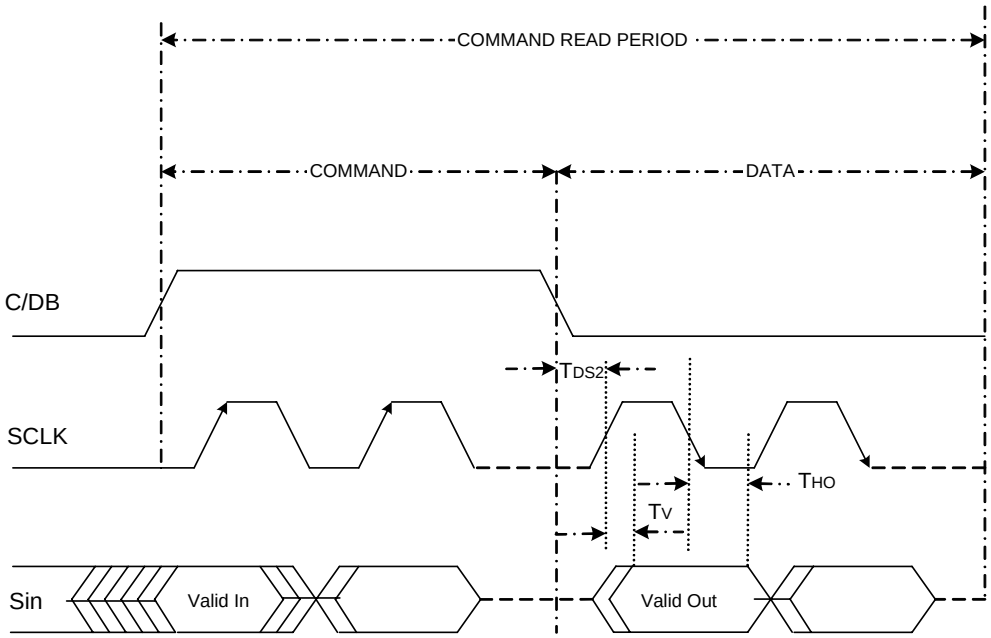
PARAMETER	SYM.	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Maximum clock pulse frequency (SCLK)	F_{MAX}	50 % duty cycle	-	2.5	5	MHz
Pulse Width	T_W	SCLK	100	-2	-	nS
Command Setting Time	T_{CS}	C/DB to SCLK	60	-2	-	nS
Data Setting Time	T_{DS1}	C/DB to SCLK (Write Mode)	30	-2	-	nS
	T_{DS2}	C/DB to SCLK (Read Mode)	30	-2	-	nS
Setup Time	T_{SU1}	Sin to SCLK (Command)	20	-2	-	nS
	T_{SU2}	Sin to SCLK (Data)	20	-2	-	nS
Hold time	T_H	SCLK to Sin	10	-2	-	nS
Input/Output Switch Time	T_{SW}	Vdd = 2.4V	-		15	nS
Output Valid Time	T_V	Vdd = 2.4V	-		10	nS
Output Hold Time	T_{HO}	Vdd = 2.4V	20		-	nS
Software Reset Recovery Time	T_{SREC}	Vdd = 2.4V	90		-	nS

System Timing

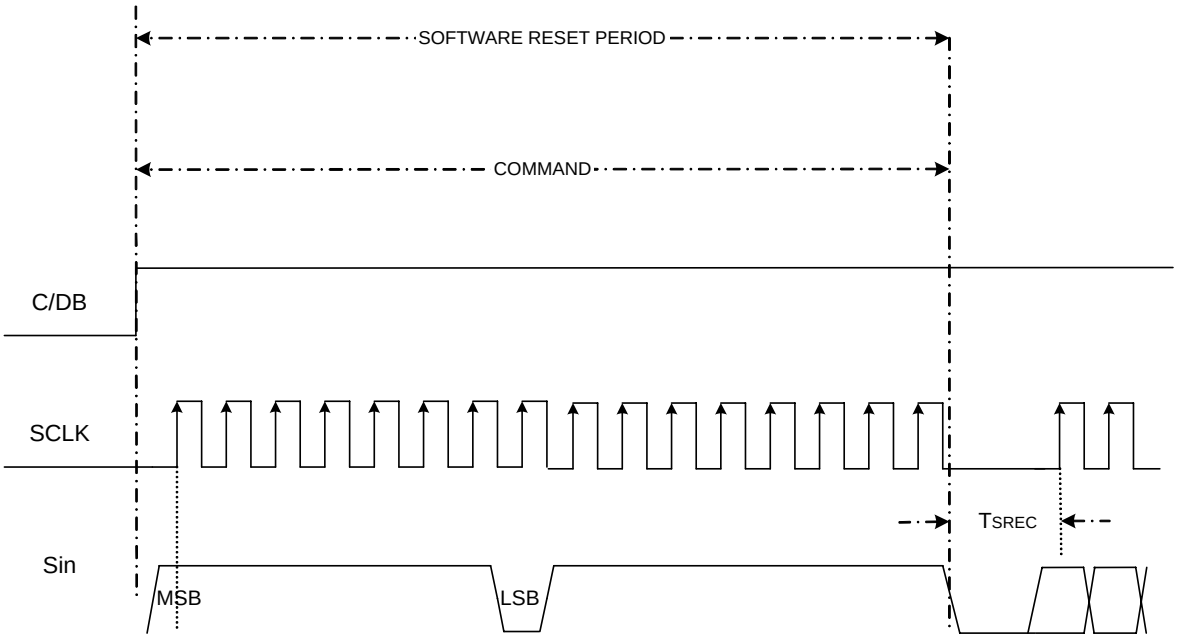
Command Write Setup Time Waveforms



Command Read Setup Time Waveforms

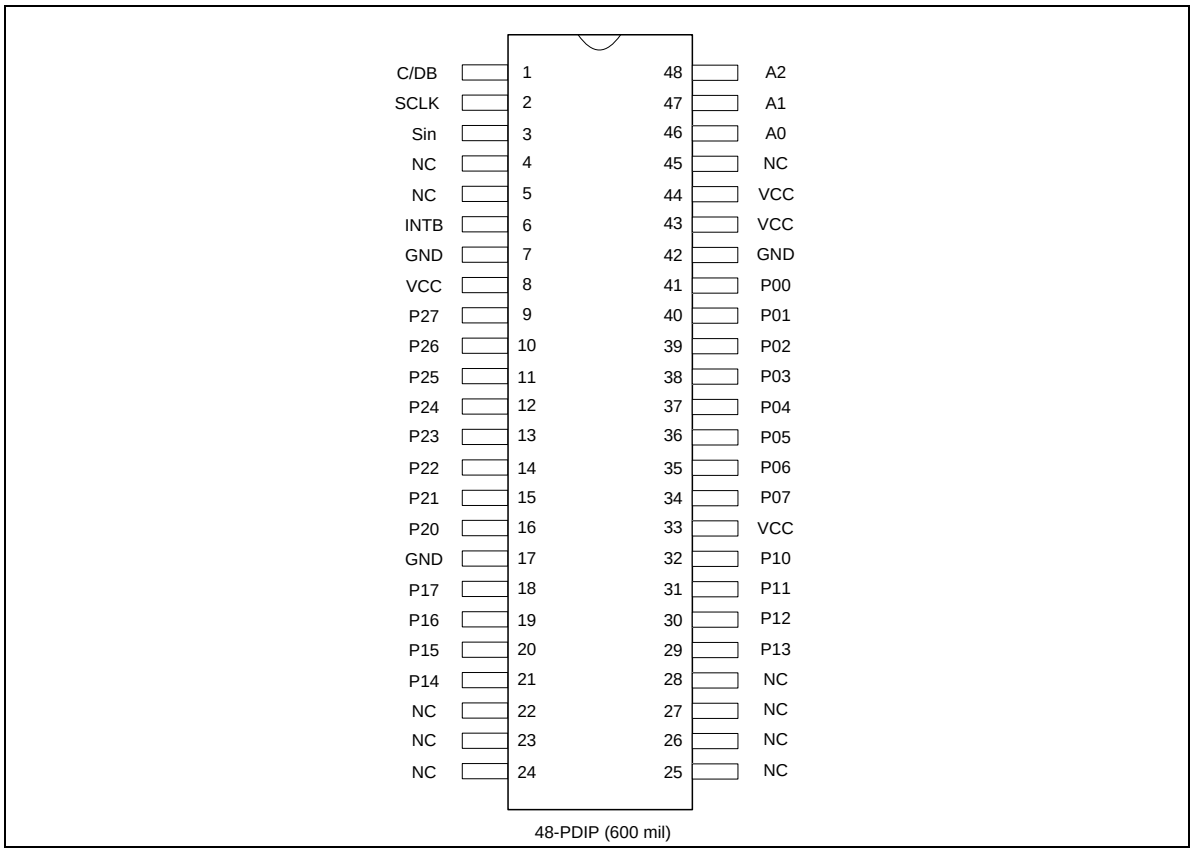


Command Reset Recovery Time Waveforms



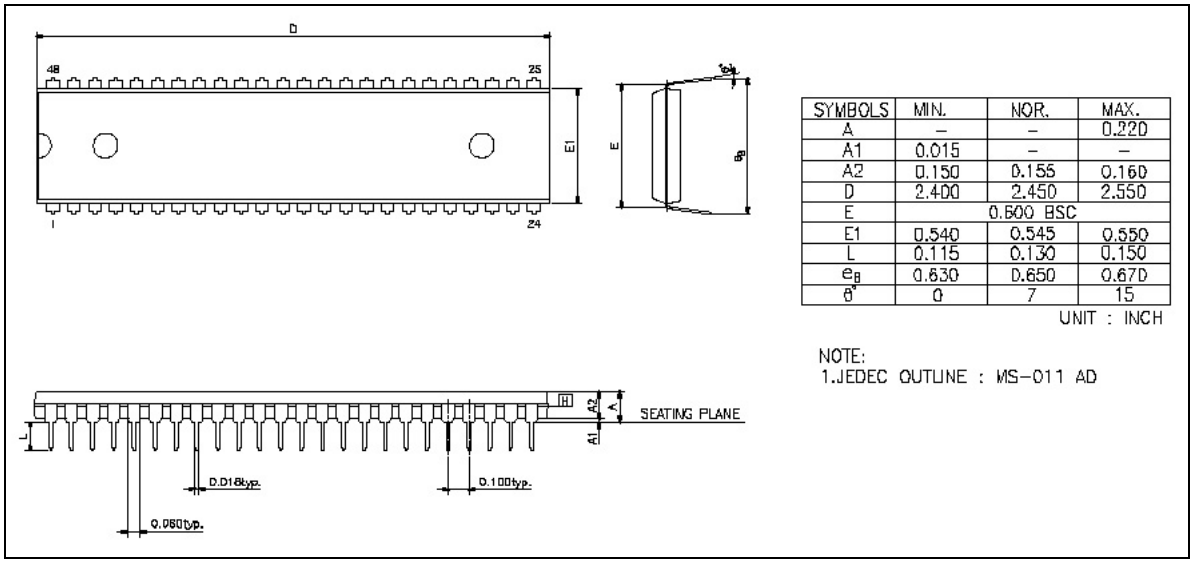
Package Information

MA009AE 48 Pin PDIP (600mil) Configuration



48-PDIP (600 mil)

48 Pin PDIP Package Dimension

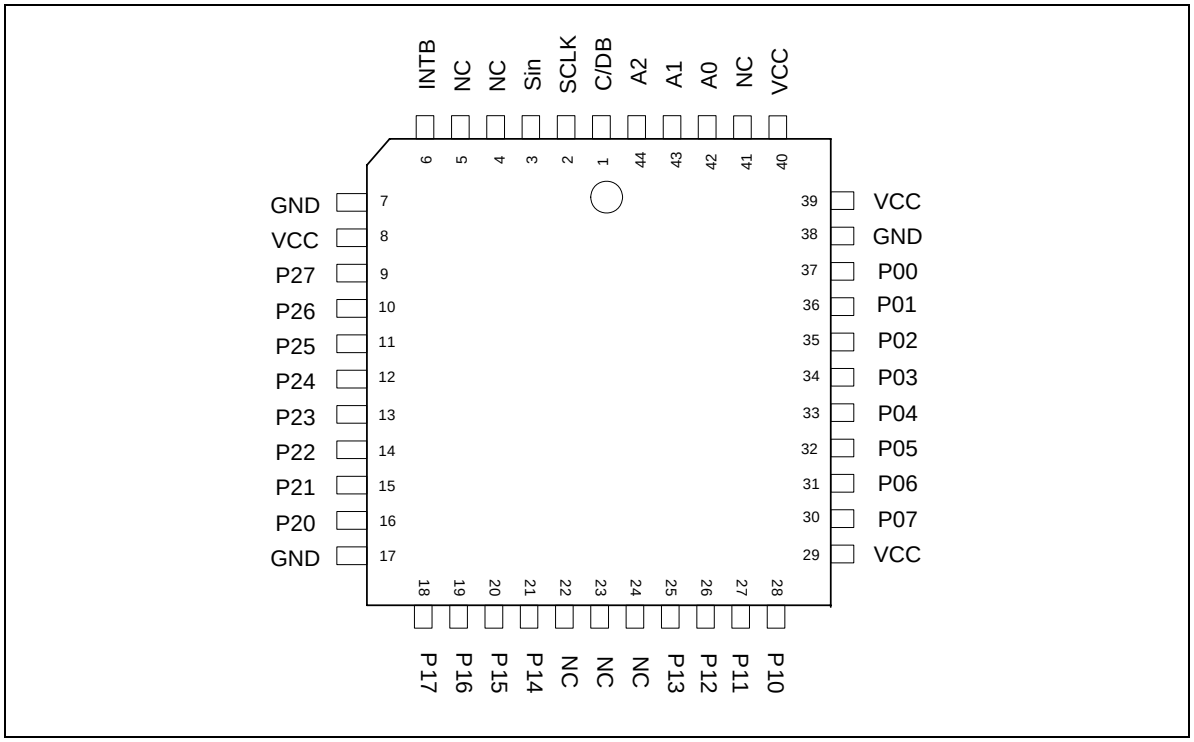


SYMBOLS	MIN.	NOR.	MAX.
A	–	–	0.220
A1	0.015	–	–
A2	0.150	0.155	0.160
D	2.400	2.450	2.550
E		0.600 BSC	
E1	0.540	0.545	0.550
L	0.115	0.130	0.150
e_B	0.630	0.650	0.670
θ°	0	7	15

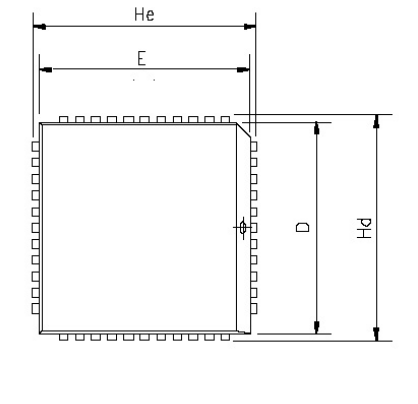
UNIT : INCH

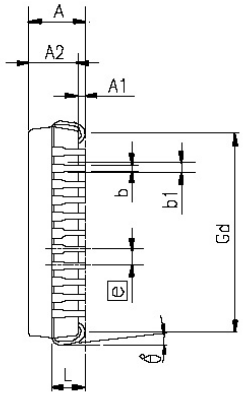
NOTE:
1.JEDEC OUTLINE : MS-011 AD

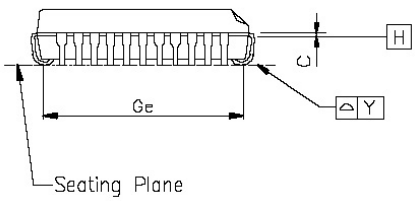
MA009AP 44 Pin PLCC Configuration



44 Pin PLCC Package Dimension







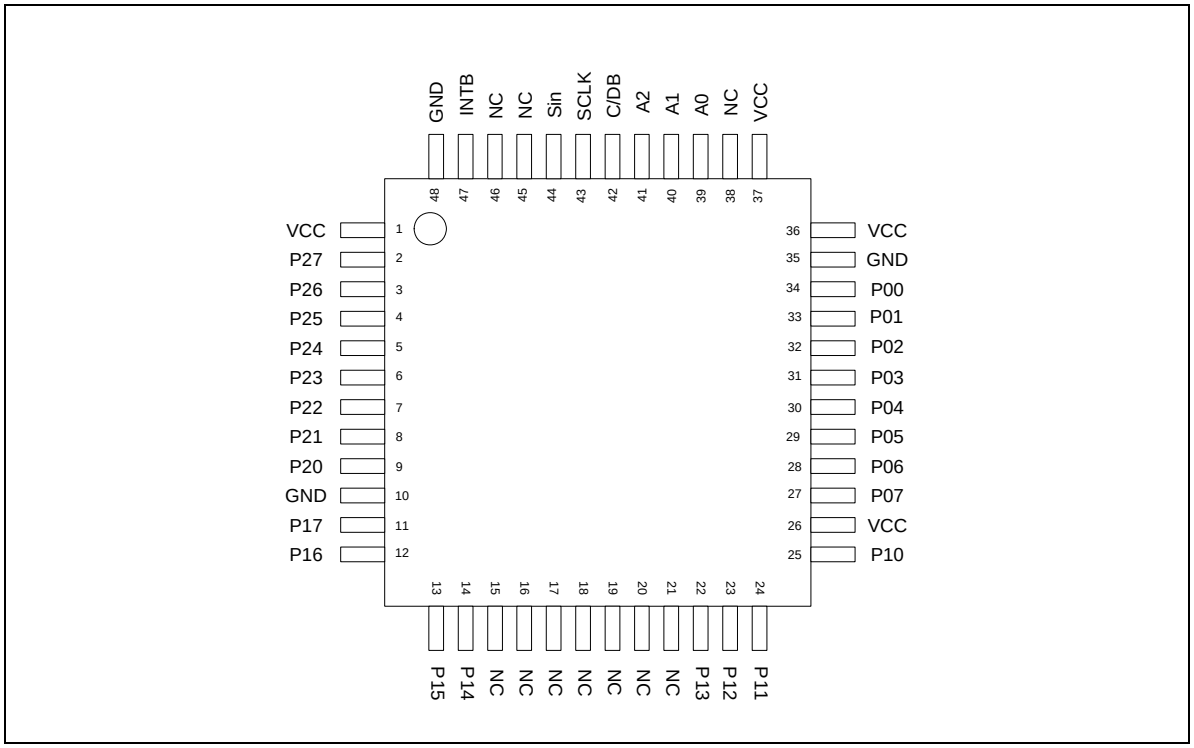
SYMBOLS	MIN.	NOM.	MAX.
A	–	–	0.185
A1	0.020	–	–
A2	0.145	0.150	0.155
b1	0.026	0.028	0.032
b	0.016	0.018	0.022
c	0.007	0.010	0.013
D	0.648	0.653	0.658
E	0.648	0.653	0.658
e		0.050 BSC	
Gd	0.590	0.610	0.630
Ge	0.590	0.610	0.630
Hd	0.680	0.690	0.700
He	0.680	0.690	0.700
L	0.090	0.100	0.110
Y	–	–	0.004

UNIT : INCH

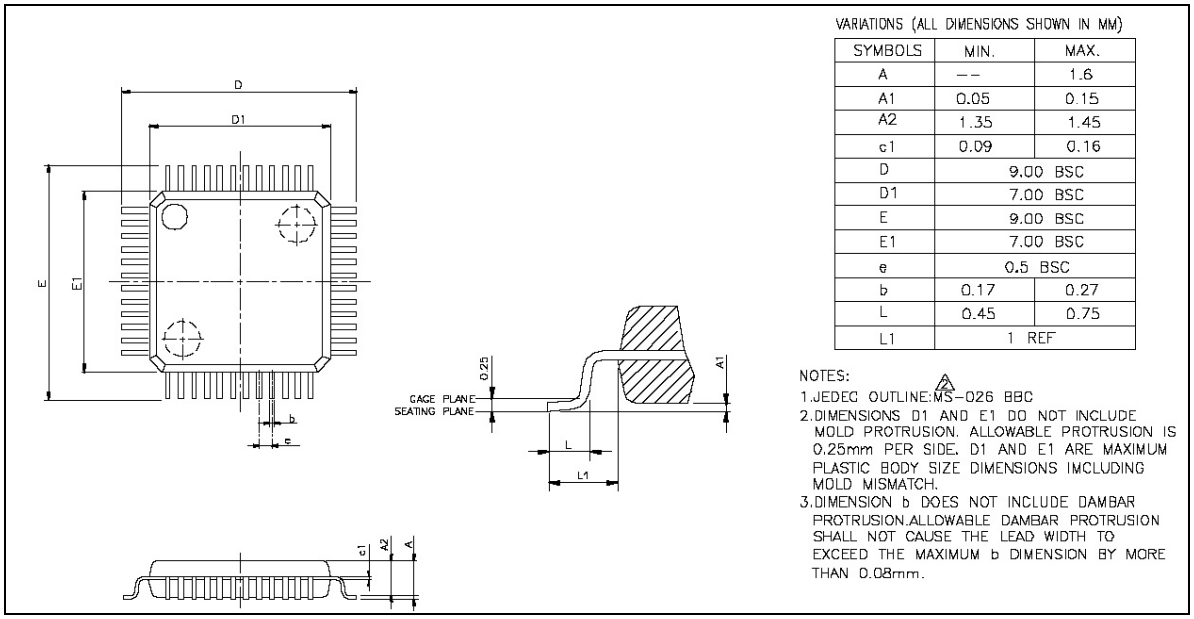
NOTE:

1. JEDEC OUTLINE : MO-047 AC
2. DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
3. DIMENSIONS E AND D DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 10 MIL PER SIDE. DIMENSIONS E AND D DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
4. DIMENSION b1 DOES NOT INCLUDE DAMBAR PROTRUSION .

MA009AD 48 Pin LQFP Configuration



48 Pin LQFP Package Dimension

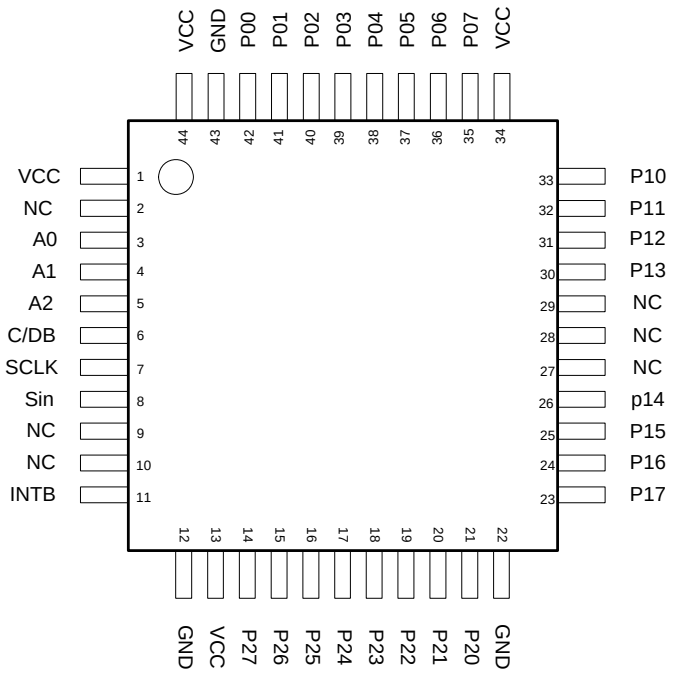


VARIATIONS (ALL DIMENSIONS SHOWN IN MM)

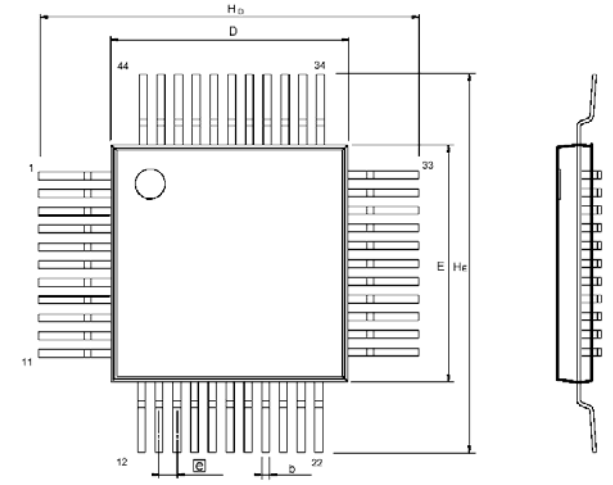
SYMBOLS	MIN.	MAX.
A	--	1.6
A1	0.05	0.15
A2	1.35	1.45
c1	0.09	0.16
D	9.00 BSC	
D1	7.00 BSC	
E	9.00 BSC	
E1	7.00 BSC	
e	0.5 BSC	
b	0.17	0.27
L	0.45	0.75
L1	1 REF	

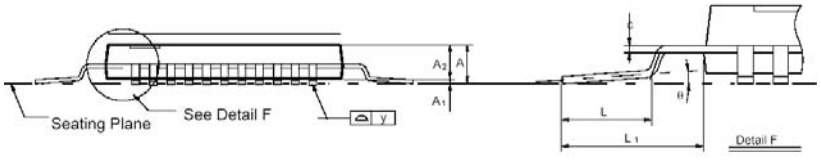
NOTES:
1. JEDEC OUTLINE: MS-026 BBC
2. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PER SIDE. D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM b DIMENSION BY MORE THAN 0.08mm.

MA009AF 44 Pin PQFP Configuration



44 Pin PQFP Package Dimension





Symbol	Dimension in inch			Dimension in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	---	---	---	---	---	---
A_1	0.002	0.01	0.02	0.05	0.25	0.5
A_2	0.075	0.081	0.087	1.90	2.05	2.20
b	0.01	0.014	0.018	0.25	0.35	0.45
c	0.004	0.006	0.010	0.101	0.152	0.254
D	0.390	0.394	0.398	9.9	10.00	10.1
E	0.390	0.394	0.398	9.9	10.00	10.1
e	0.025	0.031	0.036	0.635	0.80	0.952
H_D	0.510	0.520	0.530	12.95	13.2	13.45
H_E	0.510	0.520	0.530	12.95	13.2	13.45
L	0.025	0.031	0.037	0.65	0.8	0.95
L_1	0.051	0.063	0.075	1.295	1.6	1.905
y	—	—	0.003	—	—	0.08
θ	0°	—	7°	0°	—	7°

Notes:

1. Dimension D & E do not include interlead flash.
2. Dimension b does not include dambar protrusion/intrusion.
3. Controlling dimension: Millimeter
4. General appearance spec. should be based on final visual inspection spec.

Vision History

VERSION	DATE	PAGE	DESCRIPTION
A1	Sep. 2006		Initial issue.