

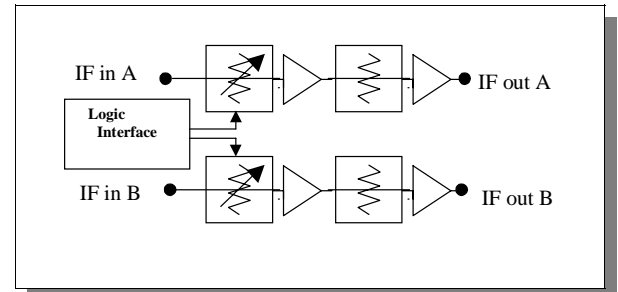
Features

- Attenuation: 0.5 dB steps to 31.5 dB
- 6 Bit Digital Gain Control
- CMOS Logic
- Serial Logic Interface
- Single Positive Voltage Supply
- 8 mm PBGA Package
- JEDEC MO-151 Footprint
- Single Package Solution for GSM,CDMA,PCS

Description

The M/A-COM AM55-0024 is a dual channel IF amplifier and digital attenuator packaged in a multi-layer multi-chip module (MCM). Gain control is via two separate serial logic interfaces. The part utilizes Plastic Ball Grid Array (PBGA) interconnect technology to achieve high circuit density and superior performance. This device is ideal for GSM/DCS/PCS digital base station applications where high dynamic range gain control is required.

Functional Block Diagram



Absolute Maximum Ratings ¹

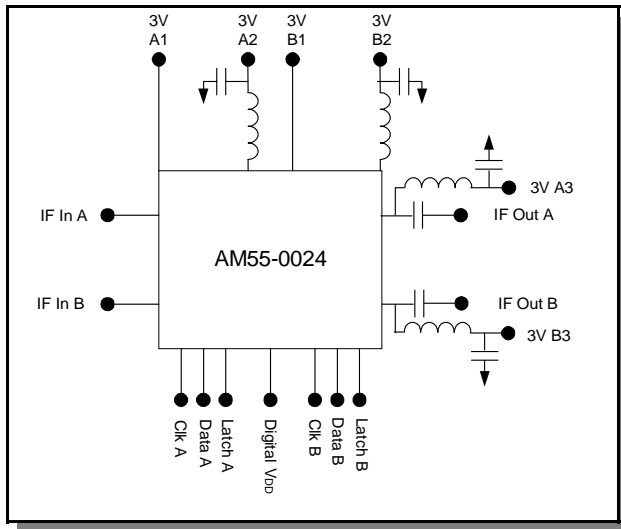
Parameter	Absolute Maximum
Input Power ²	+20 dBm
Operating Voltage ²	V _{DD} = +6 V
Operating Temperature	-40°C to +85°C
Storage Temperature	-65°C to +150°C

1. Exceeding any one or combination of these limits may cause permanent damage to this device.
2. Ambient Temperature (T_A) = +25°C.

Electrical Specifications: T_A = 25°C, Z₀ = 50 Ohms

Parameter	Test Conditions	Units	Min.	Typ.	Max.
Gain	100 - 400 MHz	dB	19.5	22.5	24.9
Gain Control Range	100 - 400 MHz	dB	—	31.5	—
Gain Control Step Size	100 - 400 MHz	dB	0	0.5	—
Attenuation Accuracy	0.5 - 15.5 dB states	dB	1.5 dB floating window		
Attenuation Accuracy (referenced to the nominal attenuation state)	16.0 - 23.5 dB states 24.0 - 31.5 dB states	dB dB	± (0.3 + 12% of atten. state) ± (0.3 + 15.5% of atten. state)		
Return Loss	100 - 400 MHz	dB	10	12	—
Output IP ₃	100 - 400 MHz @ 5V	dBm	—	30	—
Supply Voltage		V	—	3/5	—
Supply Current	@ 3V / @ 5V	mA	—	300/400	—
Switching Speed (50% TTL to 90% RF)		nS	—	50	—
Isolation		dB	—	60	—
P1dB		dBm	—	17.5	—
Noise Figure	100 - 400 MHz	dB	—	4	—

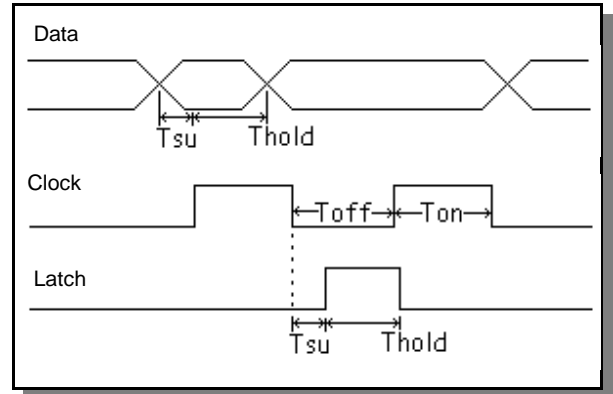
External Components ^{3,4,5}



- 3. All inductors are 470 nH
- 4. All capacitors are 10,000 pF
- 5. IF outputs must be supplied +3 Volts.

Component	Value
L	470 nH
C	10,000 pF

Clock Diagram ^{6,7,8,9,10}



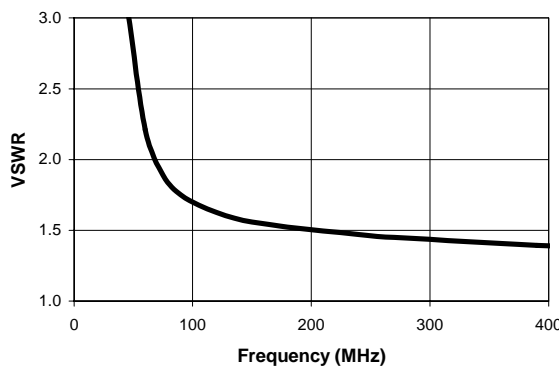
- 6. Max Clock Speed = 40 MHz
- 7. Ton = Toff
- 8. Tsu = >3ns
- 9. Thold = >7ns
- 10. Data clocked in on rising clock edge

Serial Interface

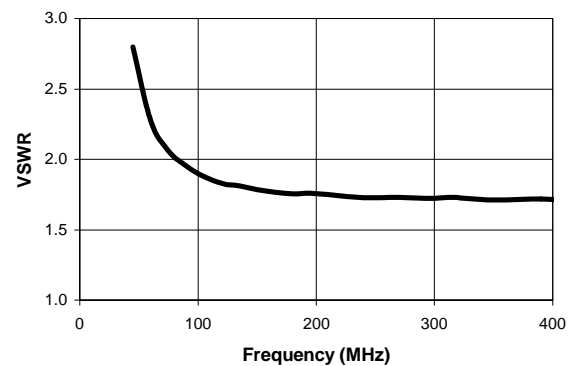
Each channel in the AM55-0024 is independently controllable with a 3 wire serial interface: Clock, Data, and Latch Enable. These lines can be shared based on application requirements. The attenuator within the device is controlled with a 6 bit word, enabling the selection of 64 possible states. The highest gain state is '000000', and the lowest is '111111'. The sequence for shifting the data is as follows: Present data (Least significant bit first), strobe clock, repeat until 6 bits have been presented and clocked, then strobe the latch enable line, which implements the state change.

Typical Performance Curves

Input VSWR



Output VSWR



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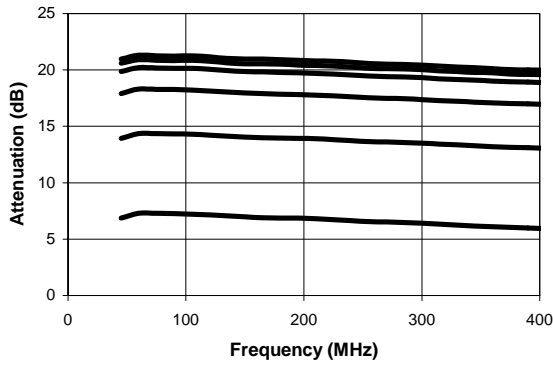
Visit www.macom.com for additional data sheets and product information.

- North America: Tel. (800) 366-2266
- Asia/Pacific: Tel.+81-44-844-8296, Fax +81-44-844-8298
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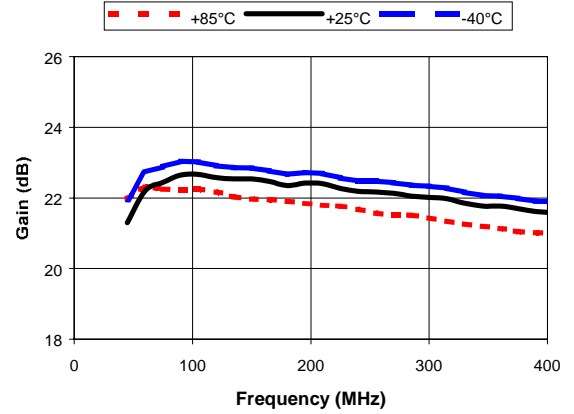


Typical Performance Curves

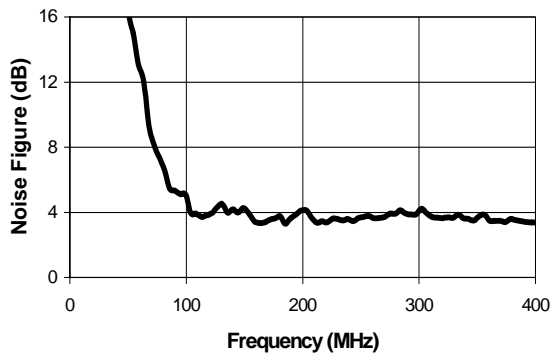
Attenuation (6 individual bits)



Gain



Noise Figure

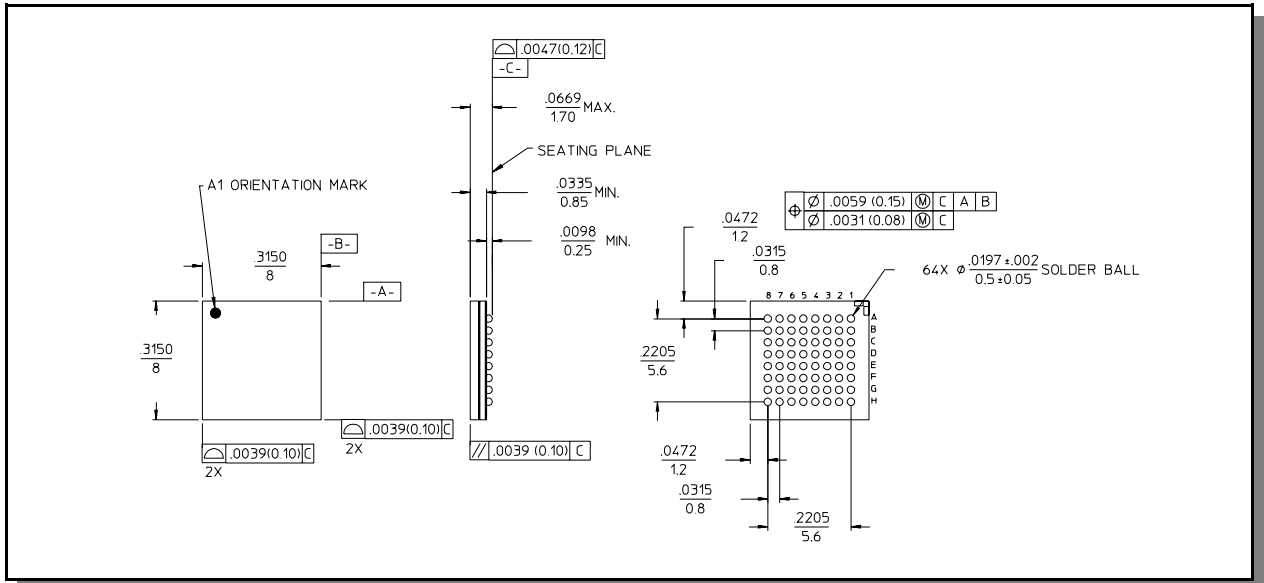


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8 mm PBGA



Pin Out

8	7	6	5	4	3	2	1	
+5V_A1	DAT_A	CLK_A	+5V_A2				RF_OUT_A	A
								B
RF_IN_A								C
LE_A								D
RF_IN_B								E
LE_B								F
CLK_B								G
DAT_B	+5V_B1			+5V_B2			RF_OUT_B	H

Ordering Information

Part Number	Package
AM55-0024	8-mm PBGA Package
AM55-0024TR*	Tape and Reel

*Reference Application note M513 for reel size information.

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