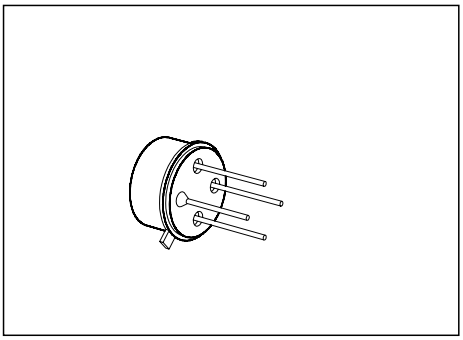
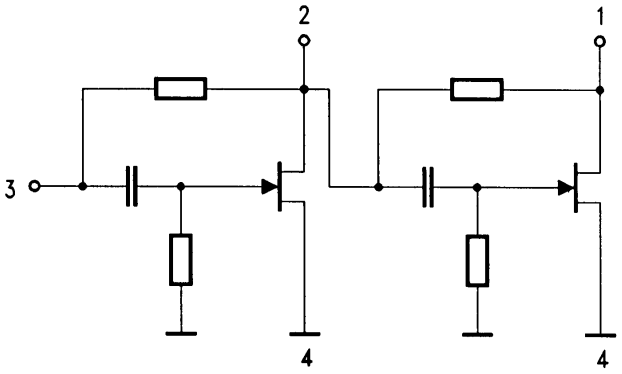
SIEMENS

GaAs MMIC — CGY 21

- Two-stage monolithic microwave IC (MMIC amplifier)
- All gold metallization
- Chip fully passivated
- Operating voltage range: 3 to 6 V
- 50 Ω input/output; RL_{IN} RL_{OUT} > 10 dB
- Gain: 21 dB at 500 MHz
- Low noise figure: 3.9 dB at 500 MHz
- Bandwidth: 2 GHz
- Hermetically sealed package



ESD: **E**lectro**s**tatic **d**ischarge sensitive device, observe handling precautions!

Type	Ordering Code	Circuit Diagram (Pin Configuration)	Package[1)]
CGY 21	Q68000-A5953	 1 RF output, V_S 2 Interstage, V_S 3 RF input 4 RF and DC ground, case	TO-12

1) For detailed information see chapter Package Outlines.

Maximum Ratings

Parameter	Symbol	Values	Unit
Supply voltage, $T_C \leq 80$ °C	V_S	6	V
Total power dissipation, $T_C \leq 50$ °C	P_{tot}	2	W
Channel temperature	T_{ch}	150	°C
Storage temperature range	T_{stg}	– 55 … + 150	

Thermal Resistance

Channel - case	R_{thchC}	50	K/W

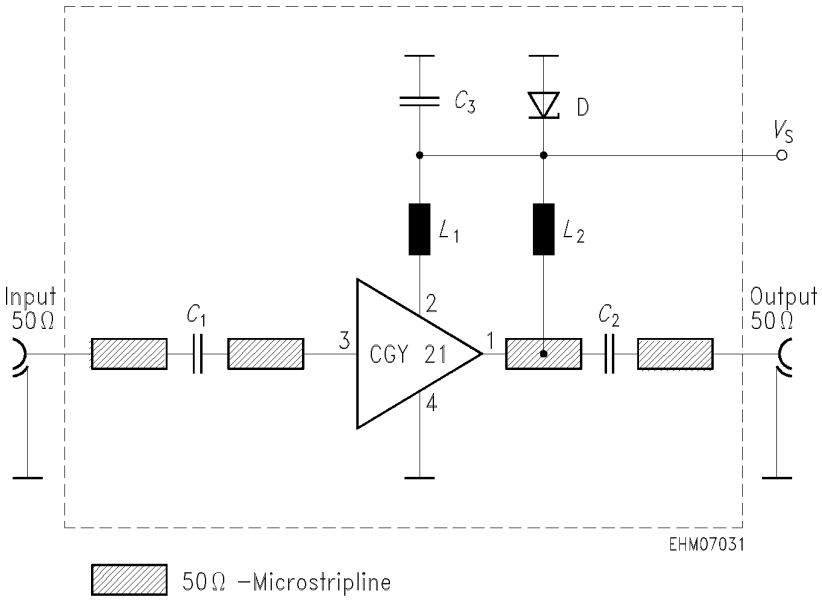
Note: Exceeding any of the maximum ratings may cause permanent damage to the device. Appropriate handling procedures are required to protect the electrostatic sensitive IC against degradation due to excess voltage or excess current spikes. Excellent ground connection of lead 4 and the package (e. g. soldered on microstripline laminate) is required to achieve guaranteed RF performance and stable operation conditions and provides adequate heat sink. Low parasitic capacitance of the bias network to port 2 gives optimum gain and flatness. Input and output connections must be DC isolated by coupling capacitors.

Electrical Characteristics
at T_A = 25 °C, V_S = 4.5 V, R_S = R_L = 50 Ω, unless otherwise specified,
(for application circuit see next page).

Parameter	Symbol	Values			Unit
		min.	typ.	max.	
Operating current	I_{op}	–	160	200	mA
Power gain f= 100 MHz to 900 MHz	G	19	21	–	dB
Gain flatness f= 100 MHz to 900 MHz	ΔG	–	1.5	2	
Noise figure f= 100 MHz to 900 MHz	F	–	3.9	5.5	
Input return loss f= 100 MHz to 900 MHz	RL_{IN}	–	12	9.5	
Output return loss f= 100 MHz to 900 MHz	RL_{OUT}	–	12	9.5	
Third order intercept point two-tone intermodulation test f_1= 806 MHz, f_2= 810 MHz, P_o = 10 dBm (both carriers)	IP_3	31	32.5	–	dBm
1 dB gain compression f= 100 MHz to 900 MHz	P_{1dB}	–	19	–	

Application Circuit

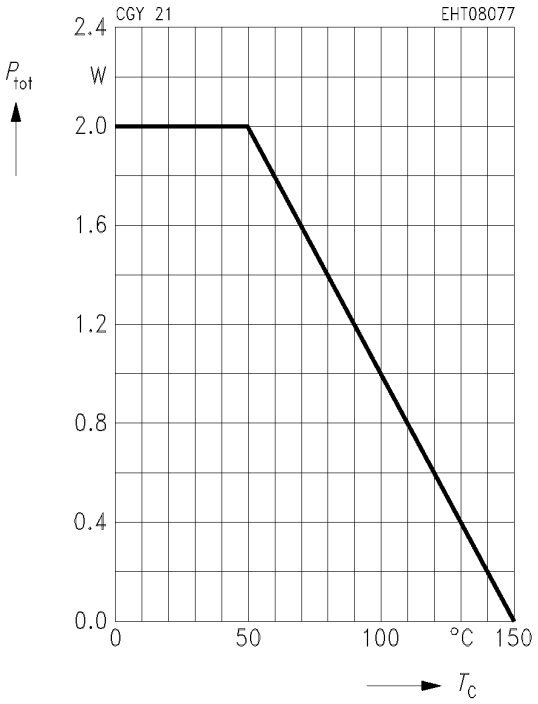
f= 100 MHz to 900 MHz



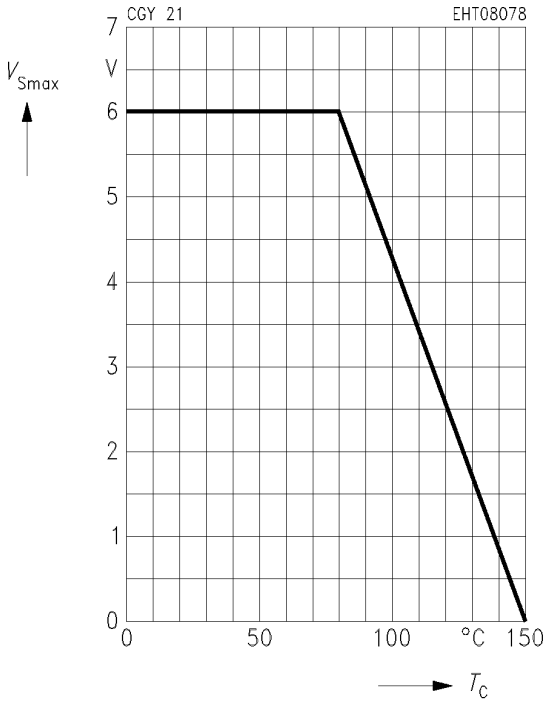
Legend of components

C_1, C_2, C_3	1 nF chip capacitors
L_1, L_2	1 µH inductance (B 78108 - T 1102K)
D	6 V2 Zener diode (BZW 22C6V2)

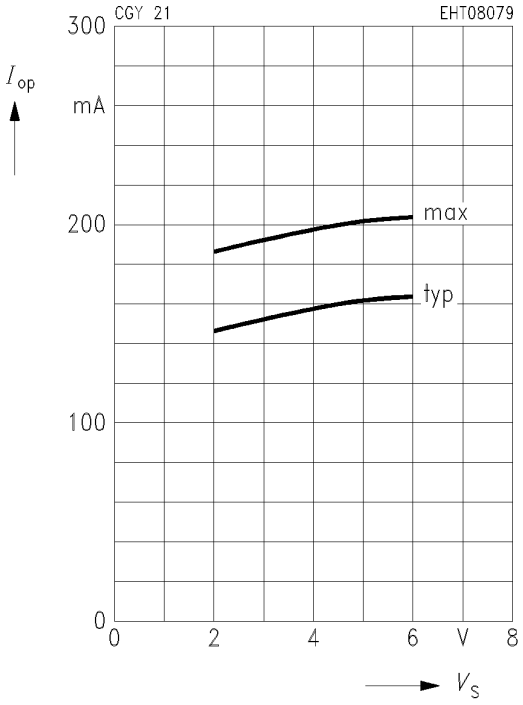
Total power dissipation $P_{tot} = f(T_C)$



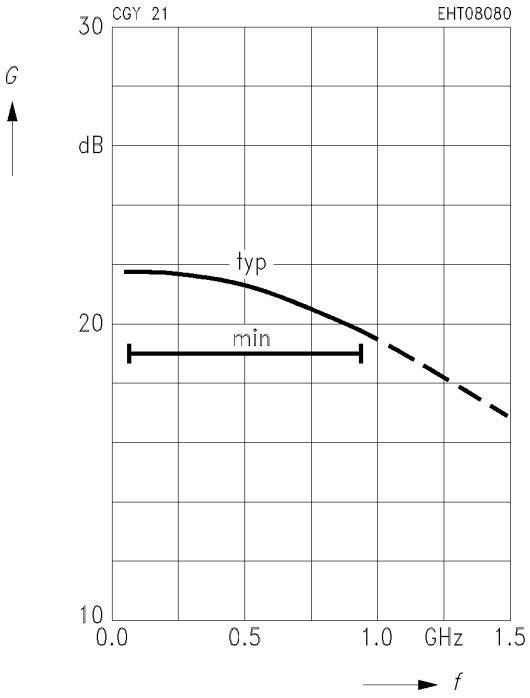
Max. supply voltage $V_{Smax} = f(T_C)$



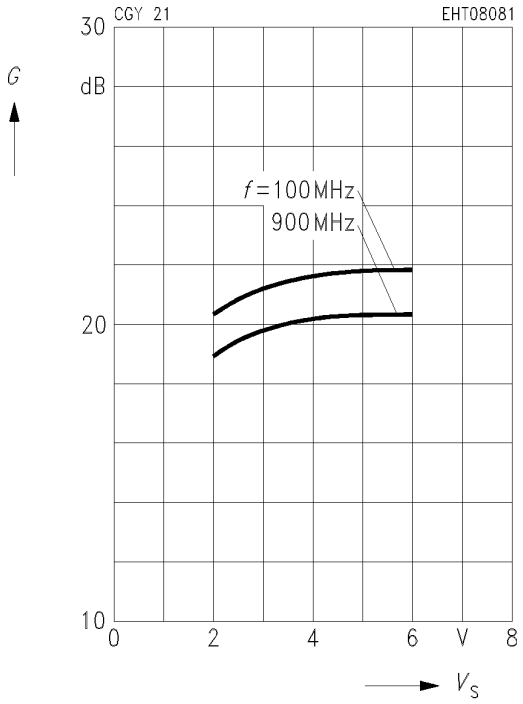
Operating current $I_{op} = f(V_S)$



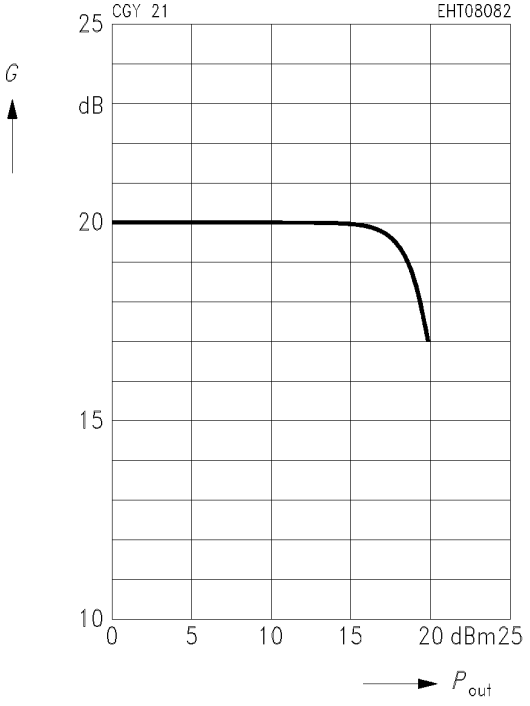
Power gain $G = f(f)$
V_S = 4.5 V, $R_S = R_L$ = 50 Ω



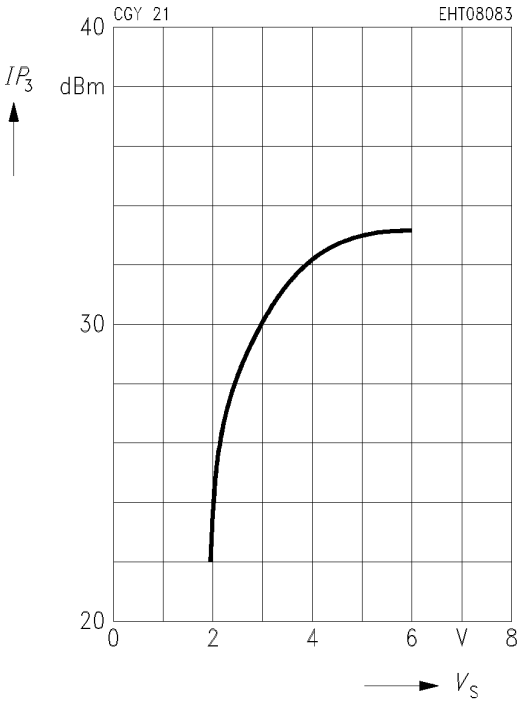
Power gain $G = f(V_S)$
$R_S = R_L$ = 50 Ω



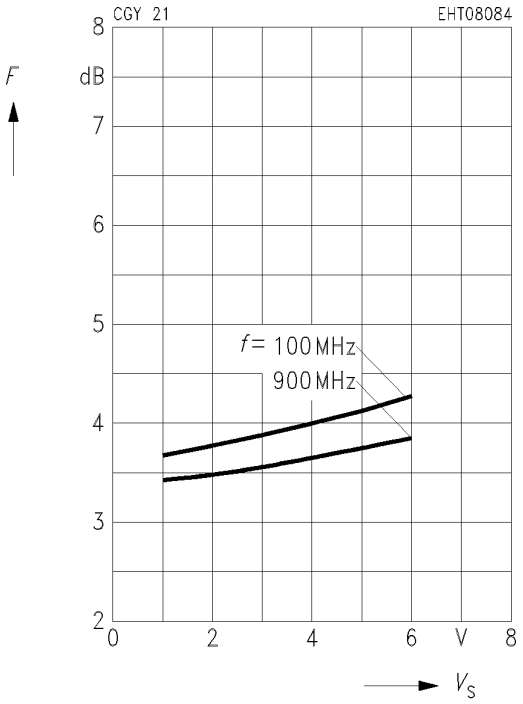
Power gain $G = f(P_{out})$
V_S = 4.5 V, $R_S = R_L$ = 50 Ω
f = 0.8 GHz



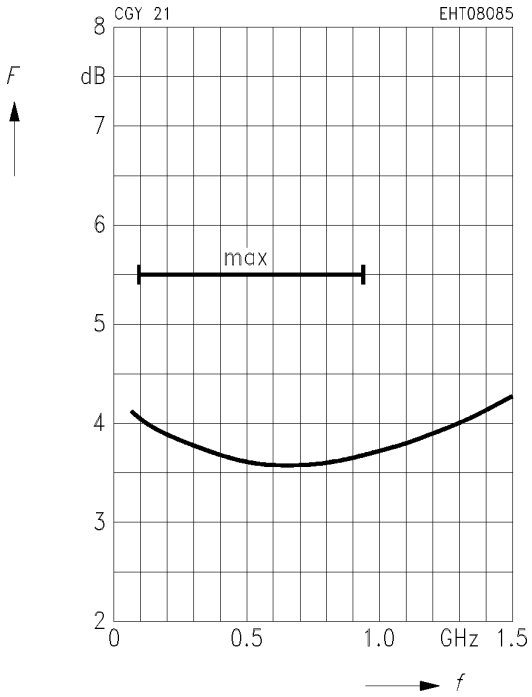
Third order intercept point $IP_3 = f(V_S)$
f= 800 MHz, $R_S = R_L$ = 50 Ω



Noise figure $F = f(V_S)$
$R_S = R_L$ = 50 Ω



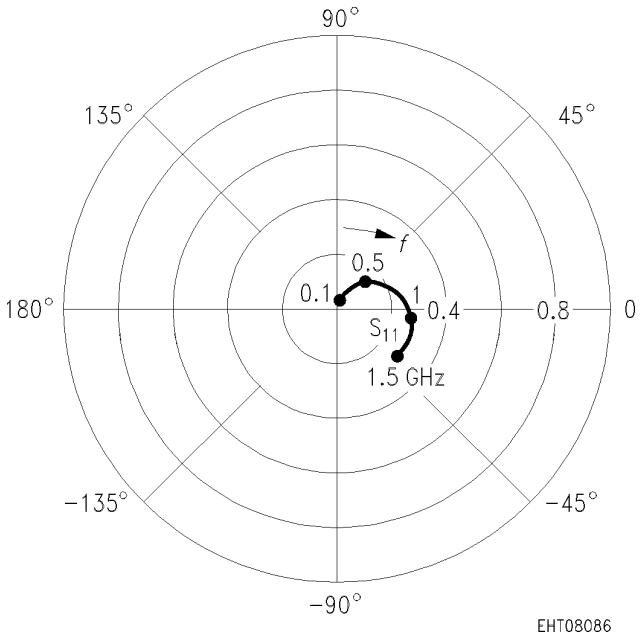
Noise figure $F = f(f)$
V_S = 4.5 V, $R_S = R_L$ = 50 Ω



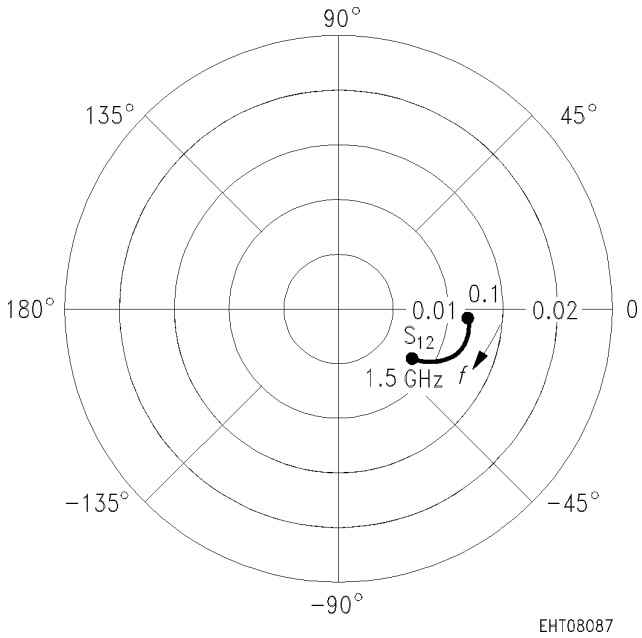
S Parameters

f	S_{11}		S_{21}		S_{12}		S_{22}	
GHz	MAG	ANG	MAG	ANG	MAG	ANG	MAG	ANG
V_S = 4.5 V, Z_0 = 50 Ω								
0.1	0.02	49	13.82	– 10	0.012	– 2	0.11	3
0.3	0.08	55	13.63	– 34	0.012	– 7	0.13	11
0.5	0.14	34	13.03	– 58	0.012	– 13	0.15	18
0.7	0.18	17	12.1	– 81	0.011	– 19	0.19	20
0.9	0.23	0	10.93	– 104	0.011	– 24	0.24	20
1.1	0.27	– 15	9.48	– 127	0.01	– 29	0.29	16
1.3	0.28	– 28	7.91	– 149	0.009	– 31	0.33	12
1.5	0.25	– 39	6.29	– 171	0.008	– 32	0.36	5

S_{11} = *f* (*f*)
V_S = 4.5 V, Z_0 = 50 Ω

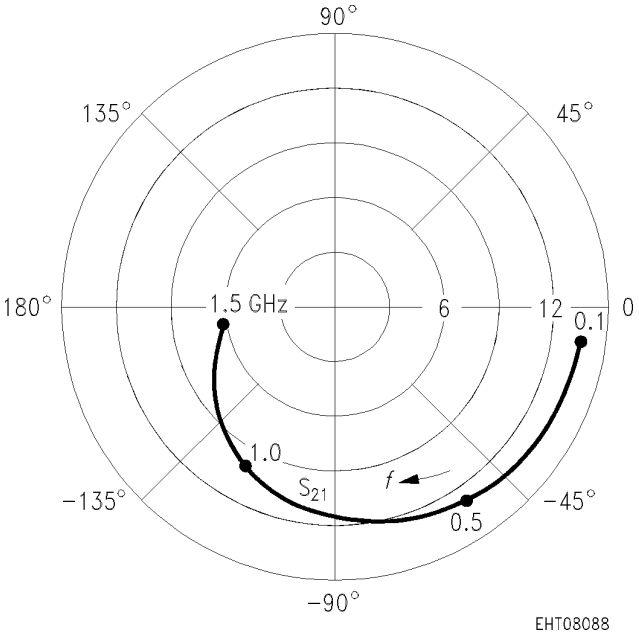


S_{12} = *f* (*f*)
V_S = 4.5 V, Z_0 = 50 Ω



S Parameters (continued)

***S*21 = *f* (*f*)**
V_S = 4.5 V, Z_0 = 50 Ω



***S*22 = *f* (*f*)**
V_S = 4.5 V, Z_0 = 50 Ω