

## Dual P-Channel 1.8-V (G-S) MOSFET

### CHARACTERISTICS

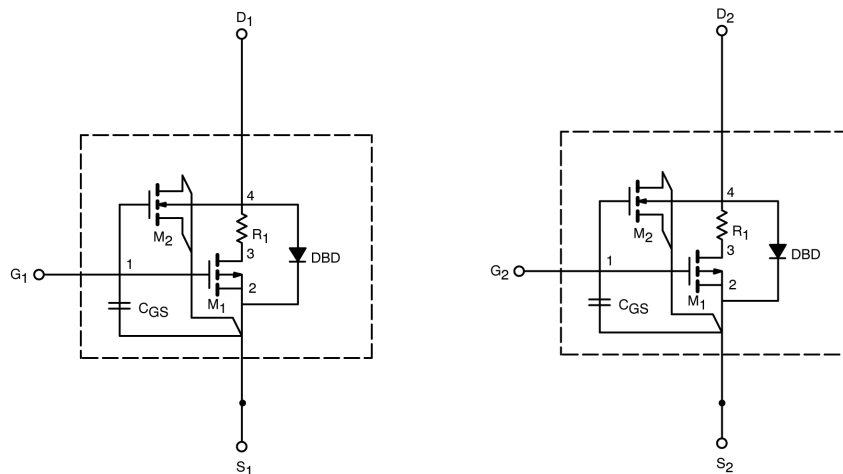
- P-Channel Vertical DMOS
- Macro Model (Subcircuit Model)
- Level 3 MOS
- Apply for both Linear and Switching Application
- Accurate over the  $-55$  to  $125^{\circ}\text{C}$  Temperature Range
- Model the Gate Charge, Transient, and Diode Reverse Recovery Characteristics

### DESCRIPTION

The attached spice model describes the typical electrical characteristics of the p-channel vertical DMOS. The subcircuit model schematic is extracted and optimized over the  $-55$  to  $125^{\circ}\text{C}$  temperature ranges under the pulsed 0-to-5V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage.

A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched  $C_{gd}$  model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device(s).

### SUBCIRCUIT MODEL SCHEMATIC



This document is intended as a SPICE modeling guideline and does not constitute a commercial product data sheet. Designers should refer to the appropriate data sheet of the same number for guaranteed specification limits.

# SPICE Device Model Si4967DY

Vishay Siliconix



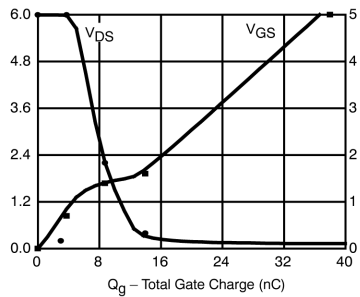
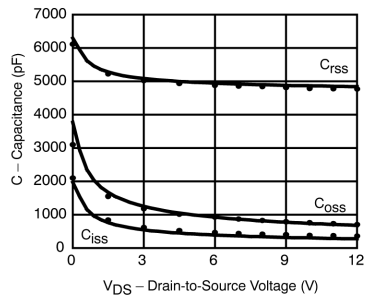
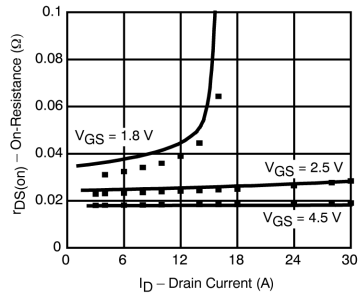
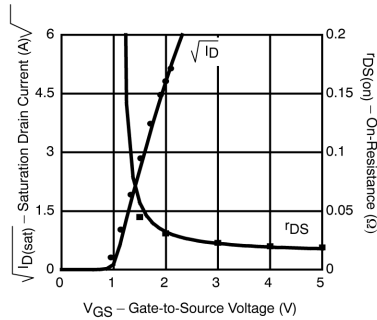
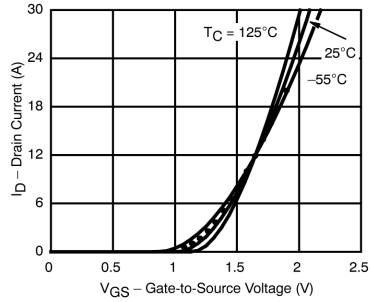
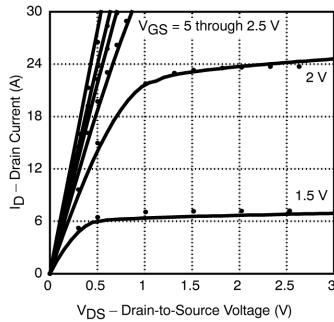
SPECIFICATIONS (T <sub>J</sub> = 25°C UNLESS OTHERWISE NOTED)				
Parameter	Symbol	Test Conditions	Typical	Unit
<b>Static</b>				
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = -250 μA	0.81	V
On-State Drain Current <sup>a</sup>	I <sub>D(on)</sub>	V <sub>DS</sub> ≥ -5 V, V <sub>GS</sub> = -4.5 V	189	A
Drain-Source On-State Resistance <sup>a</sup>	r <sub>DS(on)</sub>	V <sub>GS</sub> = -4.5 V, I <sub>D</sub> = -7.5 A	0.019	Ω
		V <sub>GS</sub> = -2.5 V, I <sub>D</sub> = -6.7 A	0.025	
		V <sub>GS</sub> = -1.8 V, I <sub>D</sub> = -5.4 A	0.037	
Forward Transconductance <sup>a</sup>	g <sub>fs</sub>	V <sub>DS</sub> = -10 V, I <sub>D</sub> = -7.5 A	29	S
Diode Forward Voltage <sup>a</sup>	V <sub>SD</sub>	I <sub>S</sub> = -1.7 A, V <sub>GS</sub> = 0 V	0.81	V
<b>Dynamic<sup>b</sup></b>				
Total Gate Charge <sup>b</sup>	Q <sub>g</sub>	V <sub>DS</sub> = -6 V, V <sub>GS</sub> = -10 V, I <sub>D</sub> = -7.5 A	35	nC
Gate-Source Charge <sup>b</sup>	Q <sub>gs</sub>		7	
Gate-Drain Charge <sup>b</sup>	Q <sub>gd</sub>		7	
Turn-On Delay Time <sup>b</sup>	t <sub>d(on)</sub>	V <sub>DD</sub> = -6 V, R <sub>L</sub> = 10 Ω I <sub>D</sub> ≅ -1 A, V <sub>GEN</sub> = -10 V, R <sub>G</sub> = 6 Ω	38	ns
Rise Time <sup>b</sup>	t <sub>r</sub>		25	
Turn-Off Delay Time <sup>b</sup>	t <sub>d(off)</sub>		189	
Fall Time <sup>b</sup>	t <sub>f</sub>		41	
Source-Drain Reverse Recovery Time	t <sub>rr</sub>	I <sub>F</sub> = -1.7 A, di/dt = 100 A/μs	67	

**Notes**

- a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.
- b. Guaranteed by design, not subject to production testing.



COMPARISON OF MODEL WITH MEASURED DATA ( $T_J=25^\circ\text{C}$  UNLESS OTHERWISE NOTED)



Note: Dots and squares represent measured data.