National Semiconductor

August 1989

# DM7556/DM8556 TRI-STATE® Programmable Binary Counters

General Description

These circuits are synchronous, edge-sensitive, fully-programmable 4-bit counters. The counters feature both conventional totem-pole and TRI-STATE outputs; such that when the outputs are in the high impedance mode, they can be used to enter data from the bus lines. In addition, the clear input operates completely independent of all other inputs. During the programming operation, data is loaded into the flip-flops on the positive-going edge of the clock pulse. To facilitate cascading of these counters, the MAX COUNT output can be tied directly into the count enable input of the next counter.

Features

- Typical clock frequency 35 MHz
- TRI-STATE outputs
- Fully independent clear
- Synchronous loading
- Cascading circuitry provided internally

Connection Diagram

Dual-In-Line Package

TL/F/6588–1
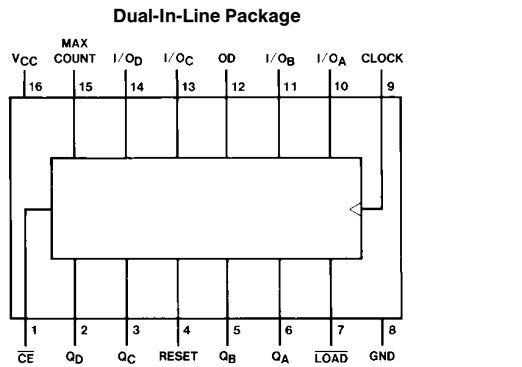
Order Number DM7556J or DM8556N
See NS Package Number J16A or N16A

Function Table

Control Inputs					I/O Ports				Active Outputs			
$\overline{\text{LOAD}}$	$\overline{\text{CE}}$	CLK	OD	Reset	I/O$_A$	I/O$_B$	I/O$_C$	I/O$_D$	Q$_A$	Q$_B$	Q$_C$	Q$_D$
H	X	X	L	H	L	L	L	L	L	L	L	L
H	X	X	H	H	Z	Z	Z	Z	L	L	L	L
H	X	L	L	L	Q$_{A0}$	Q$_{B0}$	Q$_{C0}$	Q$_{D0}$	Q$_{A0}$	Q$_{B0}$	Q$_{C0}$	Q$_{D0}$
H	X	L	H	L	Z	Z	Z	Z	Q$_{A0}$	Q$_{B0}$	Q$_{C0}$	Q$_{D0}$
L	H	↑	L	L	a	b	c	d	A	B	C	D
H	L	↑	L	L	COUNT				COUNT			
H	L	↑	H	L	Z	Z	Z	Z	COUNT			

The I/O pins are used as inputs when they are TRI-STATED, and the $\overline{\text{LOAD}}$ input is Low. They are outputs and active when $\overline{\text{LOAD}}$ input is High and OD is Low.

H = High Level (Steady State)

L = Low Level (Steady State)

X = Don't Care including transitions

a, b, c, d = The level of the steady state input at inputs A, B, C, D respectively

Q$_{A0}$, Q$_{B0}$, Q$_{C0}$, Q$_{D0}$ = The level of Q$_A$, Q$_B$, Q$_C$, Q$_D$ respectively, before the indicated steady state input conditions were established.

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Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
DM75	$-55°C$ to $+125°C$
DM85	$0°C$ to $+70°C$
Storage Temperature Range	$-65°C$ to $+150°C$

Note: *The ''Absolute Maximum Ratings'' are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the ''Electrical Characteristics'' table are not guaranteed at the absolute maximum ratings. The ''Recommended Operating Conditions'' table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter		DM7556			DM8556			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.8			0.8	V
I_{OH}	High Level Output Current				-2			-5.2	mA
I_{OL}	Low Level Output Current				16			16	mA
f_{CLK}	Clock Frequency (Note 1)		0		25	0		25	MHz
t_W	Pulse Width (Note 1)	Clock	25			25			
		Clear	20			20			ns
		Load	30			30			
$t_{\overline{CE}}$	Count Enable Time (Note 1)	Setup	30			30			ns
		Hold	-10			-10			
$t_{SETUP(1)}$	Setup Time High Logic Level (Note 1)	Data	25			25			ns
		Load	30			30			
$t_{HOLD(1)}$	Hold Time High Logic Level (Note 1)	Data	5			5			ns
		Load	-10			-10			
$t_{SETUP(0)}$	Setup Time Low Logic Level (Note 1)	Data	30			30			ns
		Load	25			25			
$t_{HOLD(0)}$	Hold Time Low Logic Level (Note 1)	Data	5			5			ns
		Load	-10			-10			
T_A	Free Air Operating Temperature		-55		125	0		70	°C

Note 1: $T_A = 25°C$ and $V_{CC} = 5V$.

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Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	$V_{CC} = $ Min, $I_I = -12$ mA				-1.5	V
V_{OH}	High Level Output Voltage	$V_{CC} = $ Min, $I_{OH} = $ Max $V_{IL} = $ Max, $V_{IH} = $ Min		2.4			V
V_{OL}	Low Level Output Voltage	$V_{CC} = $ Min, $I_{OL} = $ Max $V_{IH} = $ Min, $V_{IL} = $ Max				0.4	V
I_I	Input Current @ Max Input Voltage	$V_{CC} = $ Max, $V_I = 5.5$V				1	mA
I_{IH}	High Level Input Current	$V_{CC} = $ Max, $V_I = 2.4$V				40	μA
I_{IL}	Low Level Input Current	$V_{CC} = $ Max, $V_I = 0.4$V				-1.6	mA
I_{OZH}	Off-State Output Current with High Level Output Voltage Applied	$V_{CC} = $ Max, $V_O = 2.4$V $V_{IH} = $ Min, $V_{IL} = $ Max				40	μA
I_{OZL}	Off-State Output Current with Low Level Output Voltage Applied	$V_{CC} = $ Max, $V_O = 0.4$V $V_{IH} = $ Min, $V_{IL} = $ Max				-40	μA
I_{OS}	Short Circuit Output Current	$V_{CC} = $ Max (Note 2)	DM75	-25		-70	mA
			DM85	-25		-70	
I_{CC}	Supply Current	$V_{CC} = $ Max			75	100	mA

**Note 1:** All typicals are at $V_{CC} = $ 5V, $T_A = $ 25°C.

Note 2: Not more than one output should be shorted at a time.

## Switching Characteristics at $V_{CC} = $ 5V and $T_A = $ 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	$R_L = 400\Omega$				Units
			$C_L = 5$ pF		$C_L = 50$ pF		
			Min	Max	Min	Max	
f_{MAX}	Maximum Clock Frequency				25		MHz
t_{PLH}	Propagation Delay Time Low to High Level Output	Clock to Output				22	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clock to Output				44	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Clock to MAX-CNT				33	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clock to MAX-CNT				33	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Reset to Output				44	ns
t_{PZH}	Output Enable Time to High Level Output	Output Disable to Q				20	ns
t_{PZL}	Output Enable Time to Low Level Output	Output Disable to Q				20	ns
t_{PHZ}	Output Disable Time from High Level Output	Output Disable to Q		12			ns
t_{PLZ}	Output Disable Time from Low Level Output	Output Disable to Q		20			ns

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Logic Diagram

75/8556

TL/F/6588–2

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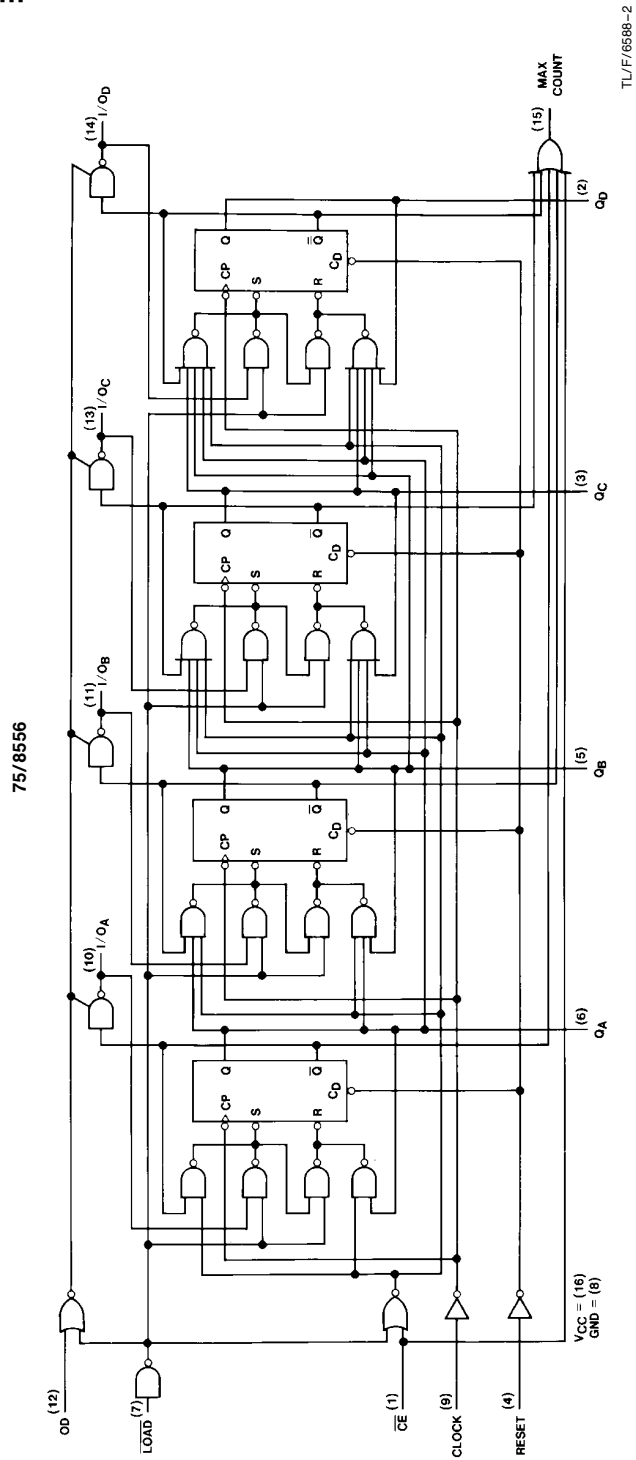
Timing Diagram

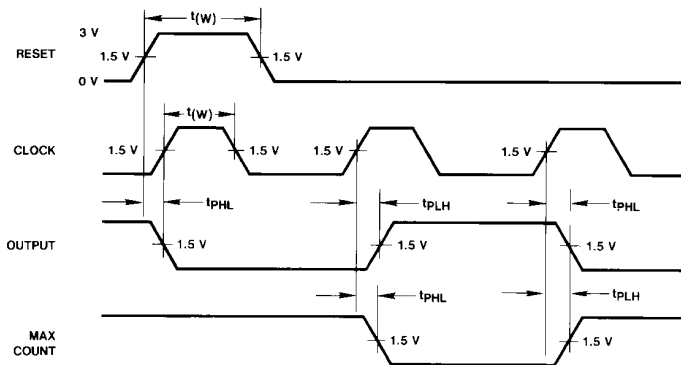### 75/8556 Typical Clear, Preset, Count, Inhibit Sequence
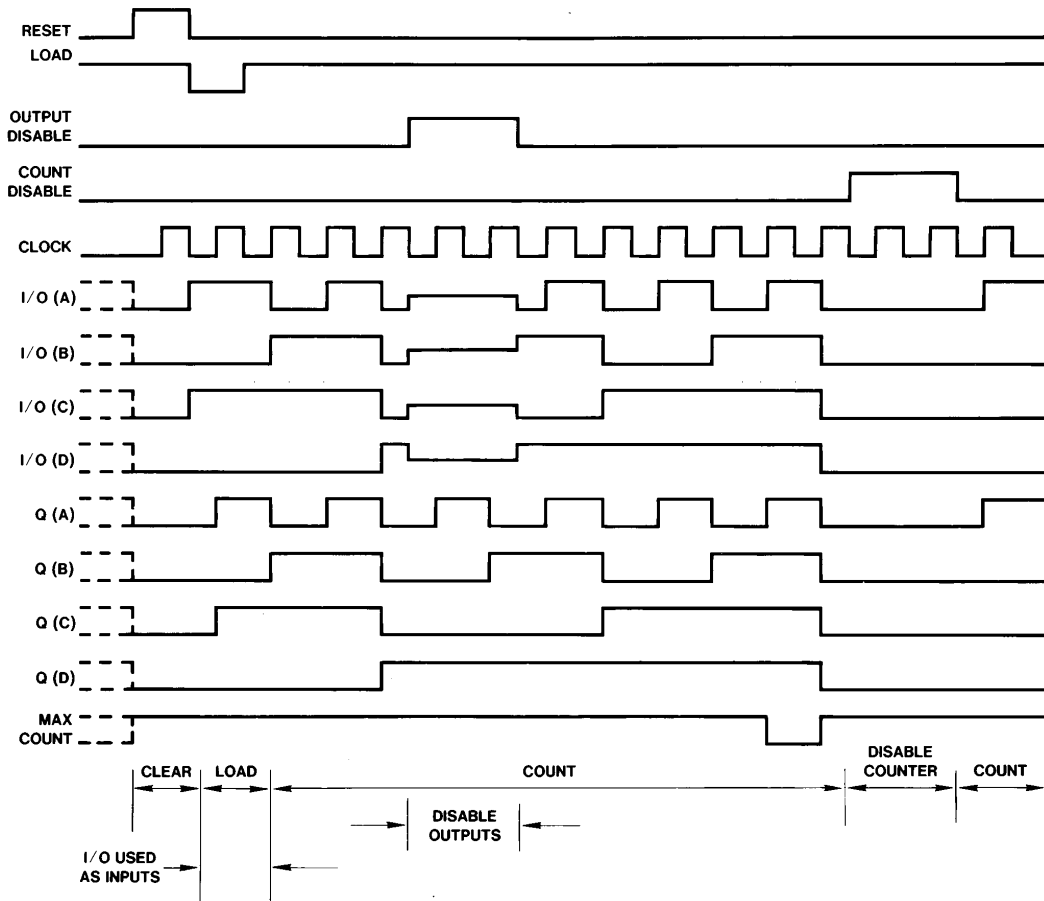
TL/F/6588–3

Sequence

(1) Clear to zero.

(2) Load binary five.

(3) Count six, seven, eight, nine, ten, eleven, twelve, thirteen, fourteen, fifteen, zero.

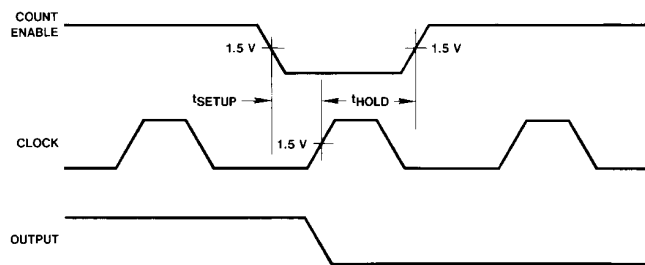(4) Disable TRI-STATE outputs.

(5) Disable counter.

(6) Count to one.

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Switching Time Waveforms
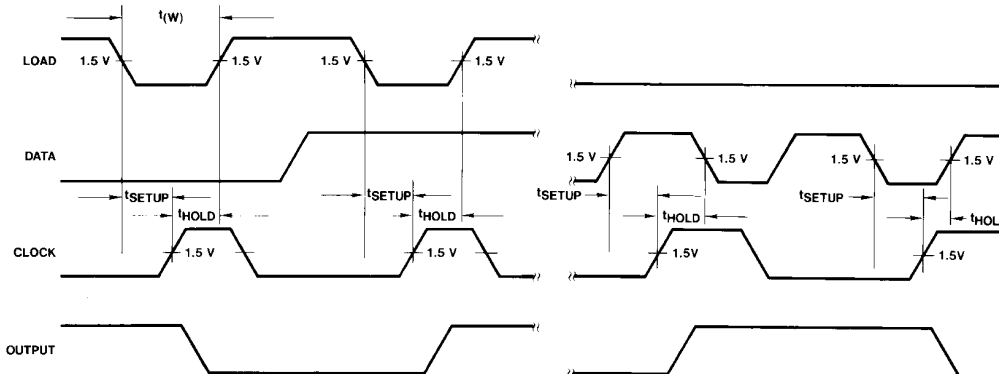
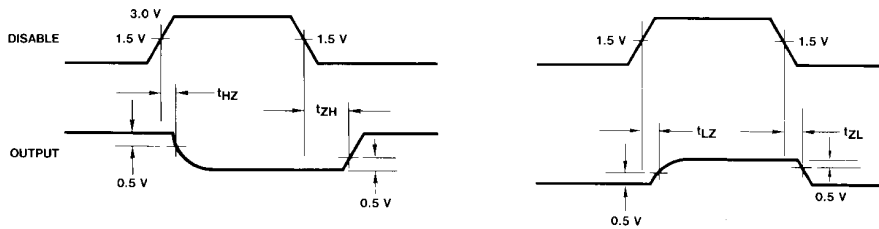### Clock and Reset Voltage

TL/F/6588-4

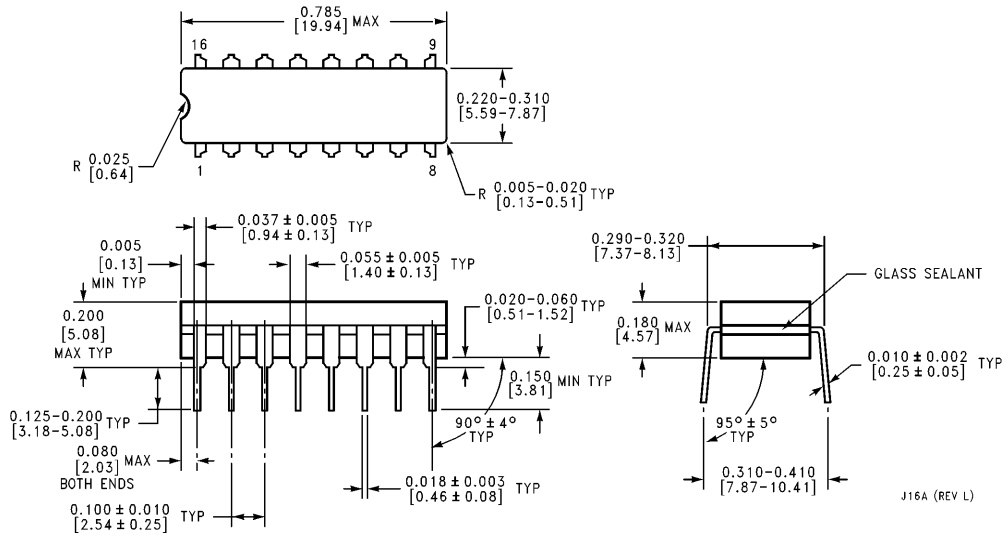### Count Enable and Clock

TL/F/6588-5

Load, Data and Clock

TL/F/6588-6

Output Disable

TL/F/6588-7

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Physical Dimensions inches (millimeters)

0.785
[19.94] MAX

16   9

0.220–0.310
[5.59–7.87]

R 0.025
[0.64]

1   8

R 0.005–0.020 TYP
[0.13–0.51]

0.037 ± 0.005 TYP
[0.94 ± 0.13]

0.005
[0.13]
MIN TYP

0.055 ± 0.005 TYP
[1.40 ± 0.13]

0.200
[5.08]
MAX TYP

0.020–0.060 TYP
[0.51–1.52]

0.290–0.320
[7.37–8.13]

GLASS SEALANT

0.180 MAX
[4.57]

0.010 ± 0.002 TYP
[0.25 ± 0.05]

0.150 MIN TYP
[3.81]

0.125–0.200 TYP
[3.18–5.08]

90° ± 4°
TYP

95° ± 5°
TYP

0.080 MAX
[2.03]
BOTH ENDS

0.018 ± 0.003 TYP
[0.46 ± 0.08]

0.310–0.410
[7.87–10.41]

0.100 ± 0.010 TYP
[2.54 ± 0.25]

J16A (REV L)

Ceramic Dual-In-Line Package (J)
Order Number DM7556J
NS Package Number J16A

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Physical Dimensions inches (millimeters) (Continued)

0.092 (2.337) DIA NOM (2X)

PIN NO. 1 IDENT

0.090 (2.286) NOM

0.843–0.870 (21.41–22.10)

0.250 ±0.005 (6.350 ±0.127)

0.280 (7.112) MIN

0.030 (0.762) MAX

0.300–0.320 (7.620–8.128)

95°±5°

0.009–0.015 (0.229–0.381)

0.325 +0.040 −0.015 (8.255 +1.016 −0.381)

0.065 (1.651)

0.060 (1.524)

0.040 (1.016) TYP

0.130 ±0.005 (3.302 ±0.127)

0.145–0.200 (3.683–5.080)

90° ±4° TYP

0.020 (0.508) MIN

0.075 ±0.015 (1.905 ±0.381)

0.018 ±0.003 (0.457 ±0.076)

0.125–0.140 (3.175–3.556)

0.100 ±0.010 (2.540 ±0.254)
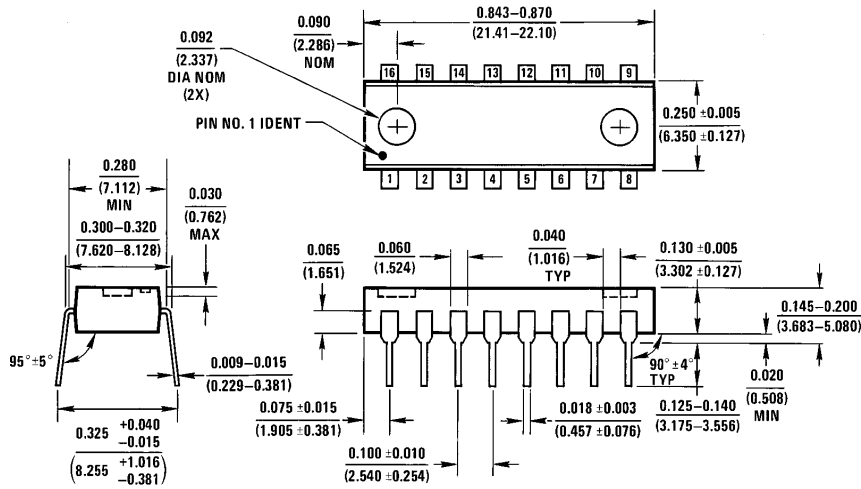
N16A (REV E)

Molded Dual-In-Line Package (N)
Order Number DM8556N
NS Package Number N16A

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