MACRONIX
INTERNATIONAL CO., LTD.

MX29LV033C

32M-BIT [4M x 8] EQUAL SECTOR FLASH MEMORY

FEATURES

GENERAL FEATURES

- 4,194,304 x 8 structure
- Sixty-four Equal Sectors with 64KB each
  - Any combination of sectors can be erased with erase suspend/resume function
- Eighteen Sector Groups
  - Provides sector group protect function to prevent program or erase operation in the protected sector group
  - Provides chip unprotected function to allow code changing
  - Provides temporary sector group unprotected function for code changing in previously protected sector groups
- Single Power Supply Operation
  - 2.7 to 3.6 volt for read, erase, and program operations
- Latch-up protected to 250mA from -1V to Vcc + 1V
- Low Vcc write inhibit is equal to or less than 1.4V
- Compatible with JEDEC standard
  - Pinout and software compatible to single power supply Flash
- **Fully compatible with MX29LV033A device**

PERFORMANCE

- High Performance
  - Fast access time: 70/90ns
  - Fast program time: 7us/byte, 36s/chip (typical)
  - Fast erase time: 0.7s/sector, 35s/chip (typical)
- Low Power Consumption
  - Low active read current: 10mA (typical) at 5MHz
  - Low standby current: 200nA (typical)
- Minimum 100,000 erase/program cycle
- 10-year data retention

SOFTWARE FEATURES

- Erase Suspend/ Erase Resume
  - Suspends sector erase operation to read data from or program data to another sector which is not being erased
- Status Reply
  - Data# polling & Toggle bits provide detection of program and erase operation completion
- Support Command Flash Interface (CFI)

HARDWARE FEATURES

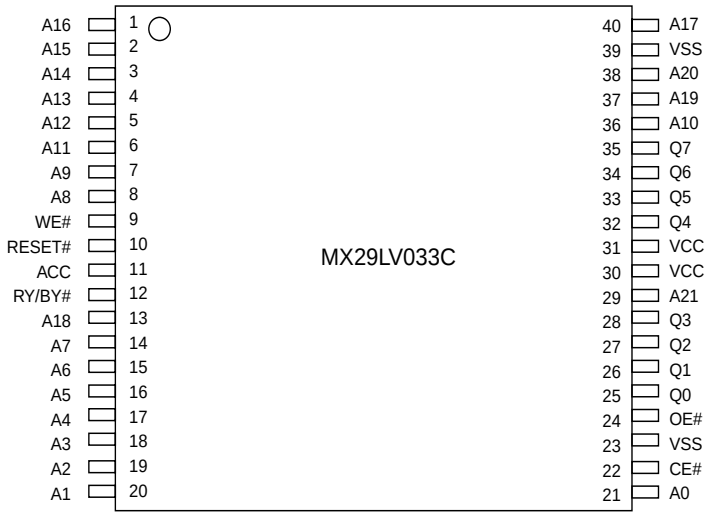
- Ready/Busy# (RY/BY#) Output
  - Provides a hardware method of detecting program and erase operation completion
- Hardware Reset (RESET#) Input
  - Provides a hardware method to reset the internal state machine to read mode
- ACC input pin
  - Provides accelerated program capability

PACKAGE

- 40-pin TSOP
- **All Pb-free devices are RoHS Compliant**

PIN CONFIGURATION

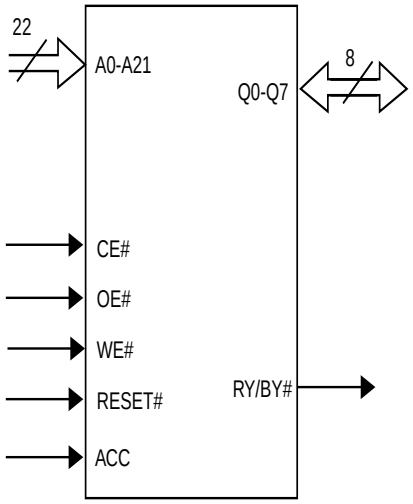
40 TSOP



PIN DESCRIPTION

SYMBOL	PIN NAME
A0~A21	Address Input
Q0~Q7	8 Data Inputs/Outputs
CE#	Chip Enable Input
WE#	Write Enable Input
OE#	Output Enable Input
RESET#	Hardware Reset Pin, Active Low
RY/BY#	Read/Busy Output
VCC	+3.3V single power supply
ACC	Hardware Acceleration Pin
VSS	Ground
NC	Pin Not Connected Internally

LOGIC SYMBOL



BLOCK DIAGRAM

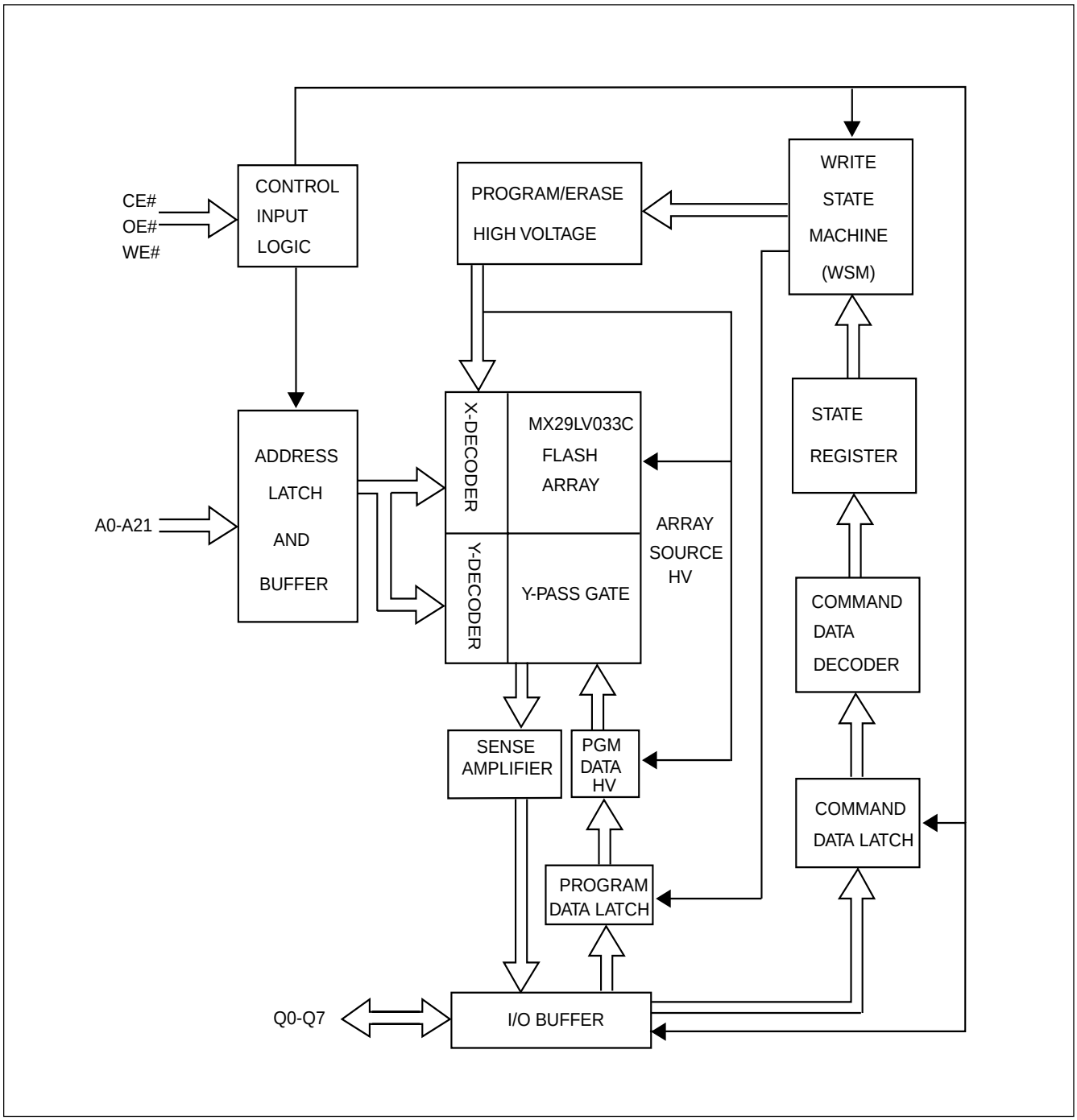


Table 1. SECTOR (GROUP) STRUCTURE

Group	Sector	A21	A20	A19	A18	A17	A16	Address Range(in hexadecimal)
SGA0	SA0	0	0	0	0	0	0	000000-00FFFF
SGA1	SA1	0	0	0	0	0	1	010000-01FFFF
SGA1	SA2	0	0	0	0	1	0	020000-02FFFF
SGA1	SA3	0	0	0	0	1	1	030000-03FFFF
SGA2	SA4	0	0	0	1	0	0	040000-04FFFF
SGA2	SA5	0	0	0	1	0	1	050000-05FFFF
SGA2	SA6	0	0	0	1	1	0	060000-06FFFF
SGA2	SA7	0	0	0	1	1	1	070000-07FFFF
SGA3	SA8	0	0	1	0	0	0	080000-08FFFF
SGA3	SA9	0	0	1	0	0	1	090000-09FFFF
SGA3	SA10	0	0	1	0	1	0	0A0000-0AFFFF
SGA3	SA11	0	0	1	0	1	1	0B0000-0BFFFF
SGA4	SA12	0	0	1	1	0	0	0C0000-0CFFFF
SGA4	SA13	0	0	1	1	0	1	0D0000-0DFFFF
SGA4	SA14	0	0	1	1	1	0	0E0000-0EFFFF
SGA4	SA15	0	0	1	1	1	1	0F0000-0FFFFF
SGA5	SA16	0	1	0	0	0	0	100000-10FFFF
SGA5	SA17	0	1	0	0	0	1	110000-11FFFF
SGA5	SA18	0	1	0	0	1	0	120000-12FFFF
SGA5	SA19	0	1	0	0	1	1	130000-13FFFF
SGA6	SA20	0	1	0	1	0	0	140000-14FFFF
SGA6	SA21	0	1	0	1	0	1	150000-15FFFF
SGA6	SA22	0	1	0	1	1	0	160000-16FFFF
SGA6	SA23	0	1	0	1	1	1	170000-17FFFF
SGA7	SA24	0	1	1	0	0	0	180000-18FFFF
SGA7	SA25	0	1	1	0	0	1	190000-19FFFF
SGA7	SA26	0	1	1	0	1	0	1A0000-1AFFFF
SGA7	SA27	0	1	1	0	1	1	1B0000-1BFFFF
SGA8	SA28	0	1	1	1	0	0	1C0000-1CFFFF
SGA8	SA29	0	1	1	1	0	1	1D0000-1DFFFF
SGA8	SA30	0	1	1	1	1	0	1E0000-1EFFFF
SGA8	SA31	0	1	1	1	1	1	1F0000-1FFFFF
SGA9	SA32	1	0	0	0	0	0	200000-20FFFF
SGA9	SA33	1	0	0	0	0	1	210000-21FFFF
SGA9	SA34	1	0	0	0	1	0	220000-22FFFF
SGA9	SA35	1	0	0	0	1	1	230000-23FFFF
SGA10	SA36	1	0	0	1	0	0	240000-24FFFF
SGA10	SA37	1	0	0	1	0	1	250000-25FFFF
SGA10	SA38	1	0	0	1	1	0	260000-26FFFF
SGA10	SA39	1	0	0	1	1	1	270000-27FFFF

Group	Sector	A21	A20	A19	A18	A17	A16	Address Range(in hexadecimal)
SGA11	SA40	1	0	1	0	0	0	280000-28FFFF
SGA11	SA41	1	0	1	0	0	1	290000-29FFFF
SGA11	SA42	1	0	1	0	1	0	2A0000-2AFFFF
SGA11	SA43	1	0	1	0	1	1	2B0000-2BFFFF
SGA12	SA44	1	0	1	1	0	0	2C0000-2CFFFF
SGA12	SA45	1	0	1	1	0	1	2D0000-2DFFFF
SGA12	SA46	1	0	1	1	1	0	2E0000-2EFFFF
SGA12	SA47	1	0	1	1	1	1	2F0000-2FFFFF
SGA13	SA48	1	1	0	0	0	0	300000-30FFFF
SGA13	SA49	1	1	0	0	0	1	310000-31FFFF
SGA13	SA50	1	1	0	0	1	0	320000-32FFFF
SGA13	SA51	1	1	0	0	1	1	330000-33FFFF
SGA14	SA52	1	1	0	1	0	0	340000-34FFFF
SGA14	SA53	1	1	0	1	0	1	350000-35FFFF
SGA14	SA54	1	1	0	1	1	0	360000-36FFFF
SGA14	SA55	1	1	0	1	1	1	370000-37FFFF
SGA15	SA56	1	1	1	0	0	0	380000-38FFFF
SGA15	SA57	1	1	1	0	0	1	390000-39FFFF
SGA15	SA58	1	1	1	0	1	0	3A0000-3AFFFF
SGA15	SA59	1	1	1	0	1	1	3B0000-3BFFFF
SGA16	SA60	1	1	1	1	0	0	3C0000-3CFFFF
SGA16	SA61	1	1	1	1	0	1	3D0000-3DFFFF
SGA16	SA62	1	1	1	1	1	0	3E0000-3EFFFF
SGA17	SA63	1	1	1	1	1	1	3F0000-3FFFFF

Table 2. BUS OPERATION--1

Mode Select	RESET#	CE#	WE#	OE#	Address	Data (I/O) Q0~Q7
Device Reset	L	X	X	X	X	HighZ
Standby Mode	Vcc±0.3V	Vcc±0.3V	X	X	X	HighZ
Output Disable	H	L	H	H	X	HighZ
Read Mode	H	L	H	L	AIN	DOUT
Write (Note1)	H	L	L	H	AIN	DIN
Temporary Sector-Group Unprotect	Vhv	X	X	X	AIN	DIN
Sector-Group Protect (Note2)	Vhv	L	L	H	Sector Address, A6=L, A1=H, A0=L	DIN, DOUT
Chip Unprotect (Note2)	Vhv	L	L	H	Sector Address, A6=H, A1=H, A0=L	DIN, DOUT

Notes:
1. All sectors will be unprotected if ACC=Vhv.
2. Q0~Q15 are input (DIN) or output (DOUT) pins according to the requests of command sequence, sector protection, or data polling algorithm.
3. AM: MSB of address.

BUS OPERATION--2

Item	Control Input			AM to A12	A11 to A10	A9	A8 to A7	A6	A5 to A2	A1	A0	Q0~Q7
	CE#	WE#	OE#									
Sector Lock Status Verification	L	H	L	SA	x	V_{hv}	x	L	x	H	L	01h or 00h (Note1)
Read Silicon ID Manufacturer Code	L	H	L	x	x	V_{hv}	x	L	x	L	L	C2H
Read Silicon ID	L	H	L	x	x	V_{hv}	x	L	x	L	H	A3H

Notes:
1. Sector unprotected code:00h. Sector protected code:01h.
2. AM: MSB of address.

WRITE COMMANDS/COMMAND SEQUENCES

To write a command to the device, system must drive WE# and CE# to Vil, and OE# to Vih. In a command cycle, all address are latched at the later falling edge of CE# and WE#, and all data are latched at the earlier rising edge of CE# and WE#.

Figure 1 illustrates the AC timing waveform of a write command, and Table 3 defines all the valid command sets of the device. System is not allowed to write invalid commands not defined in this datasheet. Writing an invalid command will bring the device to an undefined state.

REQUIREMENTS FOR READING ARRAY DATA

Read array action is to read the data stored in the array. While the memory device is in powered up or has been reset, it will automatically enter the status of read array. If the microprocessor wants to read the data stored in the array, it has to drive CE# (device enable control pin) and OE# (Output control pin) as Vil, and input the address of the data to be read into address pin at the same time. After a period of read cycle (Tce or Taa), the data being read out will be displayed on output pin for microprocessor to access. If CE# or OE# is Vih, the output will be in tri-state, and there will be no data displayed on output pin at all.

After the memory device completes embedded operation (automatic Erase or Program), it will automatically return to the status of read array, and the device can read the data in any address in the array. In the process of erasing, if the device receives the Erase suspend command, erase operation will be stopped temporarily after a period of time no more than Tready1 and the device will return to the status of read array. At this time, the device can read the data stored in any address except the sector being erased in the array. In the status of erase suspend, if user wants to read the data in the sectors being erased, the device will output status data onto the output. Similarly, if program command is issued after erase suspend, after program operation is completed, system can still read array data in any address except the sectors to be erased.

The device needs to issue reset command to enable read array operation again in order to arbitrarily read the data in the array in the following two situations:

1. In program or erase operation, the programming or erasing failure causes Q5 to go high.

2. The device is in auto select mode or CFI mode.

In the two situations above, if reset command is not issued, the device is not in read array mode and system must issue reset command before reading array data.

ACCELERATED PROGRAM OPERATION

The accelerated program can improve programming performance compared with byte program. By applying Vhv on ACC pin, the device will enter accelerated program and draw current no more than Icw from ACC pin. Removing the Vhv from ACC pin will put the device back to normal operation (not accelerated).

RESET# OPERATION

Driving RESET# pin low for a period more than Trp will reset the device back to read mode. If the device is in program or erase operation, the reset operation will take at most a period of Tready1 for the device to return to read array mode. Before the device returns to read array mode, the RY/BY# pin remains low (busy status).

When RESET# pin is held at GND±0.3V, the device consumes standby current(Isb).However, device draws larger current if RESET# pin is held at Vil but not within GND±0.3V.

It is recommended that the system to tie its reset signal to RESET# pin of flash memory, so that the flash memory will be reset during system reset and allows system to read boot code from flash memory.

SECTOR GROUP PROTECT OPERATION

When a sector group is protected, program or erase operation will be disabled on these sectors. MX29LV033C provides two methods for sector group protection.

Once the sector group is protected, the sector group remains protected until next chip unprotect, or is temporarily unprotected by asserting RESET# pin at Vhv. Refer to temporary sector group unprotect operation for further details.

The first method is by applying Vhv on RESET# pin. Refer to Figure 13 for timing diagram and Figure 14 for the algorithm for this method.

The other method is asserting Vhv on A9 and OE# pins, with A6 and CE# at Vil. The protection operation begins at the falling edge of WE# and terminates at the rising edge. Contact Macronix for details.

CHIP UNPROTECT OPERATION

MX29LV033C provides two methods for chip unprotect. The chip unprotect operation unprotects all sectors within the device. It is recommended to protect all sectors before activating chip unprotect mode. All sector groups are unprotected when shipped from the factory.

The first method is by applying Vhv on RESET# pin. Refer to Figure 13 for timing diagram and Figure 14 for algorithm of the operation.

The other method is asserting Vhv on A9 and OE# pins, with A6 at Vih and CE# at Vil (see Table 2). The unprotect operation begins at the falling edge of WE# and terminates at the rising edge. Contact Macronix for details.

TEMPORARY SECTOR GROUP UNPROTECT OPERATION

System can apply RESET# pin at Vhv to place the device in temporary unprotect mode. In this mode, previously protected sectors can be programmed or erased just as it is unprotected. The devices returns to normal operation once Vhv is removed from RESET# pin and previously protected sectors are again protected.

AUTOMATIC SELECT OPERATION

When the device is in Read array mode, erase-suspended read array mode or CFI mode, user can issue read silicon ID command to enter read silicon ID mode. After entering read silicon ID mode, user can query several silicon IDs continuously and does not need to issue read silicon ID mode again. When A0 is Low, device will output Macronix Manufacture ID C2. When A0 is high, device will output Device ID. In read silicon ID mode, issuing reset command will reset device back to read array mode or erase-suspended read array mode.

Another way to enter read silicon ID is to apply high voltage on A9 pin with CE#, OE#, A6 and A1 at Vil. While the high voltage of A9 pin is discharged, device will automatically leave read silicon ID mode and go back to read array mode or erase-suspended read array mode. When A0 is Low, device will output Macronix Manufacture ID C2. When A0 is high, device will output Device ID.

VERIFY SECTOR GROUP PROTECT STATUS OPERATION

MX29LV033C provides hardware sector protection against Program and Erase operation for protected sectors. The sector protect status can be read through Sector Protect Verify command. This method requires V_{hv} on A9 pin, Vih on WE# and A1 pins, Vil on CE#, OE#, A6 and A0 pins, and sector address on A12 to A20 pins. If the read out data is 01H, the designated sector is protected. Oppositely, if the read out data is 00H, the designated sector is not protected.

DATA PROTECTION

To avoid accidental erasure or programming of the device, the device is automatically reset to read array mode during power up. Besides, only after successful completion of the specified command sets will the device begin its erase or program operation.

Other features to protect the data from accidental alternation are described as followed.

LOW VCC WRITE INHIBIT

The device refuses to accept any write command when Vcc is less than 1.4V. This prevents data from spuriously altered. The device automatically resets itself when Vcc is lower than 1.4V and write cycles are ignored until Vcc is greater than 1.4V. System must provide proper signals on control pins after Vcc is larger than 1.4V to avoid unintentional program or erase operation

WRITE PULSE "GLITCH" PROTECTION

CE#, WE#, OE# pulses shorter than 5ns are treated as glitches and will not be regarded as an effective write cycle.

LOGICAL INHIBIT

A valid write cycle requires both CE# and WE# at Vil with OE# at Vih. Write cycle is ignored when either CE# at Vih, WE# a Vih, or OE# at Vil.

POWER-UP SEQUENCE

Upon power up, MX29LV033C is placed in read array mode. Furthermore, program or erase operation will begin only after successful completion of specified command sequences.

POWER-UP WRITE INHIBIT

When WE#, CE# is held at Vil and OE# is held at Vih during power up, the device ignores the first command on the rising edge of WE#.

POWER SUPPLY DECOUPLING

A 0.1uF capacitor should be connected between the Vcc and GND to reduce the noise effect.

TABLE 3. MX29LV033C COMMAND DEFINITIONS

Command		Read Mode	Reset Mode	Automatic Select			Program	Chip Erase	Sector Erase	CFI Read	Erase Suspend	Erase Resume
				Silicon ID	Device ID	Protect Verify						
1st Bus Cyc	Addr	Addr	XXX	XXX	XXX	XXX	XXX	XXX	XXX	XXX	XXX	XXX
	Data	Data	F0	AA	AA	AA	AA	AA	AA	98	B0	30
2nd Bus Cyc	Addr			XXX	XXX	XXX	XXX	XXX	XXX			
	Data			55	55	55	55	55	55			
3rd Bus Cyc	Addr			XXX	XXX	XXX	XXX	XXX	XXX			
	Data			90	90	90	A0	80	80			
4th Bus Cyc	Addr			X00	X01	(Sector) X02	Addr	XXX	XXX			
	Data			C2	A3	00/01	Data	AA	AA			
5th Bus Cyc	Addr							XXX	XXX			
	Data							55	55			
6th Bus Cyc	Addr							XXX	Sector			
	Data							10	30			

RESET

In the following situations, executing reset command will reset device back to read array mode:

- Among erase command sequence (before the full command set is completed)
- Sector erase time-out period
- Erase fail (while Q5 is high)
- Among program command sequence (before the full command set is completed, erase-suspended program included)
- Program fail (while Q5 is high, and erase-suspended program fail is included)
- Read silicon ID mode
- Sector protect verify
- CFI mode

While device is at the status of program fail or erase fail (Q5 is high), user must issue reset command to reset device back to read array mode. While the device is in read silicon ID mode, sector protect verify or CFI mode, user must issue reset command to reset device back to read array mode.

When the device is in the progress of programming (not program fail) or erasing (not erase fail), device will ignore reset command.

AUTOMATIC SELECT COMMAND SEQUENCE

Automatic Select mode is used to access the manufacturer ID, device ID and to verify whether or not a sector is protected. The automatic select mode has four command cycles. The first two are unlock cycles, and followed by a specific command. The fourth cycle is a normal read cycle, and user can read at any address any number of times without entering another command sequence. The reset command is necessary to exit the Automatic Select mode and back to read array. The following table shows the identification code with corresponding address.

	Address	Data (Hex)	Representation
Manufacturer ID	X00	C2	
Device ID	X02	A3	
Sector Protect Verify	(Sector address) X 04	00/01	Unprotected/protected

There is an alternative method to that shown in Table 2, which is intended for EPROM programmers and requires Vhv on address bit A9.

AUTOMATIC PROGRAMMING

The MX29LV033C can provide the user program function by the form of Byte-Mode. As long as the users enter the right cycle defined in the Table.3 (including 2 unlock cycles and A0H), any data user inputs will automatically be programmed into the array.

Once the program function is executed, the internal write state controller will automatically execute the algorithms and timings necessary for program and verification, which includes generating suitable program pulse, verifying whether the threshold voltage of the programmed cell is high enough and repeating the program pulse if any of the cells does not pass verification. Meanwhile, the internal control will prohibit the programming to cells that pass verification while the other cells fail in verification in order to avoid over-programming. With the internal write state controller, the device requires the user to write the program command and data only.

Programming will only change the bit status from "1" to "0". That is to say, it is impossible to convert the bit status from "0" to "1" by programming. Meanwhile, the internal write verification only detects the errors of the "1" that is not successfully programmed to "0".

Any command written to the device during programming will be ignored except hardware reset, which will terminate the program operation after a period of time no more than Tready1. When the embedded program algorithm is complete or the program operation is terminated by hardware reset, the device will return to the reading array data mode.

The typical chip program time at room temperature of the MX29LV033C is less than 36 seconds.

When the embedded program operation is on going, user can confirm if the embedded operation is finished or not by the following methods:

Status	Q7	Q6	Q5	RY/BY#*2
In progress*1	Q7#	Toggling	0	0
Finished	Q7	Stop toggling	0	1
Exceed time limit	Q7#	Toggling	1	0

*1: The status "in progress" means both program mode and erase-suspended program mode.
*2: RY/BY# is an open drain output pin and should be weakly connected to VDD through a pull-up resistor.
*3: When an attempt is made to program a protected sector, Q7 will output its complement data or Q6 continues to toggle for about 1us or less and the device returns to read array state without programing the data in the protected sector.

CHIP ERASE

Chip Erase is to erase all the data with "1" and "0" as all "1". It needs 6 cycles to write the action in, and the first two cycles are "unlock" cycles, the third one is a configuration cycle, the fourth and fifth are also "unlock" cycles, and the sixth cycle is the chip erase operation.

During chip erasing, all the commands will not be accepted except hardware reset or the working voltage is too low that chip erase will be interrupted. After Chip Erase, the chip will return to the state of Read Array.

When the embedded chip erase operation is on going, user can confirm if the embedded operation is finished or not by the following methods:

Status	Q7	Q6	Q5	Q2	RY/BY#
In progress	0	Toggling	0	Toggling	0
Finished	1	Stop toggling	0	1	1
Exceed time limit	0	Toggling	1	Toggling	0

SECTOR ERASE

Sector Erase is to erase all the data in a sector with "1" and "0" as all "1". It requires six command cycles to issue. The first two cycles are "unlock cycles", the third one is a configuration cycle, the fourth and fifth are also "unlock cycles" and the sixth cycle is the sector erase command. After the sector erase command sequence is issued, there is a time-out period of 50us counted internally. During the time-out period, additional sector address and sector erase command can be written multiply. Once user enters another sector erase command, the time-out period of 50us is recounted. If user enters any command other than sector erase or erase suspend during time-out period, the erase command would be aborted and the device is reset to read array condition. The number of sectors could be from one sector to all sectors. After time-out period passing by, additional erase command is not accepted and erase embedded operation begins.

During sector erasing, all commands will not be accepted except hardware reset and erase suspend and user can check the status as chip erase.

When the embedded erase operation is on going, user can confirm if the embedded operation is finished or not by the following methods:

Status	Q7	Q6	Q5	Q3	Q2	RY/BY#*2
Time-out period	0	Toggling	0	0	Toggling	0
In progress	0	Toggling	0	1	Toggling	0
Finished	1	Stop toggling	0	1	1	1
Exceed time limit	0	Toggling	1	1	Toggling	0

*1: The status Q3 is the time-out period indicator. When Q3=0, the device is in time-out period and is acceptible to another sector address to be erased. When Q3=1, the device is in erase operation and only erase suspend is valid.
*2: RY/BY# is open drain output pin and should be weakly connected to VDD through a pull-up resistor.
*3: When an attempt is made to erase a protected sector, Q7 will output its complement data or Q6 continues to toggle for 100us or less and the device returned to read array status without erasing the data in the protected sector.

SECTOR ERASE SUSPEND

During sector erasure, sector erase suspend is the only valid command. If user issue erase suspend command in the time-out period of sector erasure, device time-out period will be over immediately and the device will go back to erase-suspended read array mode. If user issue erase suspend command during the sector erase is being operated, device will suspend the ongoing erase operation, and after the Tready1 (<=20us) suspend finishes and the device will enter erase-suspended read array mode. User can judge if the device has finished erase suspend through Q6, Q7, and RY/BY#.

After device has entered erase-suspended read array mode, user can read other sectors not at erase suspend by the speed of Taa; while reading the sector in erase-suspend mode, device will output its status. User can use Q6 and Q2 to judge the sector is erasing or the erase is suspended.

Status	Q7	Q6	Q5	Q3	Q2	RY/BY#
Erase suspend read in erase suspended sector	1	No toggle	0	N/A	Toggle	1
Erase suspend read in non-erase suspended sector	Data	Data	Data	Data	Data	1
Erase suspend program in non-erase suspended sector	Q7#	Toggle	0	N/A	N/A	0

When the device has suspended erasing, user can execute the command sets except sector erase and chip erase, such as read silicon ID, sector protect verify, program, CFI query and erase resume.

SECTOR ERASE RESUME

Sector erase resume command is valid only when the device is in erase suspend state. After erase resume, user can issue another erase suspend command, but there should be a 400uS interval between erase resume and the next erase suspend. If user issue infinite suspend-resume loop, or suspend-resume exceeds 1024 times, the time for erasing will increase.

QUERY COMMAND AND COMMON FLASH INTERFACE (CFI) MODE

MX29LV033C features CFI mode. Host system can retrieve the operating characteristics, structure and vendor-specified information such as identifying information, memory size, operating voltages and timing information of this device by CFI mode. The device enters the CFI Query mode when the system writes the CFI Query command, 98H, to address XXH any time the device is ready to read array data. The system can read CFI information at the addresses given in Table 4. A reset command is required to exit CFI mode and go back to ready array mode or erase suspend mode. The system can write the CFI Query command only when the device is in read mode, erase suspend, standby mode or automatic select mode.

Table 4-1. CFI mode: Identification Data Values
(All values in these tables are in hexadecimal)

Description	Address (h) (Byte Mode)	Data (h)
Query-unique ASCII string "QRY"	10	0051
	11	0052
	12	0059
Primary vendor command set and control interface ID code	13	0002
	14	0000
Address for primary algorithm extended query table	15	0040
	16	0000
Alternate vendor command set and control interface ID code (none)	17	0000
	18	0000
Address for alternate algorithm extended query table (none)	19	0000
	1A	0000

Table 4-2. CFI Mode: System Interface Data Values

Description	Address (h) (Byte Mode)	Data (h)
Vcc supply minimum program/erase voltage	1B	0027
Vcc supply maximum program/erase voltage	1C	0036
VPP supply minimum program/erase voltage (none)	1D	0000
VPP supply maximum program/erase voltage (none)	1E	0000
Typical timeout per single byte write, 2^n uS	1F	0004
Typical timeout for maximum-size buffer write, 2^n uS (not supported)	20	0000
Typical timeout per individual block erase, 2^n mS	21	000A
Typical timeout for full chip erase, 2^n mS	22	0000
Maximum timeout for byte write, 2^n times typical	23	0005
Maximum timeout for buffer write, 2^n times typical	24	0000
Maximum timeout per individual block erase, 2^n times typical	25	0004
Maximum timeout for chip erase, 2^n times typical (not supported)	26	0000

Table 4-3. CFI Mode: Device Geometry Data Values

Description	Address (h) (Byte Mode)	Data (h)
Device size = 2^n in number of bytes	27	0016
Flash device interface description (02=asynchronous x8/x16)	28	0000
	29	0000
Maximum number of bytes in buffer write = 2^n (not support)	2A	0000
	2B	0000
Number of erase regions within device	2C	0001
Index for Erase Bank Area 1	2D	003F
[2E,2D] = # of same-size sectors in region 1-1	2E	0000
[30, 2F] = sector size in multiples of 256-bytes	2F	0000
	30	0001
Index for Erase Bank Area 2	31	0000
	32	0000
	33	0000
	34	0000
Index for Erase Bank Area 3	35	0000
	36	0000
	37	0000
	38	0000
Index for Erase Bank Area 4	39	0000
	3A	0000
	3B	0000
	3C	0000

Table 4-4. CFI Mode: Primary Vendor-Specific Extended Query Data Values

Description	Address (h) (Byte Mode)	Data (h)
Query - Primary extended table, unique ASCII string, PRI	40	0050
	41	0052
	42	0049
Major version number, ASCII	43	0031
Minor version number, ASCII	44	0030
Unlock recognizes address (0= recognize, 1= don't recognize)	45	0001
Erase suspend (2= to both read and program)	46	0002
Sector protect (N= # of sectors/group)	47	0001
Temporary sector unprotect (1=supported)	48	0004
Sector protect/Chip unprotect scheme	49	0004
Simultaneous R/W operation (0=not supported)	4A	0020
Burst mode (0=not supported)	4B	0000
Page mode (0=not supported)	4C	0000

ABSOLUTE MAXIMUM STRESS RATINGS

Surrounding Temperature with Bias . . . . . -65°C to +125°C
Storage Temperature . . . . . -65°C to +150°C
Voltage Range
Vcc . . . . . -0.5 V to +4.0 V
RESET#, A9 and OE# . . . . . -0.5 V to +12.5 V
The other pins. . . . . -0.5 V to Vcc +0.5 V
Output Short Circuit Current (less than one second) . . . . . 200 mA

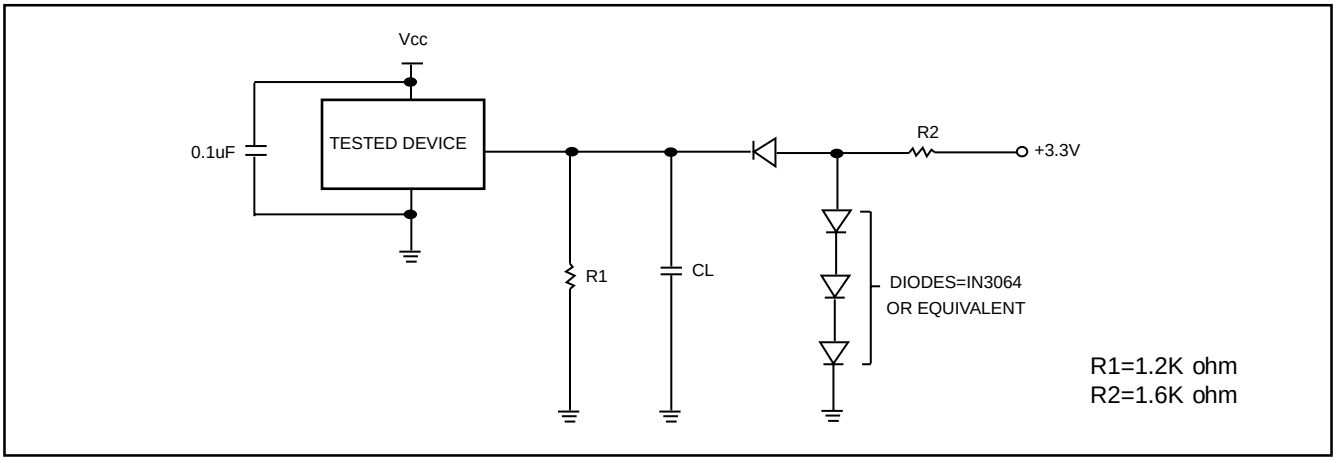
OPERATING TEMPERATURE AND VOLTAGE

Commercial (C) Grade
Surrounding Temperature (T_A). . . . . 0°C to +70°C
Industrial (I) Grade
Surrounding Temperature (T_A). . . . . -40°C to +85°C
V_{CC} Supply Voltages
V_{CC} range. . . . . +2.7 V to 3.6 V

DC CHARACTERISTICS

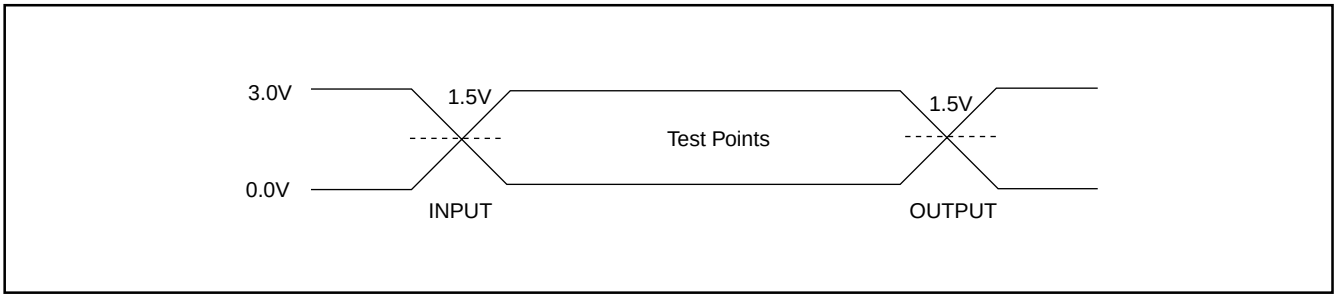
Symbol	Description	Min	Typ	Max	Remark
Iilk	Input Leak			±1.0uA	
Iilk9	A9 Leak			35uA	A9=12.5V
Iolk	Output Leak			±1.0uA	
Icr1	Read Current(5MHz)		10mA	16mA	CE#=Vil, OE#=Vih
Icr2	Read Current(1MHz)		2mA	4mA	CE#=Vil, OE#=Vih
Icw	Write Current		15mA	30mA	CE#=Vil, OE#=Vih, WE#=Vil
Isb	Standby Current		0.2uA	15uA	Vcc=Vcc max, other pin disable
Isbr	Reset Current		0.2uA	15uA	Vcc=Vccmax, Reset# enable, other pin disable
Isbs	Sleep Mode Current		0.2uA	15uA	
Icp1	Accelerated Pgm Current, ACC pin		5mA	10mA	CE#=Vil, OE#=Vih,
Icp2	Accelerated Pgm Current, Vcc pin		15mA	30mA	CE#=Vil, OE#=Vih,
Vil	Input Low Voltage	-0.5V		0.8V	
Vih	Input High Voltage	0.7xVcc		Vcc+0.3V	
Vhv	Very High Voltage for hardware Protect/Unprotect/Accelerated Program/Auto Select/Temporary Unprotect	11.5V		12.5V	
Vol	Output Low Voltage			0.45V	Iol=4.0mA
Voh1	Ouput High Voltage	0.85xVcc			Ioh1=-2mA
Voh2	Ouput High Voltage	Vcc-0.4V			Ioh2=-100uA

SWITCHING TEST CIRCUITS



Test Condition
Output Load : 1 TTL gate
Output Load Capacitance,CL : 30pF(70nS)/100pF(90nS)
Rise/Fall Times : 5nS
In/Out reference levels :1.5V

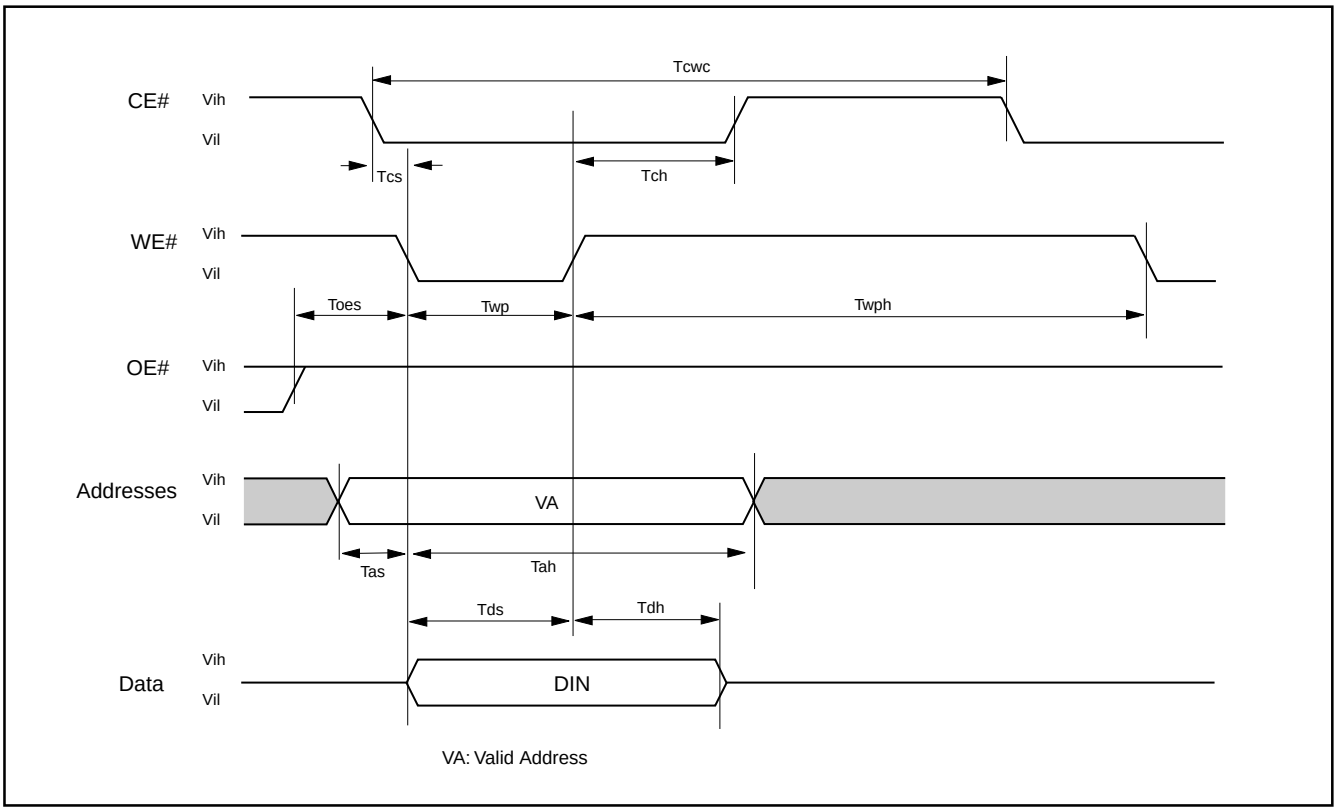
SWITCHING TEST WAVEFORMS



AC CHARACTERISTICS

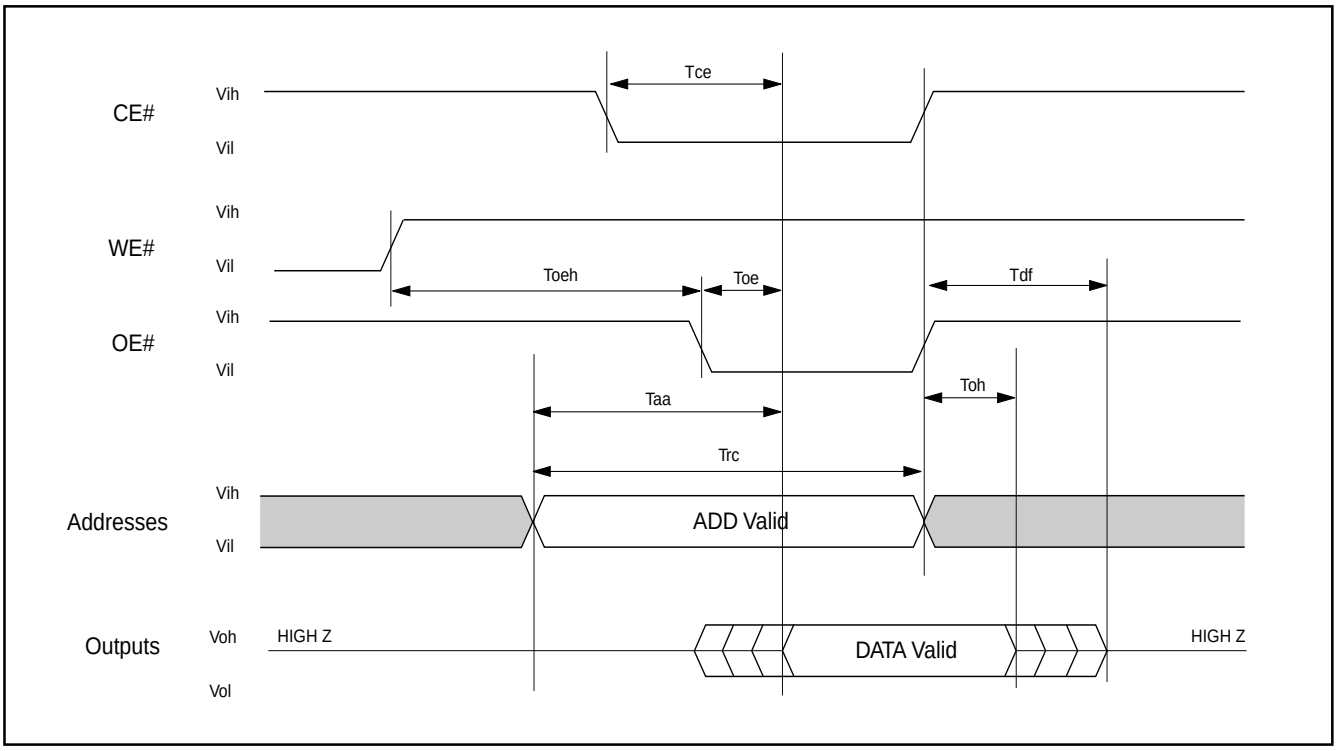
Symbol	Description		Min	Typ	Max	Unit
Taa	Valid data output after address				70/90	nS
Tce	Valid data output after CE# low				70/90	nS
Toe	Valid data output after OE# low				30/40	nS
Tdf	Data output floating after OE# high				25/30	nS
Toh	Output hold time from the earliest rising edge of address, CE#, OE#		0			nS
Trc	Read period time		70/90			nS
Twc	Write period time		70/90			nS
Tcwc	Command write period time		70/90			nS
Tas	Address setup time		0			nS
Tah	Address hold time		45			nS
Tds	Data setup time		35/45			nS
Tdh	Data hold time		0			nS
Tvcs	Vcc setup time		50			uS
Tcs	Chip enable Setup time		0			nS
Tch	Chip enable hold time		0			nS
Toes	Output enable setup time		0			nS
Toeh	Output enable hold time	Read	0			nS
Toeh		Toggle & Data# Polling	10			nS
Tws	WE# setup time		0			nS
Twh	WE# hold time		0			nS
Tcep	CE# pulse width		35/45			nS
Tceph	CE# pulse width high		30			nS
Twp	WE# pulse width		30/45			nS
Twph	WE# pulse width high		30			nS
Tbusy	Program/Erase active time by RY/BY#			90		nS
Tghwl	Read recover time before write		0			nS
Tghel	Read recover time before write		0			nS
Twhwh1	Program operation			9		uS
Twhwh1	Acc program operation			7		uS
Twhwh2	Sector erase operation			0.9		sec
Tbal	Sector add hold time				50	uS

Figure 1. COMMAND WRITE OPERATION



READ/RESET OPERATION

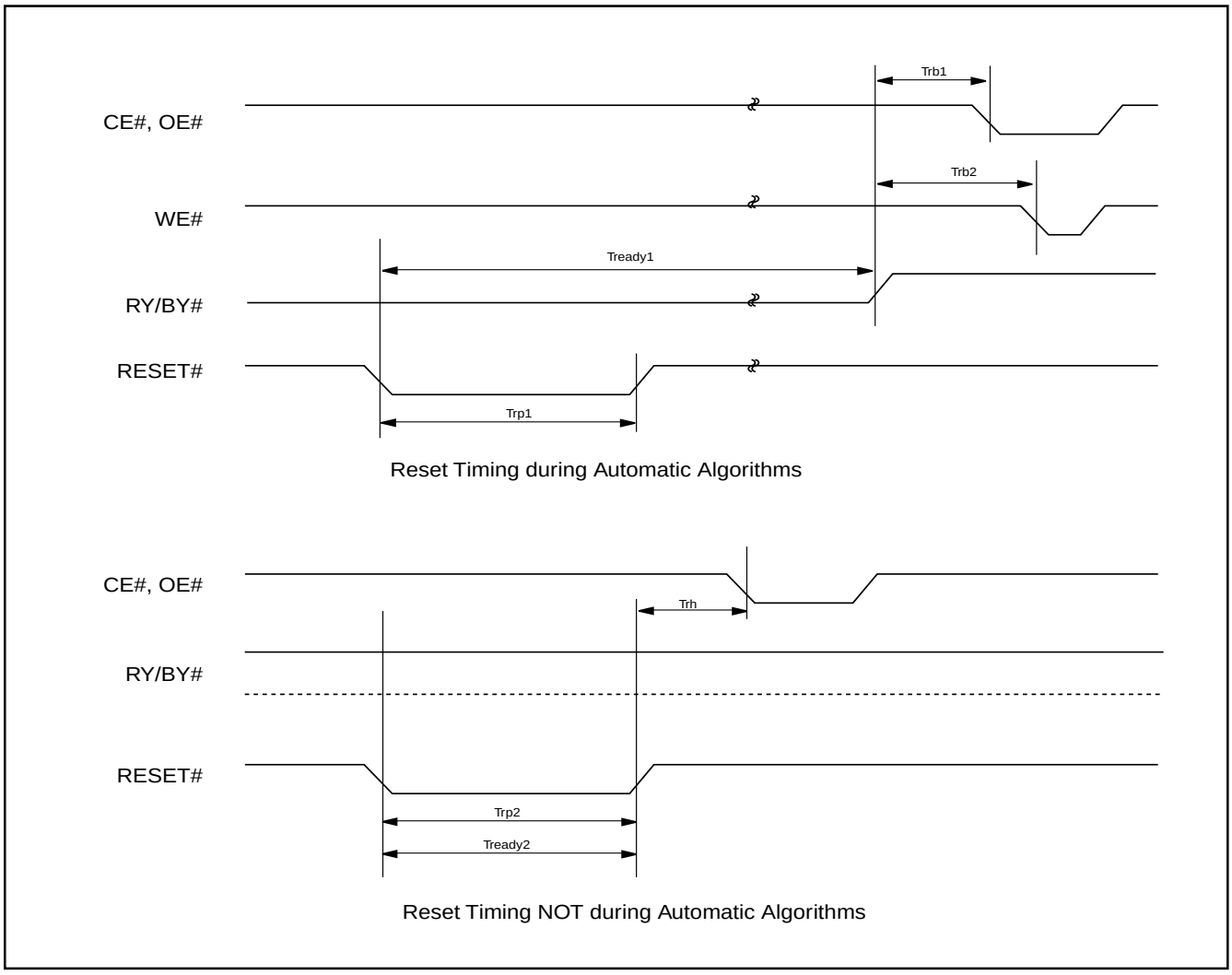
Figure 2. READ TIMING WAVEFORMS



AC CHARACTERISTICS

Item	Description	Setup	Speed	Unit
Trp1	RESET# Pulse Width (During Automatic Algorithms)	MIN	10	uS
Trp2	RESET# Pulse Width (NOT During Automatic Algorithms)	MIN	500	nS
Trh	RESET# High Time Before Read	MIN	70	nS
Trb1	RY/BY# Recovery Time (to CE#, OE# go low)	MIN	0	nS
Trb2	RY/BY# Recovery Time (to WE# go low)	MIN	50	nS
Tready1	RESET# PIN Low (During Automatic Algorithms) to Read or Write	MAX	20	uS
Tready2	RESET# PIN Low (NOT During Automatic Algorithms) to Read or Write	MAX	500	nS

Figure 3. RESET# TIMING WAVEFORM



ERASE/PROGRAM OPERATION

Figure 4. AUTOMATIC CHIP ERASE TIMING WAVEFORM

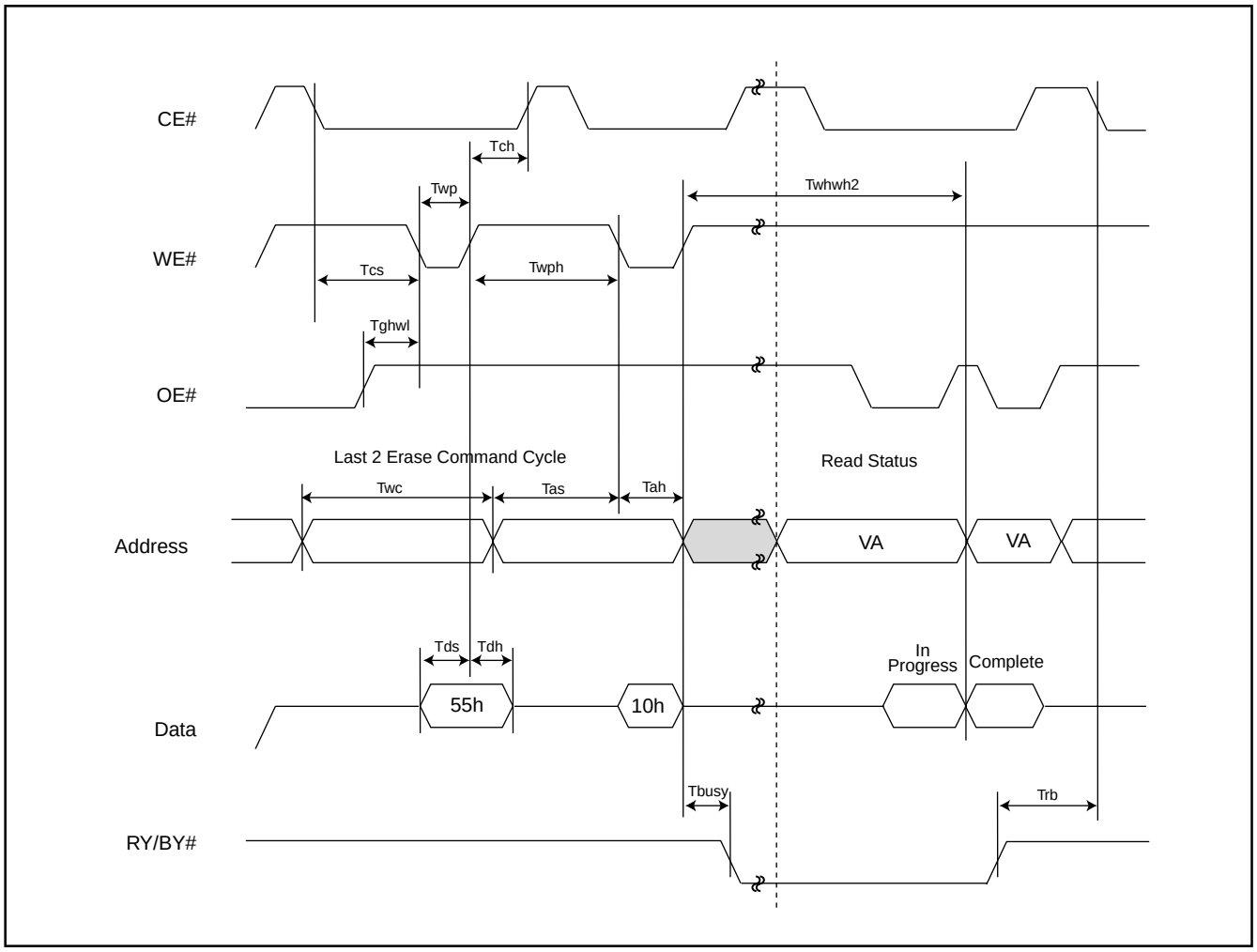


Figure 5. AUTOMATIC CHIP ERASE ALGORITHM FLOWCHART

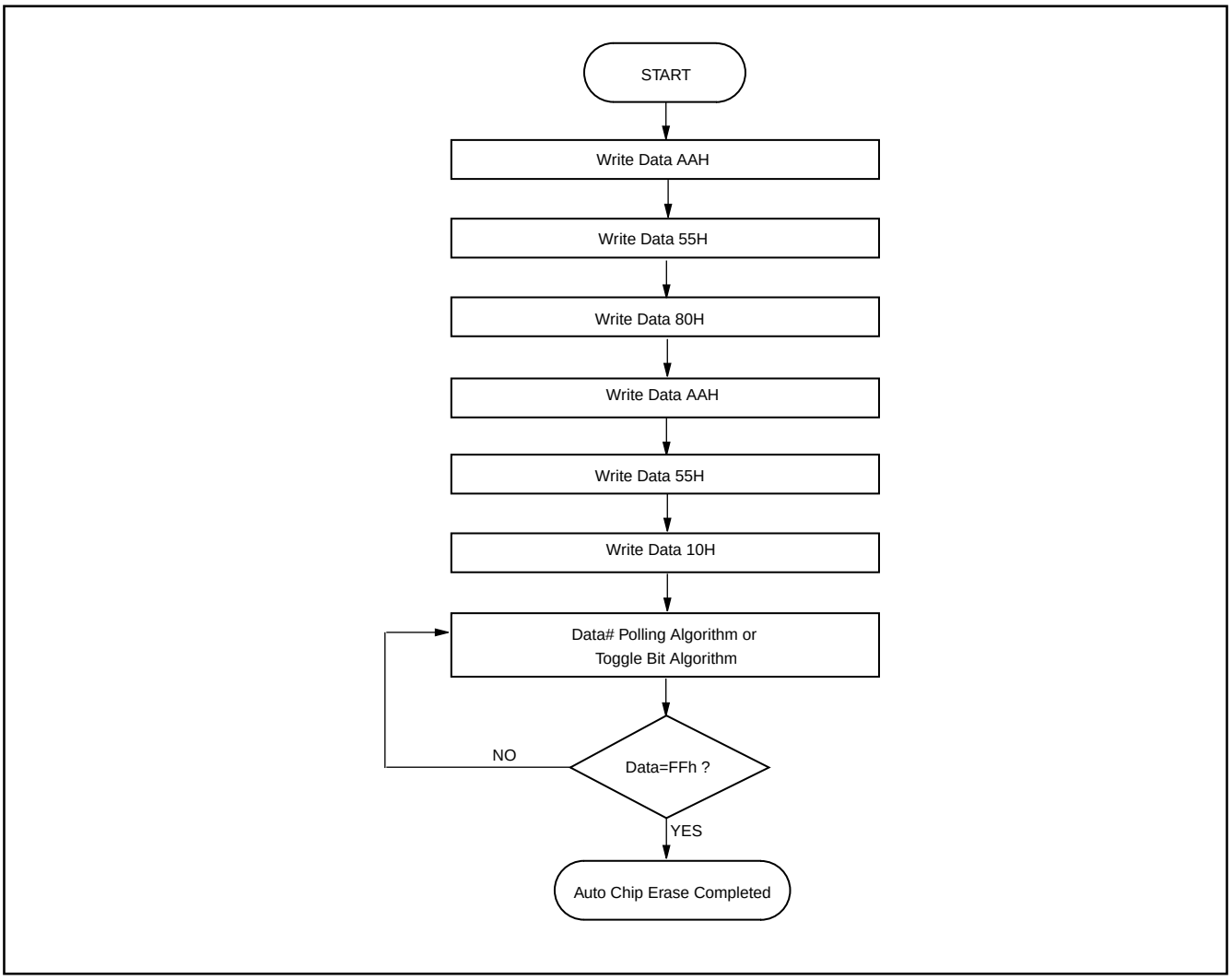


Figure 6. AUTOMATIC SECTOR ERASE TIMING WAVEFORM

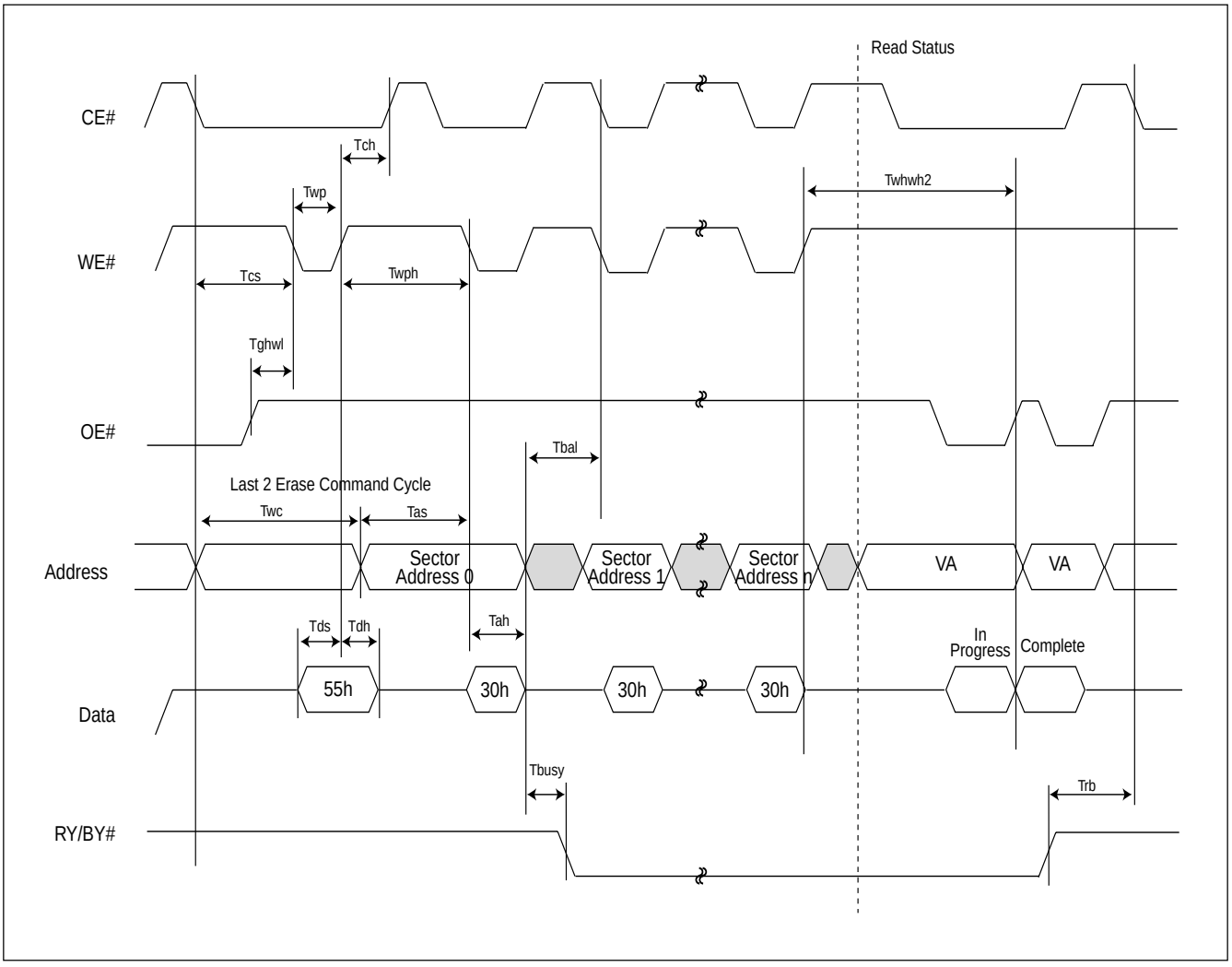


Figure 7. AUTOMATIC SECTOR ERASE ALGORITHM FLOWCHART

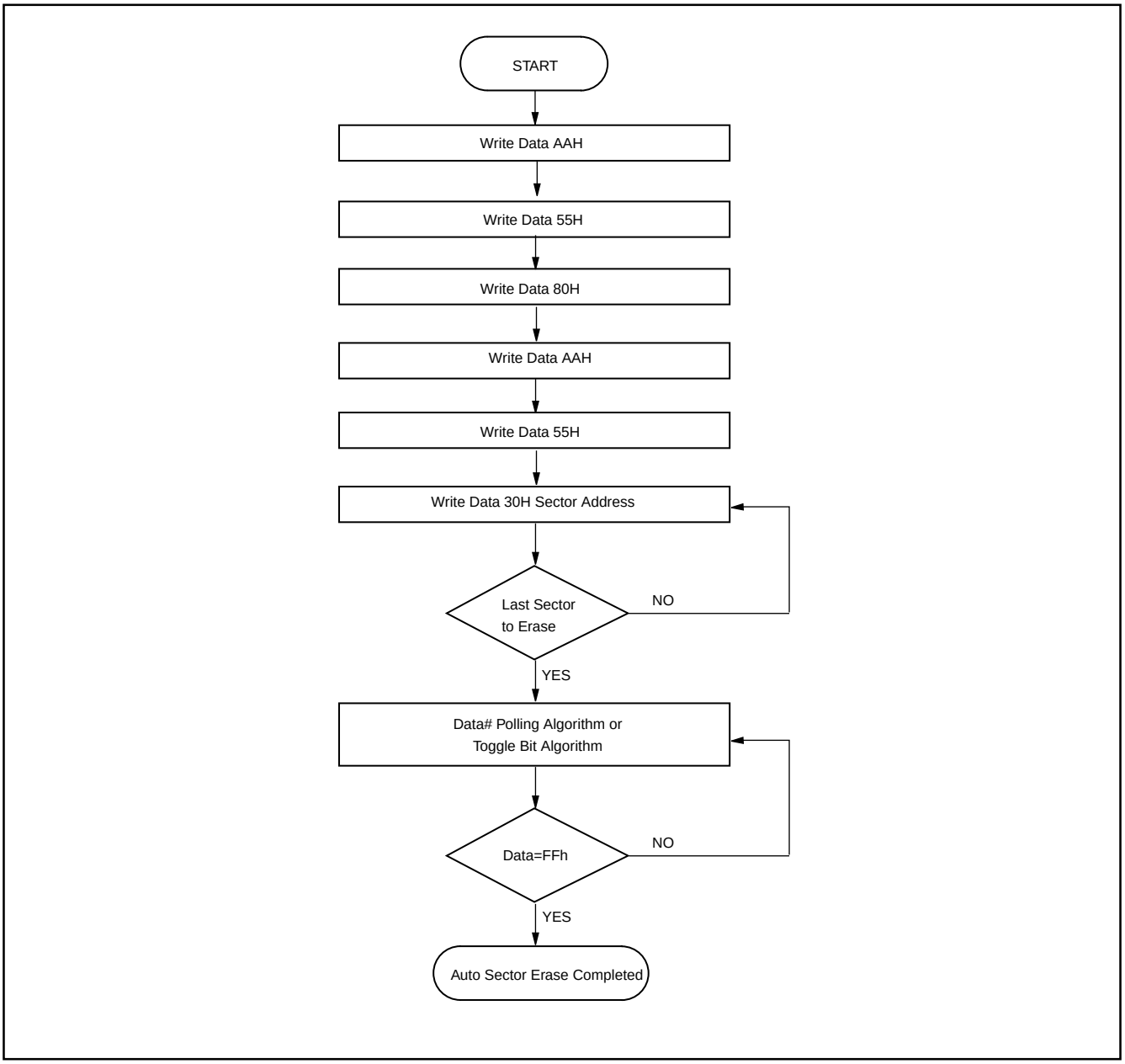


Figure 8. ERASE SUSPEND/RESUME FLOWCHART

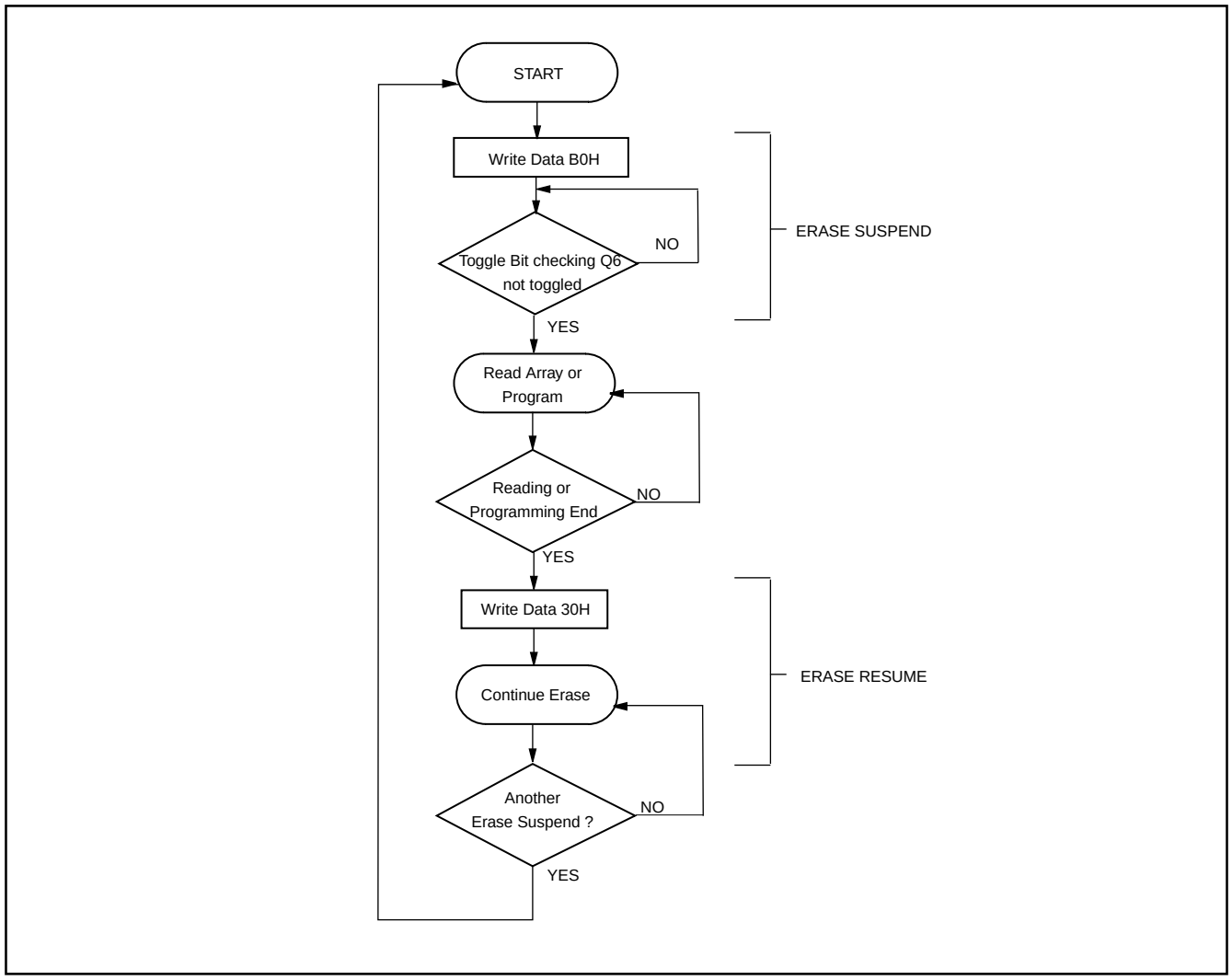


Figure 9. AUTOMATIC PROGRAM TIMING WAVEFORMS

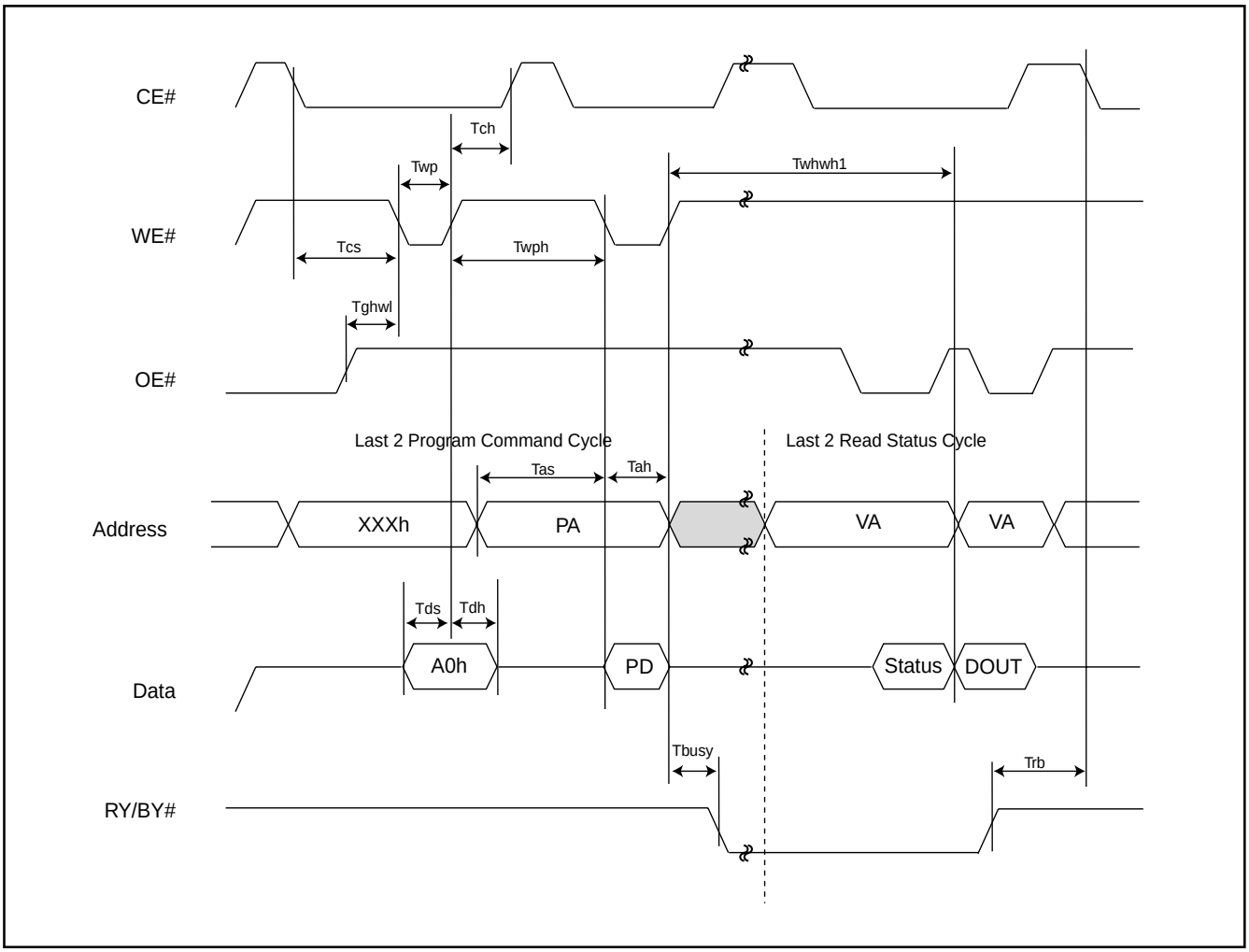


Figure 10. Accelerated Program Timing Diagram

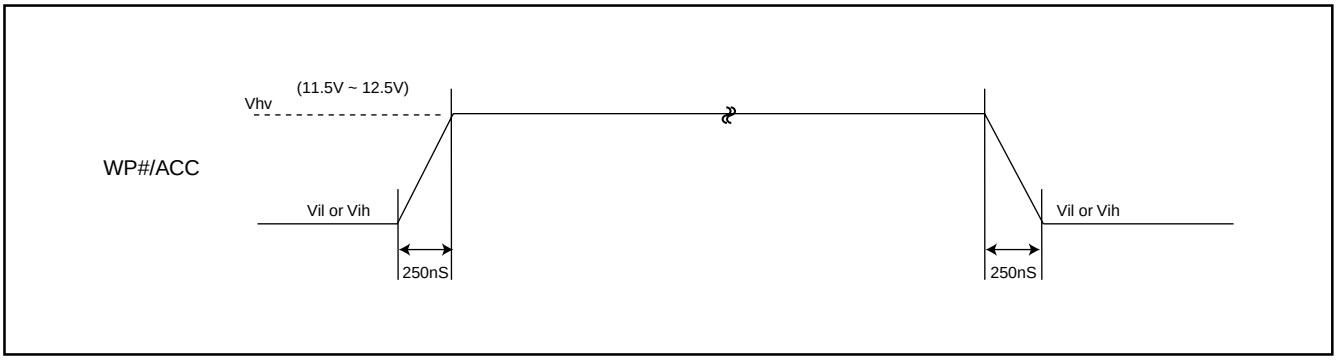


Figure 11. CE# CONTROLLED WRITE TIMING WAVEFORM

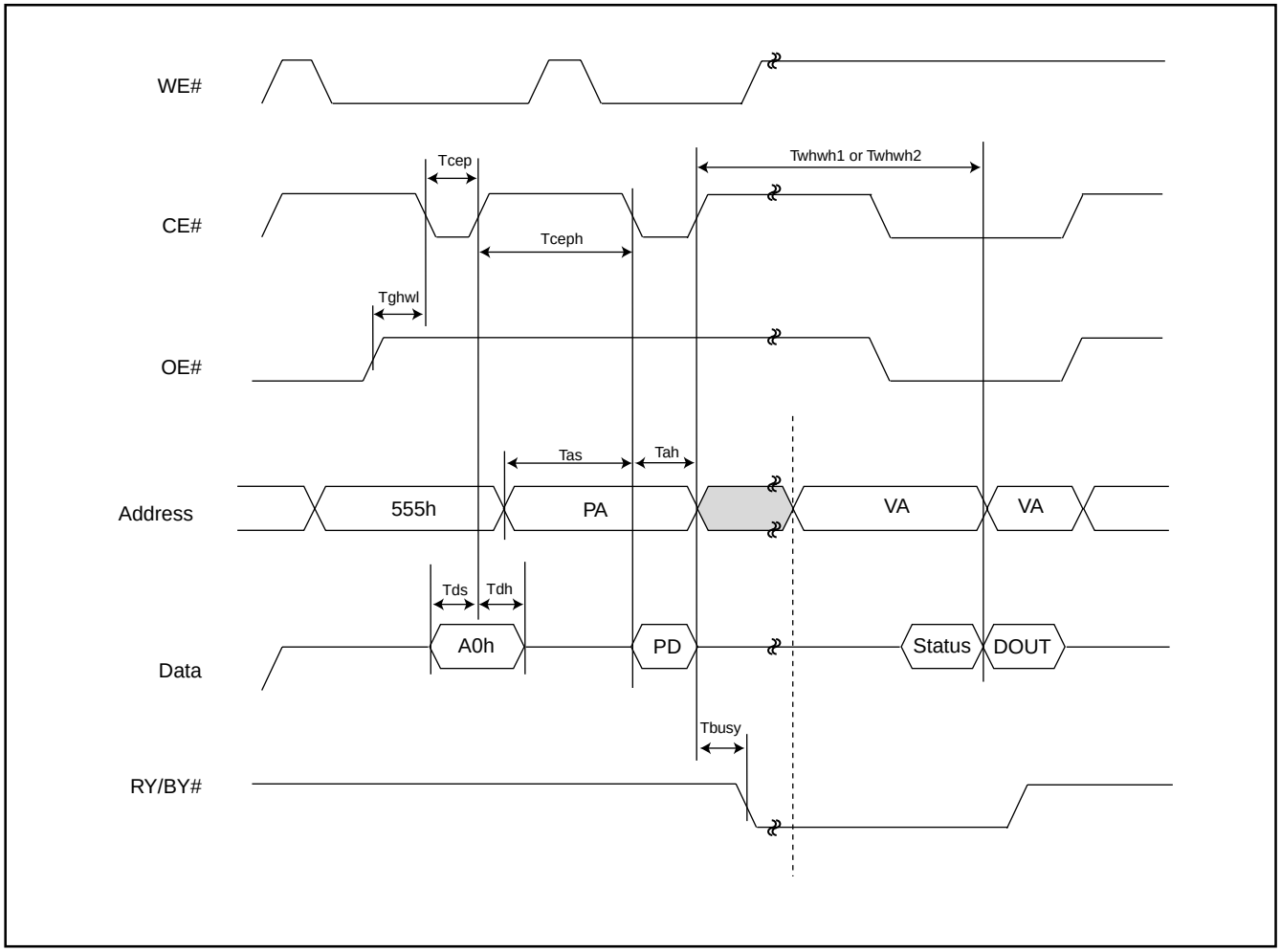
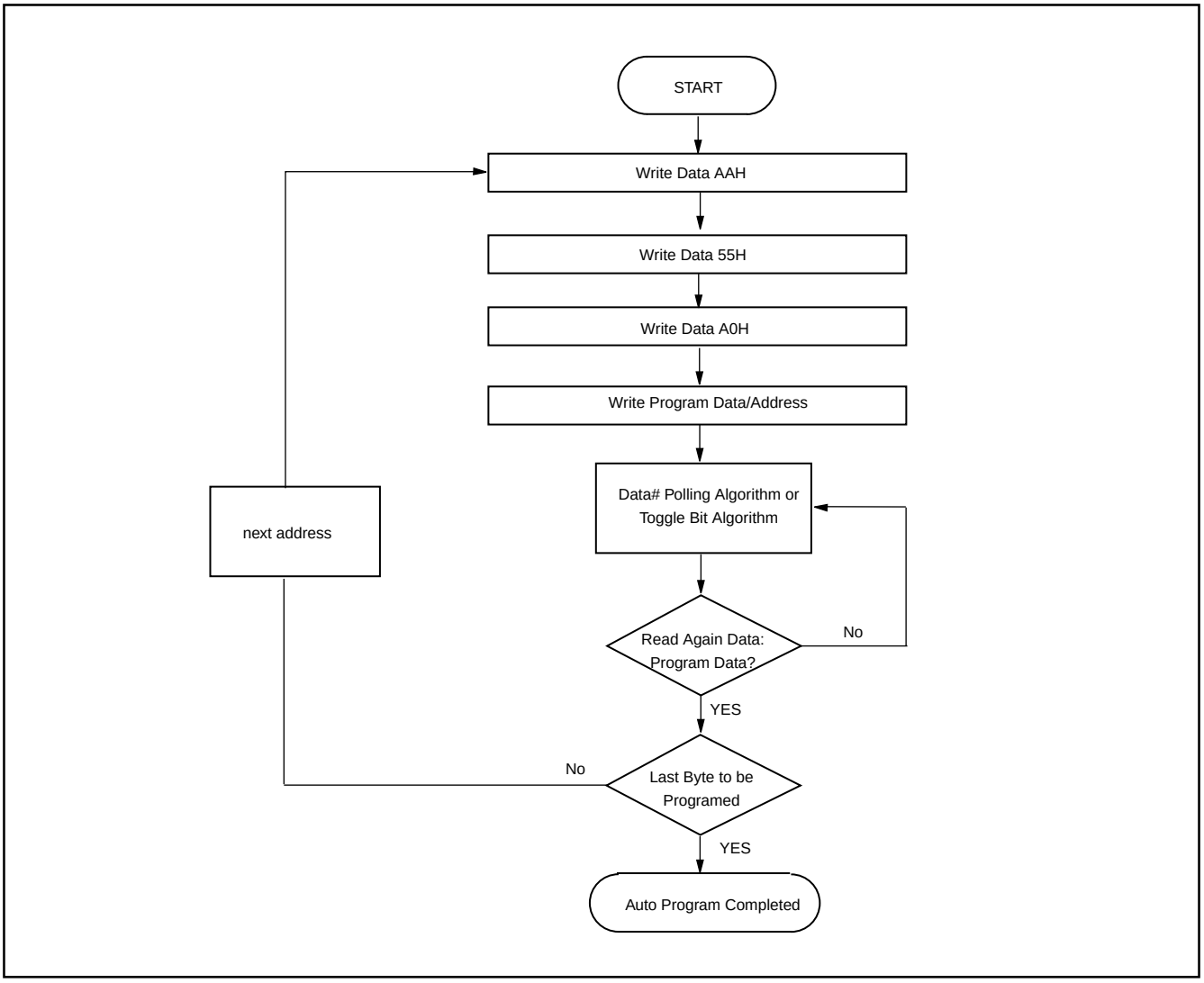


Figure 12. AUTOMATIC PROGRAMMING ALGORITHM FLOWCHART



SECTOR GROUP PROTECT/CHIP UNPROTECT

Figure 13. Sector Group Protect/Chip Unprotect Waveform (RESET# Control)

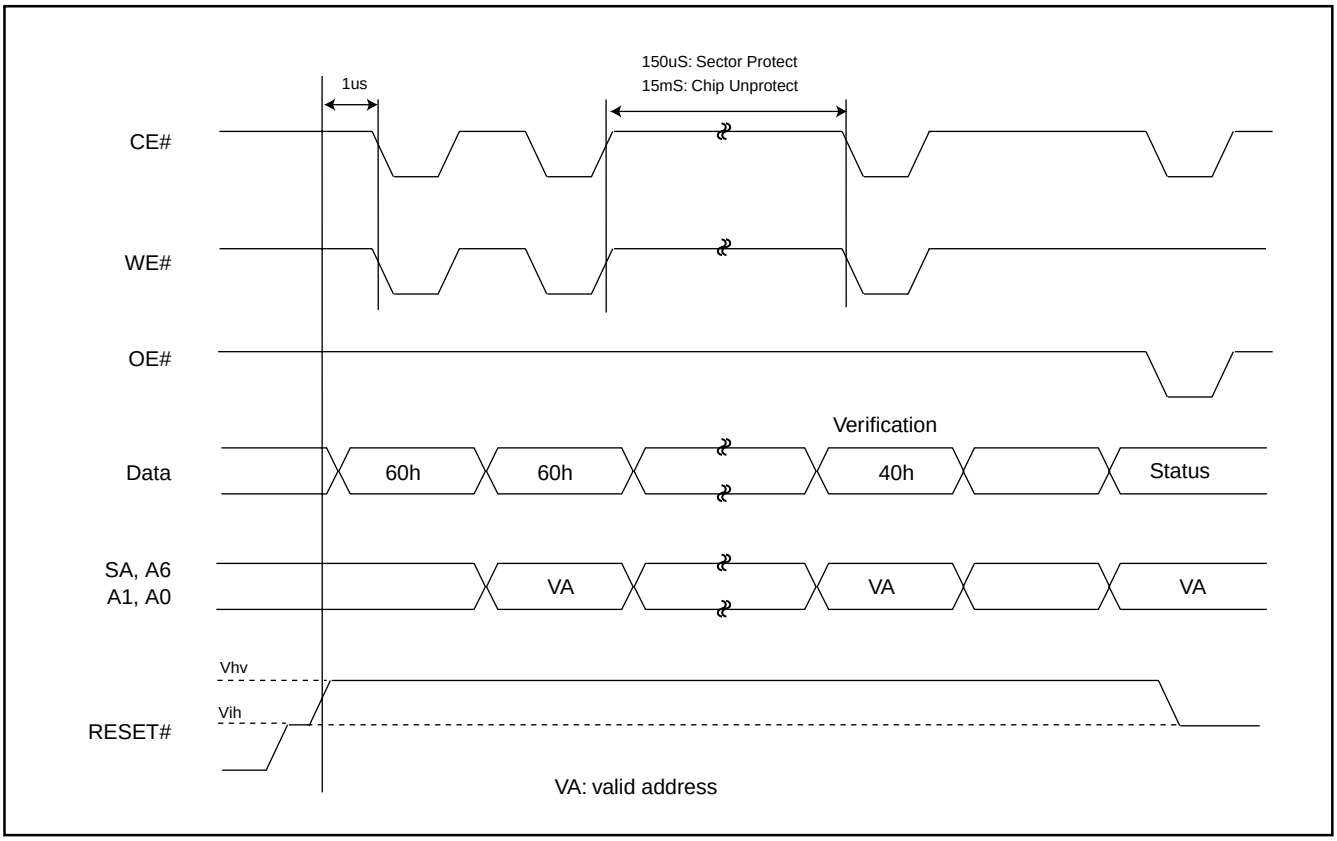


Figure 14-1. IN-SYSTEM SECTOR GROUP PROTECT WITH RESET#=Vhv

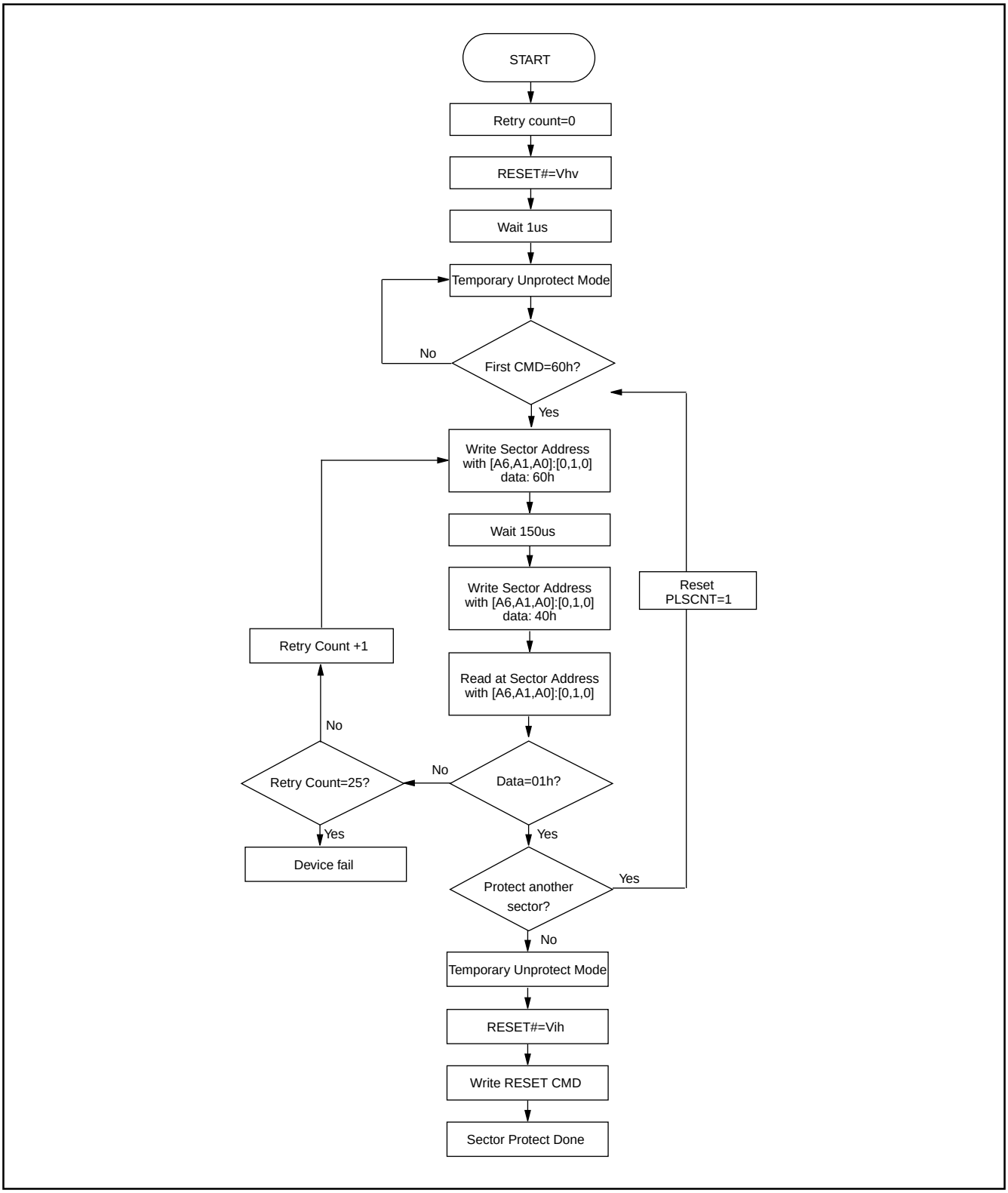


Figure 14-2. CHIP UNPROTECT ALGORITHMS WITH RESET#=Vhv

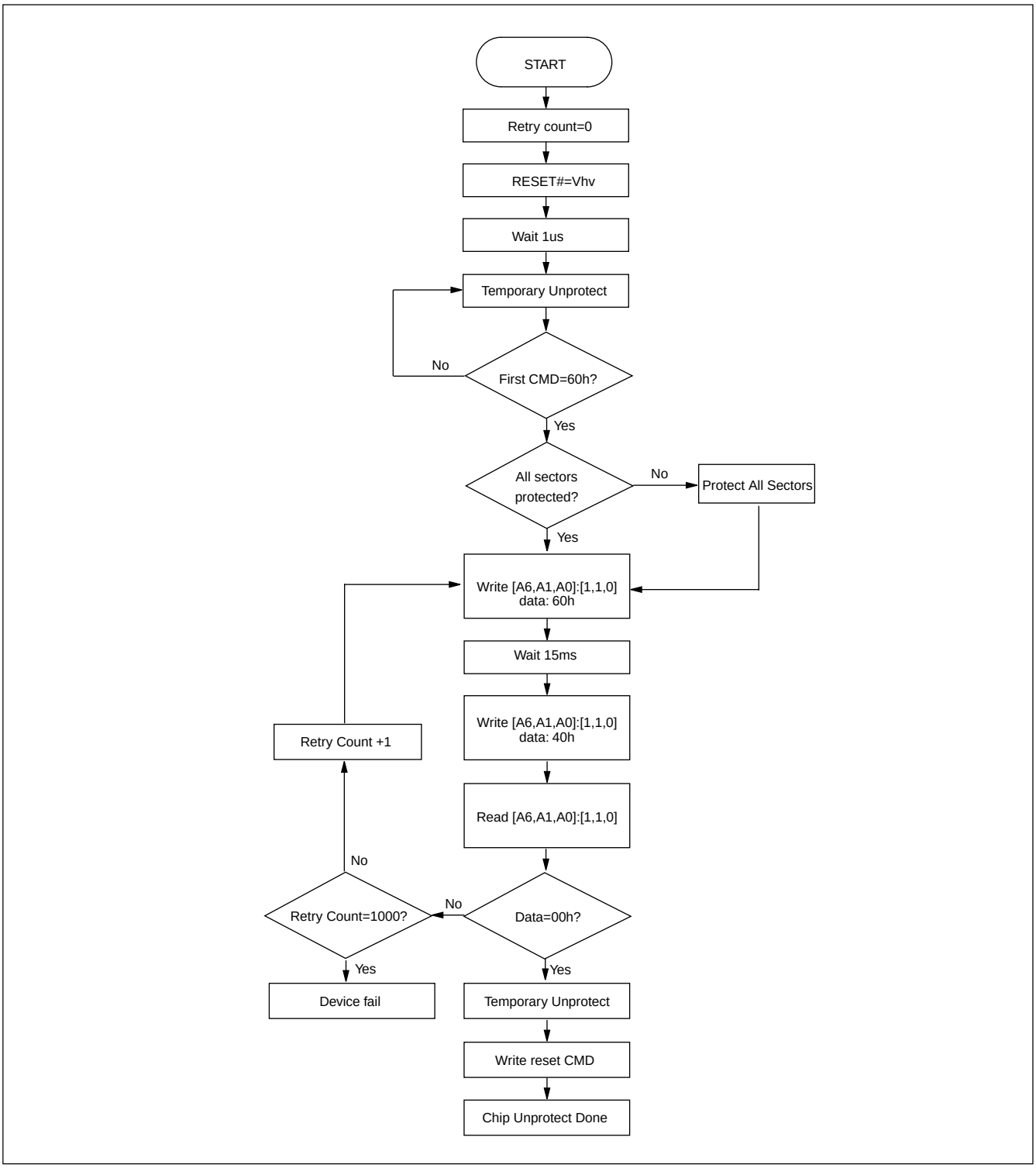


Table 5. TEMPORARY SECTOR GROUP UNPROTECT

Parameter	Alt	Description	Condition	Speed	Unit
Trpvhh	Tvidr	RESET# Rise Time to Vhv and Vhv Fall Time to RESET#	MIN	500	nS
Tvhhwl	Trsp	RESET# Vhv to WE# Low	MIN	4	uS

Figure 15. TEMPORARY SECTOR GROUP UNPROTECT WAVEFORMS

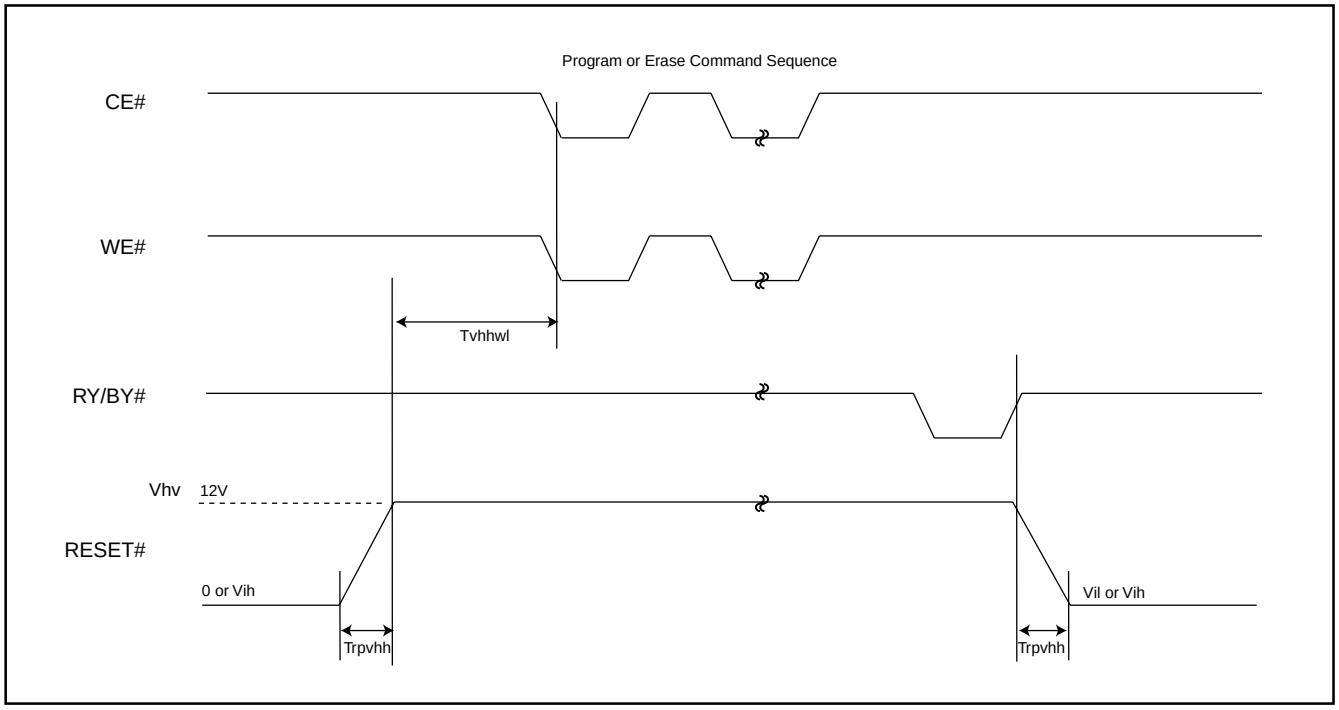
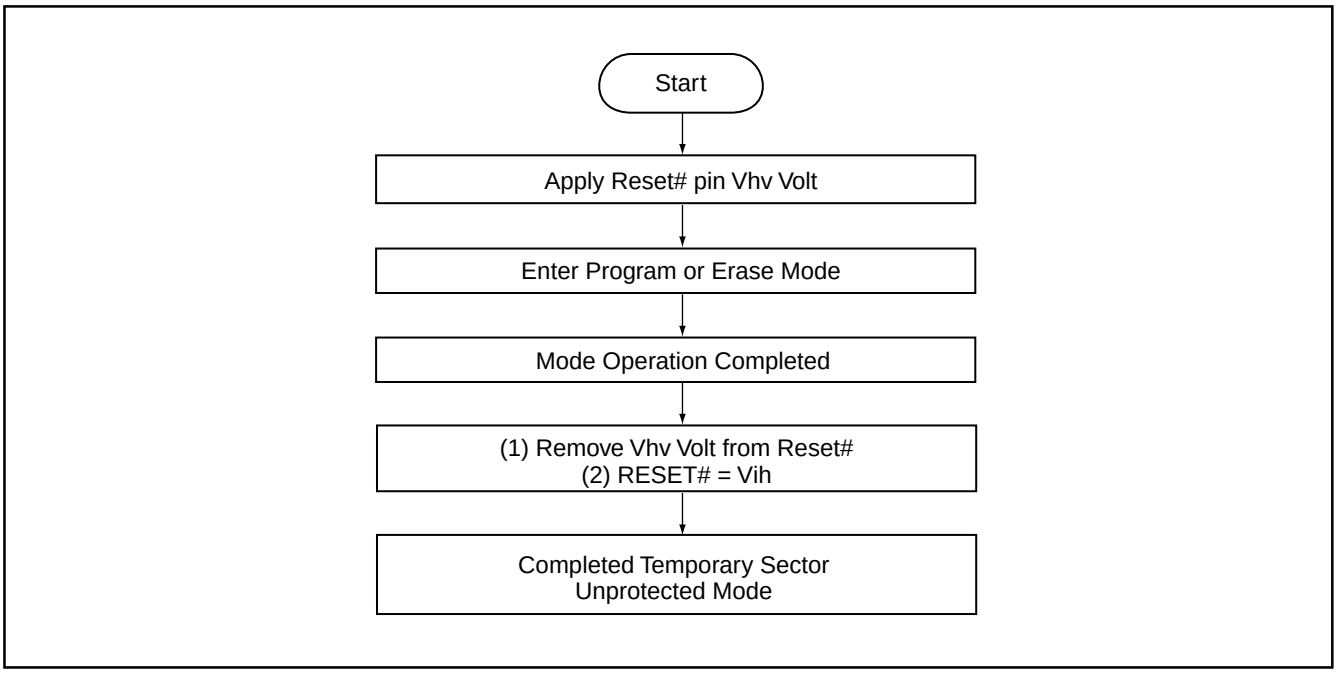
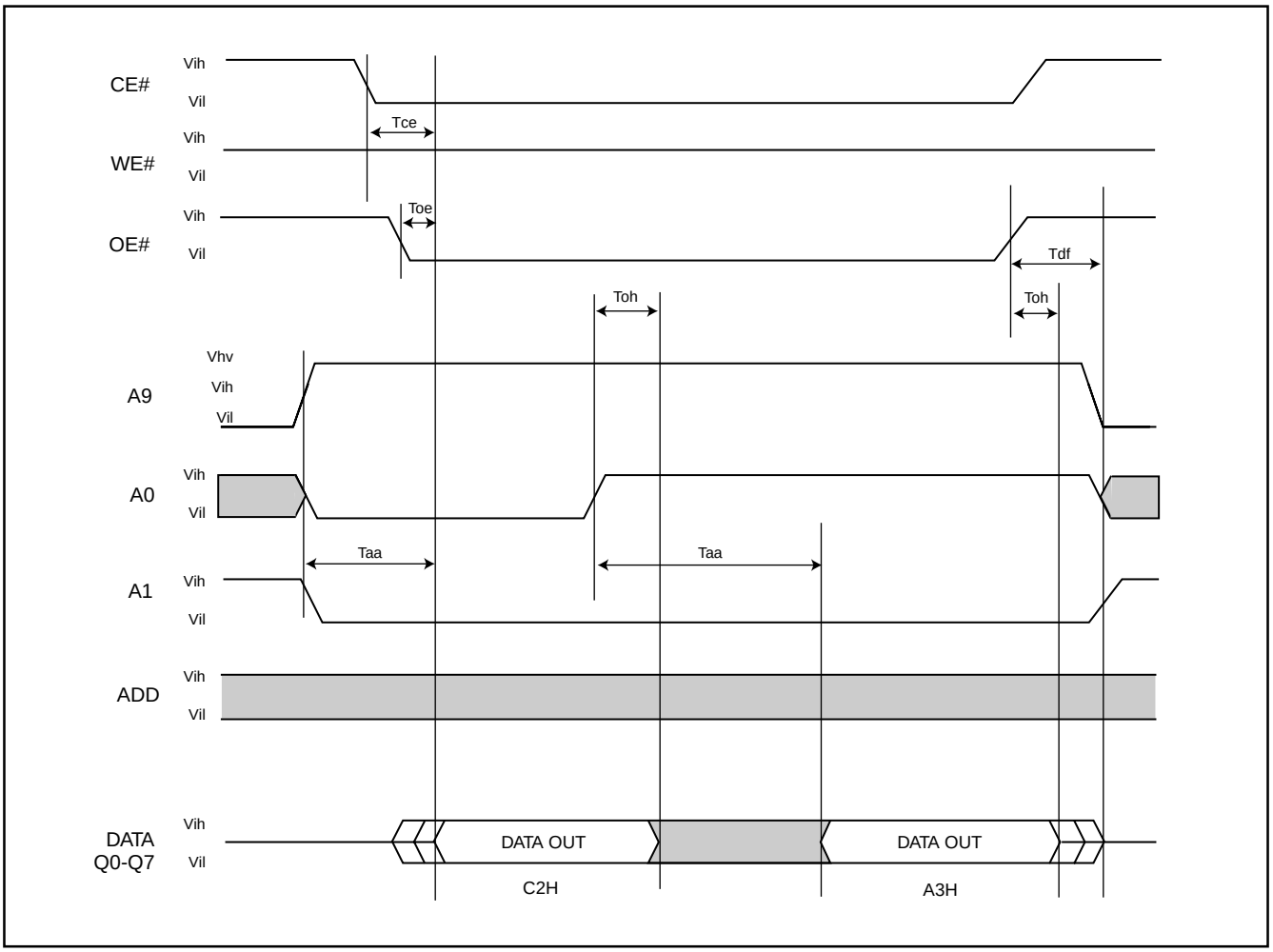


Figure 16. TEMPORARY SECTOR GROUP UNPROTECT FLOWCHART



Notes:
1. Temporary unprotect all protected sectors Vhv=11.5~12.5V.
2. After leaving temporary unprotect mode, the previously protected sectors are again protected.

Figure 17. SILICON ID READ TIMING WAVEFORM



WRITE OPERATION STATUS

Figure 18. DATA# POLLING TIMING WAVEFORMS (DURING AUTOMATIC ALGORITHMS)

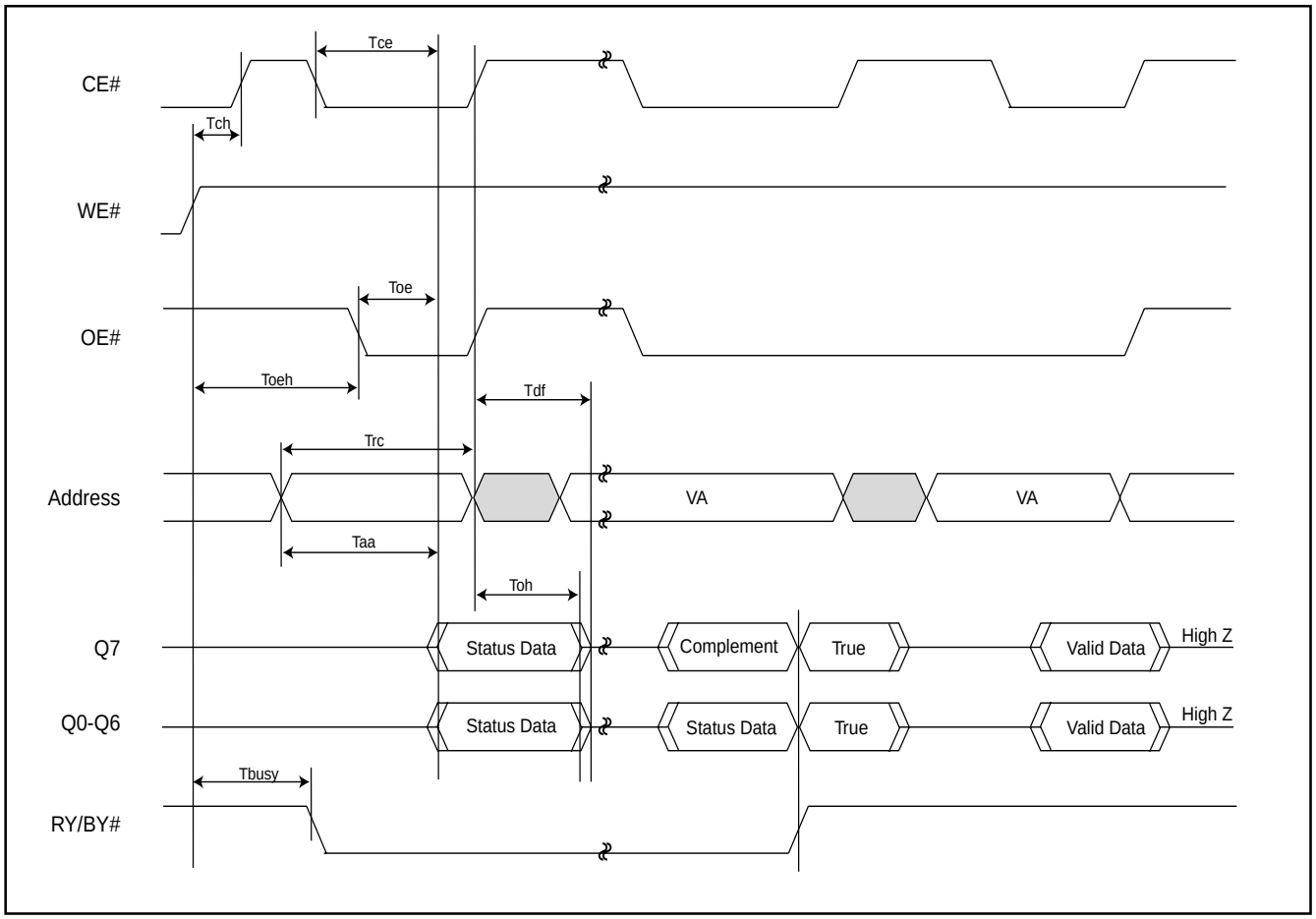
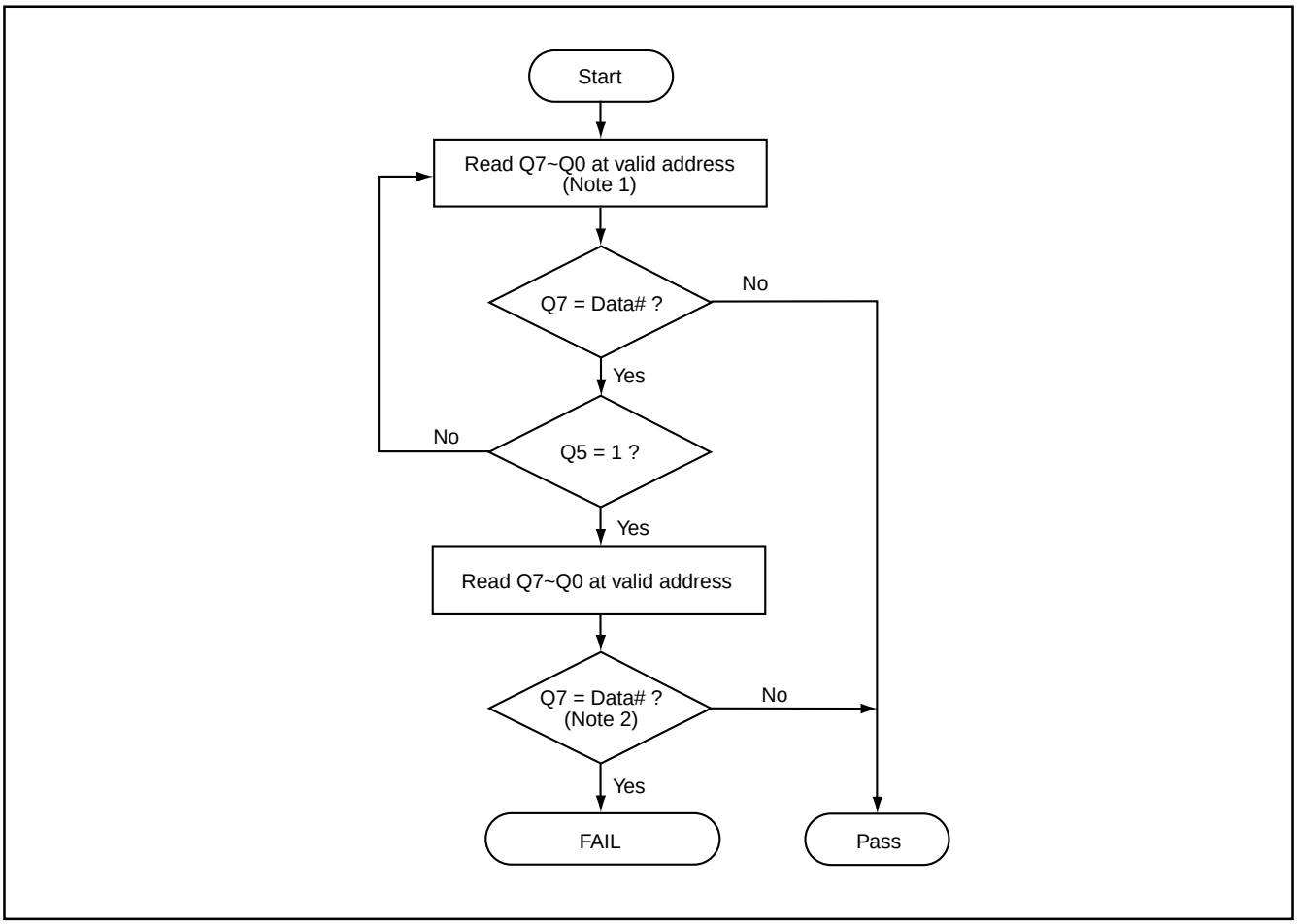


Figure 19. Data# Polling Algorithm



Notes:
1. For programming, valid address means program address.
   For erasing, valid address means erase sectors address.
2. Q7 should be rechecked even Q5="1" because Q7 may change simultaneously with Q5.

Figure 20. TOGGLE BIT TIMING WAVEFORMS (DURING AUTOMATIC ALGORITHMS)

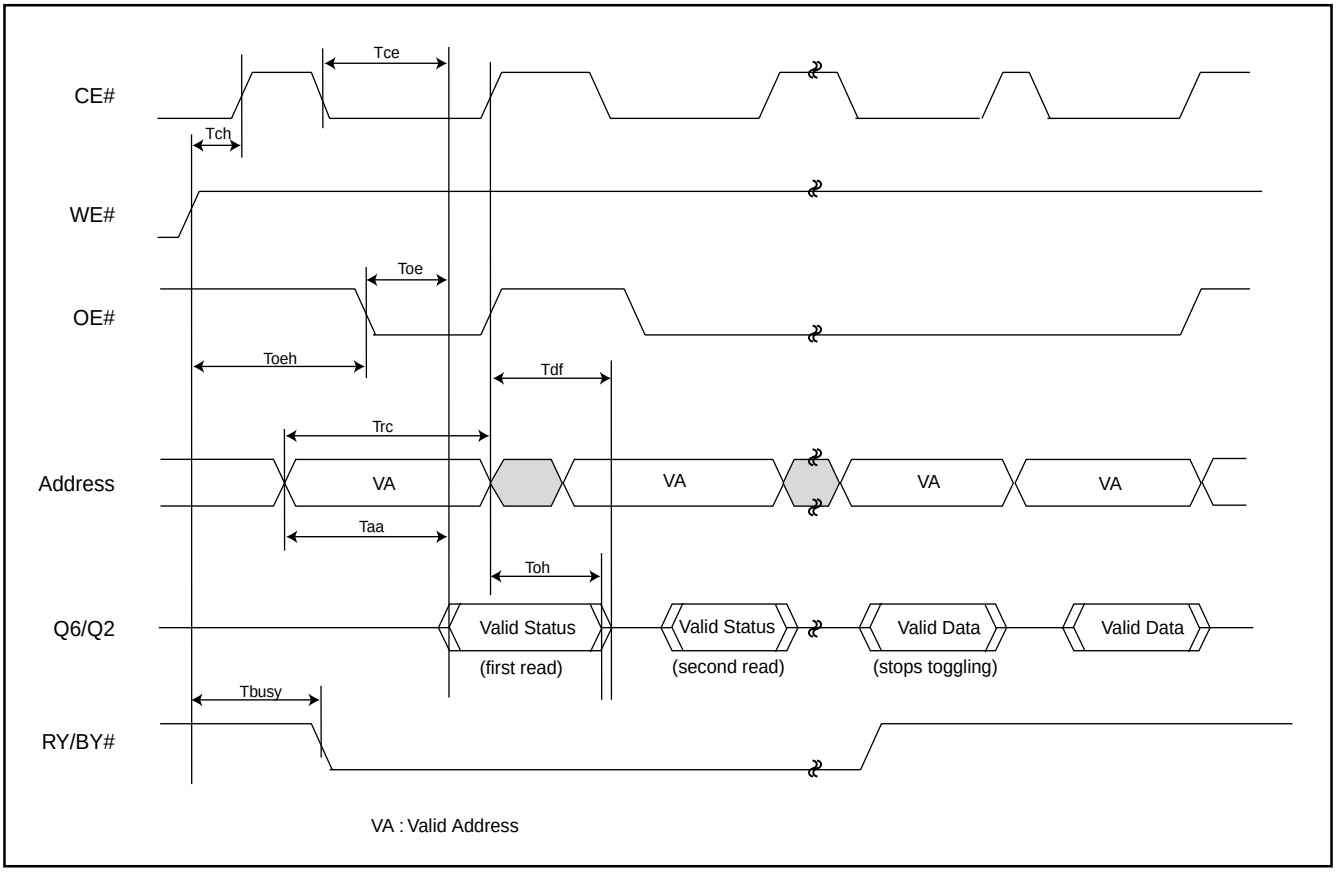
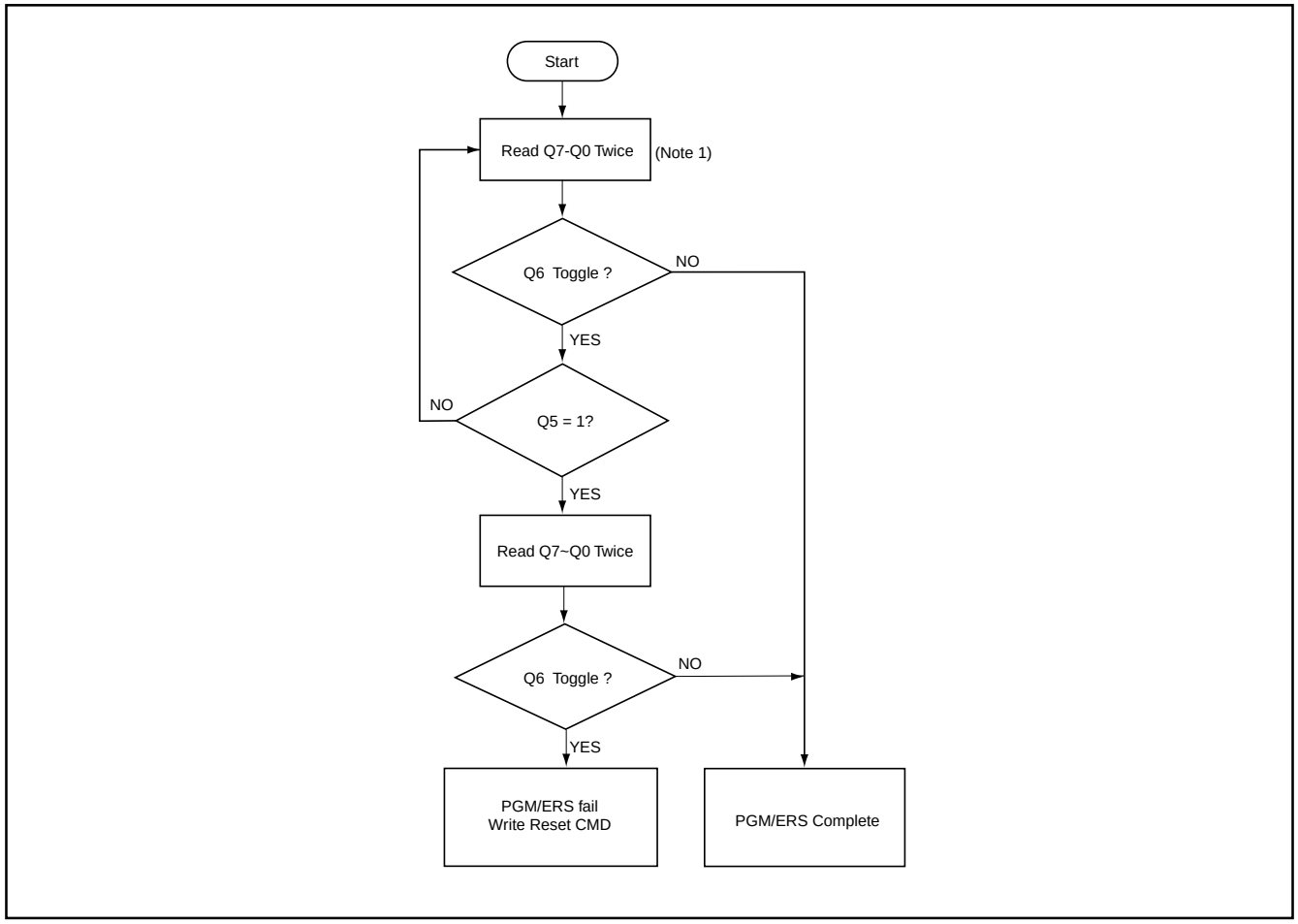


Figure 21. Toggle Bit Algorithm



Notes:
1. Read toggle bit twice to determine whether or not it is toggling.
2. Recheck toggle bit because it may stop toggling as Q5 changes to "1".

RECOMMENDED OPERATING CONDITIONS

At Device Power-Up

AC timing illustrated in Figure A is recommended for the supply voltages and the control signals at device power-up. If the timing in the figure is ignored, the device may not operate correctly.

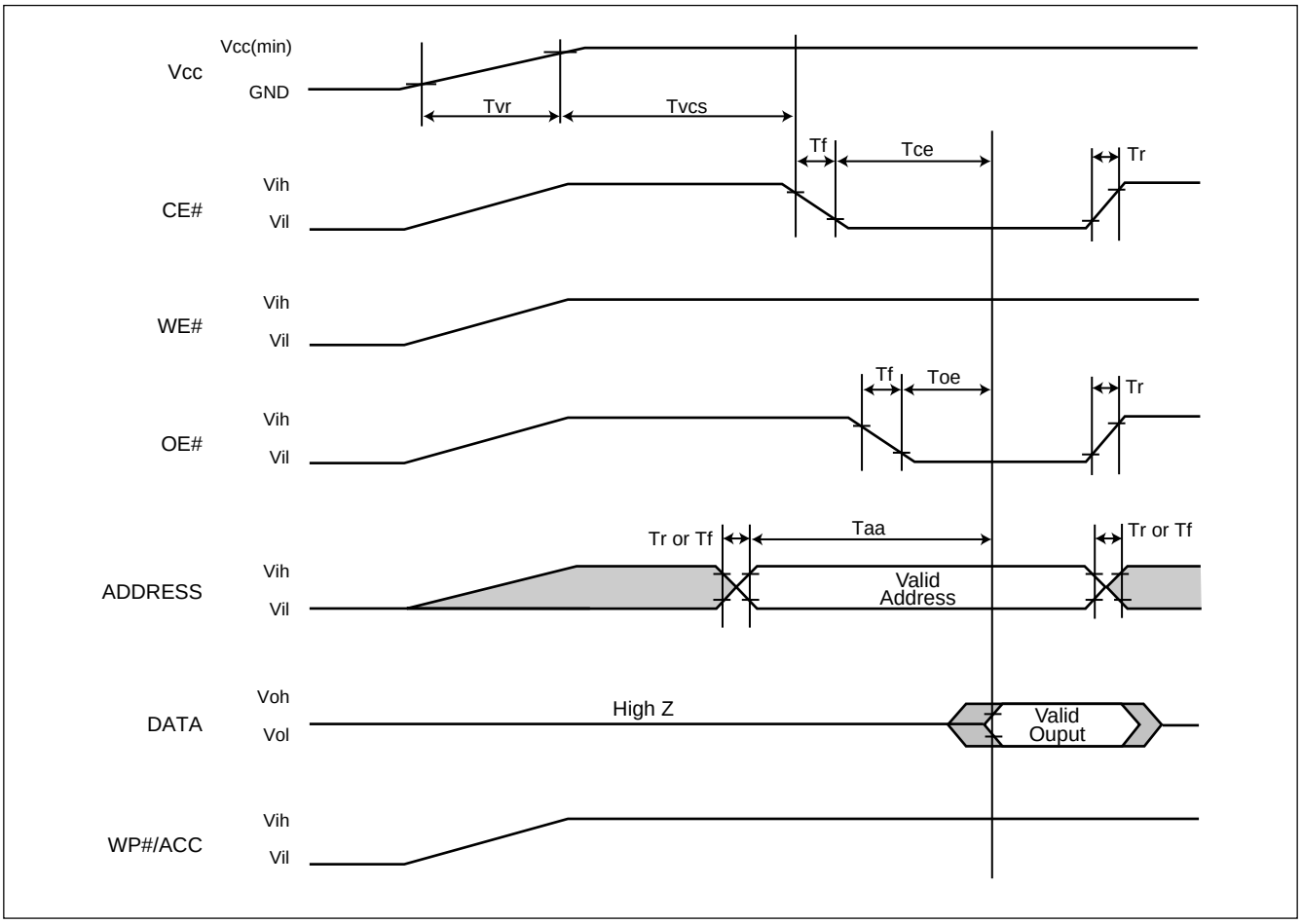


Figure A. AC Timing at Device Power-Up

Symbol	Parameter	Min.	Max.	Unit
Tvr	Vcc Rise Time	20	500000	uS/V
Tr	Input Signal Rise Time		20	uS/V
Tf	Input Signal Fall Time		20	uS/V

ERASE AND PROGRAMMING PERFORMANCE

PARAMETER	LIMITS			UNITS
	MIN.	TYP.	MAX.	
Chip Erase Time		35	50	sec
Sector Erase Time		0.7	15	sec
Erase/Program Cycles	100,000			Cycles
Chip Programming Time		36	108	sec
Byte Programming Time		7	210	uS

LATCH-UP CHARACTERISTICS

	MIN.	MAX.
Input Voltage voltage difference with GND on all pins except I/O pins	-1.0V	13.5V
Input Voltage voltage difference with GND on all I/O pins	-1.0V	Vcc + 1.0V
Vcc Current	-100mA	+100mA
All pins included except Vcc. Test conditions: Vcc = 3.0V, one pin per testing		

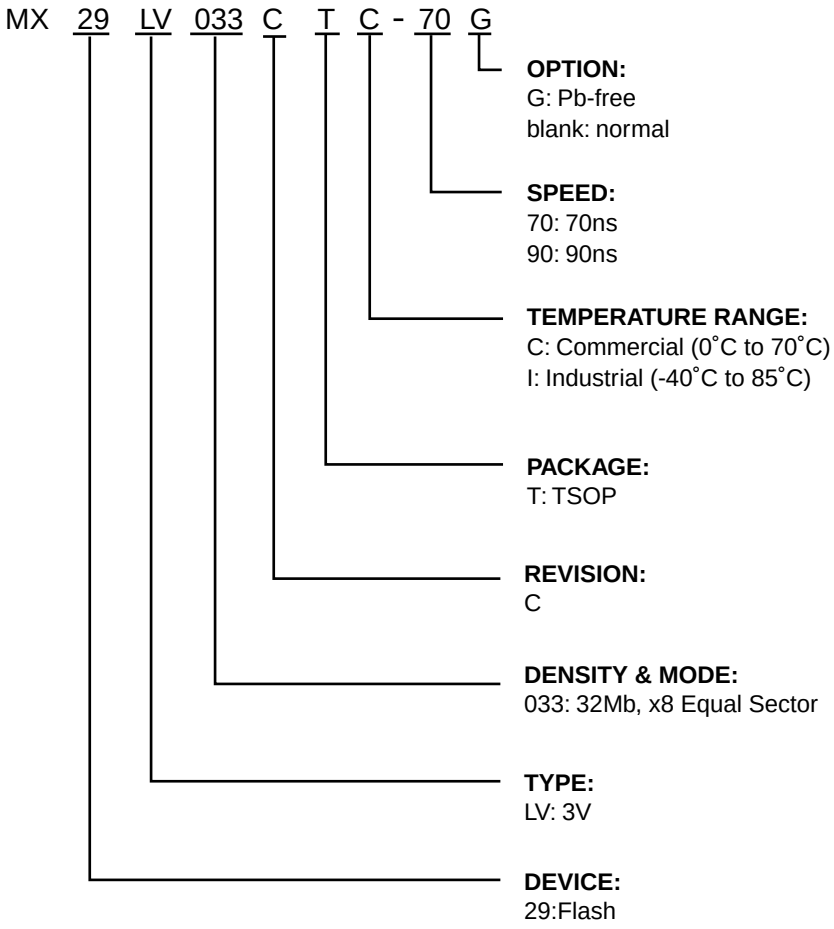
TSOP PIN CAPACITANCE

Parameter Symbol	Parameter Description	Test Set	TYP	MAX	UNIT
CIN2	Control Pin Capacitance	VIN=0	7.5	9	pF
COUT	Output Capacitance	VOUT=0	8.5	12	pF
CIN	Input Capacitance	VIN=0	6	7.5	pF

ORDERING INFORMATION

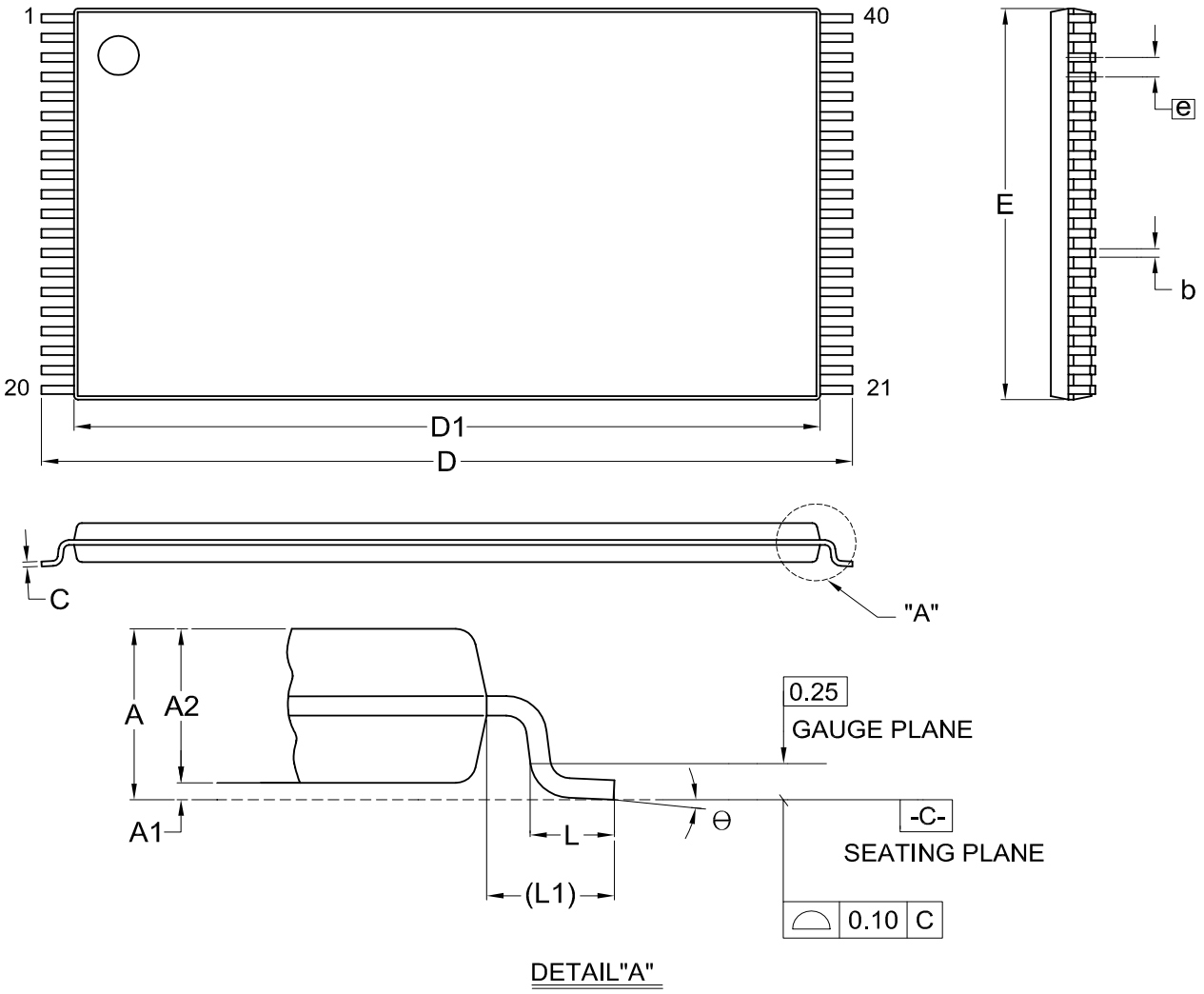
PART NO.	ACCESS TIME (ns)	OPERATING CURRENT MAX.(mA)	STANDBY CURRENT MAX. (uA)	PACKAGE
MX29LV033CTC-70	70	50	5	40 Pin TSOP (Normal Type)
MX29LV033CTC-90	90	50	5	40 Pin TSOP (Normal Type)
MX29LV033CTI-70	70	50	5	40 Pin TSOP (Normal Type)
MX29LV033CTI-90	90	50	5	40 Pin TSOP (Normal Type)
MX29LV033CTC-70G	70	50	5	40 Pin TSOP (Normal Type)
MX29LV033CTC-90G	90	50	5	40 Pin TSOP (Normal Type)
MX29LV033CTI-70G	70	50	5	40 Pin TSOP (Normal Type)
MX29LV033CTI-90G	90	50	5	40 Pin TSOP (Normal Type)

PART NAME DESCRIPTION



PACKAGE INFORMATION

Title: Package Outline for TSOP(I) 40L (10X20mm)



Dimensions (inch dimensions are derived from the original mm dimensions)

SYMBOL / UNIT		A	A1	A2	b	C	D	D1	E	e	L	L1	Θ
mm	Min.	---	0.05	0.95	0.17	0.10	19.80	18.30	9.90		0.50	0.70	0
	Nom.	—	0.10	1.00	0.20	0.13	20.00	18.40	10.00	0.50	0.60	0.80	5
	Max.	1.20	0.15	1.05	0.27	0.21	20.20	18.50	10.10		0.70	0.90	8
Inch	Min.	—	0.002	0.037	0.007	0.004	0.780	0.720	0.390		0.020	0.028	0
	Nom.	---	0.004	0.039	0.008	0.005	0.787	0.724	0.394	0.020	0.024	0.031	5
	Max.	0.047	0.006	0.041	0.011	0.008	0.795	0.728	0.398		0.028	0.035	8

DWG.NO.	REVISION	REFERENCE			ISSUE DATE
		JEDEC	EIAJ		
6110-1606	6	MO-142			12-01-'03

REVISION HISTORY

Revision No.	Description	Page	Date
1.0	1. Removed "Advanced Information" title	P1	OCT/14/2005
	2. Added description about Pb-free device is RoHS compliant	P1	
	3. Modified "Common Flash Interface(CFI) Mode"	P51,52	
1.1	1. Modified tVCS	P23	MAY/26/2006
1.2	1. Datasheet format changed	All	AUG/15/2006
1.3	1. Data modification	All	AUG/17/2006
1.4	1. Added statement	P50	NOV/06/2006
1.5	1. Modified Figure 11. CE# Controlled Write Timing Waveform	P32	FEB/25/2008

Macronix's products are not designed, manufactured, or intended for use for any high risk applications in which the failure of a single component could cause death, personal injury, severe physical damage, or other substantial harm to persons or property, such as life-support systems, high temperature automotive, medical, aircraft and military application. Macronix and its suppliers will not be liable to you and/or any third party for any claims, injuries or damages that may be incurred due to use of Macronix's products in the prohibited applications.

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