

**ST100 DSP CORES****DATA BRIEF****1 FEATURES**

- State-of-the-art DSP core architecture
  - Complete & optimized memory systems
  - Multicore solutions
  - Standard or specific tightly coupled peripherals libraries
- Advanced Load/store Architecture
  - Regular and efficient.
  - Optimized for programming in 'C/C++/EC++' languages.
- Two Instruction Sets
  - GP16, a 16-bit instruction set.
  - GP32, a 32-bit instruction set.
- Three Instruction Modes
  - GP16: 2-way superscalar, for compact microcontroller codes.
  - GP32: 2-way superscalar, for high performance microcontroller codes.
  - SLIW: one SLIW per cycle, where a SLIW (Scoreboarded Long Instruction Word), is a bundle of four GP32 instruction words. This mode is for high performance vector codes (DSP loops).
- Predicated Execution For Most Instructions
  - Removes needs of conditional branches.
  - Compact coding and increased instruction level parallelism.
- Flexible Data Format
  - The ST100 supports the following data types:
    - 16-bit, 32-bit and 40-bit unsigned/signed integer.
    - 16-bit, 32-bit, and 40-bit signed fractional.
    - Signed and unsigned byte and Bit.
  - Supports little Endian for data and program.
- Circular And Bit-reversed DSP Addressing Modes
  - Facilitates the implementation of the DSP algorithms like the FIR filters and the FFT.
- Arithmetic Capability
  - 40-bit and 32-bit arithmetic.
  - Packed Arithmetic 2 x 16-bit (SIMD).
  - Saturating (Clamping) and/or Rounding options
- Application Oriented Instructions
  - Useful instructions for ETSI (European Telecommunications Standards Institute) primitives in GP32 and GP16:
    - VITERBI...
  - General usage instructions:
    - Hardware Loop Controllers
      - Zero cycles overhead for continuous data processing.
      - Three nestable loops.
    - Memory Space
      - 32-bit addressing range, 4 Gbytes of memory space.
    - Interrupt, Trap And Context Switching
      - Fast response to external events or system errors.
    - Protection System
      - User mode and Supervisor mode.
    - Power Saving
      - Four "IDLE" modes performing power saving operations.

**2 DESCRIPTION**

STMicroelectronics' innovative ST100® DSP processor core architecture has been conceived specifically for embedded applications in custom system-on-chip products for demanding markets like cellular phones, hard disk drives, engine management units, telecommunication systems and advanced multimedia products. A completely new design, the ST100® architecture combines in a single core the advantages of a 16-bit instruction word for code compactness, a 32-bit instruction word for MCU performance and a 128-bit SLIW instruction word for high DSP performance. The ST100® core is also scaleable, so it can be implemented in many ways, ranging from low power devices for portable products to very high performance devices with a maximum of parallelism. Building on ST's experience in embedded cores, the ST100® architecture is based on an analysis of the real needs of system designers and software engineers in some of the fastest-moving segments of the industry, where high performance, low power consumption and fast time to market are all essential.

**Table 1. Revision History**

Date	Revision	Description of Changes
September 2004	1	First Issue

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