



MACRONIX
INTERNATIONAL Co., LTD.

MX29LV002C/002NC T/B
MX29LV004C T/B
MX29LV008C T/B

CMOS SINGLE VOLTAGE 3V ONLY FLASH MEMORY

FEATURES

GENERAL FEATURES

- Byte mode only:
 - 262,411 x8 (MX29LV002C/002NC)
 - 524,288 x8 (MX29LV004C)
 - 1,048,576 x8 (MX29LV008C)
- Sector Structure
 - 16K-Byte x 1, 8K-Byte x 2, 32K-Byte x 1
64K-Byte x 3 (MX29LV002C), 64K-Byte x 7 (MX29LV004C), 64K-Byte x 15 (MX29LV008C)
- Sector Protect
 - Provides sector protect function to prevent program or erase operation in the protected sector
 - Provides chip unprotect function to allow code changing
 - Provides temporary sector unprotect function for code changing in previously protected sector
- Single Power Supply Operation
 - 2.7 to 3.6 volt for read, erase, and program operations
- Latch-up protected to 250mA from -1V to Vcc + 1V
- Low Vcc write inhibit : Vcc <= 1.4V
- Compatible with JEDEC standard
 - Pinout and software compatible to single power supply Flash

PERFORMANCE

- High Performance
 - Fast access time: 45R (MX29LV004C only), 55R(for MX29LV004C and MX29LV008C), 70/90ns
 - Fast program time: 9us/Byte typical utilizing accelerate function
 - Fast erase time: 0.7s/sector
- Low Power Consumption
 - Low active read current: 7mA (typical) at 5MHz
 - Low standby current: 200nA (typical)
- Minimum 100,000 erase/program cycle
- 10 years data retention

SOFTWARE FEATURES

- Erase Suspend/ Erase Resume
 - Suspends sector erase operation to read data from or program data to another sector which is not being erased
- Status Reply
 - Data# Polling & Toggle bits provide detection of program and erase operation completion
- Support Common Flash Interface (CFI) only for 29LV002C/002NC, 29LV004C.

HARDWARE FEATURES

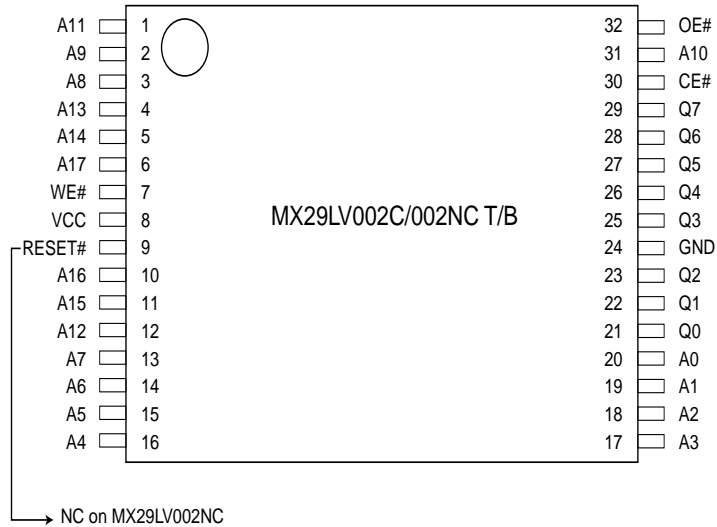
- Ready/Busy# (RY/BY#) Output only for 29LV004C, 29LV008C.
 - Provides a hardware method of detecting program and erase operation completion
- Hardware Reset (RESET#) Input
 - Provides a hardware method to reset the internal state machine to read mode

PACKAGE

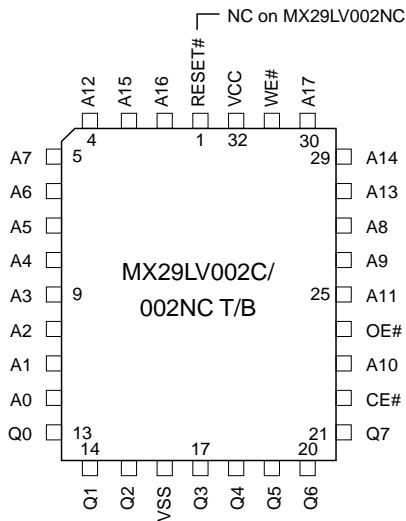
- 32-Pin TSOP (for MX29LV002C/002NC)
- 32-Pin PLCC (for MX29LV002C/002NC and MX29LV004C)
- 40-Pin TSOP (for MX29LV004C and MX29LV008C)
- **All Pb-free devices are RoHS Compliant**

MX29LV002C/002NC PIN CONFIGURATIONS

32 TSOP (TYPE 1)



32 PLCC

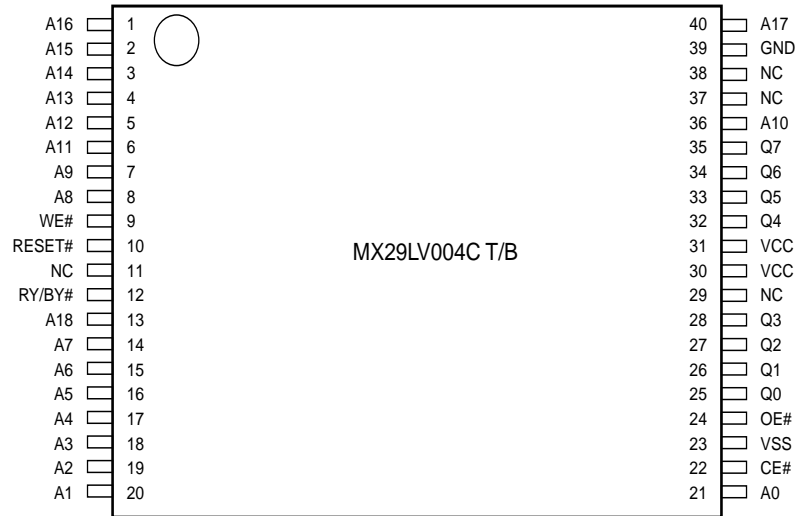


PIN DESCRIPTION

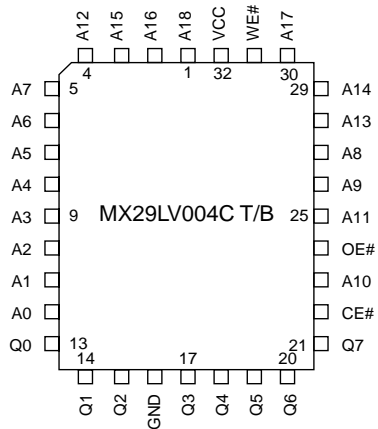
SYMBOL	PIN NAME
A0~A17	Address Input
Q0~Q7	Data Input/Output
CE#	Chip Enable Input
WE#	Write Enable Input
RESET#	Hardware Reset Pin/Sector Protect Unlock
OE#	Output Enable Input
VCC	Power Supply Pin (+3V)
GND	Ground Pin

MX29LV004C PIN CONFIGURATIONS

40 TSOP (Standard Type) (10mm x 20mm)



32 PLCC

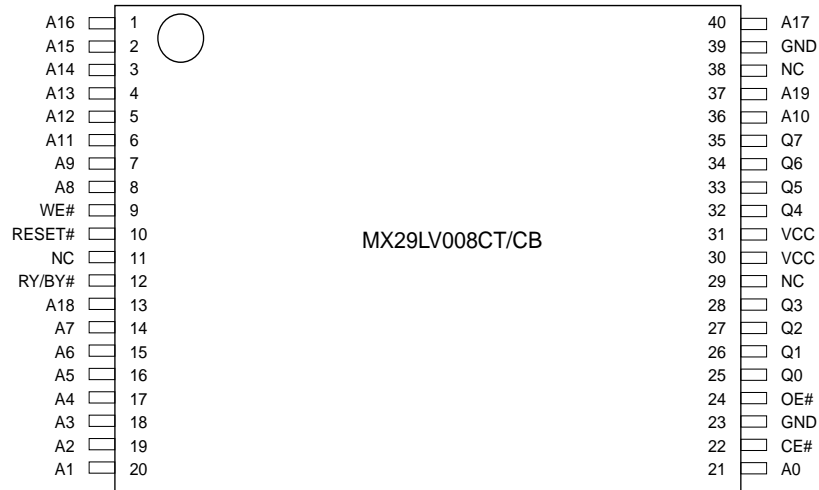


PIN DESCRIPTION

SYMBOL	PIN NAME
A0~A18	Address Input
Q0~Q7	Data Input/Output
CE#	Chip Enable Input
WE#	Write Enable Input
RESET#	Hardware Reset Pin/Sector Protect Unlock (for 40-TSOP)
OE#	Output Enable Input
RY/BY#	Ready/Busy# Output (for 40-TSOP)
VCC	Power Supply Pin (2.7V~3.6V)
GND	Ground Pin

MX29LV008C PIN CONFIGURATIONS

40TSOP (Standard Type) (10mm x 20mm)



PIN DESCRIPTION

SYMBOL	PIN NAME
A0~A19	Address Input
Q0~Q7	Data Input/Output
CE#	Chip Enable Input
WE#	Write Enable Input
RESET#	Hardware Reset Pin
OE#	Output Enable Input
RY/BY#	Ready/Busy Output
VCC	Power Supply Pin (2.7V~3.6V)
GND	Ground Pin

BLOCK DIAGRAM

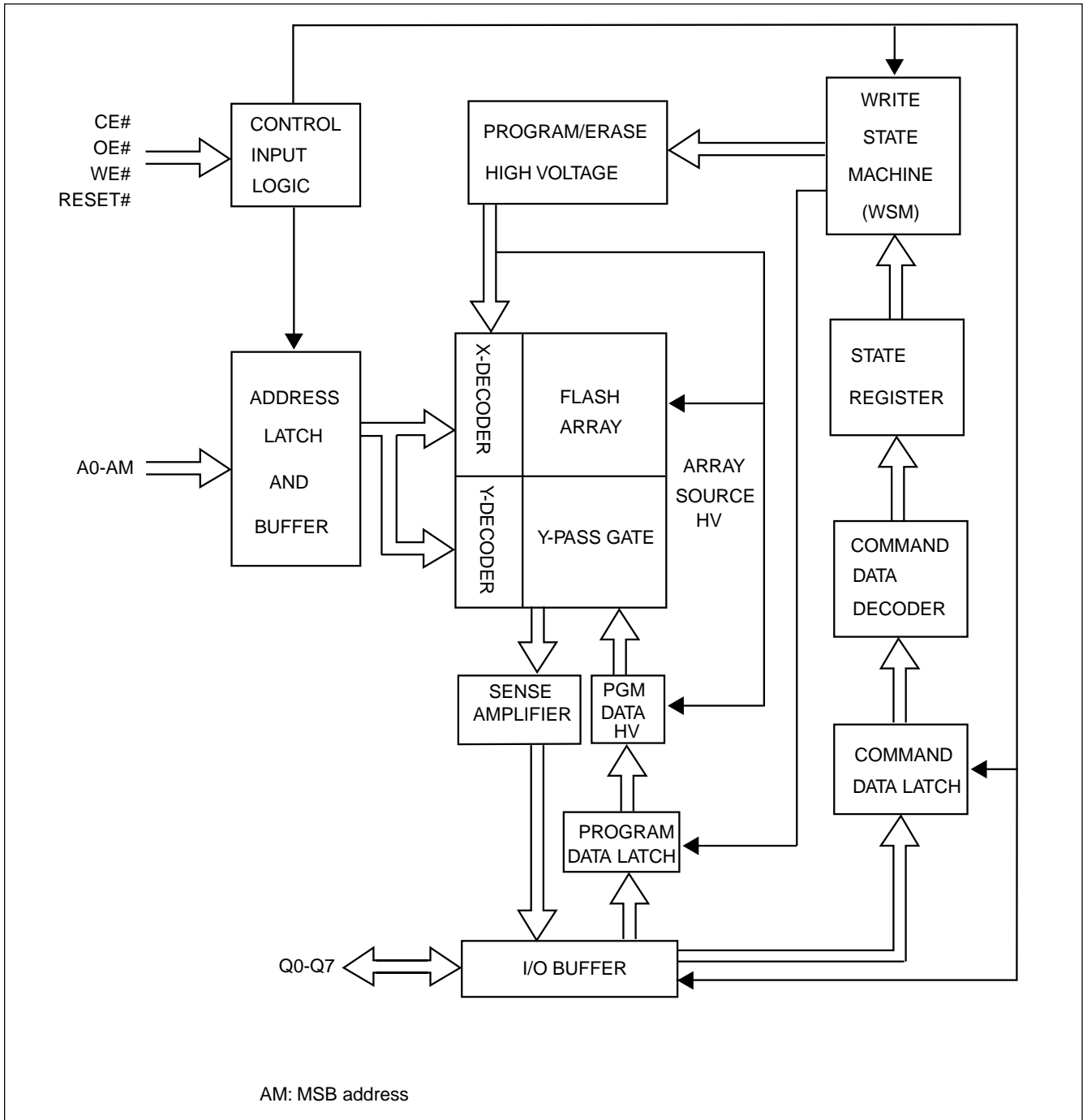


Table 1. BLOCK STRUCTURE**MX29LV002CT SECTOR ARCHITECTURE**

Sector	Sector Size Byte Mode	Address range Byte Mode (x8)	Sector Address				
			A17	A16	A15	A14	A13
SA0	64Kbytes	00000-0FFFF	0	0	X	X	X
SA1	64Kbytes	10000-1FFFF	0	1	X	X	X
SA2	64Kbytes	20000-2FFFF	1	0	X	X	X
SA3	32Kbytes	30000-37FFF	1	1	X	X	X
SA4	8Kbytes	38000-39FFF	0	0	X	X	X
SA5	8Kbytes	3A000-3BFFF	0	1	X	X	X
SA6	16Kbytes	3C000-3FFFF	1	0	X	X	X

MX29LV002CB SECTOR ARCHITECTURE

Sector	Sector Size Byte Mode	Address range Byte Mode (x8)	Sector Address				
			A17	A16	A15	A14	A13
SA0	16Kbytes	00000-03FFF	0	0	0	0	X
SA1	8Kbytes	04000-05FFF	0	0	0	1	0
SA2	8Kbytes	06000-07FFF	0	0	0	1	1
SA3	32Kbytes	08000-0FFFF	0	0	1	X	X
SA4	64Kbytes	10000-1FFFF	0	1	X	X	X
SA5	64Kbytes	20000-2FFFF	1	0	X	X	X
SA6	64Kbytes	30000-3FFFF	1	1	X	X	X

MX29LV004CT SECTOR ARCHITECTURE

Sector	Sector Size Byte Mode	Address range Byte Mode (x8)	Sector Address					
			A18	A17	A16	A15	A14	A13
SA0	64Kbytes	00000-0FFFF	0	0	0	X	X	X
SA1	64Kbytes	10000-1FFFF	0	0	1	X	X	X
SA2	64Kbytes	20000-2FFFF	0	1	0	X	X	X
SA3	64Kbytes	30000-3FFFF	0	1	1	X	X	X
SA4	64Kbytes	40000-4FFFF	1	0	0	X	X	X
SA5	64Kbytes	50000-5FFFF	1	0	1	X	X	X
SA6	64Kbytes	60000-6FFFF	1	1	0	X	X	X
SA7	32Kbytes	70000-77FFF	1	1	1	0	X	X
SA8	8Kbytes	78000-79FFF	1	1	1	1	0	0
SA9	8Kbytes	7A000-7BFFF	1	1	1	1	0	1
SA10	16Kbytes	7C000-7FFFF	1	1	1	1	1	X

MX29LV004CB SECTOR ARCHITECTURE

Sector	Sector Size Byte Mode	Address range Byte Mode (x8)	Sector Address					
			A18	A17	A16	A15	A14	A13
SA0	16Kbytes	00000-03FFF	0	0	0	0	0	X
SA1	8Kbytes	04000-05FFF	0	0	0	0	1	0
SA2	8Kbytes	06000-07FFF	0	0	0	0	1	1
SA3	32Kbytes	08000-0FFFF	0	0	0	1	X	X
SA4	64Kbytes	10000-1FFFF	0	0	1	X	X	X
SA5	64Kbytes	20000-2FFFF	0	1	0	X	X	X
SA6	64Kbytes	30000-3FFFF	0	1	1	X	X	X
SA7	64Kbytes	40000-4FFFF	1	0	0	X	X	X
SA8	64Kbytes	50000-5FFFF	1	0	1	X	X	X
SA9	64Kbytes	60000-6FFFF	1	1	0	X	X	X
SA10	64Kbytes	70000-7FFFF	1	1	1	X	X	X

MX29LV008CT SECTOR ARCHITECTURE

Sector	Sector Size	Address range	Sector Address						
			A19	A18	A17	A16	A15	A14	A13
SA0	64Kbytes	00000h-0FFFFh	0	0	0	0	X	X	X
SA1	64Kbytes	10000h-1FFFFh	0	0	0	1	X	X	X
SA2	64Kbytes	20000h-2FFFFh	0	0	1	0	X	X	X
SA3	64Kbytes	30000h-3FFFFh	0	0	1	1	X	X	X
SA4	64Kbytes	40000h-4FFFFh	0	1	0	0	X	X	X
SA5	64Kbytes	50000h-5FFFFh	0	1	0	1	X	X	X
SA6	64Kbytes	60000h-6FFFFh	0	1	1	0	X	X	X
SA7	64Kbytes	70000h-7FFFFh	0	1	1	1	X	X	X
SA8	64Kbytes	80000h-8FFFFh	1	0	0	0	X	X	X
SA9	64Kbytes	90000h-9FFFFh	1	0	0	1	X	X	X
SA10	64Kbytes	A0000h-AFFFFh	1	0	1	0	X	X	X
SA11	64Kbytes	B0000h-BFFFFh	1	0	1	1	X	X	X
SA12	64Kbytes	C0000h-CFFFFh	1	1	0	0	X	X	X
SA13	64Kbytes	D0000h-DFFFFh	1	1	0	1	X	X	X
SA14	64Kbytes	E0000h-EFFFFh	1	1	1	0	X	X	X
SA15	32Kbytes	F0000h-F7FFFh	1	1	1	1	0	X	X
SA16	8Kbytes	F8000h-F9FFFh	1	1	1	1	1	0	0
SA17	8Kbytes	FA000h-FBFFFh	1	1	1	1	1	0	1
SA18	16kbytes	FC000h-FFFFFh	1	1	1	1	1	1	X

MX29LV008CB SECTOR ARCHITECTURE

Sector	Sector Size	Address range	Sector Address						
			A19	A18	A17	A16	A15	A14	A13
SA0	16Kbytes	00000h-03FFFh	0	0	0	0	0	0	X
SA1	8Kbytes	04000h-05FFFh	0	0	0	0	0	1	0
SA2	8Kbytes	06000h-07FFFh	0	0	0	0	0	1	1
SA3	32Kbytes	08000h-0FFFFh	0	0	0	0	1	X	X
SA4	64Kbytes	10000h-1FFFFh	0	0	0	1	X	X	X
SA5	64Kbytes	20000h-2FFFFh	0	0	1	0	X	X	X
SA6	64Kbytes	30000h-3FFFFh	0	0	1	1	X	X	X
SA7	64Kbytes	40000h-4FFFFh	0	1	0	0	X	X	X
SA8	64Kbytes	50000h-5FFFFh	0	1	0	1	X	X	X
SA9	64Kbytes	60000h-6FFFFh	0	1	1	0	X	X	X
SA10	64Kbytes	70000h-7FFFFh	0	1	1	1	X	X	X
SA11	64Kbytes	80000h-8FFFFh	1	0	0	0	X	X	X
SA12	64Kbytes	90000h-9FFFFh	1	0	0	1	X	X	X
SA13	64Kbytes	A0000h-AFFFFh	1	0	1	0	X	X	X
SA14	64Kbytes	B0000h-BFFFFh	1	0	1	1	X	X	X
SA15	64Kbytes	C0000h-CFFFFh	1	1	0	0	X	X	X
SA16	64Kbytes	D0000h-DFFFFh	1	1	0	1	X	X	X
SA17	64Kbytes	E0000h-EFFFFh	1	1	1	0	X	X	X
SA18	64kbytes	F0000h-FFFFFh	1	1	1	1	X	X	X

Table 2. BUS OPERATION--1

Mode Select	RE-SET#	CE#	WE#	OE#	Address	Q0~Q7
Device Reset	L	X	X	X	X	HighZ
Standby Mode	V _{cc} ± 0.3V	V _{cc} ± 0.3V	X	X	X	HighZ
Output Disable	H	L	H	H	X	HighZ
Read Mode	H	L	H	L	AIN	DOUT
Write	H	L	L	H	AIN	DIN
Temporary Sector Unprotect	V _{hv}	X	X	X	AIN	DIN
Sector Protect	V _{hv}	L	L	H	Sector Address, A6=L, A1=H, A0=L	DIN
Chip Unprotect	V _{hv}	L	L	H	Sector Address, A6=H, A1=H, A0=L	DIN

Note:

1. Q0~Q7 are input (DIN) or output (DOUT) pins according to the requests of command sequence, sector protection, or data polling algorithm.

BUS OPERATION--2

Item	Control Input			AM	A12		A8		A5			Q0~Q7
	CE#	WE#	OE#	to A13	to A10	A9	to A7	A6	to A2	A1	A0	
Sector Protect Verification	L	H	L	SA	x	V _{hv}	x	L	x	H	L	01h or 00h (Note1)
Read Silicon ID Manufacturer Code	L	H	L	x	x	V _{hv}	x	L	x	L	L	C2H
Read Silicon ID MX29LV002CT	L	H	L	x	x	V _{hv}	x	L	x	L	H	59H
Read Silicon ID MX29LV002CB	L	H	L	x	x	V _{hv}	x	L	x	L	H	5AH
Read Silicon ID MX29LV004CT	L	H	L	x	x	V _{hv}	x	L	x	L	H	B5H
Read Silicon ID MX29LV004CB	L	H	L	x	x	V _{hv}	x	L	x	L	H	B6H
Read Silicon ID MX29LV008CT	L	H	L	x	x	V _{hv}	x	L	x	L	H	3EH
Read Silicon ID MX29LV008CB	L	H	L	x	x	V _{hv}	x	L	x	L	H	37H

Notes:

1. Sector unprotected code:00h. Sector protected code:01h.
2. AM: MSB of address.

WRITE COMMANDS/COMMAND SEQUENCES

To write a command to the device, system must drive WE# and CE# to Vil, and OE# to Vih. In a command cycle, all address are latched at the later falling edge of CE# and WE#, and all data are latched at the earlier rising edge of CE# and WE#.

Figure 1 illustrates the AC timing waveform of a write command, and Table 3 defines all the valid command sets of the device. System is not allowed to write invalid commands not defined in this datasheet. Writing an invalid command will bring the device to an undefined state.

REQUIREMENTS FOR READING ARRAY DATA

Read array action is to read the data stored in the array. While the memory device is in powered up or has been reset, it will automatically enter the status of read array. If the microprocessor wants to read the data stored in array, it has to drive CE# (device enable control pin) and OE# (Output control pin) as Vil, and input the address of the data to be read into address pin at the same time. After a period of read cycle (Tce or Taa), the data being read out will be displayed on output pin for microprocessor to access. If CE# or OE# is Vih, the output will be in tri-state, and there will be no data displayed on output pin at all.

After the memory device completes embedded operation (automatic Erase or Program), it will automatically return to the status of read array, and the device can read the data in any address in the array. In the process of erasing, if the device receives the Erase suspend command, erase operation will be stopped temporarily after a period of time no more than Tready1 and the device will return to the status of read array. At this time, the device can read the data stored in any address except the sector being erased in the array. In the status of erase suspend, if user wants to read the data in the sectors being erased, the device will output status data onto the output. Similarly, if program command is issued after erase suspend, after program operation is completed, system can still read array data in any address except the sectors to be erased

The device needs to issue reset command to enable read array operation again in order to arbitrarily read the data in the array in the following two situations:

1. In program or erase operation, the programming or erasing failure causes Q5 to go high.
2. The device is in auto select mode or CFI mode.

In the two situations above, if reset command is not issued, the device is not in read array mode and system must issue reset command before reading array data.

RESET# OPERATION

Driving RESET# pin low for a period more than T_{rp} will reset the device back to read mode. If the device is in program or erase operation, the reset operation will take at most a period of T_{ready1} for the device to return to read array mode. Before the device returns to read array mode, the RY/BY# pin remains low (busy status).

When RESET# pin is held at $GND \pm 0.3V$, the device consumes standby current (I_{sb}). However, device draws larger current if RESET# pin is held at V_{il} but not within $GND \pm 0.3V$.

It is recommended that the system to tie its reset signal to RESET# pin of flash memory, so that the flash memory will be reset during system reset and allows system to read boot code from flash memory.

SECTOR PROTECT OPERATION

When a sector is protected, program or erase operation will be disabled on that protected sector. MX29LV002C/MX29LV004C/MX29LV008C T/B provides two methods for sector protection.

Once the sector is protected, the sector remains protected until next chip unprotect, or is temporarily unprotected by asserting RESET# pin at V_{hv} . Refer to temporary sector unprotect operation for further details.

The first method is by applying V_{hv} on RESET# pin. Refer to Figure 12 for timing diagram and Figure 13 for the algorithm for this method.

The other method is asserting V_{hv} on A9 and OE# pins, with A6 and CE# at V_{il} . The protection operation begins at the falling edge of WE# and terminates at the rising edge. Contact Macronix for details.

CHIP UNPROTECT OPERATION

MX29LV002C/MX29LV004C/MX29LV008C T/B provides two methods for chip unprotect. The chip unprotect operation unprotects all sectors within the device. It is recommended to protect all sectors before activating chip unprotect mode. All sectors are unprotected when shipped from the factory.

The first method is by applying V_{hv} on RESET# pin. Refer to Figure 12 for timing diagram and Figure 13 for algorithm of the operation.

The other method is asserting V_{hv} on A9 and OE# pins, with A6 at V_{ih} and CE# at V_{il} (see Table 2). The unprotect operation begins at the falling edge of WE# and terminates at the rising edge. Contact Macronix for details.

TEMPORARY SECTOR UNPROTECT OPERATION

System can apply RESET# pin at V_{hv} to place the device in temporary unprotect mode. In this mode, previously protected sectors can be programmed or erased just as it is unprotected. The device returns to normal operation once V_{hv} is removed from RESET# pin and previously protected sectors are again protected.

AUTOMATIC SELECT OPERATION

When the device is in Read array mode, erase-suspended read array mode or CFI mode, user can issue read silicon ID command to enter read silicon ID mode. After entering read silicon ID mode, user can query several silicon IDs continuously and does not need to issue read silicon ID mode again. When A0 is Low, device will output Macronix Manufacture ID C2. When A0 is high, device will output Device ID. In read silicon ID mode, issuing reset command will reset device back to read array mode or erase-suspended read array mode.

Another way to enter read silicon ID is to apply high voltage on A9 pin with CE#, OE#, A6 and A1 at Vil. While the high voltage of A9 pin is discharged, device will automatically leave read silicon ID mode and go back to read array mode or erase-suspended read array mode. When A0 is Low, device will output Macronix Manufacture ID C2. When A0 is high, device will output Device ID.

VERIFY SECTOR PROTECT STATUS OPERATION

MX29LV002C/MX29LV004C/MX29LV008C T/B provides hardware sector protection against Program and Erase operation for protected sectors. The sector protect status can be read through Sector Protect Verify command. This method requires Vhv on A9 pin, Vih on WE# and A1 pins, Vil on CE#, OE#, A6 and A0 pins, and sector address on A13 to AM pins. If the read out data is 01H, the designated sector is protected. Oppositely, if the read out data is 00H, the designated sector is not protected.

DATA PROTECTION

To avoid accidental erasure or programming of the device, the device is automatically reset to read array mode during power up. Besides, only after successful completion of the specified command sets will the device begin its erase or program operation.

Other features to protect the data from accidental alternation are described as followed.

LOW VCC WRITE INHIBIT

The device refuses to accept any write command when Vcc is less than 1.4V. This prevents data from spuriously altered. The device automatically resets itself when Vcc is lower than 1.4V and write cycles are ignored until Vcc is greater than 1.4V. System must provide proper signals on control pins after Vcc is larger than 1.4V to avoid unintentional program or erase operation

WRITE PULSE "GLITCH" PROTECTION

CE#, WE#, OE# pulses shorter than 5ns are treated as glitches and will not be regarded as an effective write cycle.

LOGICAL INHIBIT

A valid write cycle requires both CE# and WE# at Vil with OE# at Vih. Write cycle is ignored when either CE# at Vih, WE# a Vih, or OE# at Vil.

POWER-UP SEQUENCE

Upon power up, MX29LV002C/MX29LV004C/MX29LV008C T/B is placed in read array mode. Furthermore, program or erase operation will begin only after successful completion of specified command sequences.

POWER-UP WRITE INHIBIT

When WE#, CE# is held at V_{il} and OE# is held at V_{ih} during power up, the device ignores the first command on the rising edge of WE#.

POWER SUPPLY DECOUPLING

A 0.1 μ F capacitor should be connected between the V_{cc} and GND to reduce the noise effect.

TABLE 3. MX29LV002C/MX29LV004C/MX29LV008C T/B COMMAND DEFINITIONS

Command		Read Mode	Reset Mode	Automatic Select			Program	Chip Erase	Sector Erase
				Manufacturer ID	Device ID	Sector Protect Verify			
1st Bus Cyc	Addr	Addr	XXX	555	555	555	555	555	555
	Data	Data	F0	AA	AA	AA	AA	AA	AA
2nd Bus Cyc	Addr			2AA	2AA	2AA	2AA	2AA	2AA
	Data			55	55	55	55	55	55
3rd Bus Cyc	Addr			555	555	555	555	555	555
	Data			90	90	90	A0	80	80
4th Bus Cyc	Addr			X00	X01	(Sector)X02	Addr	555	555
	Data			C2	ID	00/01	Data	AA	AA
5th Bus Cyc	Addr							2AA	2AA
	Data							55	55
6th Bus Cyc	Addr							555	Sector
	Data							10	30

Command		Erase Suspend	Erase Resume	Sector Protect	CFI (Note 4)
1st Bus Cyc	Addr	XXX	XXX	XXX	55
	Data	B0	30	60	98
2nd Bus Cyc	Addr			sector	
	Data			60	
3rd Bus Cyc	Addr			sector	
	Data			40	
4th Bus Cyc	Addr			sector	
	Data			00/01	
5th Bus Cyc	Addr				
	Data				
6th Bus Cyc	Addr				
	Data				

Notes:

1. Device ID :
29LV002C: 59H/5AH (Top/Bottom)
29LV004C: B5H/B6H (Top/Bottom)
29LV008C: 3EH/37H (Top/Bottom)
2. For sector protect verify result, 00H means sector is not protected, 01H means sector has been protected.
3. Sector Protect command is valid during V_{hv} at RESET# pin, V_{ih} at A1 pin and V_{il} at A0, A6 pins. The last Bus cyc is for protect verify.
4. For MX29LV002C/002NC and MX29LV004C.
5. It is not allowed to adopt any other code which is not in the above command definition table.

RESET

In the following situations, executing reset command will reset device back to read array mode:

- Among erase command sequence (before the full command set is completed)
- Sector erase time-out period
- Erase fail (while Q5 is high)
- Among program command sequence (before the full command set is completed, erase-suspended program included)
- Program fail (while Q5 is high, and erase-suspended program fail is included)
- Read silicon ID mode
- Sector protect verify
- CFI mode

While device is at the status of program fail or erase fail (Q5 is high), user must issue reset command to reset device back to read array mode. While the device is in read silicon ID mode, sector protect verify or CFI mode, user must issue reset command to reset device back to read array mode.

When the device is in the progress of programming (not program fail) or erasing (not erase fail), device will ignore reset command.

AUTOMATIC SELECT COMMAND SEQUENCE

Automatic Select mode is used to access the manufacturer ID, device ID and to verify whether or not a sector is protected. The automatic select mode has four command cycles. The first two are unlock cycles, and followed by a specific command. The fourth cycle is a normal read cycle, and user can read at any address any number of times without entering another command sequence. The reset command is necessary to exit the Automatic Select mode and back to read array. The following table shows the identification code with corresponding address.

	Address	Data (Hex)	Representation
Manufacturer ID	X00	C2	
Device ID	X01	ID	Top/Bottom Boot Sector
Sector Protect Verify	(Sector address) X 02	00/01	Unprotected/protected

There is an alternative method to that shown in Table 2, which is intended for EPROM programmers and requires V_{hv} on address bit A9.

Notes:

Device ID : MX29LV002CT: 59, MX29LV002CB: 5A
MX29LV004CT: B5, MX29LV004CB: B6
MX29LV008CT: 3E, MX29LV008CB: 37

AUTOMATIC PROGRAMMING

The MX29LV002C/MX29LV004C/MX29LV008C T/B can provide the user program function by the form of Byte-Mode or Word-Mode. As long as the users enter the right cycle defined in the Table.3 (including 2 unlock cycles and A0H), any data user inputs will automatically be programmed into the array.

Once the program function is executed, the internal write state controller will automatically execute the algorithms and timings necessary for program and verification, which includes generating suitable program pulse, verifying whether the threshold voltage of the programmed cell is high enough and repeating the program pulse if any of the cells does not pass verification. Meanwhile, the internal control will prohibit the programming to cells that pass verification while the other cells fail in verification in order to avoid over-programming. With the internal write state controller, the device requires the user to write the program command and data only.

Programming will only change the bit status from "1" to "0". That is to say, it is impossible to convert the bit status from "0" to "1" by programming. Meanwhile, the internal write verification only detects the errors of the "1" that is not successfully programmed to "0".

Any command written to the device during programming will be ignored except hardware reset, which will terminate the program operation after a period of time no more than Tready1. When the embedded program algorithm is complete or the program operation is terminated by hardware reset, the device will return to the reading array data mode.

When the embedded program operation is on going, user can confirm if the embedded operation is finished or not by the following methods:

Status	Q7	Q6	Q5	RY/BY#*2
In progress*1	Q7#	Toggling	0	0
Finished	Q7	Stop toggling	0	1
Exceed time limit	Q7#	Toggling	1	0

*1: The status "in progress" means both program mode and erase-suspended program mode.

*2: RY/BY# is an open drain output pin and should be weakly connected to Vcc through a pull-up resistor.

*3: When an attempt is made to program a protected sector, Q7 will output its complement data or Q6 continues to toggle for about 1us or less and the device returns to read array state without programing the data in the protected sector.

CHIP ERASE

Chip Erase is to erase all the data with "1" and "0" as all "1". It needs 6 cycles to write the action in, and the first two cycles are "unlock" cycles, the third one is a configuration cycle, the fourth and fifth are also "unlock" cycles, and the sixth cycle is the chip erase operation.

During chip erasing, all the commands will not be accepted except hardware reset or the working voltage is too low that chip erase will be interrupted. After Chip Erase, the chip will return to the state of Read Array.

When the embedded chip erase operation is on going, user can confirm if the embedded operation is finished or not by the following methods:

Status	Q7	Q6	Q5	Q2	RY/BY#
In progress	0	Toggling	0	Toggling	0
Finished	1	Stop toggling	0	1	1
Exceed time limit	0	Toggling	1	Toggling	0

SECTOR ERASE

Sector Erase is to erase all the data in a sector with "1" and "0" as all "1". It requires six command cycles to issue. The first two cycles are "unlock cycles", the third one is a configuration cycle, the fourth and fifth are also "unlock cycles" and the sixth cycle is the sector erase command. After the sector erase command sequence is issued, there is a time-out period of 50us counted internally. During the time-out period, additional sector address and sector erase command can be written multiply. Once user enters another sector erase command, the time-out period of 50us is recounted. If user enters any command other than sector eras or erase suspend during time-out period, the erase command would be aborted and the device is reset to read array condition. The number of sectors could be from one sector to all sectors. After time-out period passing by, additional erase command is not accepted and erase embedded operation begins.

During sector erasing, all commands will not be accepted except hardware reset and erase suspend and user can check the status as chip erase.

When the embedded erase operation is on going, user can confirm if the embedded operation is finished or not by the following methods:

Status	Q7	Q6	Q5	Q3	Q2	RY/BY#*2
Time-out period	0	Toggling	0	0	Toggling	0
In progress	0	Toggling	0	1	Toggling	0
Finished	1	Stop toggling	0	1	1	1
Exceed time limit	0	Toggling	1	1	Toggling	0

*1: The status Q3 is the time-out period indicator. When Q3=0, the device is in time-out period and is acceptable to another sector address to be erased. When Q3=1, the device is in erase operation and only erase suspend is valid.

*2: RY/BY# is open drain output pin and should be weakly connected to Vcc through a pull-up resistor.

*3: When an attempt is made to erase a protected sector, Q7 will output its complement data or Q6 continues to toggle for 100us or less and the device returned to read array status without erasing the data in the protected sector.

SECTOR ERASE SUSPEND

During sector erasure, sector erase suspend is the only valid command. If user issue erase suspend command in the time-out period of sector erasure, device time-out period will be over immediately and the device will go back to erase-suspended read array mode. If user issue erase suspend command during the sector erase is being operated, device will suspend the ongoing erase operation, and after the Tready1 ($\leq 20\mu\text{s}$) suspend finishes and the device will enter erase-suspended read array mode. User can judge if the device has finished erase suspend through Q6, Q7, and RY/BY#.

After device has entered erase-suspended read array mode, user can read other sectors not at erase suspend by the speed of T_{aa} ; while reading the sector in erase-suspend mode, device will output its status. User can use Q6 and Q2 to judge the sector is erasing or the erase is suspended.

Status	Q7	Q6	Q5	Q3	Q2	RY/BY#
Erase suspend read in erase suspended sector	1	No toggle	0	N/A	Toggle	1
Erase suspend read in non-erase suspended sector	Data	Data	Data	Data	Data	1
Erase suspend program in non-erase suspended sector	Q7#	Toggle	0	N/A	N/A	0

When the device has suspended erasing, user can execute the command sets except sector erase and chip erase, such as read silicon ID, sector protect verify, program, CFI query and erase resume.

SECTOR ERASE RESUME

Sector erase resume command is valid only when the device is in erase suspend state. After erase resume, user can issue another erase suspend command, but there should be a 400 μs interval between erase resume and the next erase suspend. If user issue infinite suspend-resume loop, or suspend-resume exceeds 1024 times, the time for erasing will increase.

QUERY COMMAND AND COMMON FLASH INTERFACE (CFI) MODE

MX29LV002C/MX29LV004C T/B features CFI mode. Host system can retrieve the operating characteristics, structure and vendor-specified information such as identifying information, memory size, byte/word configuration, operating voltages and timing information of this device by CFI mode. If the system writes the CFI Query command "98h", to address "55h"/"AAh" (depending on Word/Byte mode), the device will enter the CFI Query Mode, any time the device is ready to read array data. The system can read CFI information at the addresses given in Table 4.

Once user enters CFI query mode, user can not issue any other commands except reset command. The reset command is required to exit CFI mode and go back to the mode before entering CFI. The system can write the CFI Query command only when the device is in read mode, erase suspend, standby mode or automatic select mode.

Table 4-1. CFI mode: Identification Data Values (MX29LV002C/002NC and 004C only)
(All values in these tables are in hexadecimal)

Description	Address (h)	Data (h)
Query-unique ASCII string "QRY"	10	0051
	11	0052
	12	0059
Primary vendor command set and control interface ID code	13	0002
	14	0000
Address for primary algorithm extended query table	15	0040
	16	0000
Alternate vendor command set and control interface ID code	17	0000
	18	0000
Address for alternate algorithm extended query table	19	0000
	1A	0000

Table 4-2. CFI Mode: System Interface Data Values

Description	Address (h)	Data (h)
Vcc supply minimum program/erase voltage	1B	0027
Vcc supply maximum program/erase voltage	1C	0036
VPP supply minimum program/erase voltage	1D	0000
VPP supply maximum program/erase voltage	1E	0000
Typical timeout per single word/byte write, 2 ⁿ us	1F	0004
Typical timeout for maximum-size buffer write, 2 ⁿ us	20	0000
Typical timeout per individual block erase, 2 ⁿ ms	21	000A
Typical timeout for full chip erase, 2 ⁿ ms	22	0000
Maximum timeout for word/byte write, 2 ⁿ times typical	23	0005
Maximum timeout for buffer write, 2 ⁿ times typical	24	0000
Maximum timeout per individual block erase, 2 ⁿ times typical	25	0004
Maximum timeout for chip erase, 2 ⁿ times typical	26	0000

Table 4-3. CFI Mode: Device Geometry Data Values

Description	Address (h)	Data (h)
Device size = 2 ⁿ in number of bytes (MX29LV002C)	27	0012
Device size = 2 ⁿ in number of bytes (MX29LV004C)	27	0013
Flash device interface description	28	0000
	29	0000
Maximum number of bytes in buffer write = 2 ⁿ (not support)	2A	0000
	2B	0000
Number of erase regions within device	2C	0004
Index for Erase Bank Area 1	2D	0000
[2E,2D] = # of same-size sectors in region 1-1	2E	0000
[30, 2F] = sector size in multiples of 256-bytes	2F	0040
	30	0000
Index for Erase Bank Area 2	31	0001
	32	0000
	33	0020
	34	0000
Index for Erase Bank Area 3	35	0000
	36	0000
	37	0080
	38	0000
Index for Erase Bank Area 4 (for MX29LV002C)	39	0002
Index for Erase Bank Area 4 (for MX29LV004C)	39	0006
	3A	0000
	3B	0000
	3C	0001

Table 4-4. CFI Mode: Primary Vendor-Specific Extended Query Data Values

Description	Address (h)	Data (h)
Query - Primary extended table, unique ASCII string, PRI	40	0050
	41	0052
	42	0049
Major version number, ASCII	43	0031
Minor version number, ASCII	44	0030
Unlock recognizes address (0= recognize, 1= don't recognize)	45	0000
Erase suspend (2= to both read and program)	46	0002
Sector protect (N= # of sectors/group)	47	0001
Temporary sector unprotect (1=supported)	48	0001
Sector protect/Chip unprotect scheme	49	0004
Simultaneous R/W operation (0=not supported)	4A	0000
Burst mode (0=not supported)	4B	0000
Page mode (0=not supported)	4C	0000



ABSOLUTE MAXIMUM STRESS RATINGS

Surrounding Temperature with Bias	-65°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage Range	
Vcc	-0.5 V to +4.0 V
RESET#, A9 and OE#	-0.5 V to +12.5 V
The other pins.	-0.5 V to Vcc +0.5 V
Output Short Circuit Current (less than one second)200 mA

OPERATING TEMPERATURE AND VOLTAGE

Commercial (C) Grade

Surrounding Temperature (TA).....	0°C to +70°C
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Industrial (I) Grade

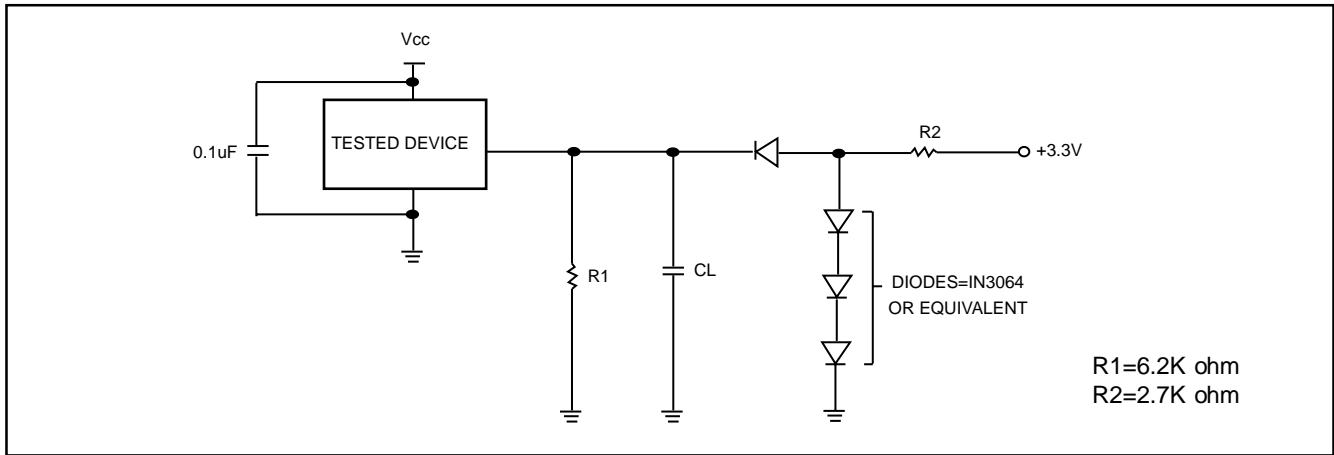
Surrounding Temperature (TA).....	-40°C to +85°C
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Vcc Supply Voltages

Full Vcc Range.....	+2.7 V to 3.6 V
Regulated Vcc Voltage Range.....	+3.0 V to 3.6 V

DC CHARACTERISTICS

Symbol	Description	Min	Typ	Max	Remark
Iilk	Input Leak			± 1.0uA	
Iilk9	A9 Leak			35uA	A9=12.5V
Iolk	Output Leak			± 1.0uA	
Icr1	Read Current(5MHz)		7mA	12mA	CE#=Vil, OE#=Vih
Icr2	Read Current(1MHz)		2mA	4mA	CE#=Vil, OE#=Vih
Icw	Write Current		15mA	30mA	CE#=Vil, OE#=Vih, WE#=Vil
I _{sb}	Standby Current		0.2uA	5uA	V _{cc} =V _{cc} max, other pin disable
I _{sr}	Reset Current		0.2uA	5uA	V _{cc} =V _{cc} max, RESET# enable, other pin disable
I _{sb} s	Sleep Mode Current		0.2uA	5uA	
V _{il}	Input Low Voltage	-0.5V		0.8V	
V _{ih}	Input High Voltage	0.7xV _{cc}		V _{cc} +0.3V	
V _{hv}	Very High Voltage for hardware Protect/Unprotect/Auto Select/ Temporary Unprotect	11.5V		12.5V	
V _{ol}	Output Low Voltage			0.45V	I _{ol} =4.0mA
V _{oh1}	Ouput High Voltage	0.85xV _{cc}			I _{oh1} =-2mA
V _{oh2}	Ouput High Voltage	V _{cc} -0.4V			I _{oh2} =-100uA

SWITCHING TEST CIRCUITS

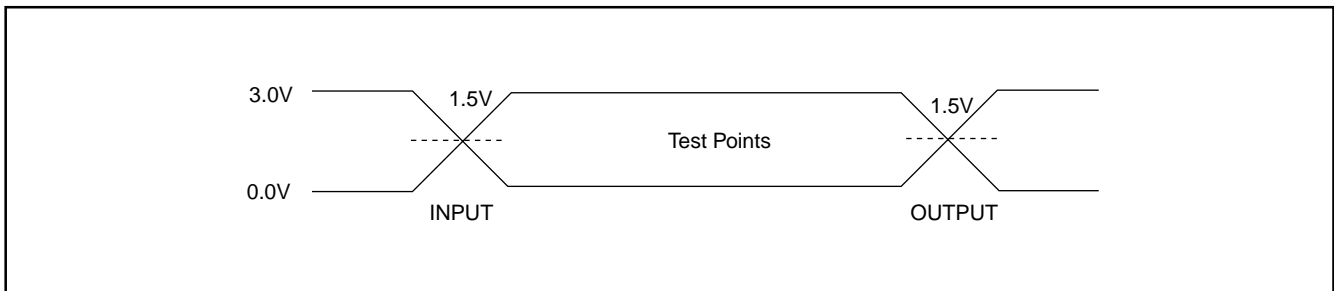
Test Condition

Output Load : 1 TTL gate

Output Load Capacitance, CL : 30pF(45R/55R/70ns)/100pF(90ns)

Rise/Fall Times : 5ns

In/Out reference levels : 1.5V

SWITCHING TEST WAVEFORMS

AC CHARACTERISTICS

MX29LV002C/002NC

Symbol	Description	Min	Typ	Max	Unit
Taa	Valid data output after address			70/90	ns
Tce	Valid data output after CE# low			70/90	ns
Toe	Valid data output after OE# low			30/35	ns
Tdf	Data output floating after OE# high			25/30	ns
Toh	Output hold time from the earliest rising edge of address, CE#, OE#	0			ns
Trc	Read period time	70/90			ns
Twc	Write period time	70/90			ns
Tcwc	Command write period time	70/90			ns
Tas	Address setup time	0			ns
Tah	Address hold time	45			ns
Tds	Data setup time	35/45			ns
Tdh	Data hold time	0			ns
Tvcs	Vcc setup time	50			us
Tcs	Chip enable Setup time	0			ns
Tch	Chip enable hold time	0			ns
Toes	Output enable setup time	0			ns
Toeh	Output enable hold time	Read	0		ns
Toeh		Toggle & Data# Polling	10		ns
Tws	WE# setup time	0			ns
Twh	WE# hold time	0			ns
Tcep	CE# pulse width	35			ns
Tceph	CE# pulse width high	30			ns
Twp	WE# pulse width	35			ns
Twph	WE# pulse width high	30			ns
Tbusy	Program/Erase active time by RY/BY#			90	ns
Tghwl	Read recover time before write	0			ns
Tghel	Read recover time before write (CE# Control)	0			ns
Twhwh1	Byte Program operation		9	300	us
Twhwh2	Sector Erase Operation		0.7	15	sec
Tbal	Sector Add hold time			50	us

MX29LV004C (Restricted Vcc=3.0V~3.6V for 45R/55R)

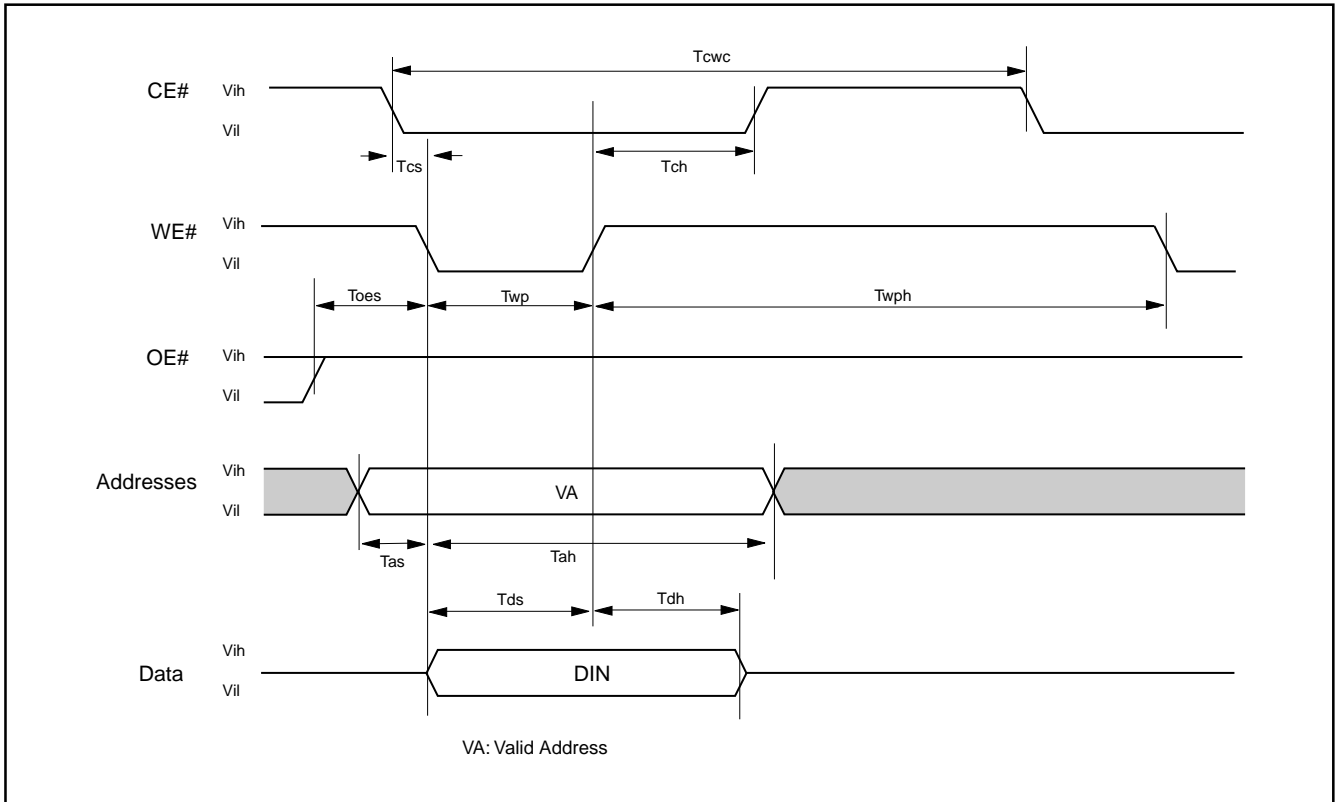
Symbol	Description	Min	Typ	Max	Unit
Taa	Valid data output after address			45/55/70/90	ns
Tce	Valid data output after CE# low			45/55/70/90	ns
Toe	Valid data output after OE# low			30/30/30/35	ns
Tdf	Data output floating after OE# high			25/25/25/30	ns
Tch	Output hold time from the earliest rising edge of address, CE#, OE#	0			ns
Trc	Read period time	45/55/70/90			ns
Twc	Write period time	45/55/70/90			ns
Tcwc	Command write period time	45/55/70/90			ns
Tas	Address setup time	0			ns
Tah	Address hold time	45			ns
Tds	Data setup time	35/35/35/45			ns
Tdh	Data hold time	0			ns
Tvcs	Vcc setup time	50			us
Tcs	Chip enable Setup time	0			ns
Tch	Chip enable hold time	0			ns
Toes	Output enable setup time	0			ns
Toeh	Output enable hold time	Read	0		ns
Toeh		Toggle & Data# Polling	10		ns
Tws	WE# setup time	0			ns
Twh	WE# hold time	0			ns
Tcep	CE# pulse width	35			ns
Tceph	CE# pulse width high	30			ns
Twp	WE# pulse width	35			ns
Twph	WE# pulse width high	30			ns
Tbusy	Program/Erase active time by RY/BY#			90	ns
Tghwl	Read recover time before write	0			ns
Tghel	Read recover time before write (CE# Control)	0			ns
Twhwh1	Byte Program operation		9	300	us
Twhwh2	Sector Erase Operation		0.7	15	sec
Tbal	Sector Add hold time			50	us

Notes: Only 40-TSOP provide RY/BY# pin.

MX29LV008C (Restricated Vcc=3.0V~3.6V for 55R)

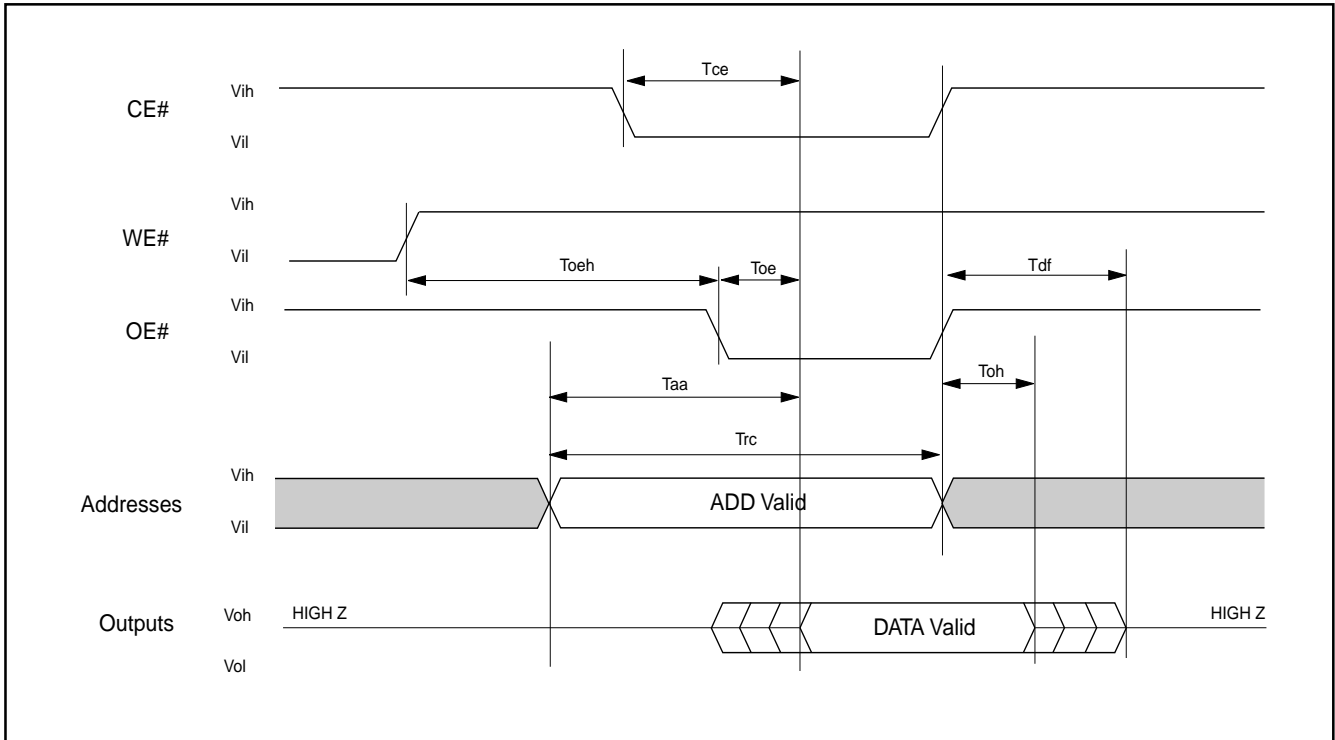
Symbol	Description	Min	Typ	Max	Unit
Taa	Valid data output after address			55/70/90	ns
Tce	Valid data output after CE# low			55/70/90	ns
Toe	Valid data output after OE# low			30/30/35	ns
Tdf	Data output floating after OE# high			25/25/30	ns
Toh	Output hold time from the earliest rising edge of address, CE#, OE#	0			ns
Trc	Read period time	55/70/90			ns
Twc	Write period time	55/70/90			ns
Tcwc	Command write period time	55/70/90			ns
Tas	Address setup time	0			ns
Tah	Address hold time	45			ns
Tds	Data setup time	35/35/45			ns
Tdh	Data hold time	0			ns
Tvcs	Vcc setup time	50			us
Tcs	Chip enable Setup time	0			ns
Tch	Chip enable hold time	0			ns
Toes	Output enable setup time	0			ns
Toeh	Output enable hold time	Read	0		ns
Toeh		Toggle & Data# Polling	10		ns
Tws	WE# setup time	0			ns
Twh	WE# hold time	0			ns
Tcep	CE# pulse width	35			ns
Tceph	CE# pulse width high	30			ns
Twp	WE# pulse width	35			ns
Twph	WE# pulse width high	30			ns
Tbusy	Program/Erase active time by RY/BY#			90	ns
Tghwl	Read recover time before write	0			ns
Tghel	Read recover time before write (CE# Control)	0			ns
Twhwh1	Byte Program operation		9	300	us
Twhwh2	Sector Erase Operation		0.7	15	sec
Tbal	Sector Add hold time			50	us

Figure 1. COMMAND WRITE OPERATION



READ/RESET OPERATION

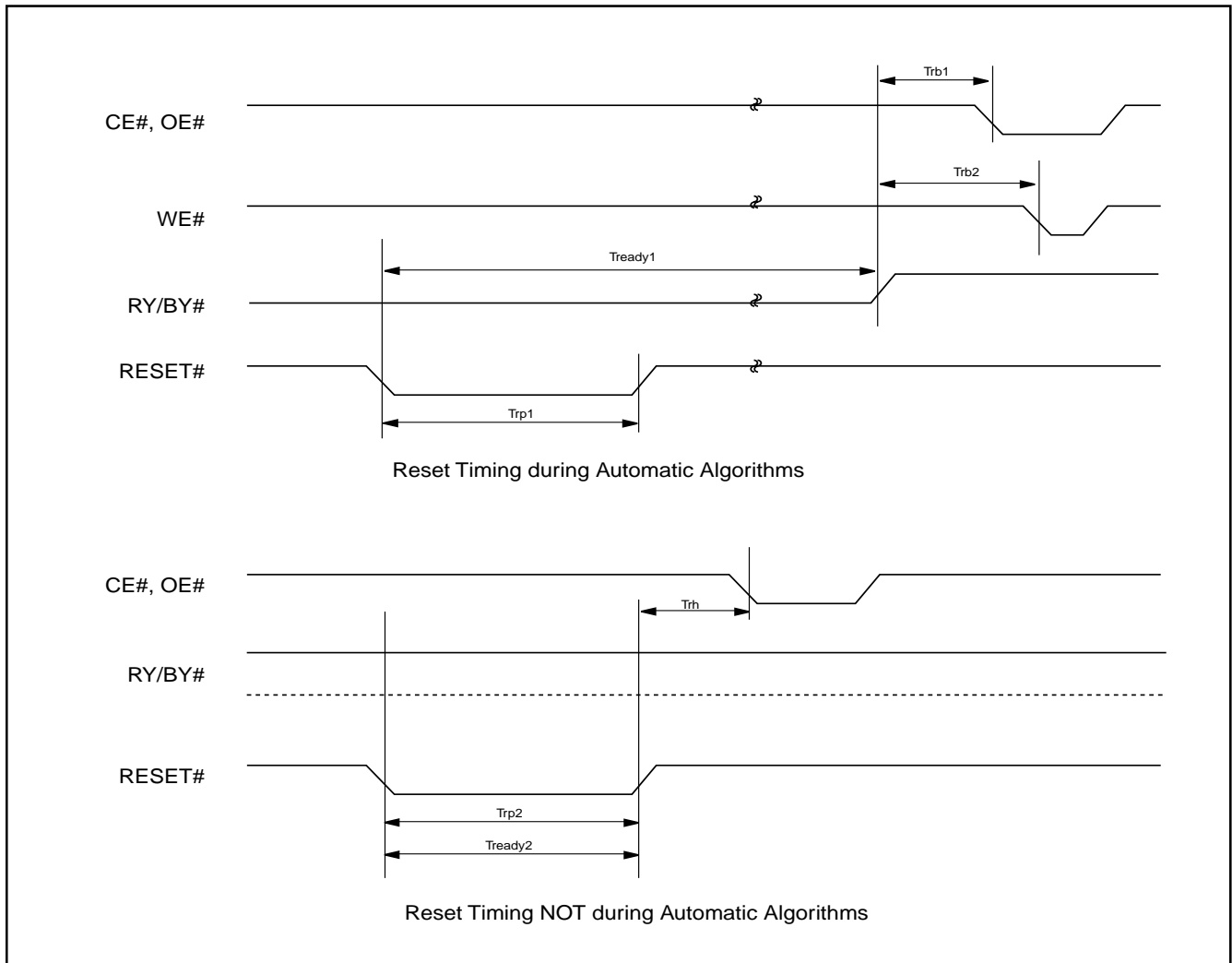
Figure 2. READTIMING WAVEFORMS



AC CHARACTERISTICS

Item	Description	Setup	Speed	Unit
Trp1	RESET# Pulse Width (During Automatic Algorithms)	MIN	500	ns
Trp2	RESET# Pulse Width (NOT During Automatic Algorithms)	MIN	500	ns
Trh	RESET# High Time Before Read	MIN	50	ns
Trb1	RY/BY# Recovery Time (to CE#, OE# go low)	MIN	0	ns
Trb2	RY/BY# Recovery Time (to WE# go low)	MIN	50	ns
Tready1	RESET# PIN Low (During Automatic Algorithms) to Read or Write	MAX	20	us
Tready2	RESET# PIN Low (NOT During Automatic Algorithms) to Read or Write	MAX	500	ns

Figure 3. RESET# TIMING WAVEFORM



ERASE/PROGRAM OPERATION

Figure 4. AUTOMATIC CHIP ERASE TIMING WAVEFORM

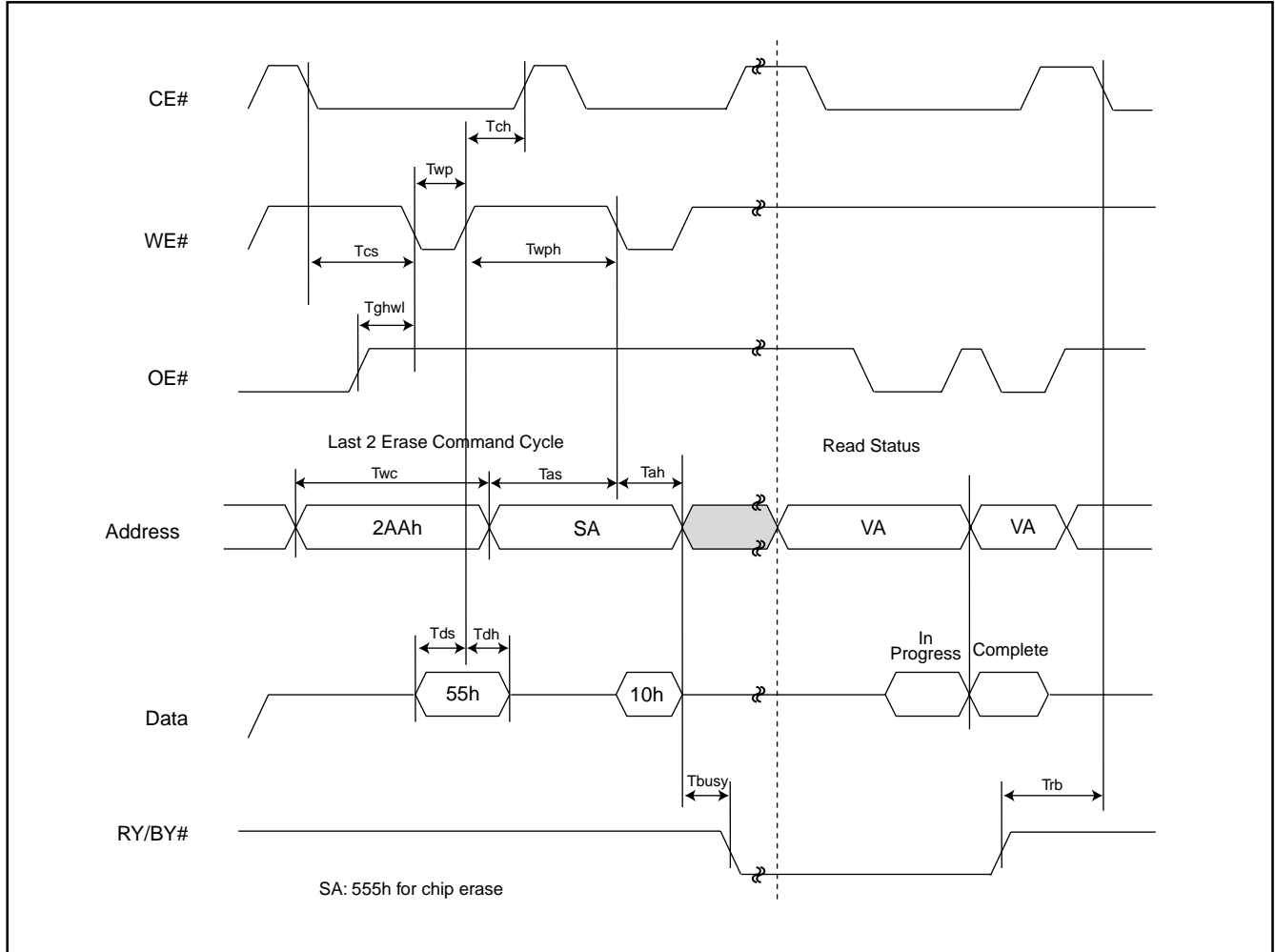


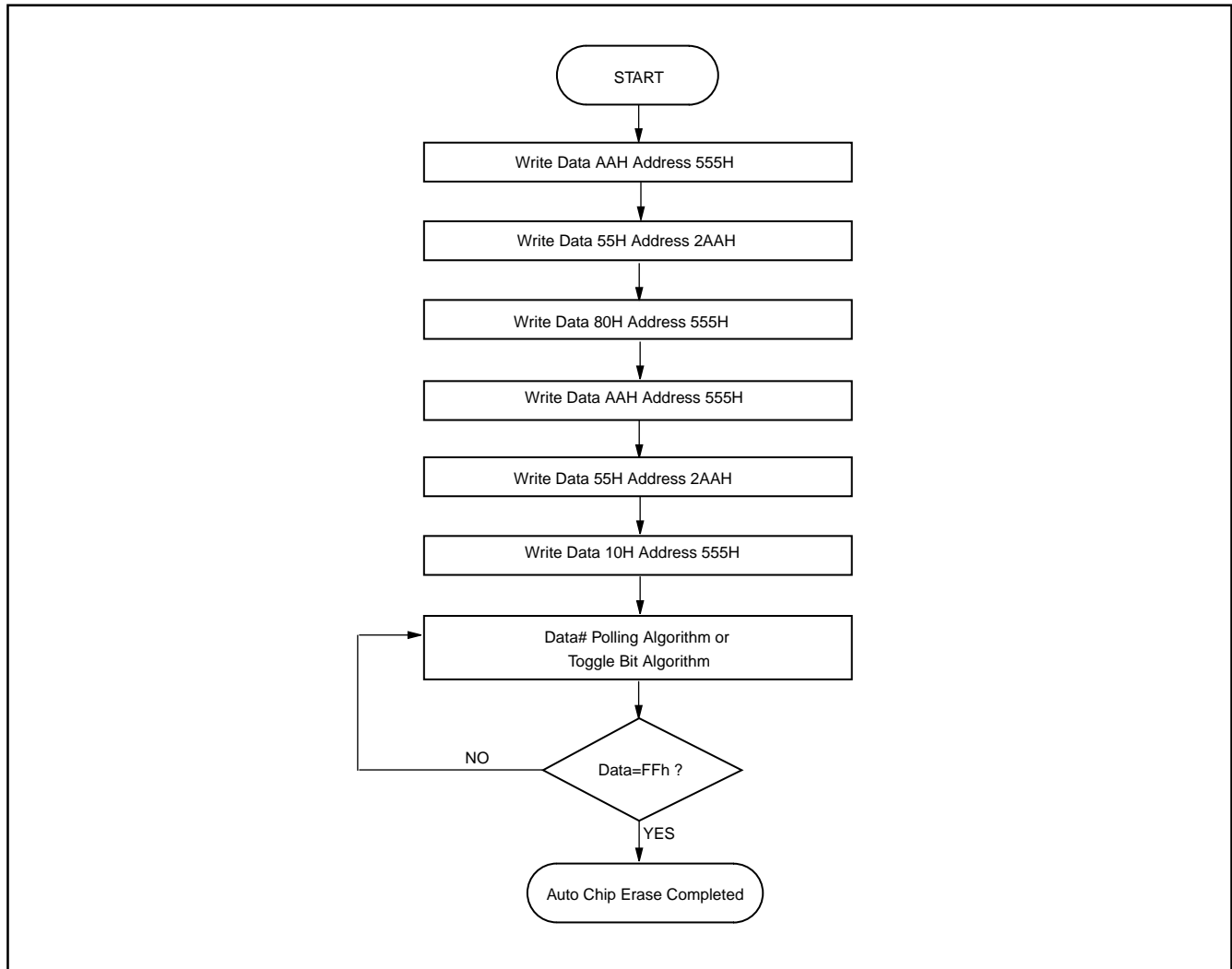
Figure 5. AUTOMATIC CHIP ERASE ALGORITHM FLOWCHART

Figure 6. AUTOMATIC SECTOR ERASE TIMING WAVEFORM

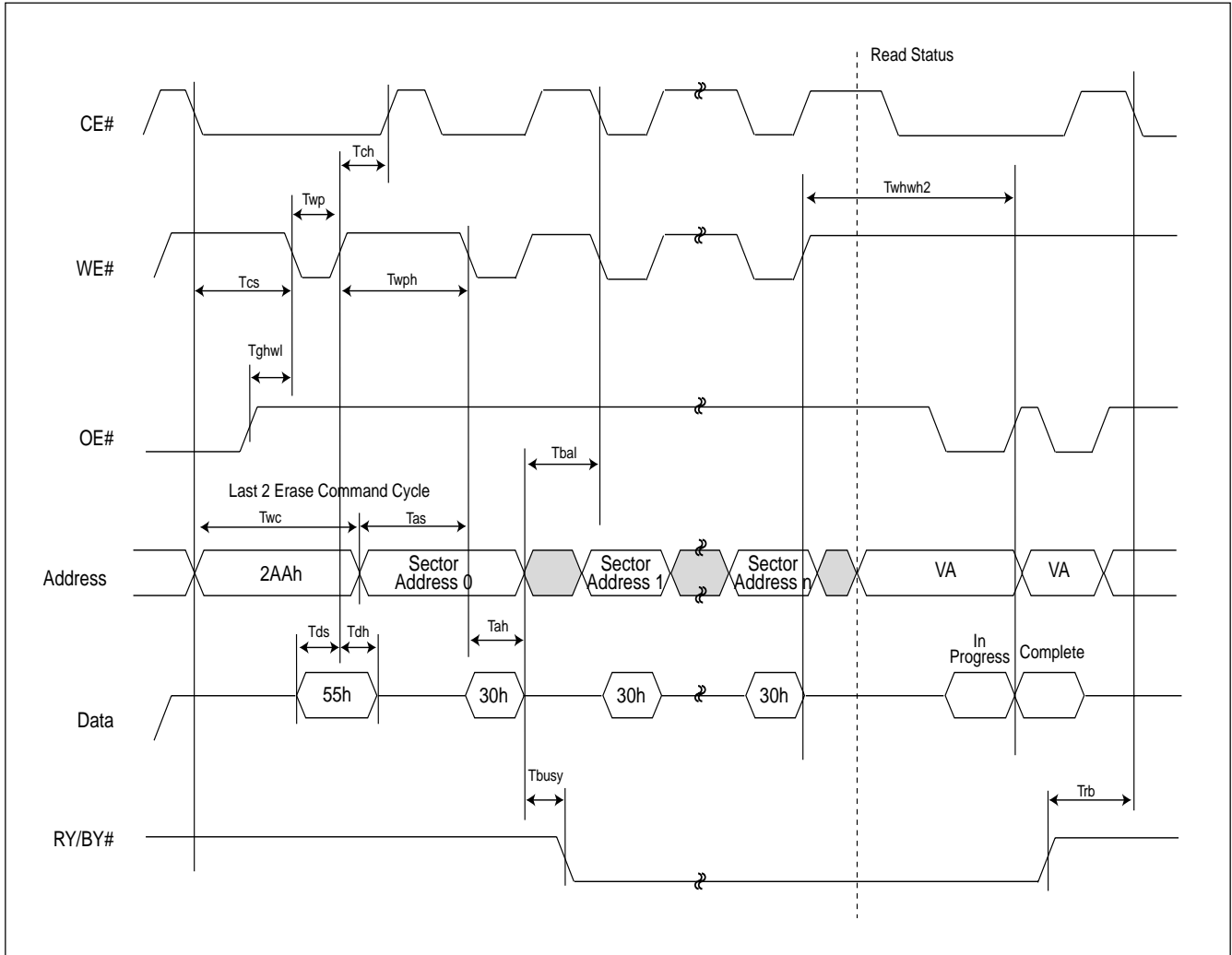


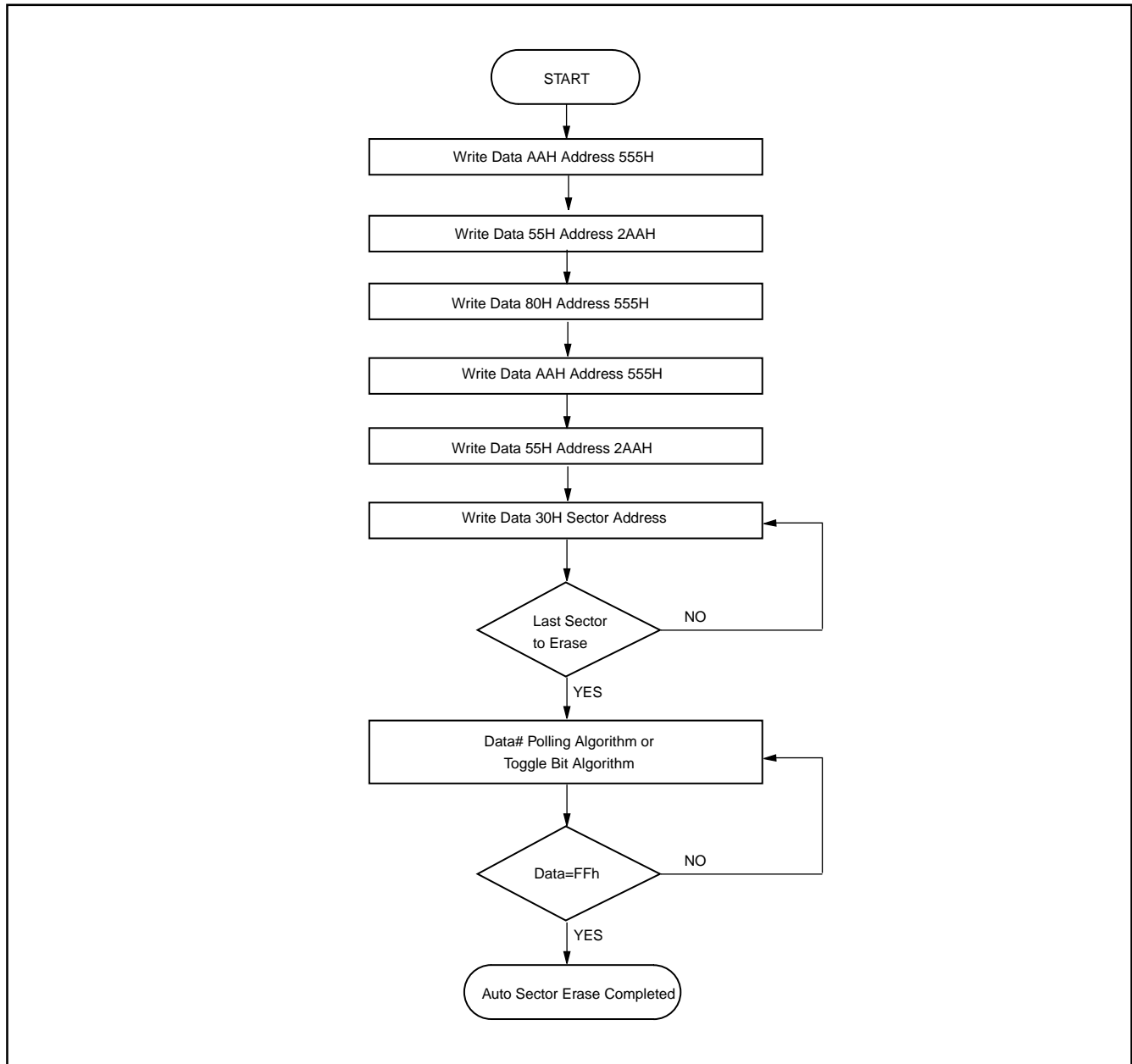
Figure 7. AUTOMATIC SECTOR ERASE ALGORITHM FLOWCHART

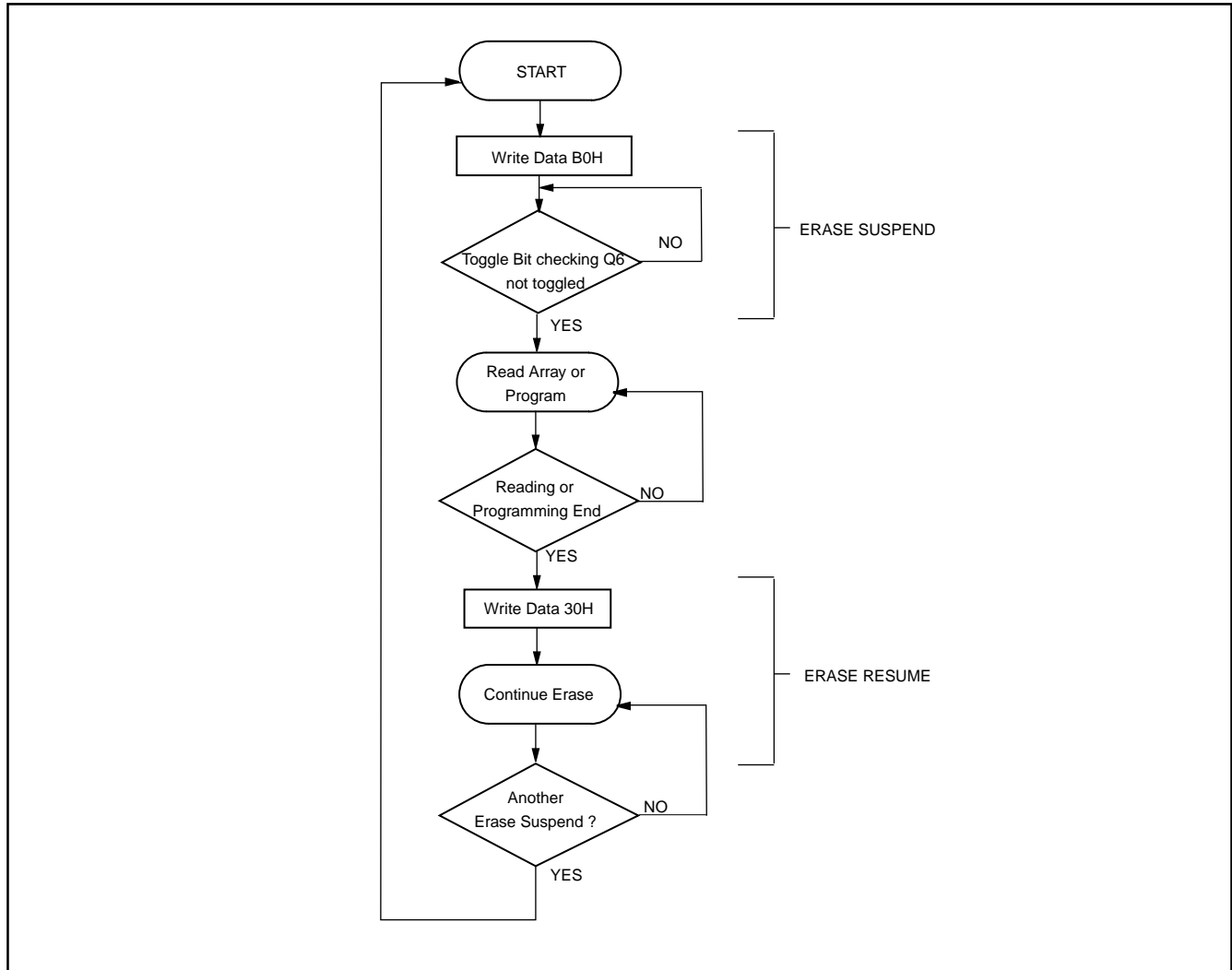
Figure 8. ERASE SUSPEND/RESUME FLOWCHART

Figure 9. AUTOMATIC PROGRAMTIMING WAVEFORMS

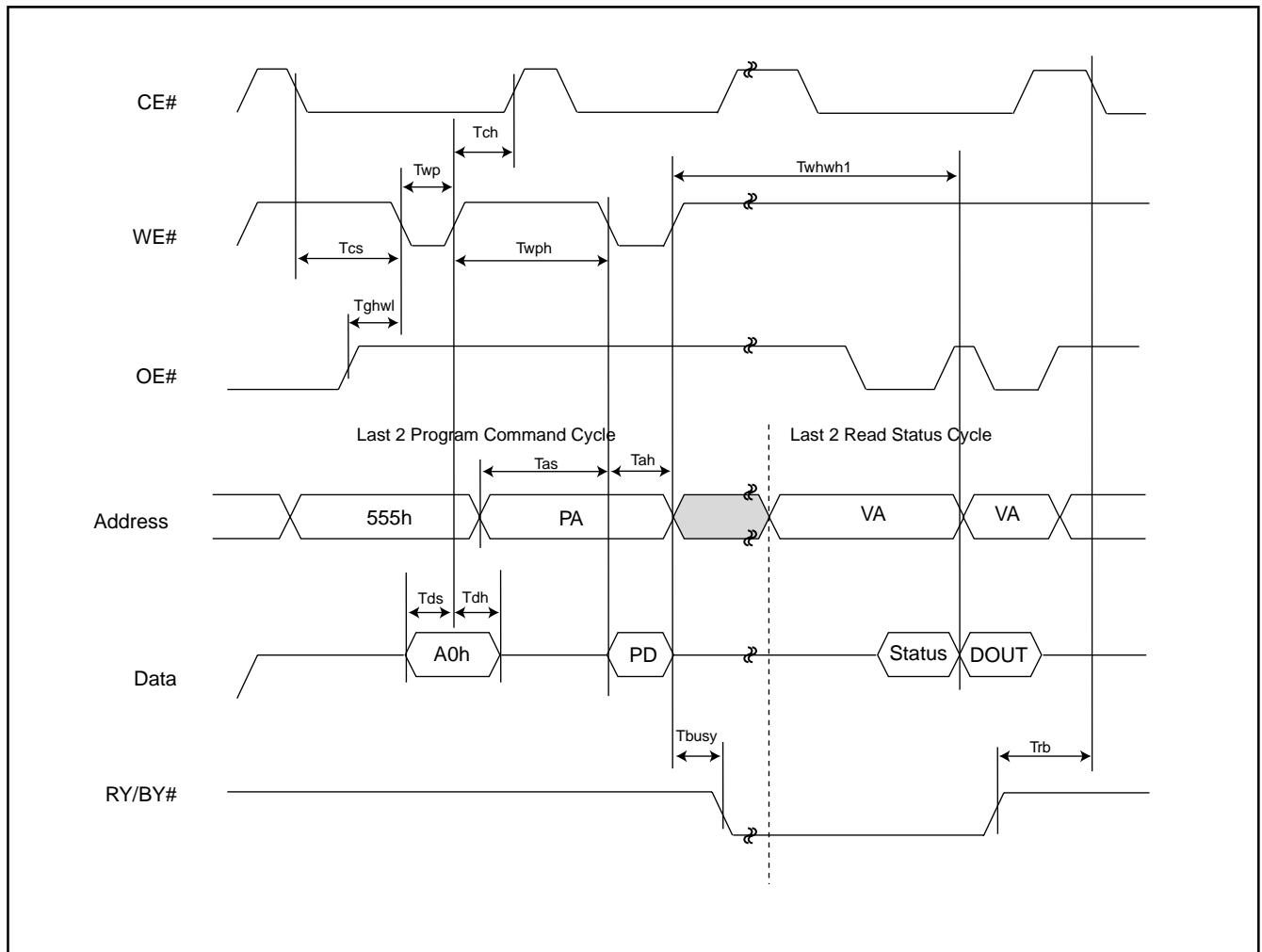


Figure 10. CE# CONTROLLED WRITE TIMING WAVEFORM

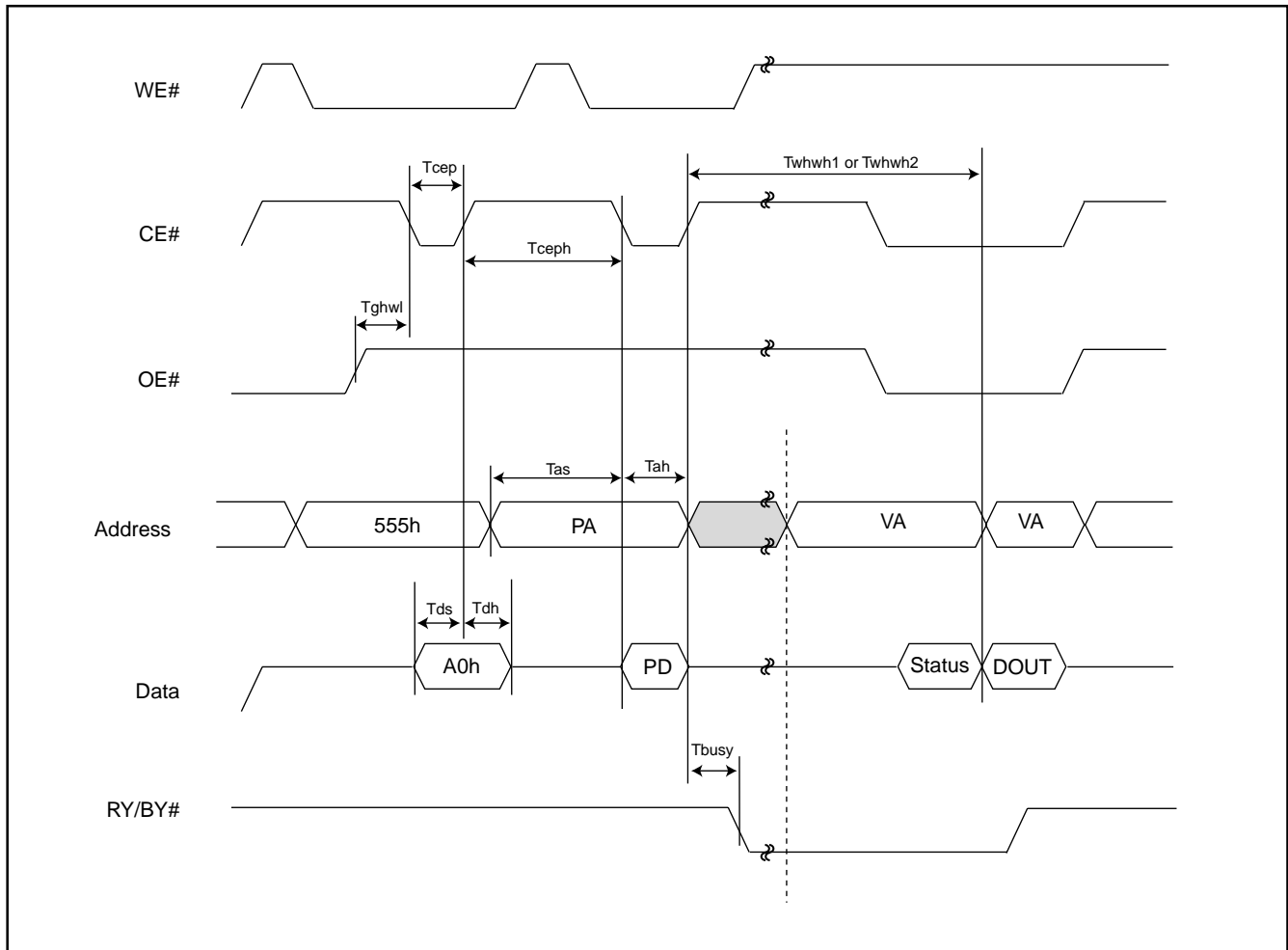
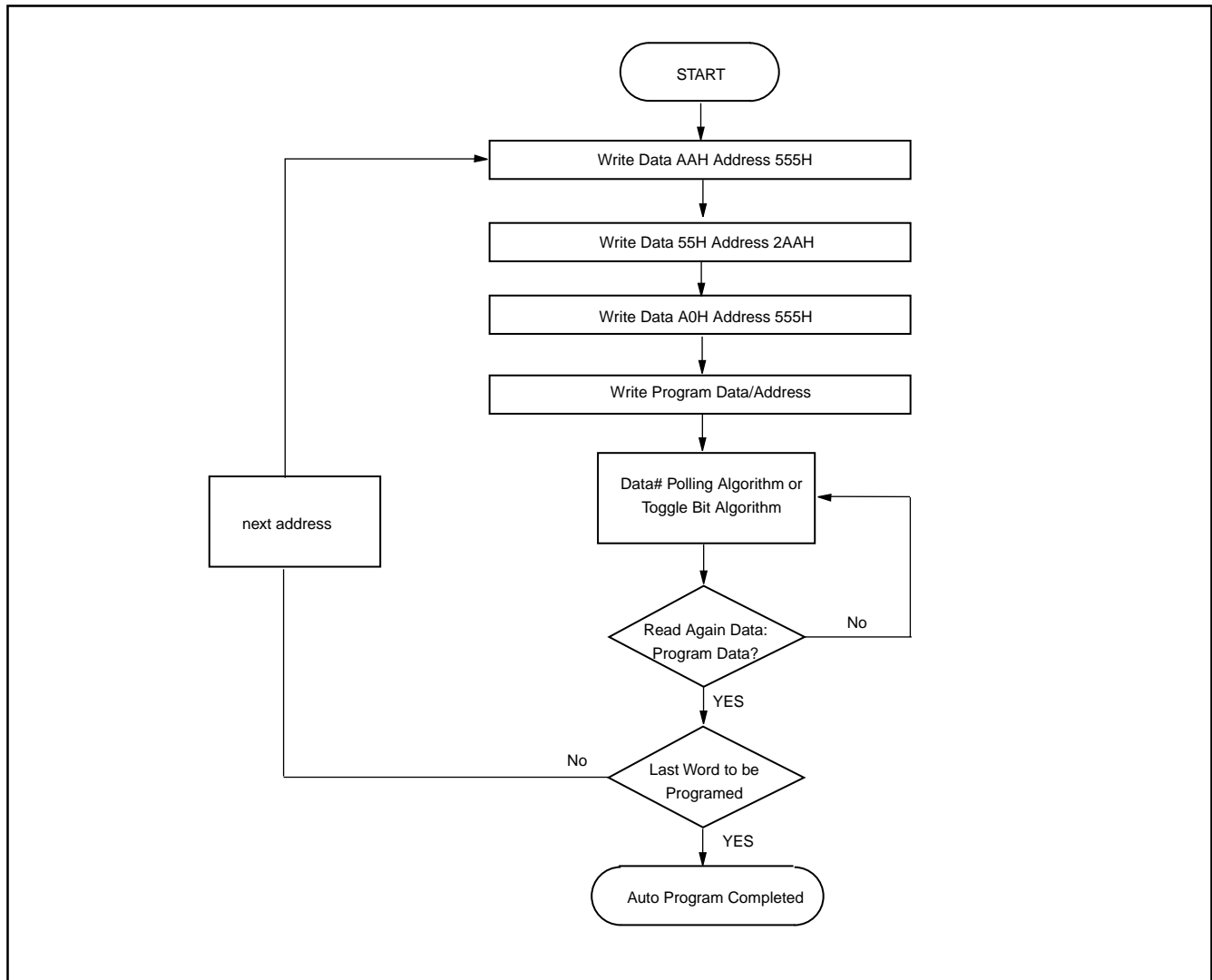


Figure 11. AUTOMATIC PROGRAMMING ALGORITHM FLOWCHART

SECTOR PROTECT/CHIP UNPROTECT

Figure 12. Sector Protect/Chip Unprotect Waveform (RESET# Control)

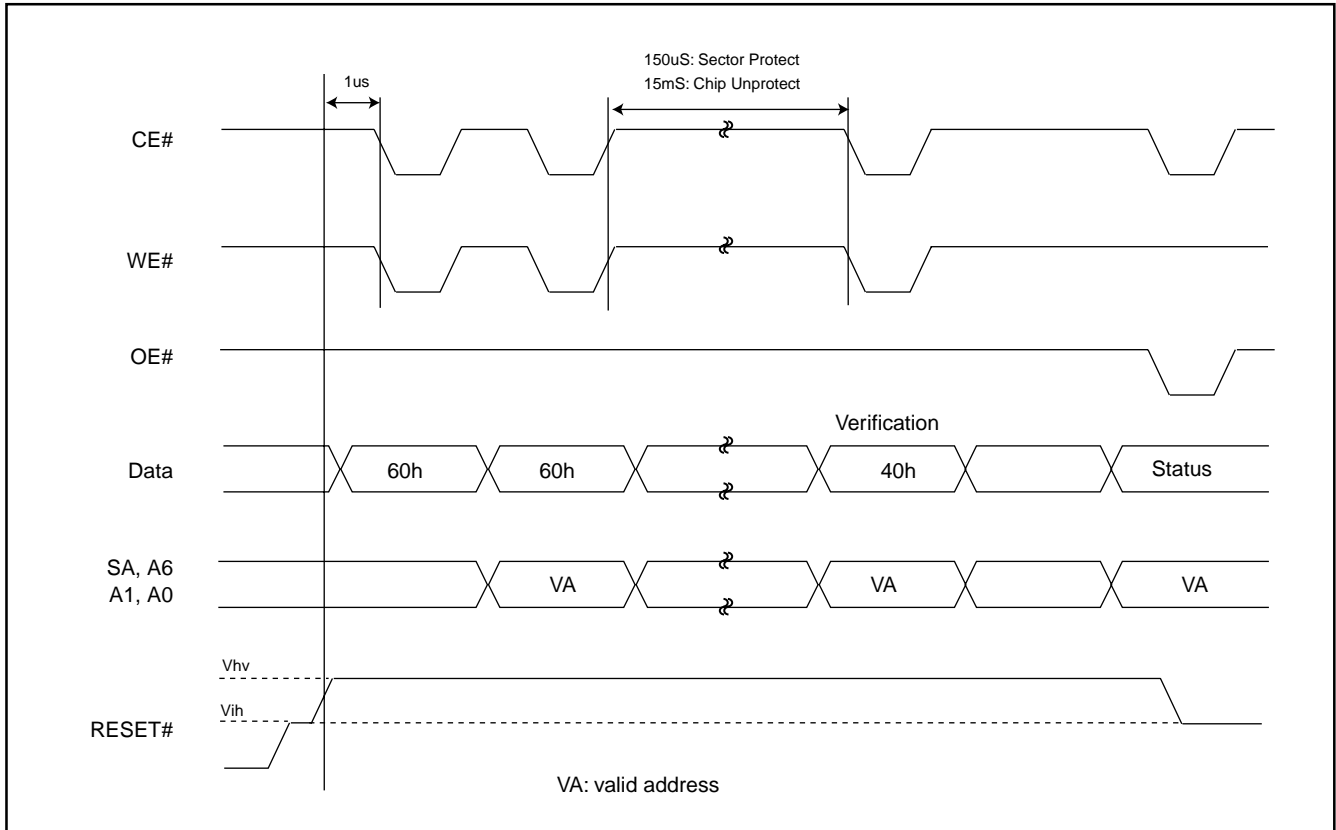


Figure 13-1. IN-SYSTEM SECTOR PROTECT WITH RESET# = Vhv

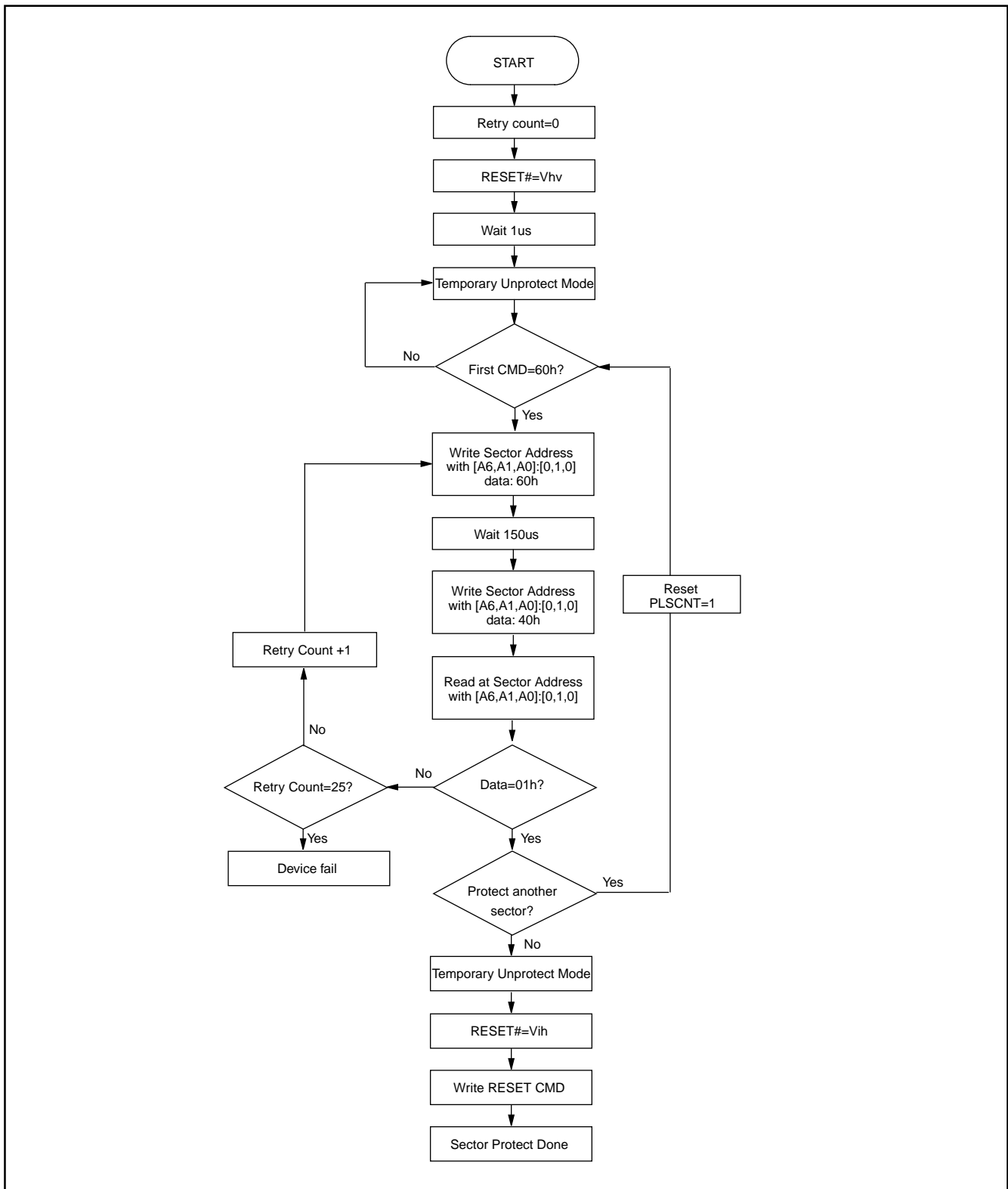


Figure 13-2. CHIP UNPROTECT ALGORITHMS WITH RESET#=Vhv

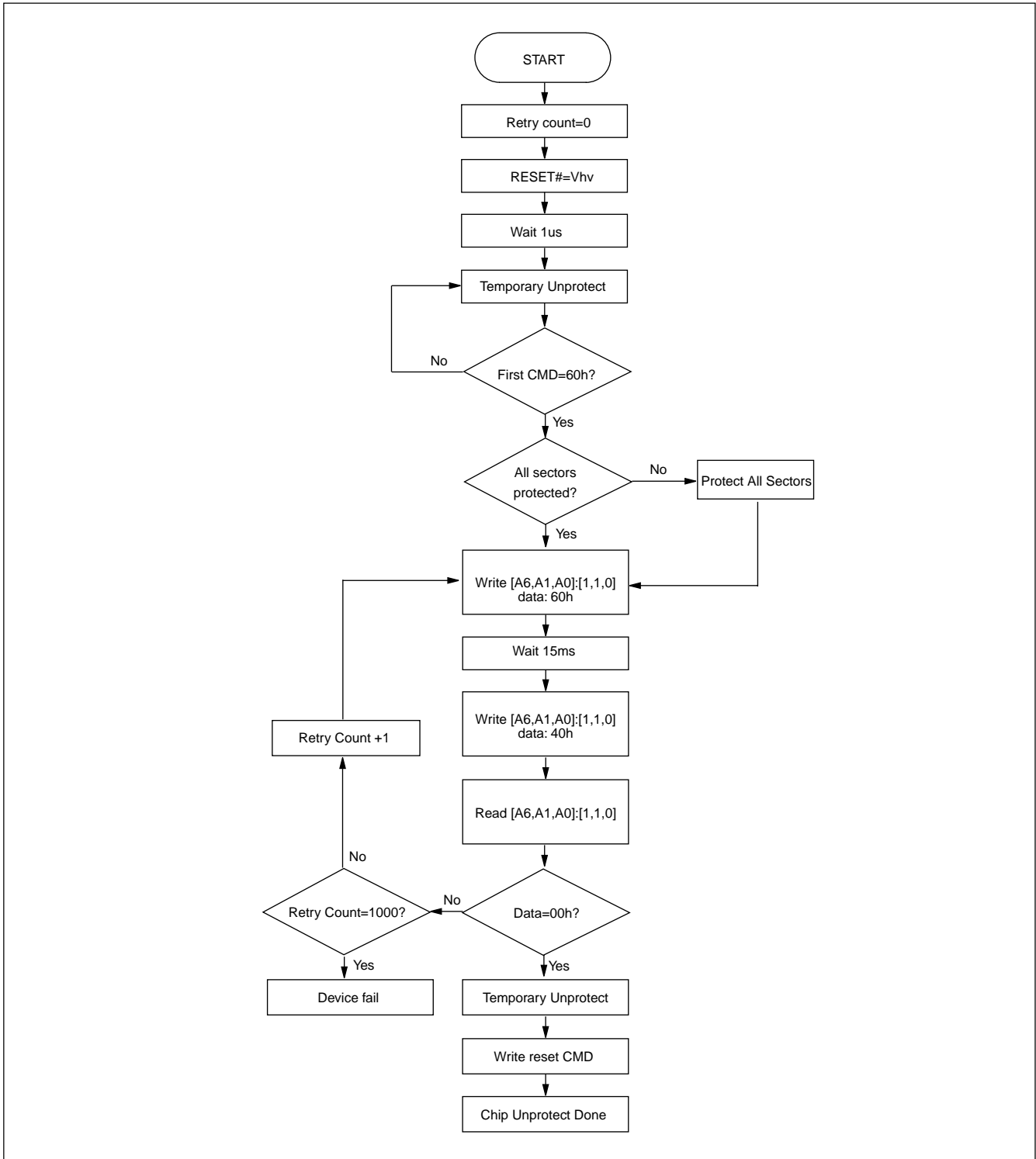
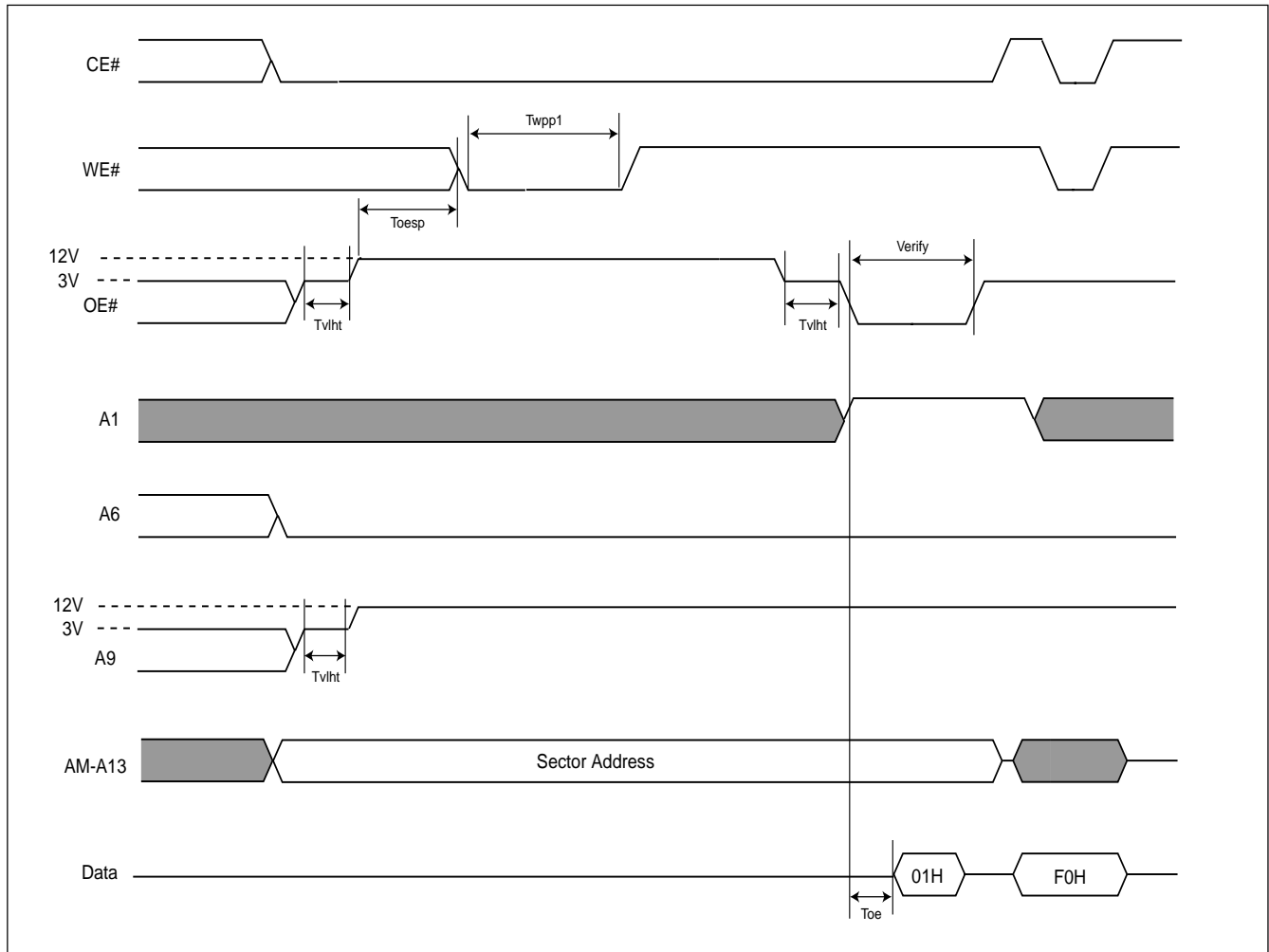


Figure 14. SECTOR PROTECT TIMING WAVEFORM (A9, OE# Control)



- Notes:
- T_{vht} (Voltage transition time)=4us min.
 - T_{wpp1} (Write pulse width for sector protect)=100ns min, 10us(Typ.)
 - T_{wpp2} (Write pulse width for chip unprotected)=100ns min, 12ms(Typ.)
 - T_{oesp} (OE# setup time to WE# active)=4us min.

Figure 15. SECTOR PROTECTION ALGORITHM (A9, OE# Control)

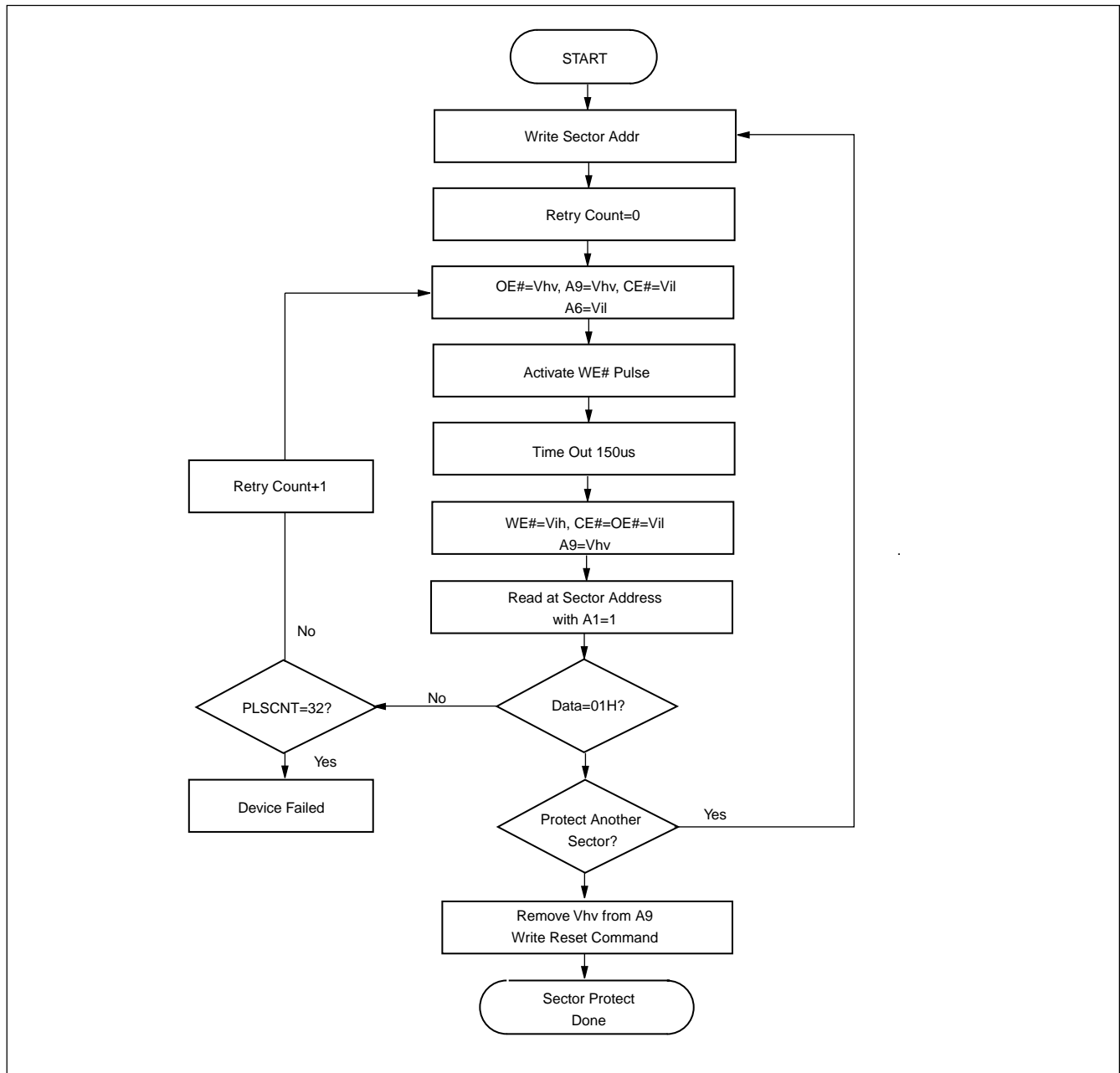
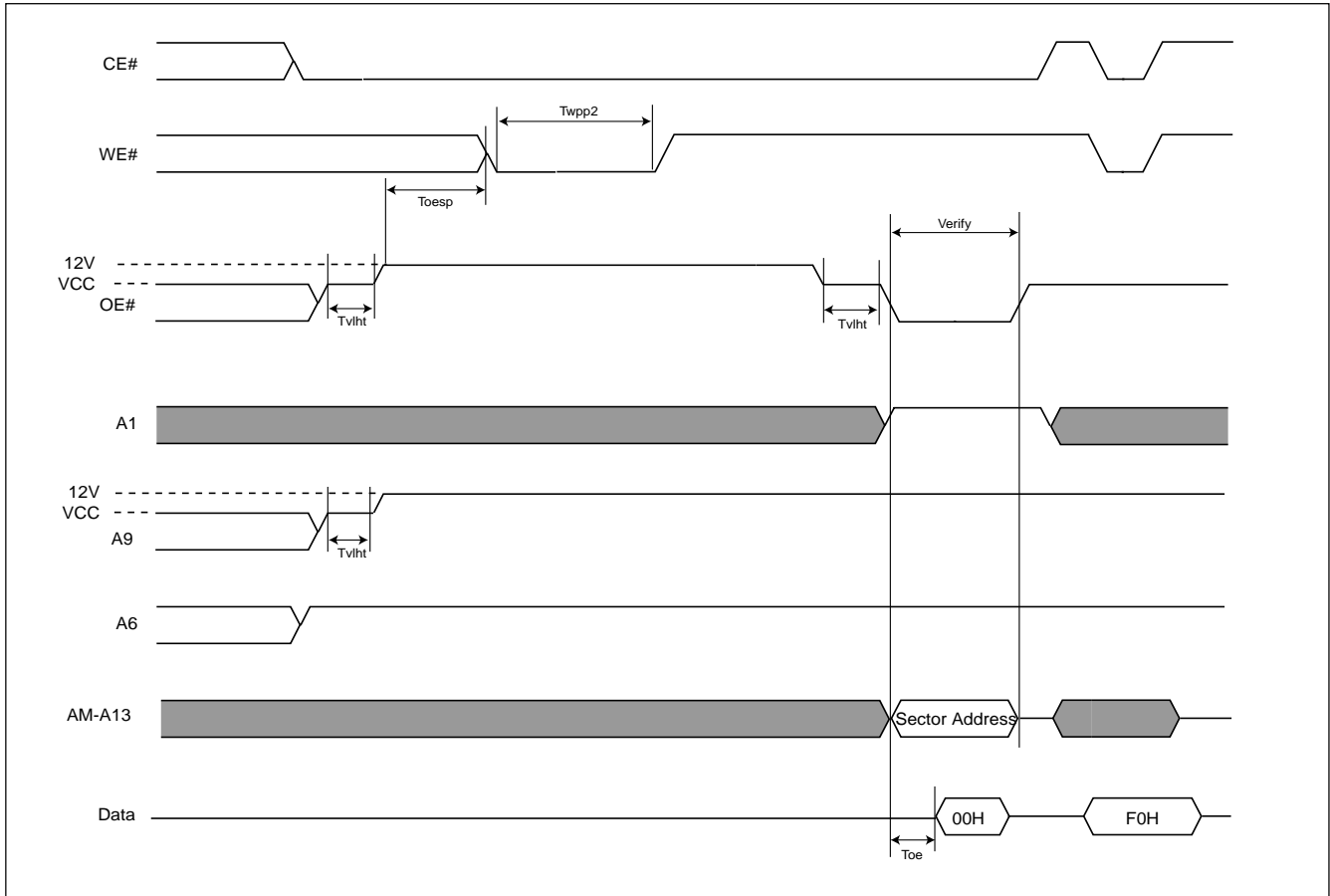


Figure 16. TIMING WAVEFORM FOR CHIP UNPROTECTION (A9, OE# Control)



- Notes:
- T_{vlt} (Voltage transition time)=4us min.
 - T_{wpp1} (Write pulse width for sector protect)=100ns min, 10us(Typ.)
 - T_{wpp2} (Write pulse width for chip unprotect)=100ns min, 12ms(Typ.)
 - T_{oesp} (OE# setup time to WE# active)=4us min.

Figure 17. CHIP UNPROTECTION ALGORITHM (A9, OE# Control)

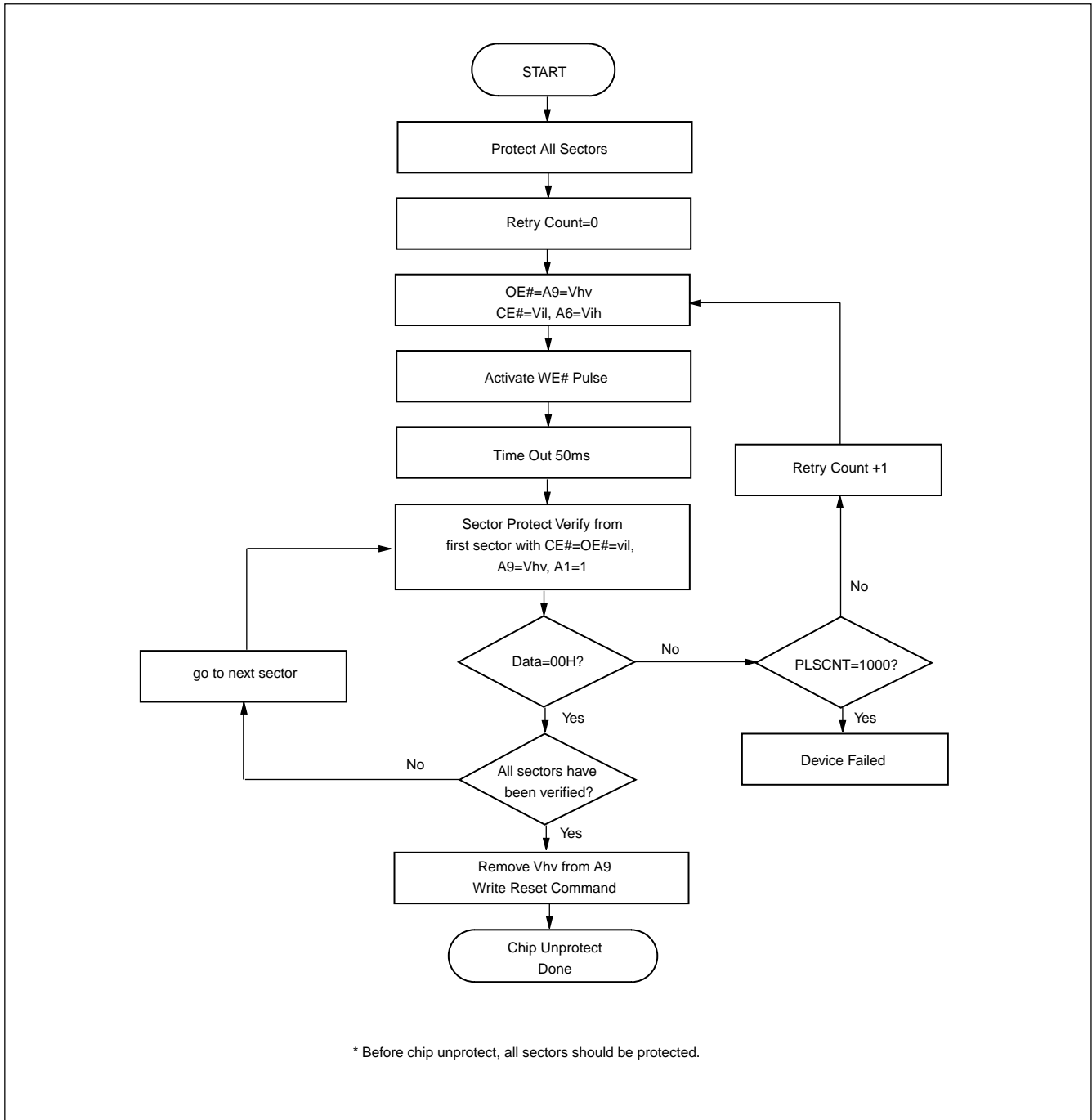


Table 5. TEMPORARY SECTOR UNPROTECT

Parameter	Alt	Description	Condition	Speed	Unit
Trpvhh	Tvidr	RESET# Rise Time to Vhv and Vhv Fall Time to RESET#	MIN	500	ns
Tvhhwl	Trsp	RESET# Vhv to WE# Low	MIN	4	us

Figure 18. TEMPORARY SECTOR UNPROTECT WAVEFORMS

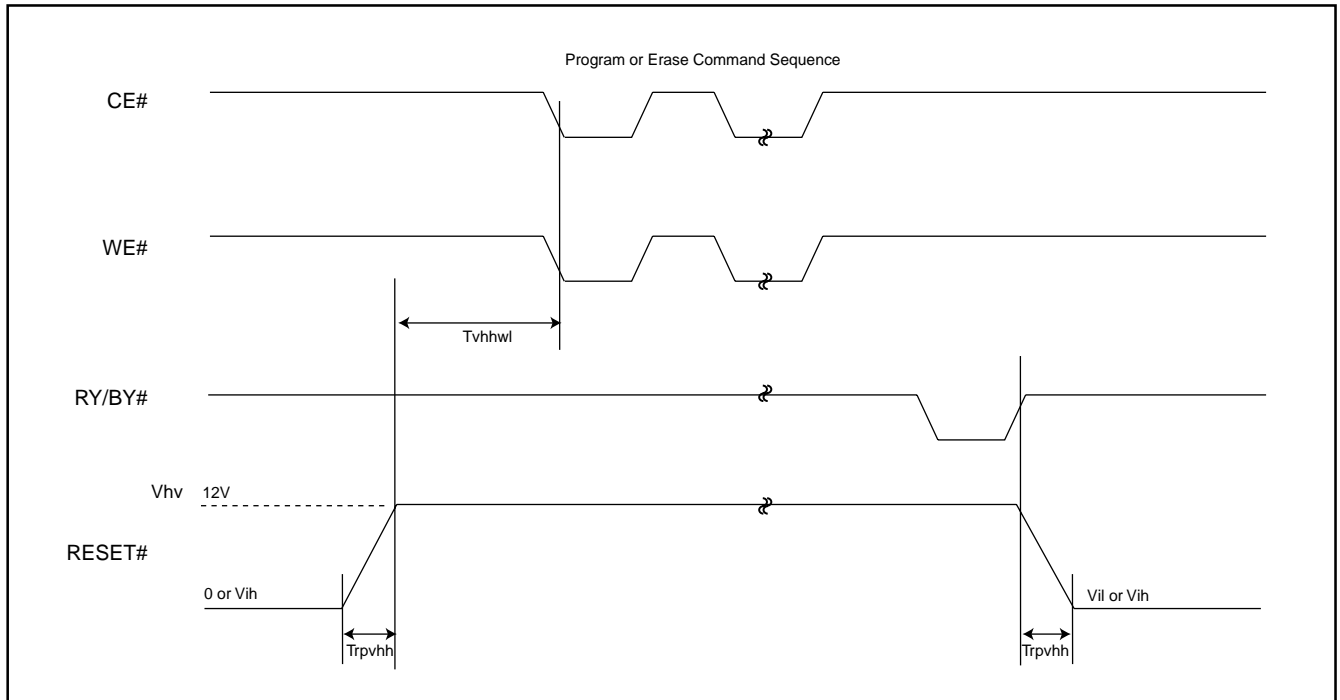
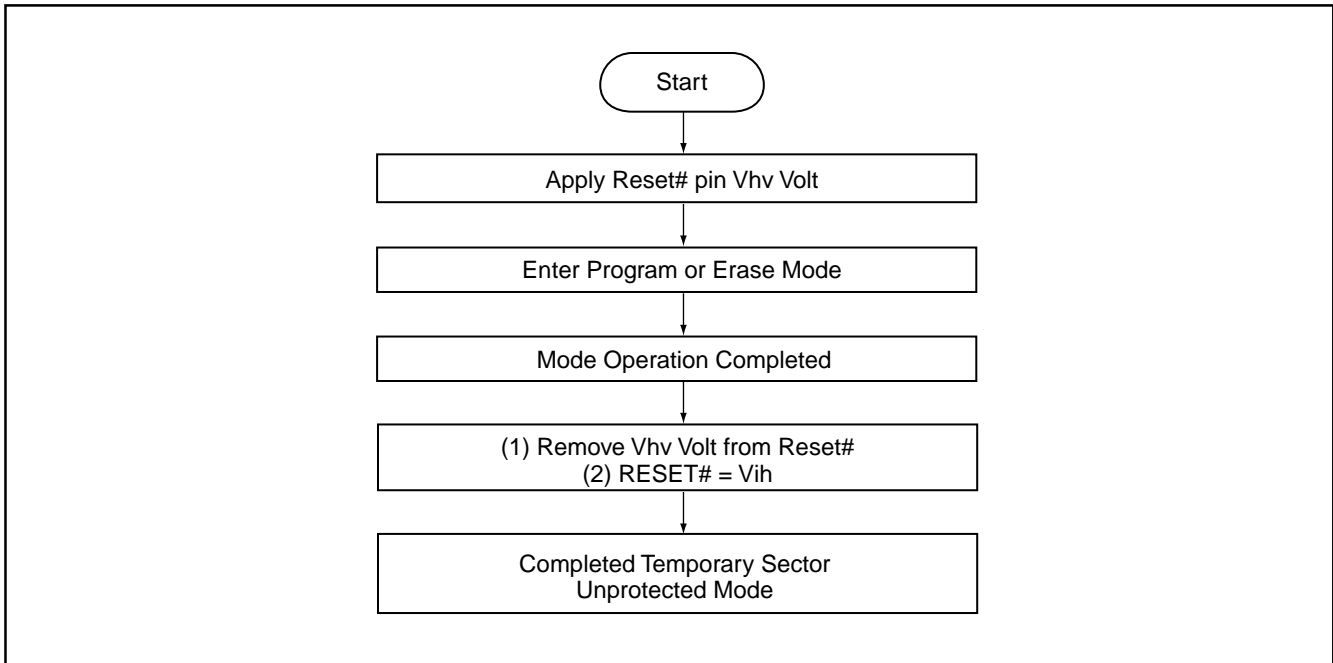
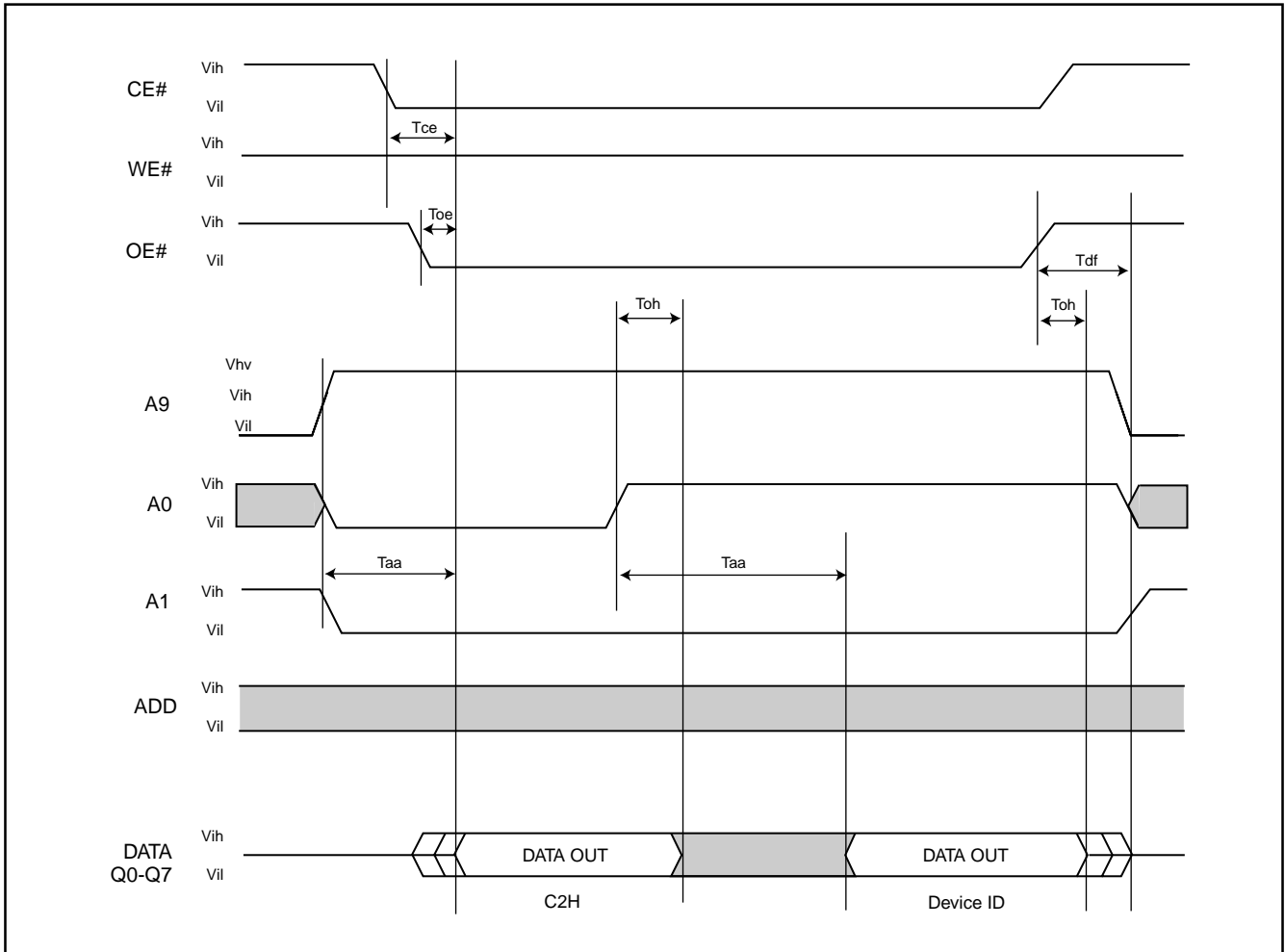


Figure 19. TEMPORARY SECTOR UNPROTECT FLOWCHART**Notes:**

1. Temporary unprotect all protected sectors Vhv=11.5~12.5V.
2. The protected conditions of the protected sectors are the same to temporary sector unprotect mode.

Figure 20. SILICON ID READTIMING WAVEFORM



Notes:

Device ID : MX29LV002CT: 59, MX29LV002CB: 5A
 MX29LV004CT: B5, MX29LV004CB: B6
 MX29LV008CT: 3E, MX29LV008CB: 37

WRITE OPERATION STATUS

Figure 21. DATA# POLLING TIMING WAVEFORMS (DURING AUTOMATIC ALGORITHMS)

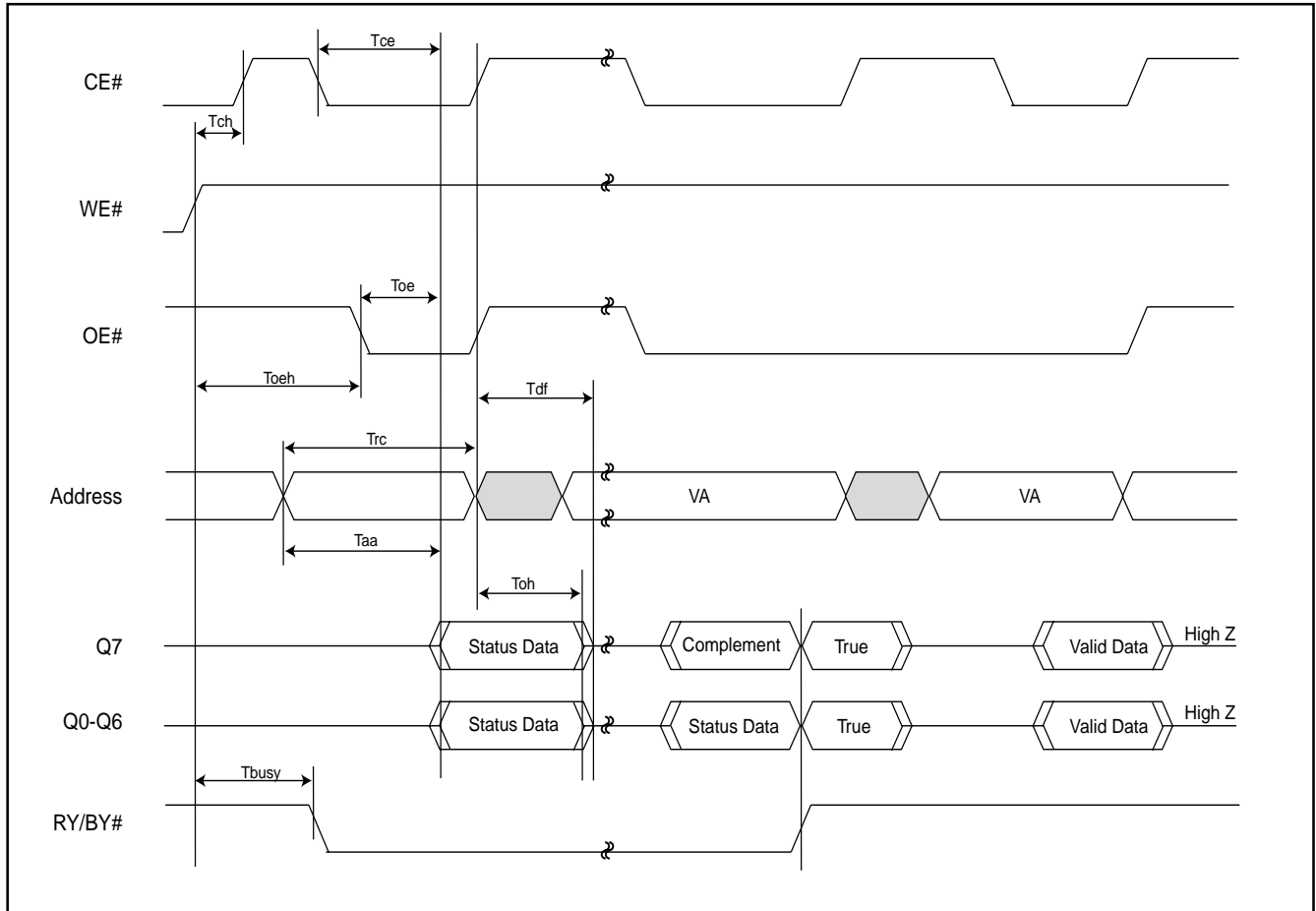
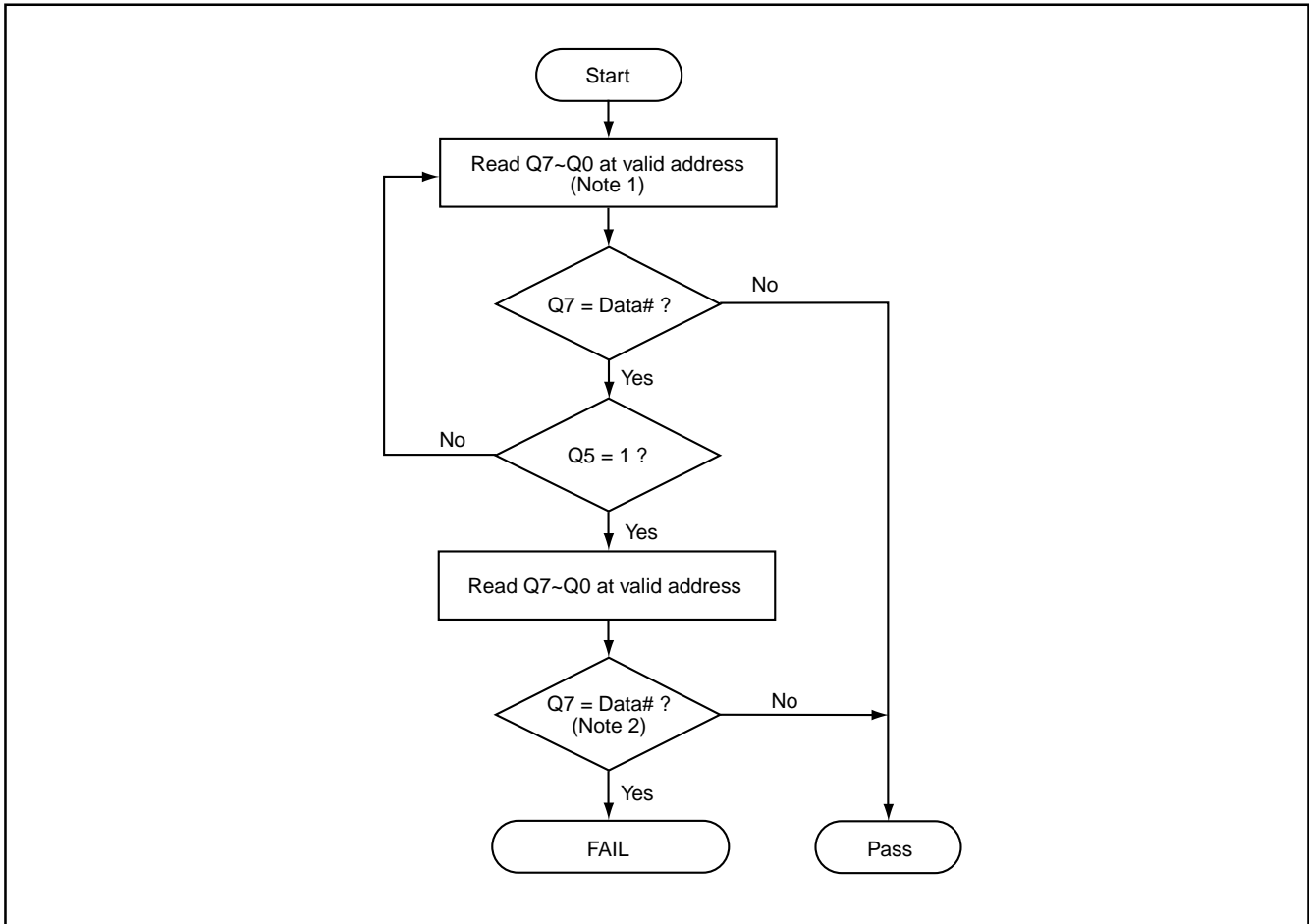


Figure 22. Data# Polling Algorithm**Notes:**

1. For programming, valid address means program address.
For erasing, valid address means erase sectors address.
2. Q7 should be rechecked even Q5="1" because Q7 may change simultaneously with Q5.

Figure 23. TOGGLE BIT TIMING WAVEFORMS (DURING AUTOMATIC ALGORITHMS)

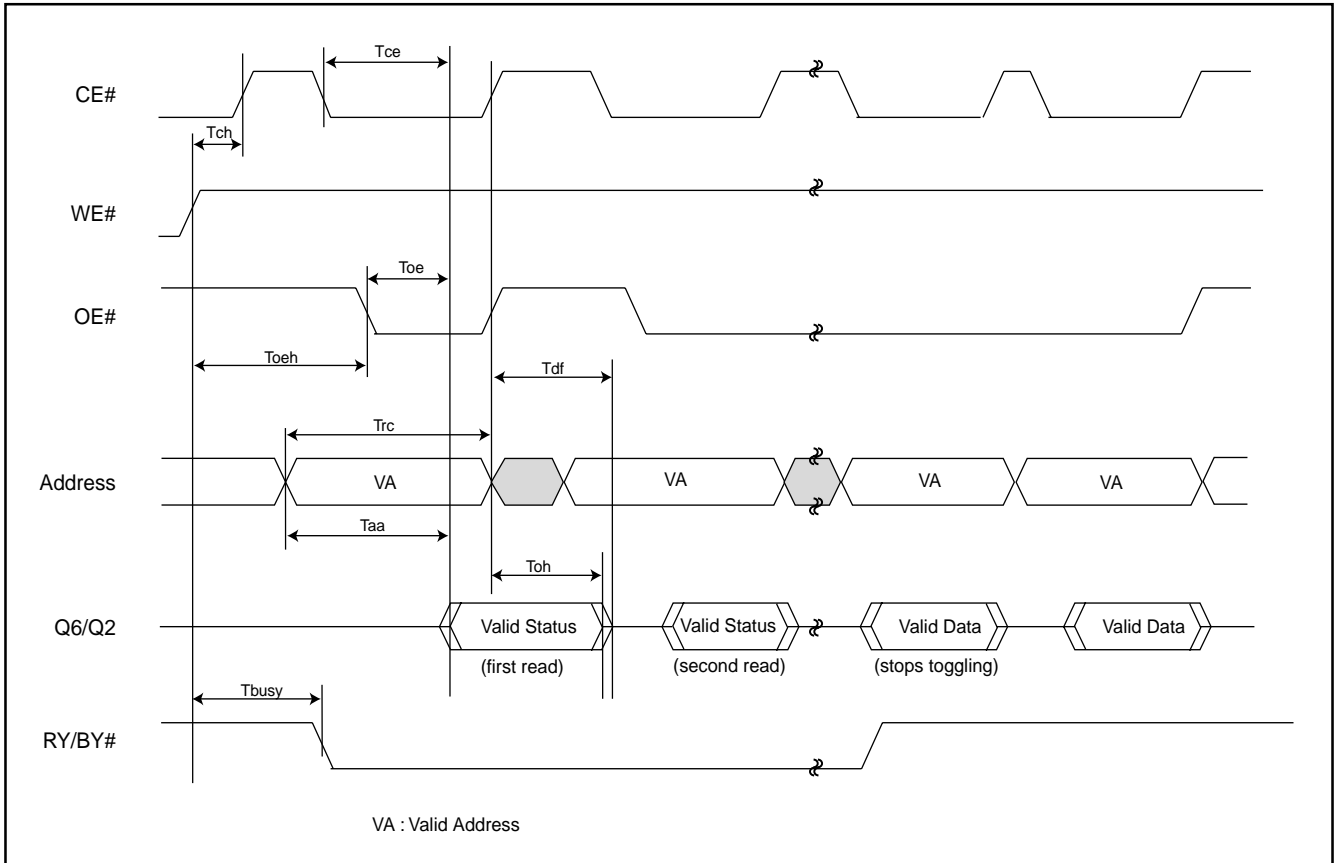
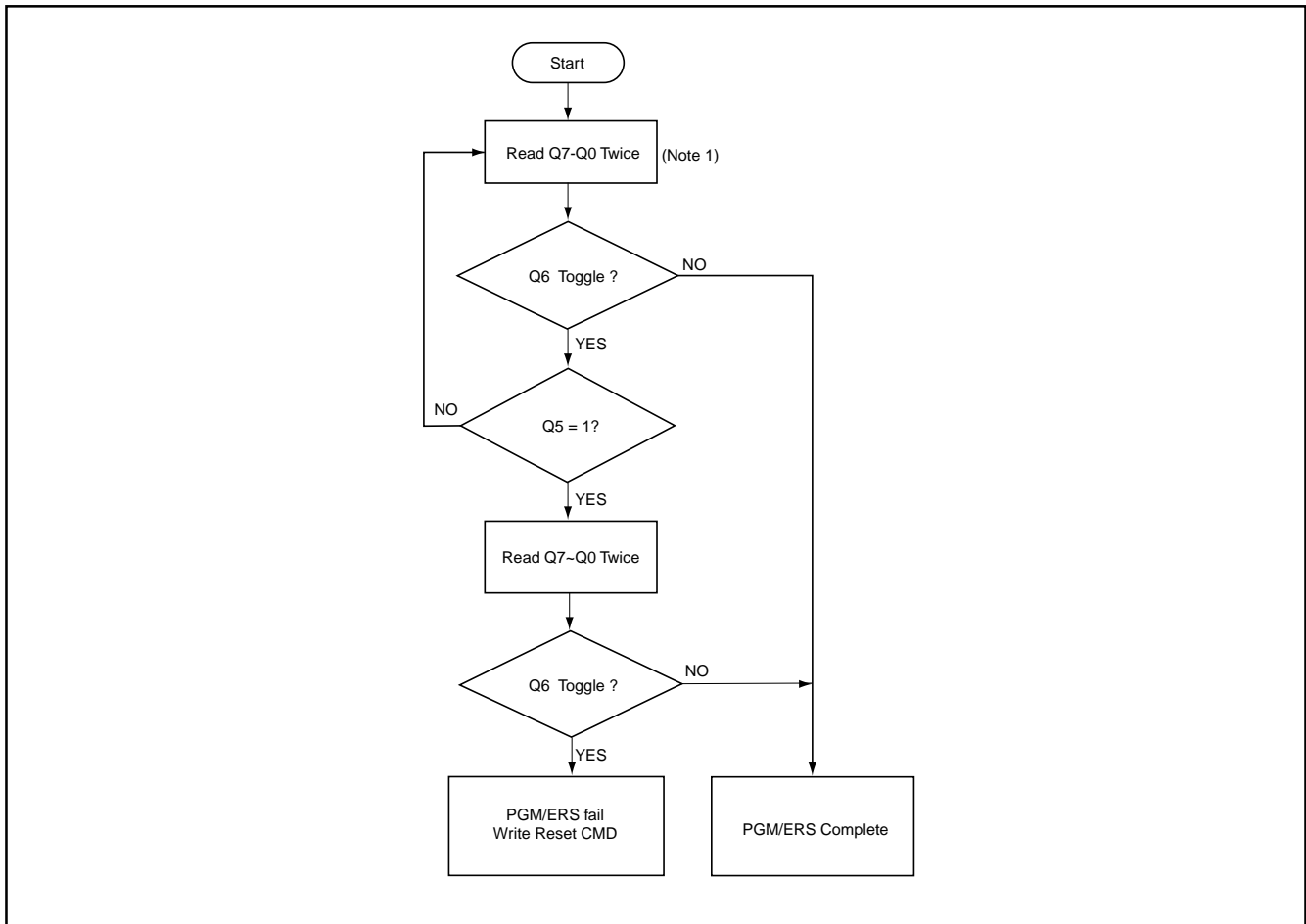


Figure 24. Toggle Bit Algorithm**Notes:**

1. Read toggle bit twice to determine whether or not it is toggling.
2. Recheck toggle bit because it may stop toggling as Q5 changes to "1".

RECOMMENDED OPERATING CONDITIONS

At Device Power-Up

AC timing illustrated in Figure A is recommended for the supply voltages and the control signals at device power-up. If the timing in the figure is ignored, the device may not operate correctly.

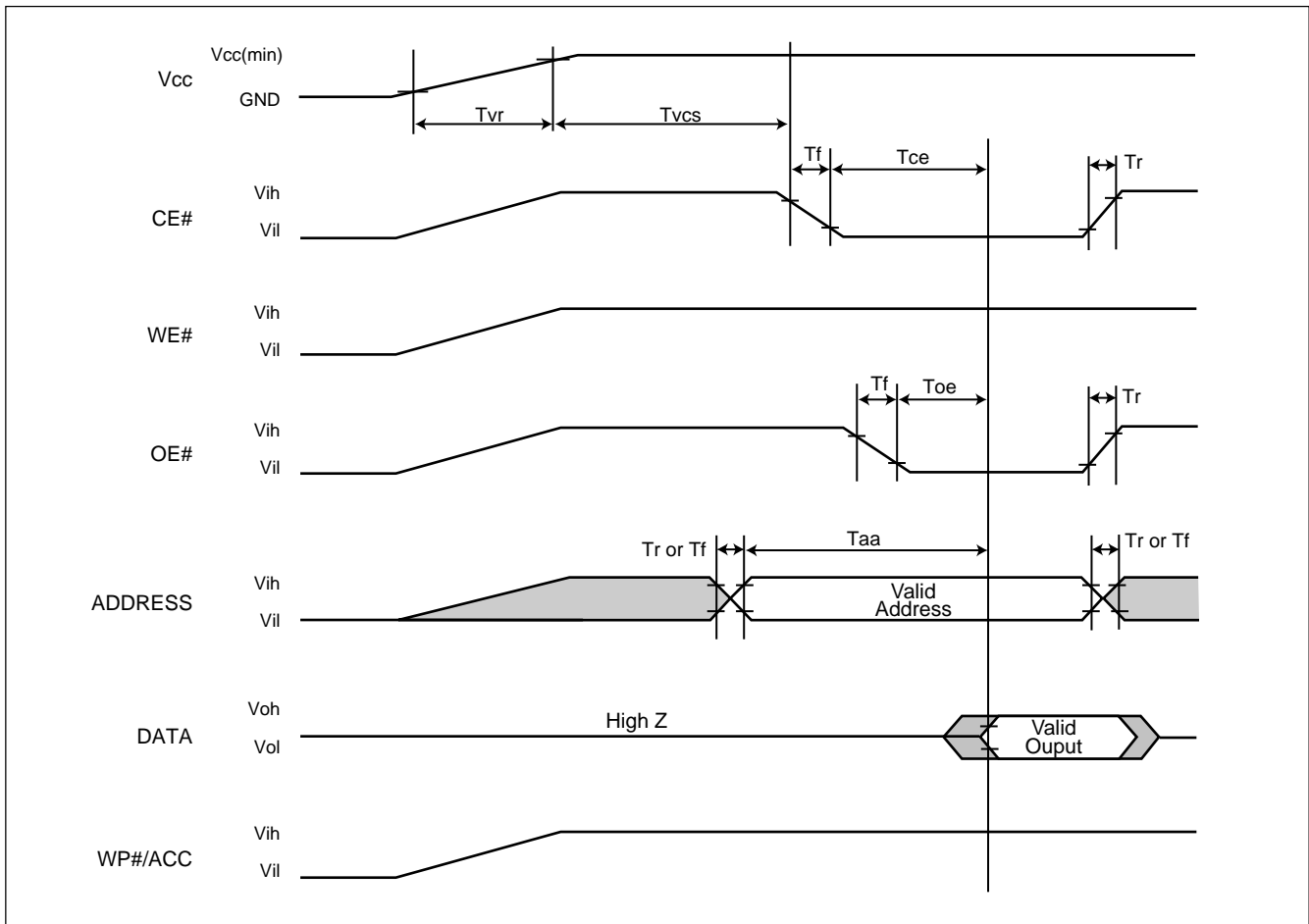


Figure A. AC Timing at Device Power-Up

Symbol	Parameter	Min.	Max.	Unit
Tvr	Vcc Rise Time	20	500000	us/V
Tr	Input Signal Rise Time		20	us/V
Tf	Input Signal Fall Time		20	us/V

ERASE AND PROGRAMMING PERFORMANCE

PARAMETER		LIMITS			UNITS
		MIN.	TYP.	MAX.	
Chip Erase Time	MX29LV002C		4	32	sec
	MX29LV004C		4	32	sec
	MX29LV008C		14		sec
Sector Erase Time			0.7	15	sec
Erase/Program Cycles		100,000			Cycles
Chip Programming Time	MX29LV002C		4.5	13.5	sec
	MX29LV004C		4.5	13.5	sec
	MX29LV008C		9	27	sec
Byte Programming Time			9	300	us

LATCH-UP CHARACTERISTICS

	MIN.	MAX.
Input Voltage voltage difference with GND on all pins except I/O pins	-1.0V	12.5V
Input Voltage voltage difference with GND on all I/O pins	-1.0V	V _{cc} + 1.0V
V _{cc} Current	-100mA	+100mA
All pins included except V _{cc} . Test conditions: V _{cc} = 3.0V, one pin per testing		

TSOP PIN CAPACITANCE

Parameter Symbol	Parameter Description	Test Set	TYP	MAX	UNIT
CIN2	Control Pin Capacitance	VIN=0		12	pF
COUT	Output Capacitance	VOUT=0		12	pF
CIN	Input Capacitance	VIN=0		8	pF

ORDERING INFORMATION

MX29LV002C

PART NO.	Access Time	Operating Current	Standby Current	PACKAGE	Remark
	(ns)	MAX. (mA)	MAX. (uA)		
MX29LV002CTTC-70	70	30	5	32 Pin TSOP	
MX29LV002CBTC-70	70	30	5	32 Pin TSOP	
MX29LV002CTTC-90	90	30	5	32 Pin TSOP	
MX29LV002CBTC-90	90	30	5	32 Pin TSOP	
MX29LV002CTTI-70	70	30	5	32 Pin TSOP	
MX29LV002CBTI-70	70	30	5	32 Pin TSOP	
MX29LV002CTTI-90	90	30	5	32 Pin TSOP	
MX29LV002CBTI-90	90	30	5	32 Pin TSOP	
MX29LV002CTQC-70	70	30	5	32 Pin PLCC	
MX29LV002CBQC-70	70	30	5	32 Pin PLCC	
MX29LV002CTQC-90	70	30	5	32 Pin PLCC	
MX29LV002CBQC-90	70	30	5	32 Pin PLCC	
MX29LV002CTQI-70	70	30	5	32 Pin PLCC	
MX29LV002CBQI-70	70	30	5	32 Pin PLCC	
MX29LV002CTQI-90	70	30	5	32 Pin PLCC	
MX29LV002CBQI-90	70	30	5	32 Pin PLCC	
MX29LV002CTTC-70G	70	30	5	32 Pin TSOP	PB free
MX29LV002CTTC-90G	90	30	5	32 Pin TSOP	PB free
MX29LV002CBTC-70G	70	30	5	32 Pin TSOP	PB free
MX29LV002CBTC-90G	90	30	5	32 Pin TSOP	PB free
MX29LV002CTTI-70G	70	30	5	32 Pin TSOP	PB free
MX29LV002CTTI-90G	90	30	5	32 Pin TSOP	PB free
MX29LV002CBTI-70G	70	30	5	32 Pin TSOP	PB free
MX29LV002CBTI-90G	90	30	5	32 Pin TSOP	PB free
MX29LV002CTQC-70G	70	30	5	32 Pin PLCC	PB free
MX29LV002CTQC-90G	90	30	5	32 Pin PLCC	PB free
MX29LV002CBQC-70G	70	30	5	32 Pin PLCC	PB free
MX29LV002CBQC-90G	90	30	5	32 Pin PLCC	PB free
MX29LV002CTQI-70G	70	30	5	32 Pin PLCC	PB free
MX29LV002CTQI-90G	90	30	5	32 Pin PLCC	PB free
MX29LV002CBQI-70G	70	30	5	32 Pin PLCC	PB free
MX29LV002CBQI-90G	90	30	5	32 Pin PLCC	PB free

PART NO.	Access Time	Operating Current	Standby Current	PACKAGE	Remark
	(ns)	MAX. (mA)	MAX. (uA)		
MX29LV002NCTTC-70	70	30	5	32 Pin TSOP	
MX29LV002NCBTC-70	70	30	5	32 Pin TSOP	
MX29LV002NCTTC-90	90	30	5	32 Pin TSOP	
MX29LV002NCBTC-90	90	30	5	32 Pin TSOP	
MX29LV002NCTTI-70	70	30	5	32 Pin TSOP	
MX29LV002NCBTI-70	70	30	5	32 Pin TSOP	
MX29LV002NCTTI-90	90	30	5	32 Pin TSOP	
MX29LV002NCBTI-90	90	30	5	32 Pin TSOP	
MX29LV002NCTQC-70	70	30	5	32 Pin PLCC	
MX29LV002NCBQC-70	70	30	5	32 Pin PLCC	
MX29LV002NCTQC-90	70	30	5	32 Pin PLCC	
MX29LV002NCBQC-90	70	30	5	32 Pin PLCC	
MX29LV002NCTQI-70	70	30	5	32 Pin PLCC	
MX29LV002NCBQI-70	70	30	5	32 Pin PLCC	
MX29LV002NCTQI-90	70	30	5	32 Pin PLCC	
MX29LV002NCBQI-90	70	30	5	32 Pin PLCC	
MX29LV002NCTTC-70G	70	30	5	32 Pin TSOP	PB free
MX29LV002NCTTC-90G	90	30	5	32 Pin TSOP	PB free
MX29LV002NCBTC-70G	70	30	5	32 Pin TSOP	PB free
MX29LV002NCBTC-90G	90	30	5	32 Pin TSOP	PB free
MX29LV002NCTTI-70G	70	30	5	32 Pin TSOP	PB free
MX29LV002NCTTI-90G	90	30	5	32 Pin TSOP	PB free
MX29LV002NCBTI-70G	70	30	5	32 Pin TSOP	PB free
MX29LV002NCBTI-90G	90	30	5	32 Pin TSOP	PB free
MX29LV002NCTQC-70G	70	30	5	32 Pin PLCC	PB free
MX29LV002NCTQC-90G	90	30	5	32 Pin PLCC	PB free
MX29LV002NCBQC-70G	70	30	5	32 Pin PLCC	PB free
MX29LV002NCBQC-90G	90	30	5	32 Pin PLCC	PB free
MX29LV002NCTQI-70G	70	30	5	32 Pin PLCC	PB free
MX29LV002NCTQI-90G	90	30	5	32 Pin PLCC	PB free
MX29LV002NCBQI-70G	70	30	5	32 Pin PLCC	PB free
MX29LV002NCBQI-90G	90	30	5	32 Pin PLCC	PB free

MX29LV004C

PART NO.	Access Time	Operating Current	Standby Current	PACKAGE	Remark
	(ns)	MAX. (mA)	MAX. (uA)		
MX29LV004CTTC-55R	55	30	5	40 Pin TSOP	
MX29LV004CBTC-55R	55	30	5	40 Pin TSOP	
MX29LV004CTTC-70	70	30	5	40 Pin TSOP	
MX29LV004CBTC-70	70	30	5	40 Pin TSOP	
MX29LV004CTTC-90	90	30	5	40 Pin TSOP	
MX29LV004CBTC-90	90	30	5	40 Pin TSOP	
MX29LV004CTTI-55R	55	30	5	40 Pin TSOP	
MX29LV004CBTI-55R	55	30	5	40 Pin TSOP	
MX29LV004CTTI-70	70	30	5	40 Pin TSOP	
MX29LV004CBTI-70	70	30	5	40 Pin TSOP	
MX29LV004CTTI-90	90	30	5	40 Pin TSOP	
MX29LV004CBTI-90	90	30	5	40 Pin TSOP	
MX29LV004CTQC-55R	55	30	5	32 Pin PLCC	
MX29LV004CBQC-55R	55	30	5	32 Pin PLCC	
MX29LV004CTQC-70	70	30	5	32 Pin PLCC	
MX29LV004CBQC-70	70	30	5	32 Pin PLCC	
MX29LV004CTQC-90	70	30	5	32 Pin PLCC	
MX29LV004CBQC-90	70	30	5	32 Pin PLCC	
MX29LV004CTQI-55R	55	30	5	32 Pin PLCC	
MX29LV004CBQI-55R	55	30	5	32 Pin PLCC	
MX29LV004CTQI-70	70	30	5	32 Pin PLCC	
MX29LV004CBQI-70	70	30	5	32 Pin PLCC	
MX29LV004CTQI-90	70	30	5	32 Pin PLCC	
MX29LV004CBQI-90	70	30	5	32 Pin PLCC	
MX29LV004CTTC-55Q	55	30	5	40 Pin TSOP	PB free
MX29LV004CBTC-55Q	55	30	5	40 Pin TSOP	PB free
MX29LV004CTTC-70G	70	30	5	40 Pin TSOP	PB free
MX29LV004CBTC-70G	70	30	5	40 Pin TSOP	PB free
MX29LV004CTTC-90G	90	30	5	40 Pin TSOP	PB free
MX29LV004CBTC-90G	90	30	5	40 Pin TSOP	PB free
MX29LV004CTTI-55Q	55	30	5	40 Pin TSOP	PB free
MX29LV004CBTI-55Q	55	30	5	40 Pin TSOP	PB free
MX29LV004CTTI-70G	70	30	5	40 Pin TSOP	PB free
MX29LV004CBTI-70G	70	30	5	40 Pin TSOP	PB free
MX29LV004CTTI-90G	90	30	5	40 Pin TSOP	PB free
MX29LV004CBTI-90G	90	30	5	40 Pin TSOP	PB free

PART NO.	Access Time	Operating Current	Standby Current	PACKAGE	Remark
	(ns)	MAX. (mA)	MAX. (uA)		
MX29LV004CTQC-55Q	55	30	5	32 Pin PLCC	PB free
MX29LV004CBQC-55Q	55	30	5	32 Pin PLCC	PB free
MX29LV004CTQC-70G	70	30	5	32 Pin PLCC	PB free
MX29LV004CBQC-70G	70	30	5	32 Pin PLCC	PB free
MX29LV004CTQC-90G	90	30	5	32 Pin PLCC	PB free
MX29LV004CBQC-90G	90	30	5	32 Pin PLCC	PB free
MX29LV004CTQI-55Q	55	30	5	32 Pin PLCC	PB free
MX29LV004CBQI-55Q	55	30	5	32 Pin PLCC	PB free
MX29LV004CTQI-70G	70	30	5	32 Pin PLCC	PB free
MX29LV004CBQI-70G	70	30	5	32 Pin PLCC	PB free
MX29LV004CTQI-90G	90	30	5	32 Pin PLCC	PB free
MX29LV004CBQI-90G	90	30	5	32 Pin PLCC	PB free
MX29LV004CTTI-45Q	45	30	5	40 Pin TSOP	PB free
MX29LV004CBTI-45Q	45	30	5	40 Pin TSOP	PB free

MX29LV008C

PART NO.	ACCESS	OPERATING	STANDBY	PACKAGE	Remark
	TIME (ns)	Current MAX. (mA)	Current MAX. (uA)		
MX29LV008CTTC-55R	55	30	5	40 Pin TSOP	
MX29LV008CTTC-70	70	30	5	40 Pin TSOP	
MX29LV008CTTC-90	90	30	5	40 Pin TSOP	
MX29LV008CBTC-55R	55	30	5	40 Pin TSOP	
MX29LV008CBTC-70	70	30	5	40 Pin TSOP	
MX29LV008CBTC-90	90	30	5	40 Pin TSOP	
MX29LV008CTTI-55R	55	30	5	40 Pin TSOP	
MX29LV008CTTI-70	70	30	5	40 Pin TSOP	
MX29LV008CTTI-90	90	30	5	40 Pin TSOP	
MX29LV008CBTI-55R	55	30	5	40 Pin TSOP	
MX29LV008CBTI-70	70	30	5	40 Pin TSOP	
MX29LV008CBTI-90	90	30	5	40 Pin TSOP	
MX29LV008CTTC-55Q	55	30	5	40 Pin TSOP	Pb-free
MX29LV008CTTC-70G	70	30	5	40 Pin TSOP	Pb-free
MX29LV008CTTC-90G	90	30	5	40 Pin TSOP	Pb-free
MX29LV008CBTC-55Q	55	30	5	40 Pin TSOP	Pb-free
MX29LV008CBTC-70G	70	30	5	40 Pin TSOP	Pb-free
MX29LV008CBTC-90G	90	30	5	40 Pin TSOP	Pb-free
MX29LV008CTTI-55Q	55	30	5	40 Pin TSOP	Pb-free
MX29LV008CTTI-70G	70	30	5	40 Pin TSOP	Pb-free
MX29LV008CTTI-90G	90	30	5	40 Pin TSOP	Pb-free
MX29LV008CBTI-55Q	55	30	5	40 Pin TSOP	Pb-free
MX29LV008CBTI-70G	70	30	5	40 Pin TSOP	Pb-free
MX29LV008CBTI-90G	90	30	5	40 Pin TSOP	Pb-free

PART NAME DESCRIPTION

MX 29 LV 002 C T T C - 70 G

OPTION:

G: Lead-free package

R: Restricted Vcc (3.0V~3.6V)

Q: Restricted Vcc (3.0V~3.6V) with Lead-free package

blank: normal

SPEED:

45: 45ns

55: 55ns

70: 70ns

90: 90ns

TEMPERATURE RANGE:

C: Commercial (0° C to 70° C)

I: Industrial (-40° C to 85° C)

PACKAGE:

Q: PLCC

T: TSOP

BOOT BLOCK TYPE:

T: Top Boot

B: Bottom Boot

REVISION:

C

DENSITY & MODE:

002/002N: 2Mb, x8 Boot Block

004: 4Mb, x8 Boot Block

008: 8Mb, x8 Boot Block

TYPE:

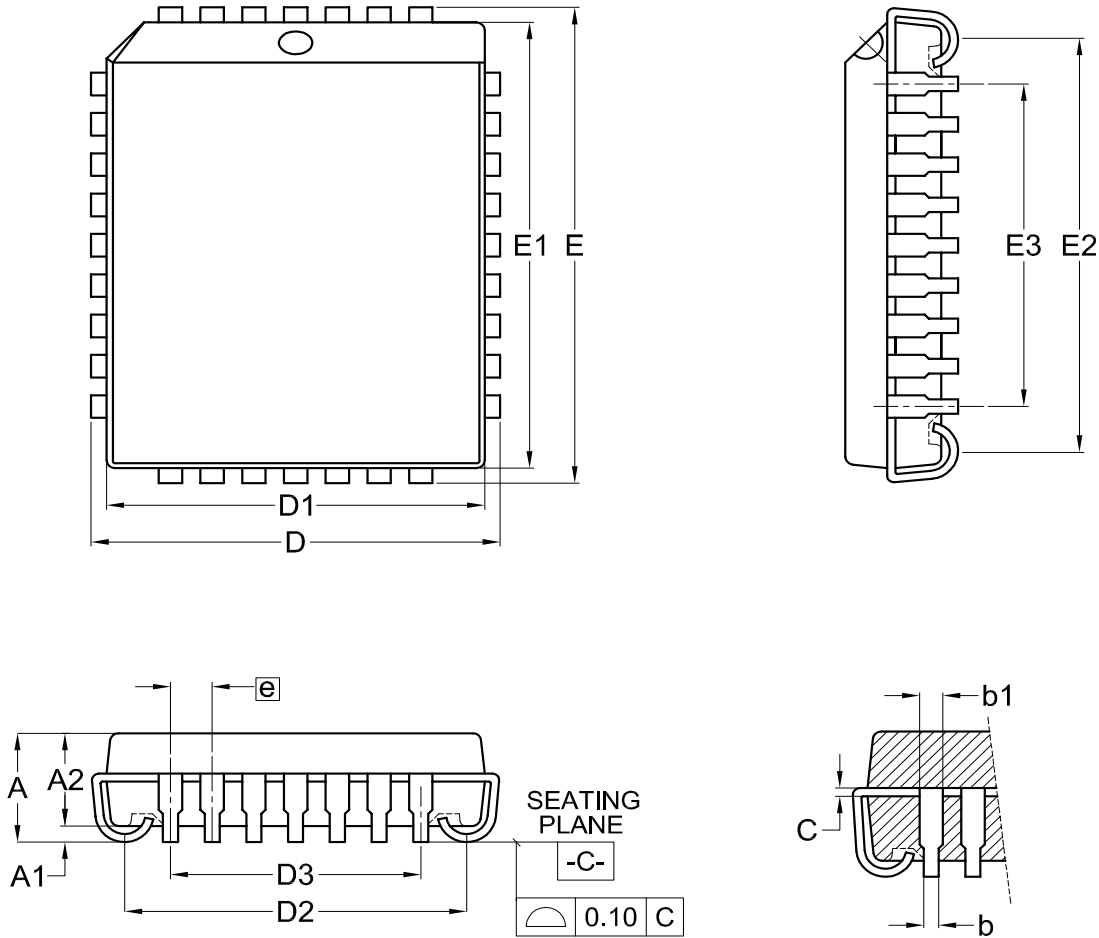
LV: 3V

DEVICE:

29:Flash

PACKAGE INFORMATION

Title: Package Outline for 32L PLCC

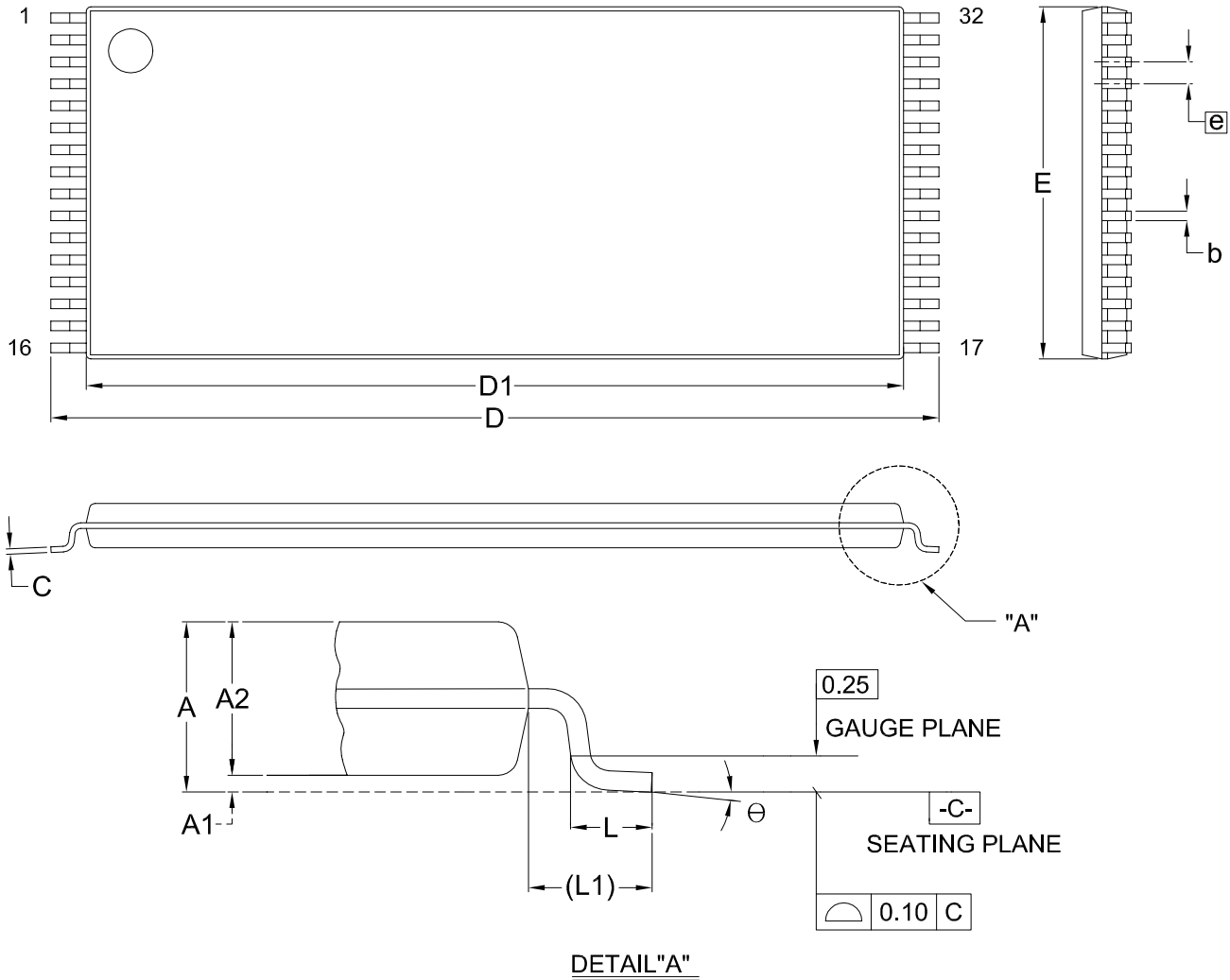


Dimensions (inch dimensions are derived from the original mm dimensions)

SYMBOL		A	A1	A2	b	b1	C	D	D1	D2	D3	E	E1	E2	E3	e
mm	Min.	—	0.38	2.69	0.38	0.61	0.20	12.32	11.36	10.11		14.86	13.98	12.65		
	Nom.	—	0.58	2.79	0.46	0.71	0.25	12.45	11.43	10.41	7.62	14.99	14.05	12.95	10.16	1.27
	Max.	3.55	0.81	2.89	0.54	0.81	0.30	12.58	11.50	10.71		15.12	14.12	13.25		
Inch	Min.	---	0.015	0.106	0.015	0.024	0.008	0.485	0.447	0.398		0.585	0.550	0.498		
	Nom.	---	0.023	0.110	0.018	0.028	0.010	0.490	0.450	0.410	0.300	0.590	0.553	0.510	0.400	0.050
	Max.	0.140	0.032	0.114	0.021	0.032	0.012	0.495	0.453	0.422		0.595	0.556	0.522		

DWG.NO.	REVISION	REFERENCE			ISSUE DATE
		JEDEC	EIAJ		
6110-2002	7	MS-016			12-10-'03

Title: Package Outline for TSOP(I) 32L (8X20mm)

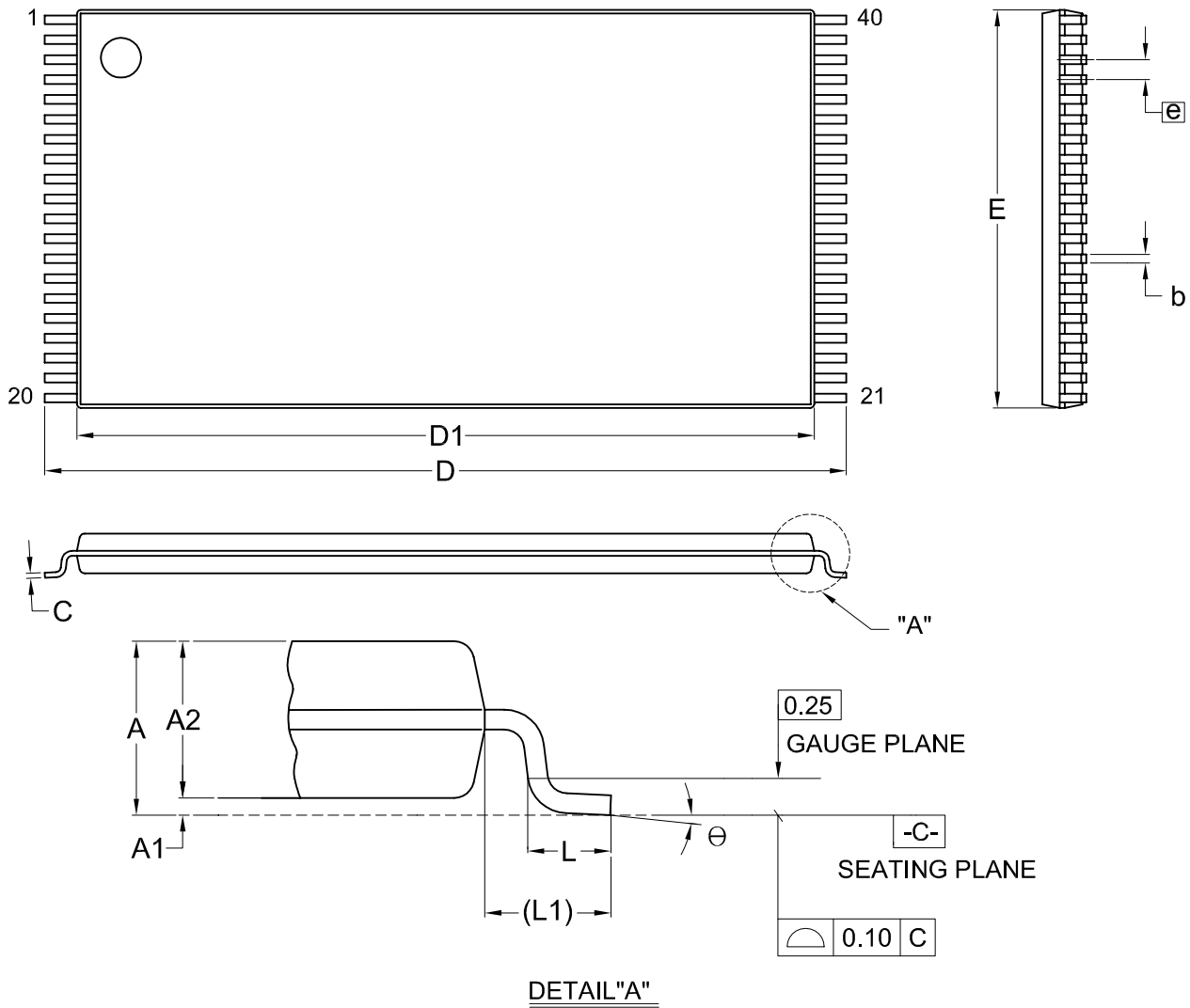


Dimensions (inch dimensions are derived from the original mm dimensions)

SYMBOL		A	A1	A2	b	C	D	D1	E	e	L	L1	θ
UNIT													
mm	Min.	---	0.05	0.95	0.17	0.10	19.80	18.30	7.90		0.50	0.70	0
	Nom.	---	0.10	1.00	0.20	0.15	20.00	18.40	8.00	0.50	0.60	0.80	5
	Max.	1.20	0.15	1.05	0.27	0.21	20.20	18.50	8.10		0.70	0.90	8
Inch	Min.	---	0.002	0.037	0.007	0.004	0.780	0.720	0.311		0.020	0.028	0
	Nom.	---	0.004	0.039	0.008	0.006	0.787	0.724	0.315	0.020	0.024	0.031	5
	Max.	0.047	0.006	0.041	0.011	0.008	0.795	0.728	0.319		0.028	0.035	8

DWG.NO.	REVISION	REFERENCE			ISSUE DATE
		JEDEC	EIAJ		
6110-1604	9	MO-142			11-26-'03

Title: Package Outline for TSOP(I) 40L (10X20mm)



DETAIL "A"

Dimensions (inch dimensions are derived from the original mm dimensions)

SYMBOL		A	A1	A2	b	C	D	D1	E	e	L	L1	θ
mm	Min.	---	0.05	0.95	0.17	0.10	19.80	18.30	9.90		0.50	0.70	0
	Nom.	---	0.10	1.00	0.20	0.13	20.00	18.40	10.00	0.50	0.60	0.80	5
	Max.	1.20	0.15	1.05	0.27	0.21	20.20	18.50	10.10		0.70	0.90	8
Inch	Min.	---	0.002	0.037	0.007	0.004	0.780	0.720	0.390		0.020	0.028	0
	Nom.	---	0.004	0.039	0.008	0.005	0.787	0.724	0.394	0.020	0.024	0.031	5
	Max.	0.047	0.006	0.041	0.011	0.008	0.795	0.728	0.398		0.028	0.035	8

DWG.NO.	REVISION	REFERENCE			ISSUE DATE
		JEDEC	EIAJ		
6110-1606	6	MO-142			12-01-'03



MACRONIX
INTERNATIONAL Co., LTD.

MX29LV002C/002NC T/B
MX29LV004C T/B
MX29LV008C T/B

REVISION HISTORY

Revision No.	Description	Page	Date
1.1	1. Corrected wrong CFI address data	P21~23	AUG/25/2006
1.2	1. Added statement	P67	NOV/06/2006
1.3	1. Correct typo	P16,18,19, P42,52	DEC/12/2007
1.4	1. Revised statement	P21	DEC/28/2007
1.5	1. Added note 5 into table 3. Command Definitions	P16	JAN/17/2008
1.6	1. Modified Figure 10. CE# Controlled Write Timing Waveform	P39	FEB/21/2008



MACRONIX
INTERNATIONAL Co., LTD.

MX29LV002C/002NC T/B
MX29LV004C T/B
MX29LV008C T/B

Macronix's products are not designed, manufactured, or intended for use for any high risk applications in which the failure of a single component could cause death, personal injury, severe physical damage, or other substantial harm to persons or property, such as life-support systems, high temperature automotive, medical, aircraft and military application. Macronix and its suppliers will not be liable to you and/or any third party for any claims, injuries or damages that may be incurred due to use of Macronix's products in the prohibited applications.

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