



RF Power Field Effect Transistors

N-Channel Enhancement-Mode Lateral MOSFETs

Designed for broadband commercial and industrial applications with frequencies up to 1000 MHz. The high gain and broadband performance of these devices make them ideal for large-signal, common-source amplifier applications in 28 volt base station equipment.

- Typical Two-Tone Performance at 945 MHz, 28 Volts
 Output Power — 45 Watts PEP
 Power Gain — 18.8 dB
 Efficiency — 42%
 IMD — -32 dBc
- Capable of Handling 10:1 VSWR, @ 28 Vdc, 945 MHz, 45 Watts CW Output Power

Features

- Integrated ESD Protection
- Designed for Maximum Gain and Insertion Phase Flatness
- Excellent Thermal Stability
- Characterized with Series Equivalent Large-Signal Impedance Parameters
- Low Gold Plating Thickness on Leads. L Suffix Indicates 40μ" Nominal.
- RoHS Compliant
- In Tape and Reel. R1 Suffix = 500 Units per 32 mm, 13 inch Reel.

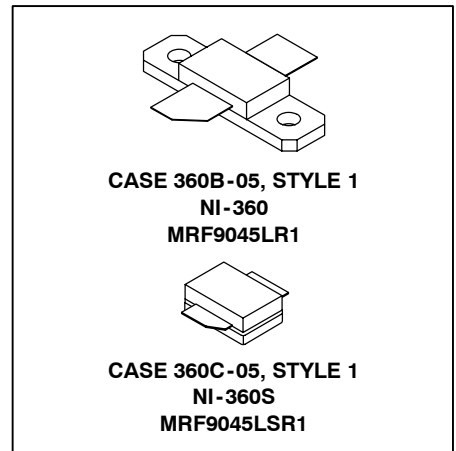
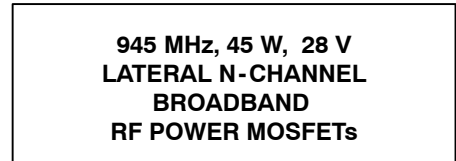
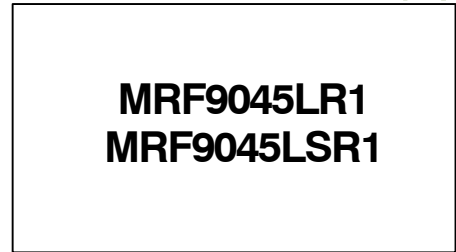


Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain-Source Voltage	V _{DSS}	- 0.5, +65	Vdc
Gate-Source Voltage	V _{GS}	- 0.5, +15	Vdc
Total Device Dissipation @ T _C = 25°C Derate above 25°C	P _D	125 0.71 175 1	W W/°C
Storage Temperature Range	T _{stg}	- 65 to +150	°C
Case Operating Temperature	T _C	150	°C
Operating Junction Temperature	T _J	200	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case	R _{θJC}	1.4 1.0	°C/W

Table 3. ESD Protection Characteristics

Test Conditions	Class
Human Body Model	1 (Minimum)
Machine Model	M1 (Minimum)

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Table 4. Electrical Characteristics ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Off Characteristics					
Zero Gate Voltage Drain Leakage Current ($V_{DS} = 65\text{ Vdc}$, $V_{GS} = 0\text{ Vdc}$)	I_{DSS}	—	—	10	μA
Zero Gate Voltage Drain Leakage Current ($V_{DS} = 28\text{ Vdc}$, $V_{GS} = 0\text{ Vdc}$)	I_{DSS}	—	—	1	μA
Gate-Source Leakage Current ($V_{GS} = 5\text{ Vdc}$, $V_{DS} = 0\text{ Vdc}$)	I_{GSS}	—	—	1	μA
On Characteristics					
Gate Threshold Voltage ($V_{DS} = 10\text{ Vdc}$, $I_D = 150\ \mu\text{A}$)	$V_{GS(th)}$	2	3	4	Vdc
Gate Quiescent Voltage ($V_{DS} = 28\text{ Vdc}$, $I_D = 350\ \text{mA}$)	$V_{GS(Q)}$	—	3.7	—	Vdc
Drain-Source On-Voltage ($V_{GS} = 10\text{ Vdc}$, $I_D = 1\ \text{A}$)	$V_{DS(on)}$	—	0.19	0.4	Vdc
Forward Transconductance ($V_{DS} = 10\text{ Vdc}$, $I_D = 3\ \text{A}$)	g_{fs}	—	4	—	S
Dynamic Characteristics					
Input Capacitance ($V_{DS} = 28\text{ Vdc} \pm 30\ \text{mV(rms)ac}$ @ 1 MHz, $V_{GS} = 0\text{ Vdc}$)	C_{iss}	—	69	—	pF
Output Capacitance ($V_{DS} = 28\text{ Vdc} \pm 30\ \text{mV(rms)ac}$ @ 1 MHz, $V_{GS} = 0\text{ Vdc}$)	C_{oss}	—	37	—	pF
Reverse Transfer Capacitance ($V_{DS} = 28\text{ Vdc} \pm 30\ \text{mV(rms)ac}$ @ 1 MHz, $V_{GS} = 0\text{ Vdc}$)	C_{rss}	—	1.5	—	pF

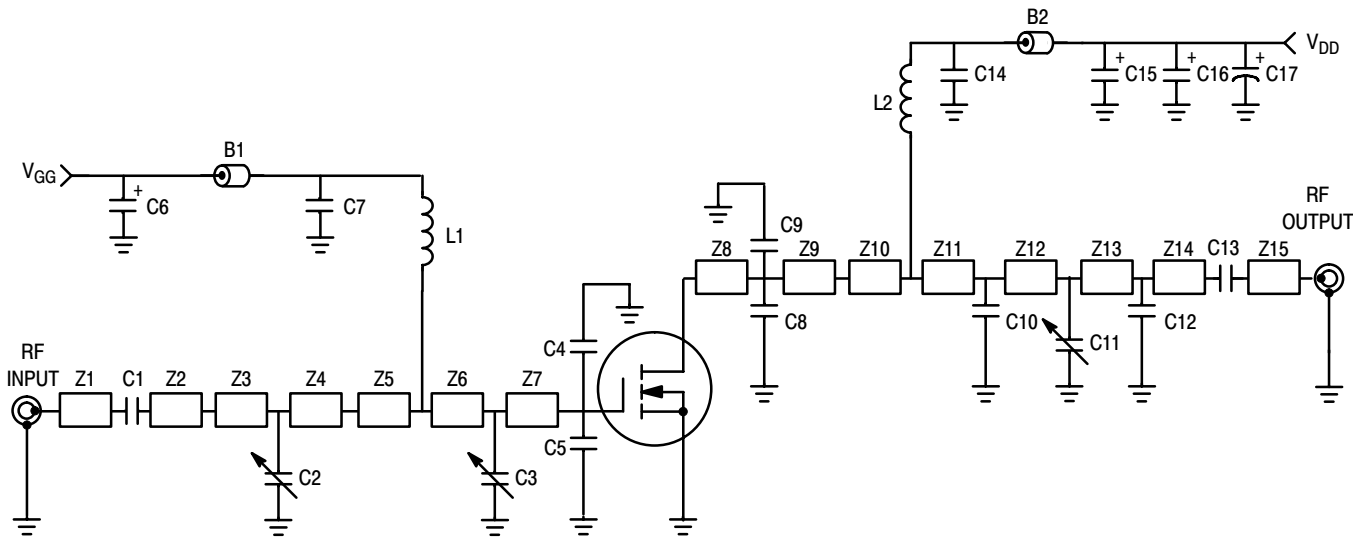
(continued)

Table 4. Electrical Characteristics ($T_C = 25^\circ\text{C}$ unless otherwise noted) (continued)

Characteristic	Symbol	Min	Typ	Max	Unit
Functional Tests (In Freescale Test Fixture, 50 ohm system)					
Two-Tone Common-Source Amplifier Power Gain ($V_{DD} = 28\text{ Vdc}$, $P_{out} = 45\text{ W PEP}$, $I_{DQ} = 350\text{ mA}$, $f_1 = 945.0\text{ MHz}$, $f_2 = 945.1\text{ MHz}$)	G_{ps}	17	18.8	—	dB
Two-Tone Drain Efficiency ($V_{DD} = 28\text{ Vdc}$, $P_{out} = 45\text{ W PEP}$, $I_{DQ} = 350\text{ mA}$, $f_1 = 945.0\text{ MHz}$, $f_2 = 945.1\text{ MHz}$)	η	38	42	—	%
3rd Order Intermodulation Distortion ($V_{DD} = 28\text{ Vdc}$, $P_{out} = 45\text{ W PEP}$, $I_{DQ} = 350\text{ mA}$, $f_1 = 945.0\text{ MHz}$, $f_2 = 945.1\text{ MHz}$)	IMD	—	-32	-28	dBc
Input Return Loss ($V_{DD} = 28\text{ Vdc}$, $P_{out} = 45\text{ W PEP}$, $I_{DQ} = 350\text{ mA}$, $f_1 = 945.0\text{ MHz}$, $f_2 = 945.1\text{ MHz}$)	IRL	—	-14	-9	dB
Two-Tone Common-Source Amplifier Power Gain ($V_{DD} = 28\text{ Vdc}$, $P_{out} = 45\text{ W PEP}$, $I_{DQ} = 350\text{ mA}$, $f_1 = 930.0\text{ MHz}$, $f_2 = 930.1\text{ MHz}$ and $f_1 = 960.0\text{ MHz}$, $f_2 = 960.1\text{ MHz}$)	G_{ps}	—	18.5	—	dB
Two-Tone Drain Efficiency ($V_{DD} = 28\text{ Vdc}$, $P_{out} = 45\text{ W PEP}$, $I_{DQ} = 350\text{ mA}$, $f_1 = 930.0\text{ MHz}$, $f_2 = 930.1\text{ MHz}$ and $f_1 = 960.0\text{ MHz}$, $f_2 = 960.1\text{ MHz}$)	η	—	41	—	%
3rd Order Intermodulation Distortion ($V_{DD} = 28\text{ Vdc}$, $P_{out} = 45\text{ W PEP}$, $I_{DQ} = 350\text{ mA}$, $f_1 = 930.0\text{ MHz}$, $f_2 = 930.1\text{ MHz}$ and $f_1 = 960.0\text{ MHz}$, $f_2 = 960.1\text{ MHz}$)	IMD	—	-33	—	dBc
Input Return Loss ($V_{DD} = 28\text{ Vdc}$, $P_{out} = 45\text{ W PEP}$, $I_{DQ} = 350\text{ mA}$, $f_1 = 930.0\text{ MHz}$, $f_2 = 930.1\text{ MHz}$ and $f_1 = 960.0\text{ MHz}$, $f_2 = 960.1\text{ MHz}$)	IRL	—	13	—	dB
Power Output, 1 dB Compression Point ($V_{DD} = 28\text{ Vdc}$, $P_{out} = 45\text{ W CW}$, $I_{DQ} = 350\text{ mA}$, $f_1 = 945.0\text{ MHz}$)	P_{1dB}	—	55	—	W
Common-Source Amplifier Power Gain ($V_{DD} = 28\text{ Vdc}$, $P_{out} = 45\text{ W CW}$, $I_{DQ} = 350\text{ mA}$, $f_1 = 945.0\text{ MHz}$)	G_{ps}	—	18	—	dB
Drain Efficiency ($V_{DD} = 28\text{ Vdc}$, $P_{out} = 45\text{ W CW}$, $I_{DQ} = 350\text{ mA}$, $f_1 = 945.0\text{ MHz}$)	η	—	60	—	%

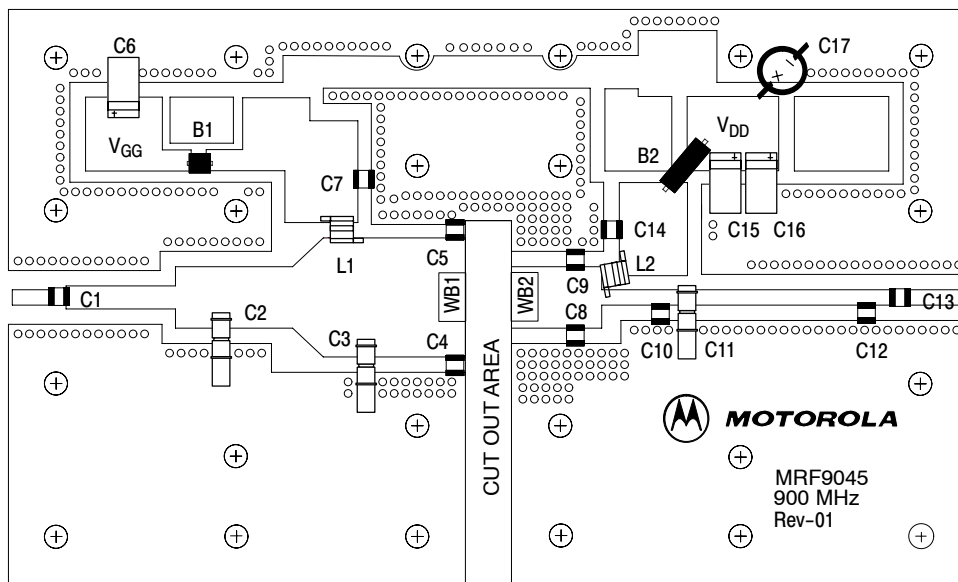
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B1	Short Ferrite Bead Surface Mount	Z4	0.360" x 0.320" Microstrip
B2	Long Ferrite Bead Surface Mount	Z5	0.240" x 0.320" x 0.620", Taper
C1, C7, C13, C14	47 pF Chip Capacitors	Z6	0.140" x 0.620" Microstrip
C2, C3, C11	0.8 - 8.0 pF Gigatrim Variable Trim Capacitors	Z7	0.510" x 0.620" Microstrip
C4, C5, C8, C9	10 pF Chip Capacitors	Z8	0.330" x 0.320" Microstrip
C6, C15, C16	10 μF, 35 V Tantalum Surface Mount Chip Capacitors	Z9	0.140" x 0.320" Microstrip
C10	2.2 pF Chip Capacitor	Z10	0.070" x 0.080" Microstrip
C12	0.7 pF Chip Capacitor - MRF9045LS	Z11	0.240" x 0.080" Microstrip
C17	220 μF, 50 V Electrolytic Capacitor	Z12	0.140" x 0.080" Microstrip
L1, L2	12.5 nH Surface Mount Inductors, Coilcraft	Z13	0.930" x 0.080" Microstrip
Z1	0.260" x 0.080" Microstrip	Z14	0.180" x 0.080" Microstrip
Z2	0.610" x 0.120" Microstrip	Z15	0.350" x 0.080" Microstrip
Z3	0.260" x 0.320" Microstrip	PCB	Arlon GX-0300-55-22, 0.03", ε _r = 2.55

Figure 1. 930 - 960 MHz Broadband Test Circuit Schematic



Freescle has begun the transition of marking Printed Circuit Boards (PCBs) with the Freescle Semiconductor signature/logo. PCBs may have either Motorola or Freescle markings during the transition period. These changes will have no impact on form, fit or function of the current product.

Figure 2. 930 - 960 MHz Broadband Test Circuit Component Layout

TYPICAL CHARACTERISTICS

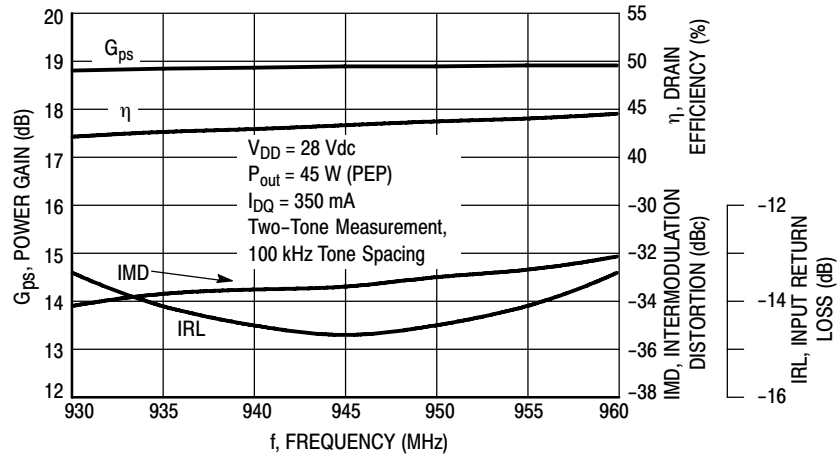


Figure 3. Class AB Broadband Circuit Performance

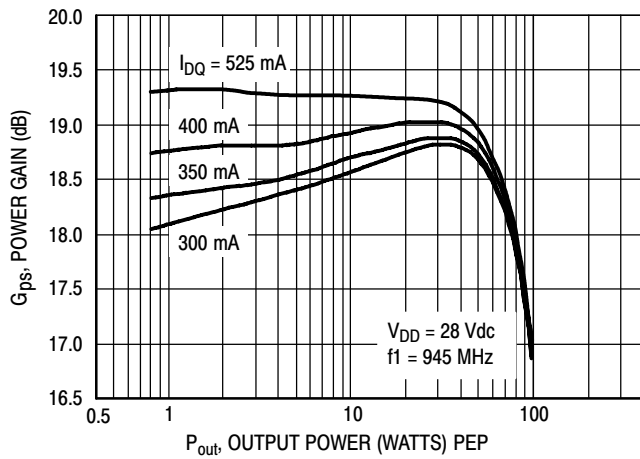


Figure 4. Power Gain versus Output Power

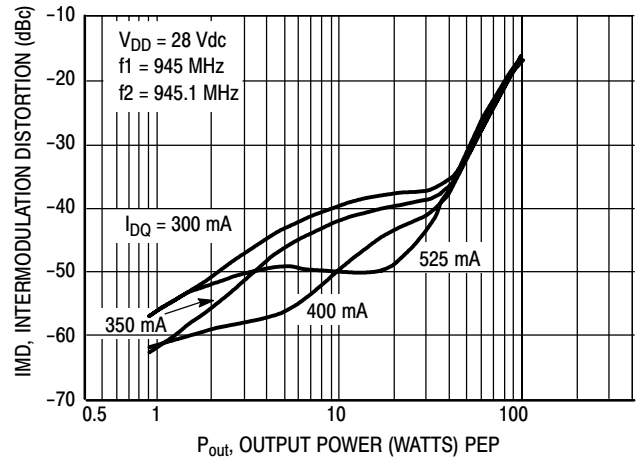


Figure 5. Intermodulation Distortion versus Output Power

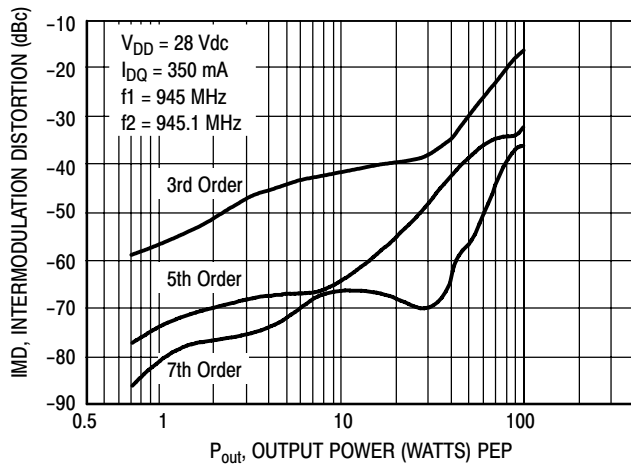


Figure 6. Intermodulation Distortion Products versus Output Power

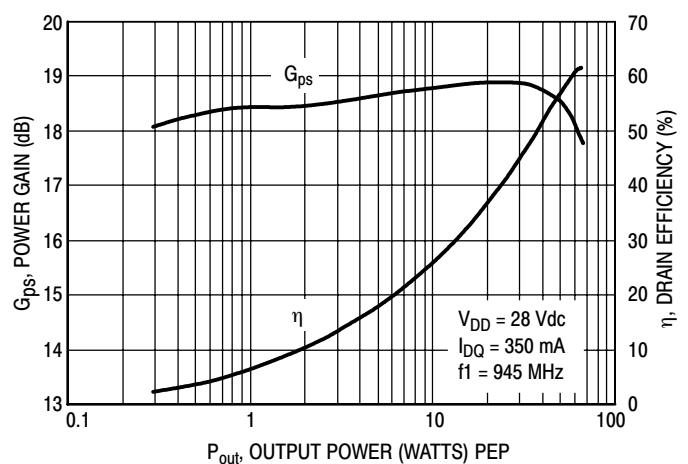
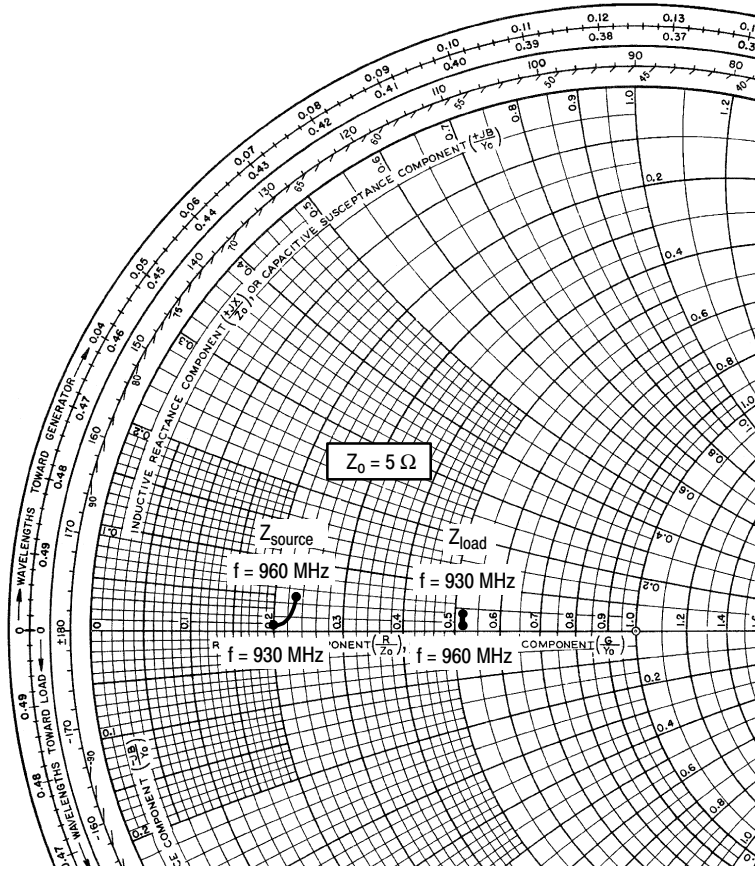


Figure 7. Power Gain, Efficiency versus Output Power



$V_{DD} = 28\text{ V}$, $I_{DQ} = 350\text{ mA}$, $P_{out} = 45\text{ W PEP}$

f MHz	Z_{source} Ω	Z_{load} Ω
930	$1.02 + j0.06$	$2.6 + j0.20$
945	$1.10 + j0.11$	$2.6 + j0.16$
960	$1.15 + j0.25$	$2.6 + j0.10$

Z_{source} = Test circuit impedance as measured from gate to ground.

Z_{load} = Test circuit impedance as measured from drain to ground.

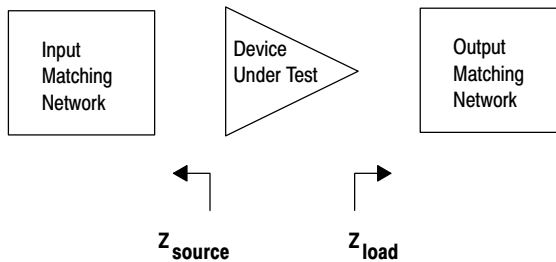
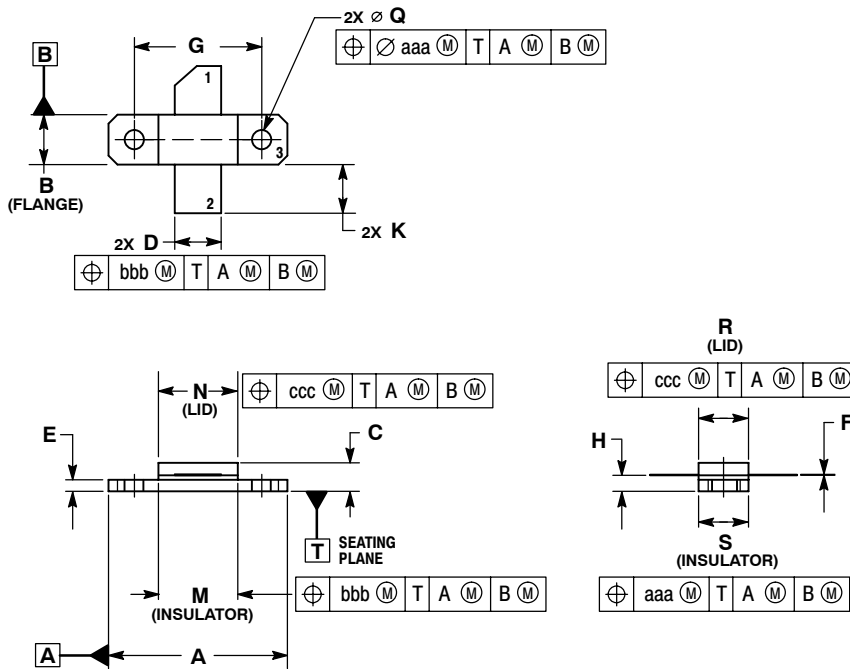


Figure 8. Series Equivalent Source and Load Impedance

PACKAGE DIMENSIONS



NOTES:

1. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M-1994.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION H IS MEASURED 0.030 (0.762) AWAY FROM PACKAGE BODY.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.795	0.805	20.19	20.45
B	0.225	0.235	5.72	5.97
C	0.125	0.175	3.18	4.45
D	0.210	0.220	5.33	5.59
E	0.055	0.065	1.40	1.65
F	0.004	0.006	0.10	0.15
G	0.562 BSC		14.28 BSC	
H	0.077	0.087	1.96	2.21
K	0.220	0.250	5.59	6.35
M	0.355	0.365	9.02	9.27
N	0.357	0.363	9.07	9.22
Q	0.125	0.135	3.18	3.43
R	0.227	0.233	5.77	5.92
S	0.225	0.235	5.72	5.97
aaa	0.005 REF		0.13 REF	
bbb	0.010 REF		0.25 REF	
ccc	0.015 REF		0.38 REF	

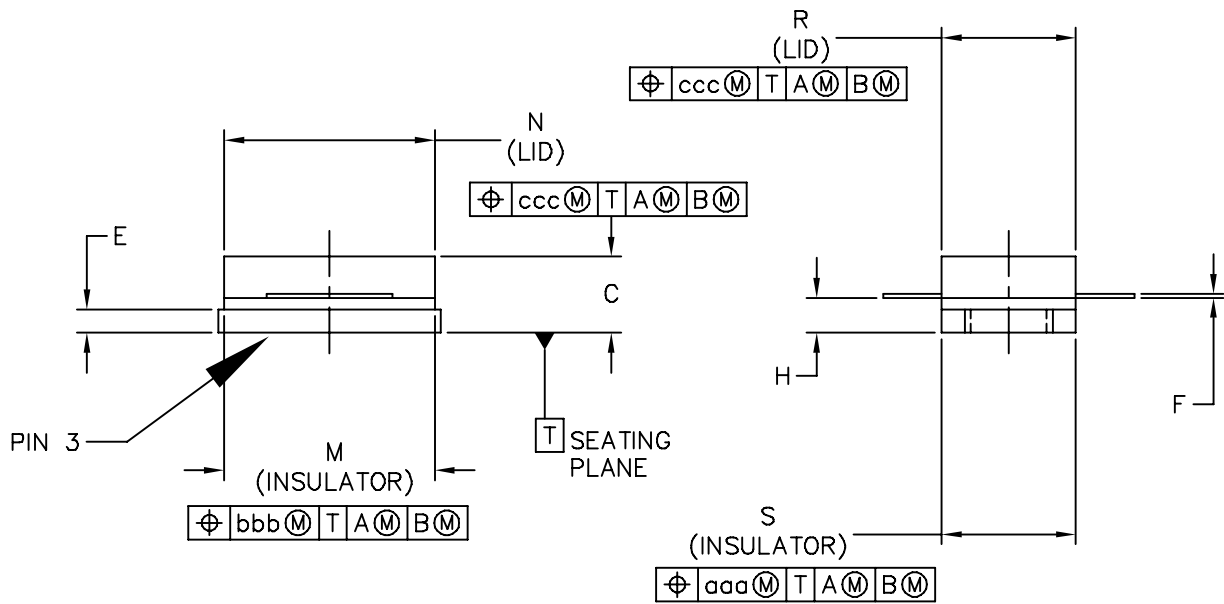
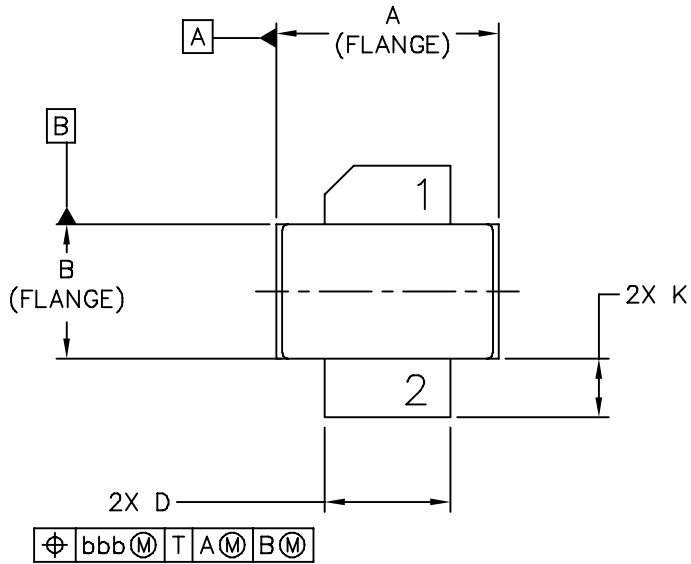
STYLE 1:

- PIN 1. DRAIN
2. GATE
3. SOURCE

**CASE 360B-05
ISSUE G
NI-360
MRF9045LR1**

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	CASE NUMBER: 360C-05	10 MAR 2006
	STANDARD: NON-JEDEC	

NOTES:

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STYLE 1:
 PIN 1 - DRAIN
 2 - GATE
 3 - SOURCE

DIM	INCH		MILLIMETER		DIM	INCH		MILLIMETER	
	MIN	MAX	MIN	MAX		MIN	MAX	MIN	MAX
A	.375	.385	9.53	9.78	N	.357	.363	9.07	9.22
B	.225	.235	5.72	5.97	R	.227	.233	5.77	5.92
C	.105	.155	2.67	3.94	S	.225	.235	5.72	5.97
D	.210	.220	5.33	5.59					
E	.035	.045	0.89	1.14	aaa	.005		0.13	
F	.004	.006	0.1	0.15	bbb	.010		0.25	
H	.057	.067	1.45	1.7	ccc	.015		0.38	
K	.085	.115	2.16	2.92					
M	.355	.365	9.02	9.27					

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PRODUCT DOCUMENTATION

Refer to the following documents to aid your design process.

Engineering Bulletins

- EB212: Using Data Sheet Impedances for RF LDMOS Devices

REVISION HISTORY

The following table summarizes revisions to this document.

Revision	Date	Description
11	Sept. 2008	<ul style="list-style-type: none">• Replaced Case Outline 360C-05, Issue E with Issue F, p. 8-9.• Added Product Documentation and Revision History, p. 10

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