

RF Power Field Effect Transistor

N-Channel Enhancement-Mode Lateral MOSFET

Designed for broadband commercial and industrial applications with frequencies up to 1000 MHz. The high gain and broadband performance of this device make it ideal for large-signal, common-source amplifier applications in 26 volt base station equipment.

- Typical Two-Tone Performance at 945 MHz, 26 Volts
 - Output Power — 30 Watts PEP
 - Power Gain — 19 dB
 - Efficiency — 41.5%
 - IMD — -32.5 dBc
- Capable of Handling 10:1 VSWR, @ 26 Vdc, 945 MHz, 30 Watts CW Output Power

Features

- Integrated ESD Protection
- Designed for Maximum Gain and Insertion Phase Flatness
- Excellent Thermal Stability
- Characterized with Series Equivalent Large-Signal Impedance Parameters
- Low Gold Plating Thickness on Leads. L Suffix Indicates 40μ" Nominal.
- RoHS Compliant
- In Tape and Reel. R1 Suffix = 500 Units per 32 mm, 13 inch Reel.

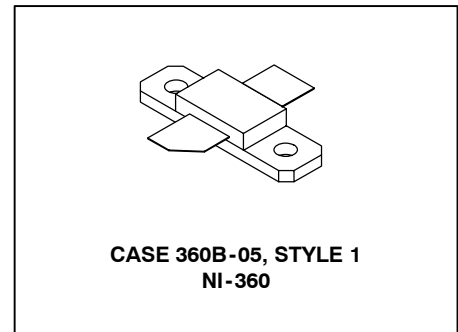
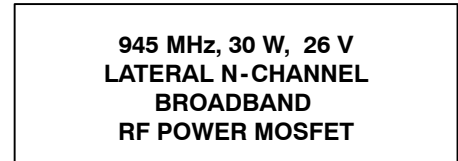


Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	- 0.5, +68	Vdc
Gate-Source Voltage	V_{GS}	- 0.5, +15	Vdc
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	92 0.53	W W/°C
Storage Temperature Range	T_{stg}	- 65 to +150	°C
Case Operating Temperature	T_C	150	°C
Operating Junction Temperature	T_J	200	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.9	°C/W

Table 3. ESD Protection Characteristics

Test Conditions	Class
Human Body Model	1 (Minimum)
Machine Model	M1 (Minimum)

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Table 4. Electrical Characteristics ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Off Characteristics					
Zero Gate Voltage Drain Leakage Current ($V_{DS} = 68\text{ Vdc}$, $V_{GS} = 0\text{ Vdc}$)	I_{DSS}	—	—	10	μAdc
Zero Gate Voltage Drain Leakage Current ($V_{DS} = 26\text{ Vdc}$, $V_{GS} = 0\text{ Vdc}$)	I_{DSS}	—	—	1	μAdc
Gate-Source Leakage Current ($V_{GS} = 5\text{ Vdc}$, $V_{DS} = 0\text{ Vdc}$)	I_{GSS}	—	—	1	μAdc
On Characteristics					
Gate Threshold Voltage ($V_{DS} = 10\text{ Vdc}$, $I_D = 100\ \mu\text{Adc}$)	$V_{GS(th)}$	2	2.9	4	Vdc
Gate Quiescent Voltage ($V_{DS} = 26\text{ Vdc}$, $I_D = 250\text{ mAdc}$)	$V_{GS(Q)}$	—	3.8	—	Vdc
Drain-Source On-Voltage ($V_{GS} = 10\text{ Vdc}$, $I_D = 0.7\text{ Adc}$)	$V_{DS(on)}$	—	0.19	0.4	Vdc
Forward Transconductance ($V_{DS} = 10\text{ Vdc}$, $I_D = 2\text{ Adc}$)	g_{fs}	—	3	—	S
Dynamic Characteristics					
Input Capacitance ($V_{DS} = 26\text{ Vdc} \pm 30\text{ mV(rms)ac}$ @ 1 MHz, $V_{GS} = 0\text{ Vdc}$)	C_{iss}	—	49.5	—	pF
Output Capacitance ($V_{DS} = 26\text{ Vdc} \pm 30\text{ mV(rms)ac}$ @ 1 MHz, $V_{GS} = 0\text{ Vdc}$)	C_{oss}	—	26.5	—	pF
Reverse Transfer Capacitance ($V_{DS} = 26\text{ Vdc} \pm 30\text{ mV(rms)ac}$ @ 1 MHz, $V_{GS} = 0\text{ Vdc}$)	C_{rss}	—	1	—	pF

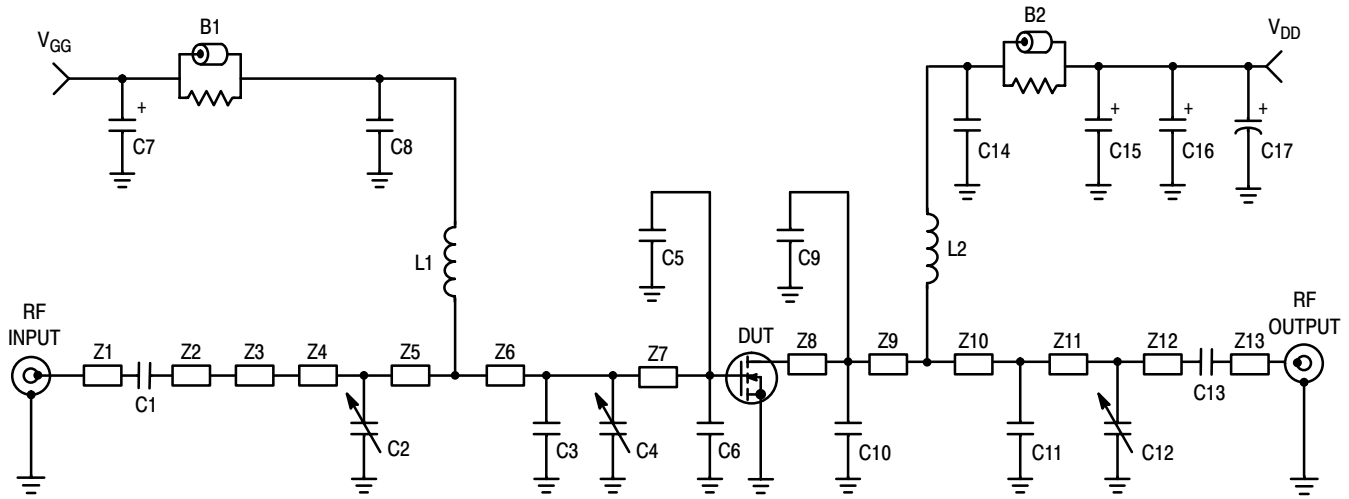
(continued)

Table 4. Electrical Characteristics ($T_C = 25^\circ\text{C}$ unless otherwise noted) (continued)

Characteristic	Symbol	Min	Typ	Max	Unit
Functional Tests (In Freescale Test Fixture, 50 ohm system)					
Two-Tone Common-Source Amplifier Power Gain ($V_{DD} = 26\text{ Vdc}$, $P_{out} = 30\text{ W PEP}$, $I_{DQ} = 250\text{ mA}$, $f_1 = 945.0\text{ MHz}$, $f_2 = 945.1\text{ MHz}$)	G_{ps}	18	19	—	dB
Two-Tone Drain Efficiency ($V_{DD} = 26\text{ Vdc}$, $P_{out} = 30\text{ W PEP}$, $I_{DQ} = 250\text{ mA}$, $f_1 = 945.0\text{ MHz}$, $f_2 = 945.1\text{ MHz}$)	η	37	41.5	—	%
3rd Order Intermodulation Distortion ($V_{DD} = 26\text{ Vdc}$, $P_{out} = 30\text{ W PEP}$, $I_{DQ} = 250\text{ mA}$, $f_1 = 945.0\text{ MHz}$, $f_2 = 945.1\text{ MHz}$)	IMD	—	-32.5	-28	dBc
Input Return Loss ($V_{DD} = 26\text{ Vdc}$, $P_{out} = 30\text{ W PEP}$, $I_{DQ} = 250\text{ mA}$, $f_1 = 945.0\text{ MHz}$, $f_2 = 945.1\text{ MHz}$)	IRL	—	-15.5	-9	dB
Two-Tone Common-Source Amplifier Power Gain ($V_{DD} = 26\text{ Vdc}$, $P_{out} = 30\text{ W PEP}$, $I_{DQ} = 250\text{ mA}$, $f_1 = 930.0\text{ MHz}$, $f_2 = 930.1\text{ MHz}$ and $f_1 = 960.0\text{ MHz}$, $f_2 = 960.1\text{ MHz}$)	G_{ps}	—	19	—	dB
Two-Tone Drain Efficiency ($V_{DD} = 26\text{ Vdc}$, $P_{out} = 30\text{ W PEP}$, $I_{DQ} = 250\text{ mA}$, $f_1 = 930.0\text{ MHz}$, $f_2 = 930.1\text{ MHz}$ and $f_1 = 960.0\text{ MHz}$, $f_2 = 960.1\text{ MHz}$)	η	—	41.5	—	%
3rd Order Intermodulation Distortion ($V_{DD} = 26\text{ Vdc}$, $P_{out} = 30\text{ W PEP}$, $I_{DQ} = 250\text{ mA}$, $f_1 = 930.0\text{ MHz}$, $f_2 = 930.1\text{ MHz}$ and $f_1 = 960.0\text{ MHz}$, $f_2 = 960.1\text{ MHz}$)	IMD	—	-33	—	dBc
Input Return Loss ($V_{DD} = 26\text{ Vdc}$, $P_{out} = 30\text{ W PEP}$, $I_{DQ} = 250\text{ mA}$, $f_1 = 930.0\text{ MHz}$, $f_2 = 930.1\text{ MHz}$ and $f_1 = 960.0\text{ MHz}$, $f_2 = 960.1\text{ MHz}$)	IRL	—	-14	—	dB
Power Output, 1 dB Compression Point ($V_{DD} = 26\text{ Vdc}$, $P_{out} = 30\text{ W CW}$, $I_{DQ} = 250\text{ mA}$, $f_1 = 945.0\text{ MHz}$)	P_{1dB}	—	30	—	W
Common-Source Amplifier Power Gain ($V_{DD} = 26\text{ Vdc}$, $P_{out} = 30\text{ W CW}$, $I_{DQ} = 250\text{ mA}$, $f_1 = 945.0\text{ MHz}$)	G_{ps}	—	19	—	dB
Drain Efficiency ($V_{DD} = 26\text{ Vdc}$, $P_{out} = 30\text{ W CW}$, $I_{DQ} = 250\text{ mA}$, $f_1 = 945.0\text{ MHz}$)	η	—	60	—	%

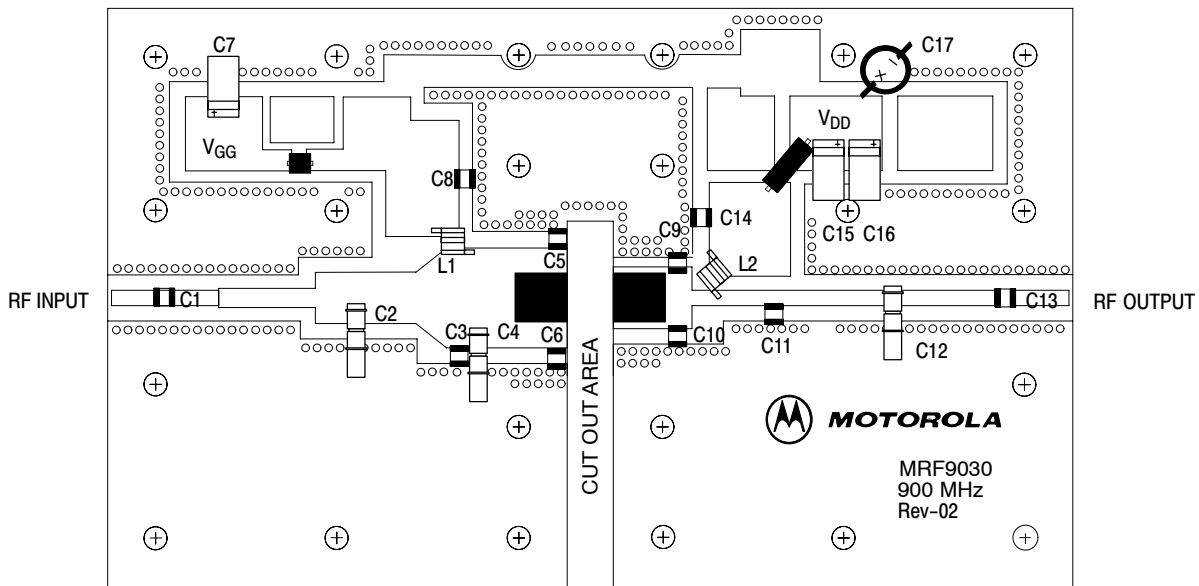
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B1	Short Ferrite Bead	Z3	0.500" x 0.100" Microstrip
B2	Long Ferrite Bead	Z4	0.215" x 0.270" Microstrip
C1, C8, C13, C14	47 pF Chip Capacitors	Z5	0.315" x 0.270" Microstrip
C2, C4	0.8 pF to 8.0 pF Trim Capacitors	Z6	0.160" x 0.270" x 0.520", Taper
C3	3.9 pF Chip Capacitor	Z7	0.285" x 0.520" Microstrip
C5, C6	7.5 pF Chip Capacitors	Z8	0.450" x 0.270" Microstrip
C7, C15, C16	10 μ F, 35 V Tantalum Capacitors	Z9	0.140" x 0.270" Microstrip
C9, C10	10 pF Chip Capacitors	Z10	0.250" x 0.060" Microstrip
C11	9.1 pF Chip Capacitor	Z11	0.720" x 0.060" Microstrip
C12	0.6 pF to 4.5 pF Trim Capacitor	Z12	0.490" x 0.060" Microstrip
C17	220 μ F, 50 V Electrolytic Capacitor	Z13	0.290" x 0.060" Microstrip
L1, L2	12.5 nH Surface Mount Inductors	PCB	Taconic RF-35-0300, 30 mil, $\epsilon_r = 3.55$
Z1	0.260" x 0.060" Microstrip		
Z2	0.240" x 0.060" Microstrip		

Figure 1. 945 MHz Broadband Test Circuit Schematic



Freescle has begun the transition of marking Printed Circuit Boards (PCBs) with the Freescle Semiconductor signature/logo. PCBs may have either Motorola or Freescle markings during the transition period. These changes will have no impact on form, fit or function of the current product.

Figure 2. 945 MHz Broadband Test Circuit Component Layout

TYPICAL CHARACTERISTICS

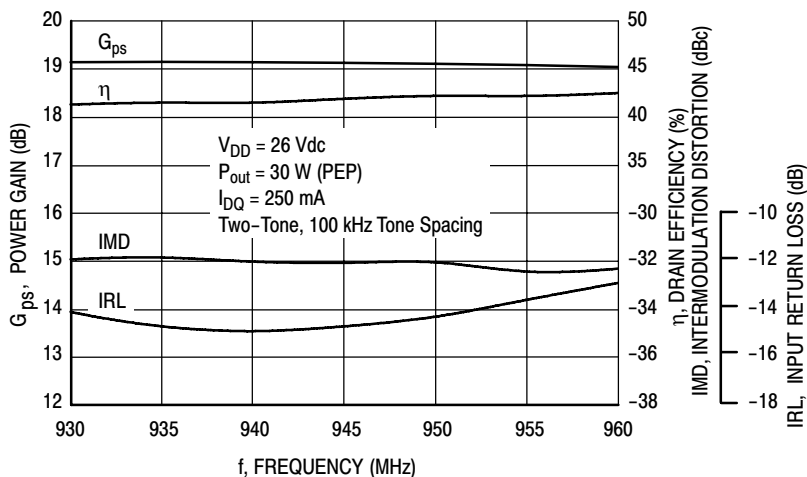


Figure 3. Class AB Broadband Circuit Performance

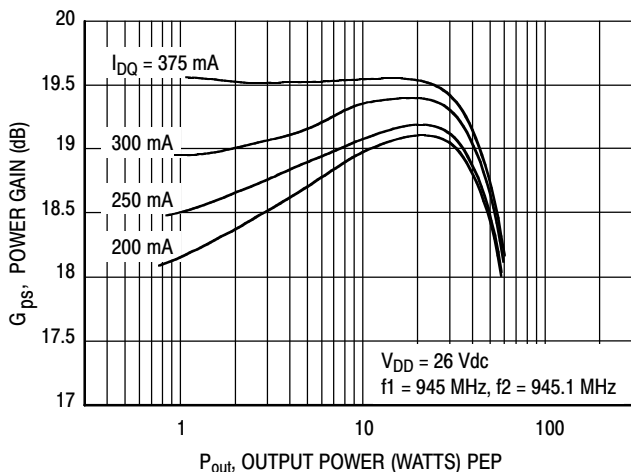


Figure 4. Power Gain versus Output Power

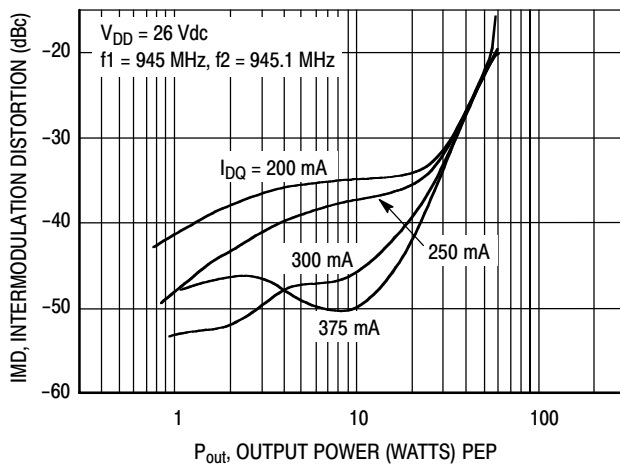


Figure 5. Intermodulation Distortion versus Output Power

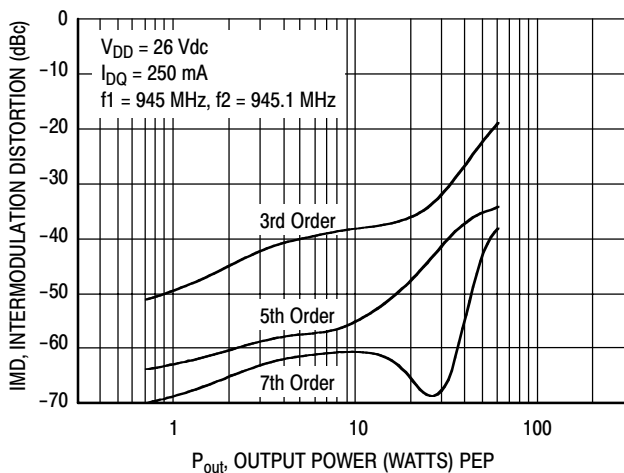


Figure 6. Intermodulation Distortion Products versus Output Power

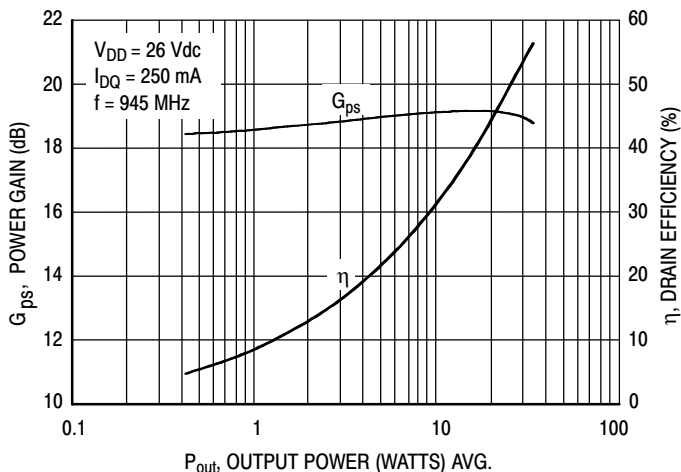


Figure 7. Power Gain and Efficiency versus Output Power

TYPICAL CHARACTERISTICS

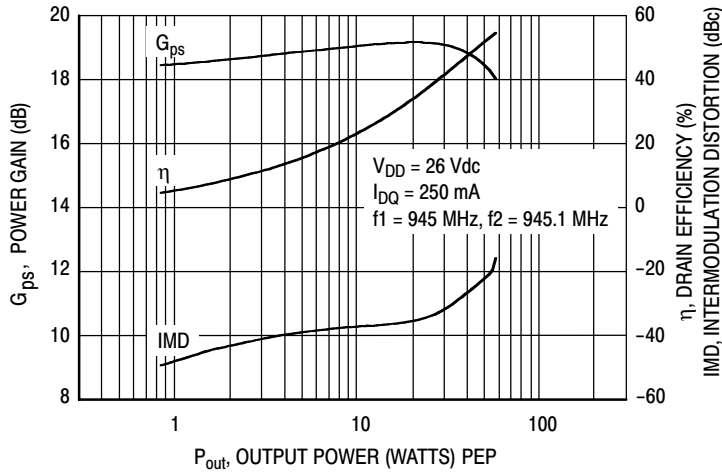
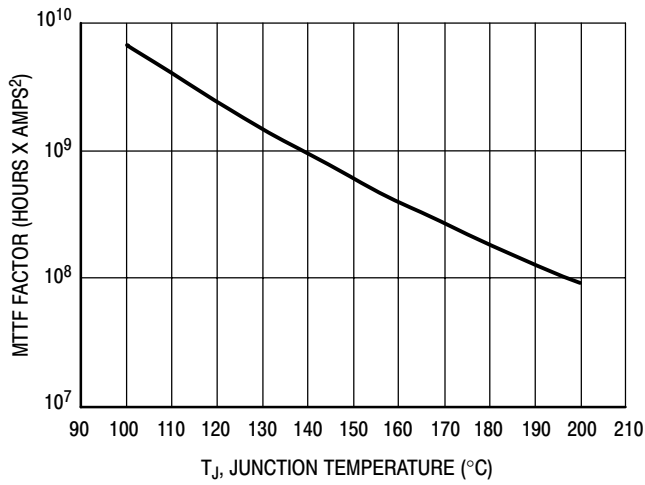
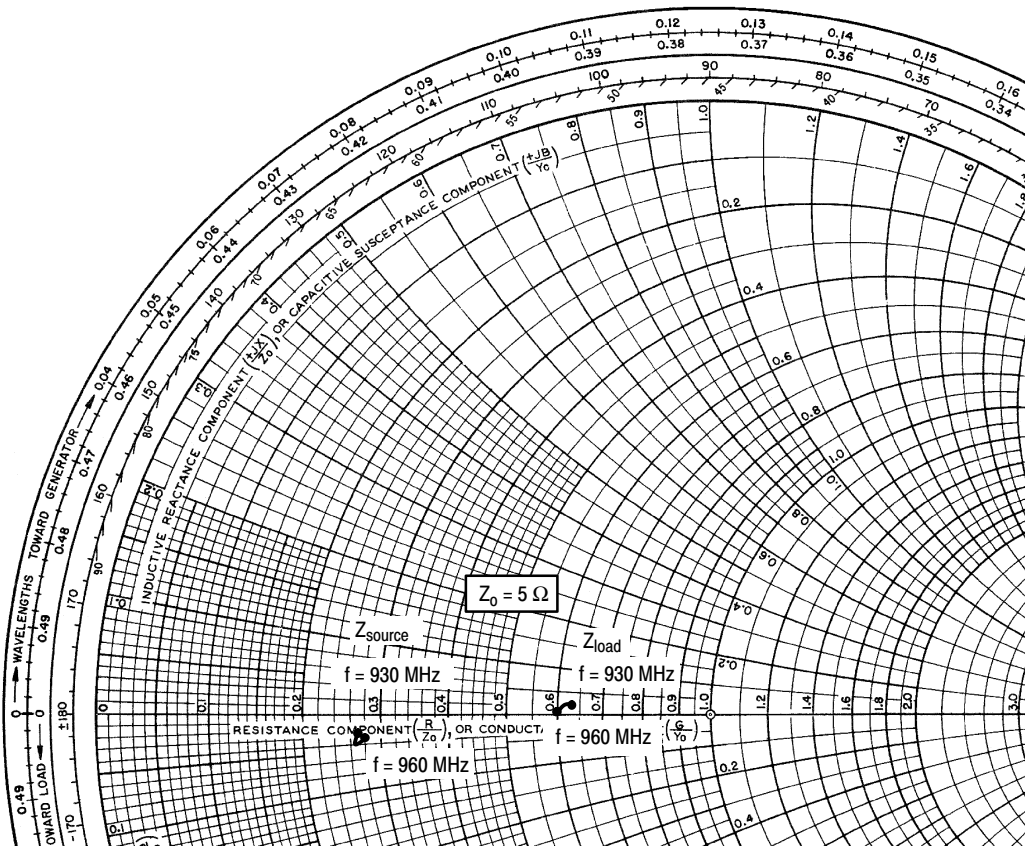


Figure 8. Power Gain, Efficiency and IMD versus Output Power



This above graph displays calculated MTTF in hours x ampere² drain current. Life tests at elevated temperatures have correlated to better than $\pm 10\%$ of the theoretical prediction for metal failure. Divide MTTF factor by I_D^2 for MTTF in a particular application.

Figure 9. MTTF Factor versus Junction Temperature



$V_{DD} = 26\text{ V}$, $I_{DQ} = 250\text{ mA}$, $P_{out} = 30\text{ W PEP}$

f MHz	Z_{source} Ω	Z_{load} Ω
930	$1.34 - j0.1$	$3.175 + j0.09$
945	$1.36 - j0.2$	$3.1 + j0.08$
960	$1.4 - j0.14$	$3.0 + j0.05$

Z_{source} = Test circuit impedance as measured from gate to ground.

Z_{load} = Test circuit impedance as measured from drain to ground.

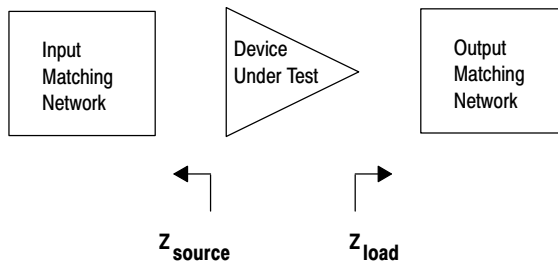
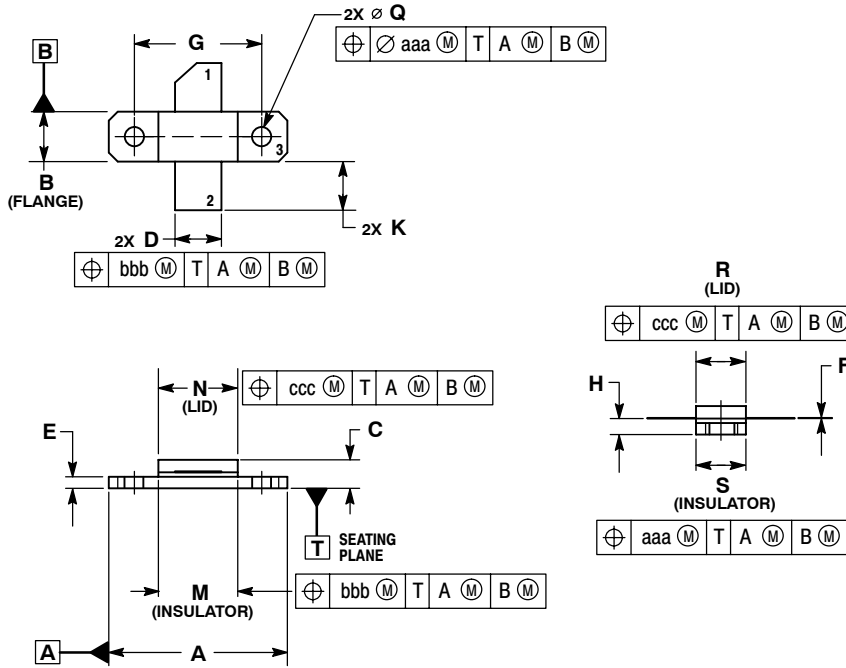


Figure 10. Series Equivalent Source and Load Impedance

PACKAGE DIMENSIONS



- NOTES:
1. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M-1994.
 2. CONTROLLING DIMENSION: INCH.
 3. DIMENSION H IS MEASURED 0.030 (0.762) AWAY FROM PACKAGE BODY.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.795	0.805	20.19	20.45
B	0.225	0.235	5.72	5.97
C	0.125	0.175	3.18	4.45
D	0.210	0.220	5.33	5.59
E	0.055	0.065	1.40	1.65
F	0.004	0.006	0.10	0.15
G	0.562 BSC		14.28 BSC	
H	0.077	0.087	1.96	2.21
K	0.220	0.250	5.59	6.35
M	0.355	0.365	9.02	9.27
N	0.357	0.363	9.07	9.22
Q	0.125	0.135	3.18	3.43
R	0.227	0.233	5.77	5.92
S	0.225	0.235	5.72	5.97
aaa	0.005 REF		0.13 REF	
bbb	0.010 REF		0.25 REF	
ccc	0.015 REF		0.38 REF	

- STYLE 1:
 PIN 1. DRAIN
 2. GATE
 3. SOURCE

CASE 360B-05
ISSUE G
NI-360
MRF9030LR1

PRODUCT DOCUMENTATION

Refer to the following documents to aid your design process.

Engineering Bulletins

- EB212: Using Data Sheet Impedances for RF LDMOS Devices

REVISION HISTORY

The following table summarizes revisions to this document.

Revision	Date	Description
8	Sept. 2008	<ul style="list-style-type: none">• Data sheet revised to reflect part status change, p. 1, including use of applicable overlay.• Added Product Documentation and Revision History, p. 9

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