

Replaced by MRF6S18060NR1/NBR1. There are no form, fit or function changes with this part replacement. N suffix added to part number to indicate transition to lead-free terminations.

## RF Power Field Effect Transistors

### N-Channel Enhancement-Mode Lateral MOSFETs

Designed for GSM and GSM EDGE base station applications with frequencies from 1800 to 2000 MHz. Suitable for TDMA, CDMA, and multicarrier amplifier applications.

#### GSM Application

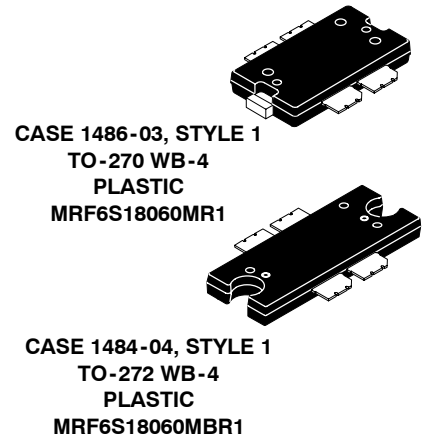
- Typical GSM Performance:  $V_{DD} = 26$  Vdc,  $I_{DQ} = 600$  mA,  $P_{out} = 60$  Watts CW, Full Frequency Band (1805-1880 MHz or 1930-1990 MHz)  
 Power Gain — 15 dB  
 Drain Efficiency - 50%

#### GSM EDGE Application

- Typical GSM EDGE Performance:  $V_{DD} = 26$  Volts,  $I_{DQ} = 450$  mA,  $P_{out} = 25$  Watts Avg., Full Frequency Band (1805-1880 MHz or 1930-1990 MHz)  
 Power Gain — 15.5 dB  
 Spectral Regrowth @ 400 kHz Offset = -62 dBc  
 Spectral Regrowth @ 600 kHz Offset = -76 dBc  
 EVM — 2% rms
- Capable of Handling 5:1 VSWR, @ 26 Vdc, 1990 MHz, 60 Watts CW Output Power
- Characterized with Series Equivalent Large-Signal Impedance Parameters
- Internally Matched for Ease of Use
- Qualified Up to a Maximum of 32  $V_{DD}$  Operation
- Integrated ESD Protection
- 200°C Capable Plastic Package
- In Tape and Reel. R1 Suffix = 500 Units per 44 mm, 13 inch Reel.

**MRF6S18060MR1**  
**MRF6S18060MBR1**

**1800-2000 MHz, 60 W, 26 V**  
**GSM/GSM EDGE**  
**LATERAL N-CHANNEL**  
**RF POWER MOSFETs**



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**Table 1. Maximum Ratings**

Rating	Symbol	Value	Unit
Drain-Source Voltage	$V_{DSS}$	-0.5, +68	Vdc
Gate-Source Voltage	$V_{GS}$	-0.5, +12	Vdc
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	$P_D$	216 1.2	W W/°C
Storage Temperature Range	$T_{stg}$	- 65 to +175	°C
Operating Junction Temperature	$T_J$	200	°C

**Table 2. Thermal Characteristics**

Characteristic	Symbol	Value <sup>(1)</sup>	Unit
Thermal Resistance, Junction to Case Case Temperature 80°C, 60 W CW Case Temperature 77°C, 25 W CW	$R_{\theta JC}$	0.81 0.95	°C/W

1. MTTF calculator available at <http://www.freescale.com/rtf>. Select Tools/Software/Application Software/Calculators to access the MTTF calculators by product.

**NOTE - CAUTION** - MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

**Table 3. ESD Protection Characteristics**

Test Methodology	Class
Human Body Model (per JESD22-A114)	1B (Minimum)
Machine Model (per EIA/JESD22-A115)	A (Minimum)
Charge Device Model (per JESD22-C101)	III (Minimum)

**Table 4. Moisture Sensitivity Level**

Test Methodology	Rating	Package Peak Temperature	Unit
Per JESD 22-A113, IPC/JEDEC J-STD-020	3	260	°C

**Table 5. Electrical Characteristics** ( $T_C = 25^\circ\text{C}$  unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
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**Off Characteristics**

Zero Gate Voltage Drain Leakage Current ( $V_{DS} = 68\text{ Vdc}$ , $V_{GS} = 0\text{ Vdc}$ )	$I_{DSS}$	—	—	10	$\mu\text{Adc}$
Zero Gate Voltage Drain Leakage Current ( $V_{DS} = 26\text{ Vdc}$ , $V_{GS} = 0\text{ Vdc}$ )	$I_{DSS}$	—	—	1	$\mu\text{Adc}$
Gate-Source Leakage Current ( $V_{GS} = 5\text{ Vdc}$ , $V_{DS} = 0\text{ Vdc}$ )	$I_{GSS}$	—	—	1	$\mu\text{Adc}$

**On Characteristics**

Gate Threshold Voltage ( $V_{DS} = 10\text{ Vdc}$ , $I_D = 200\ \mu\text{Adc}$ )	$V_{GS(th)}$	1	2	3	Vdc
Gate Quiescent Voltage ( $V_{DS} = 26\text{ Vdc}$ , $I_D = 600\ \text{mAdc}$ )	$V_{GS(Q)}$	2	2.8	4	Vdc
Drain-Source On-Voltage ( $V_{GS} = 10\text{ Vdc}$ , $I_D = 2\ \text{Adc}$ )	$V_{DS(on)}$	—	0.24	—	Vdc
Forward Transconductance ( $V_{DS} = 10\text{ Vdc}$ , $I_D = 2\ \text{Adc}$ )	$g_{fs}$	—	5.3	—	S

**Dynamic Characteristics**

Reverse Transfer Capacitance <sup>(1)</sup> ( $V_{DS} = 26\text{ Vdc} \pm 30\ \text{mV(rms)ac}$ @ 1 MHz, $V_{GS} = 0\text{ Vdc}$ )	$C_{rss}$	—	1.5	—	pF
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**Functional Tests** (In Freescale Test Fixture, 50 ohm system)  $V_{DD} = 26\text{ Vdc}$ ,  $I_{DQ} = 600\ \text{mA}$ ,  $P_{out} = 60\ \text{W}$ ,  $f = 1930\ \text{MHz}$ ,  $f = 1990\ \text{MHz}$ 

Power Gain	$G_{ps}$	14	15	17	dB
Drain Efficiency	$\eta_D$	48	50	—	%
Input Return Loss	IRL	—	-12	-9	dB
$P_{out}$ @ 1 dB Compression Point	P1dB	60	65	—	W

1. Part is internally matched both on input and output.

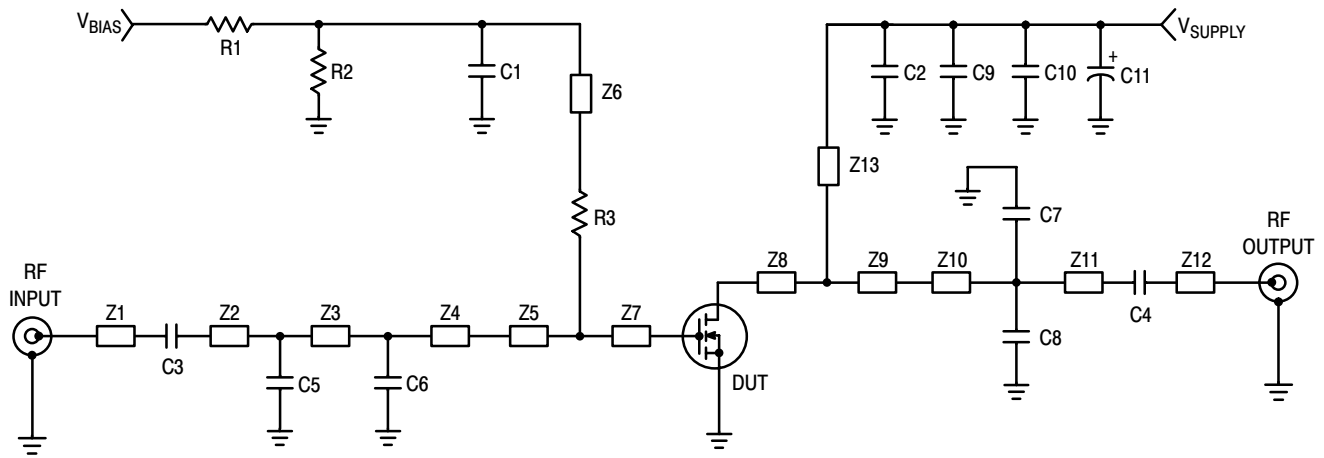
(continued)

**Table 5. Electrical Characteristics** ( $T_C = 25^\circ\text{C}$  unless otherwise noted) (continued)

Characteristic	Symbol	Min	Typ	Max	Unit
<b>Typical GSM EDGE Performances</b> (In Freescale Broadband Test Fixture, 50 ohm system) $V_{DD} = 26\text{ Vdc}$ , $I_{DQ} = 450\text{ mA}$ , $P_{out} = 25\text{ W Avg.}$ , 1805 MHz<Frequency<1880 MHz or 1930 MHz<Frequency<1990 MHz					
Power Gain	$G_{ps}$	—	15.5	—	dB
Drain Efficiency	$\eta_D$	—	32	—	%
Error Vector Magnitude	EVM	—	2	—	% rms
Spectral Regrowth at 400 kHz Offset	SR1	—	-62	—	dBc
Spectral Regrowth at 600 kHz Offset	SR2	—	-76	—	dBc

**Typical CW Performances** (In Freescale Broadband Test Fixture, 50 ohm system)  $V_{DD} = 26\text{ Vdc}$ ,  $I_{DQ} = 600\text{ mA}$ ,  $P_{out} = 60\text{ W}$ , 1805 MHz<Frequency<1880 MHz or 1930 MHz<Frequency<1990 MHz

Power Gain	$G_{ps}$	—	15	—	dB
Drain Efficiency	$\eta_D$	—	50	—	%
Input Return Loss	IRL	—	-12	—	dB
$P_{out}$ @ 1 dB Compression Point, CW	P1dB	—	65	—	W



Z1	0.250" x 0.083" Microstrip	Z9	0.485" x 1.000" Microstrip
Z2*	0.950" x 0.083" Microstrip	Z10*	0.500" x 0.083" Microstrip
Z3*	0.250" x 0.083" Microstrip	Z11*	0.895" x 0.083" Microstrip
Z4*	0.315" x 0.083" Microstrip	Z12	0.250" x 0.083" Microstrip
Z5	0.365" x 1.000" Microstrip	Z13	0.200" x 0.080" Microstrip
Z6	0.680" x 0.080" Microstrip	PCB	Taconic TLX8-0300, 0.030", $\epsilon_r = 2.55$
Z7, Z8	0.115" x 1.000" Microstrip		* Variable for tuning

**Figure 1. MRF6S18060MR1 (MBR1) Test Circuit Schematic — 1900 MHz**

**Table 6. MRF6S18060MR1 (MBR1) Test Circuit Component Designations and Values — 1900 MHz**

Part	Description	Part Number	Manufacturer
C1, C2, C3, C4	6.8 pF 100B Chip Capacitors	100B6R8CW	ATC
C5	1.5 pF 100B Chip Capacitor	100B1R5BW	ATC
C6	1.8 pF 100B Chip Capacitor	100B1R8BW	ATC
C7, C8	1 pF 100B Chip Capacitors	100B1R0BW	ATC
C9, C10	10 $\mu$ F Chip Capacitors (2220)	C5750X5R1H106MT	TDK
C11	220 $\mu$ F, 63 V Electrolytic Capacitor, Radial	13668221	Philips
R1, R2	10 k $\Omega$ , 1/4 W Chip Resistors (1206)		
R3	10 $\Omega$ , 1/4 W Chip Resistor (1206)		

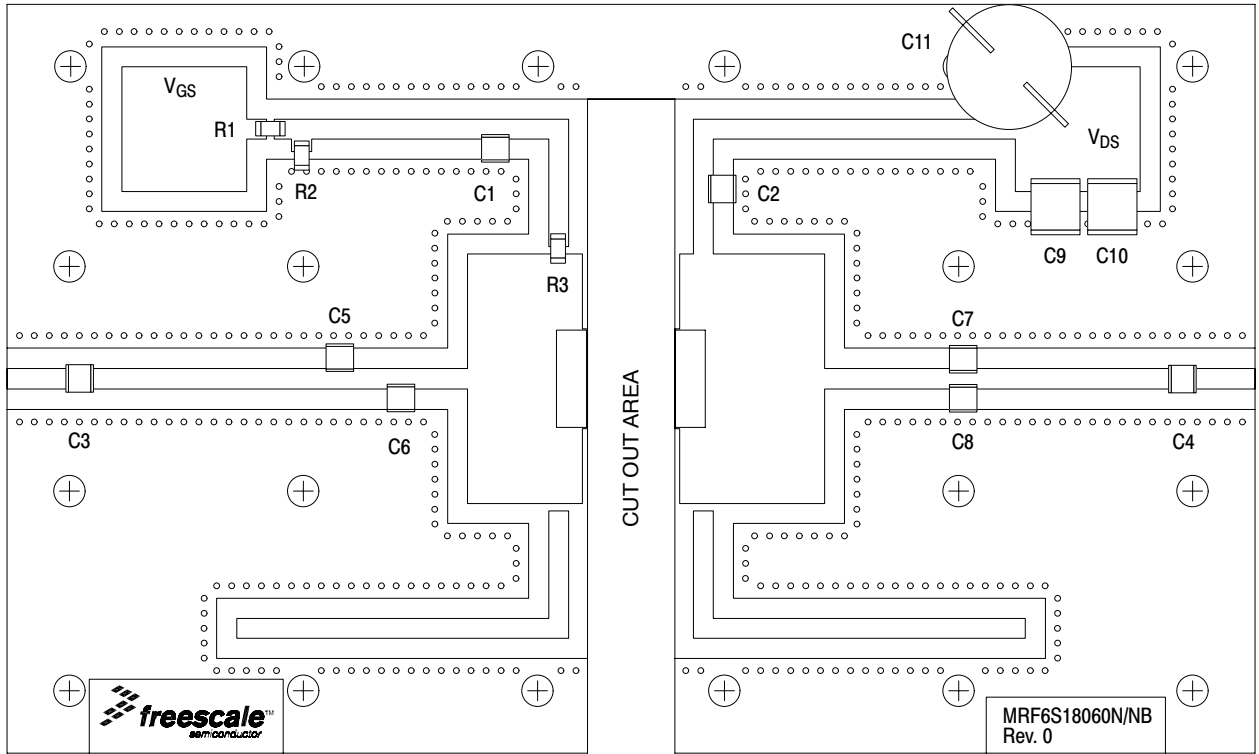


Figure 2. MRF6S18060MR1 (MBR1) Test Circuit Component Layout — 1900 MHz

TYPICAL CHARACTERISTICS — 1900 MHz

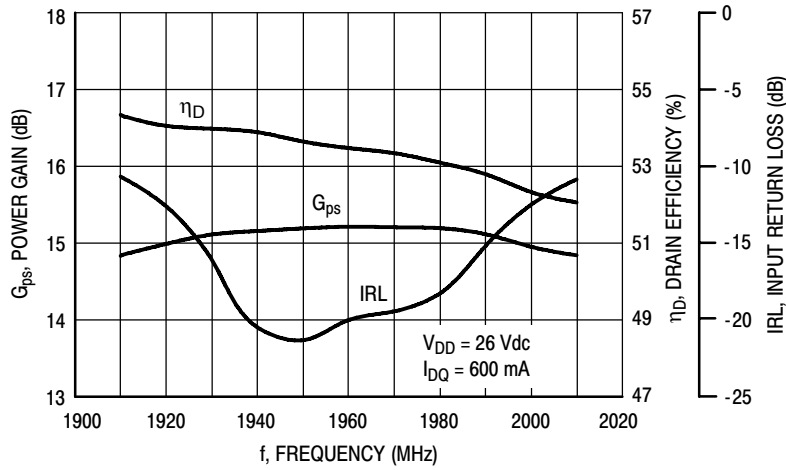


Figure 3. Power Gain, Input Return Loss and Drain Efficiency versus Frequency @  $P_{out} = 60$  Watts

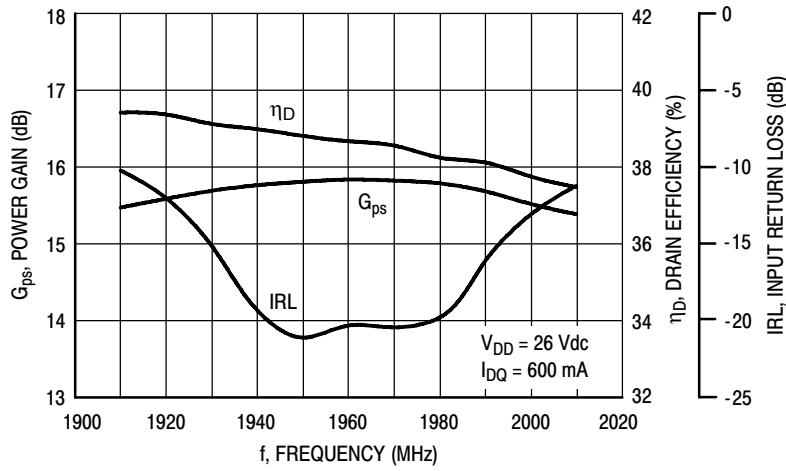


Figure 4. Power Gain, Input Return Loss and Drain Efficiency versus Frequency @  $P_{out} = 30$  Watts

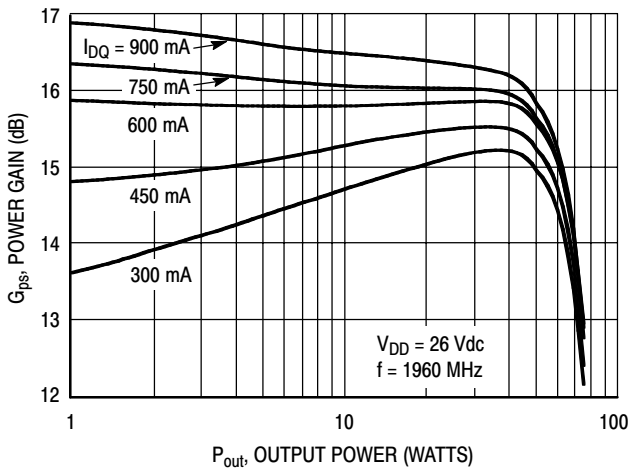


Figure 5. Power Gain versus Output Power

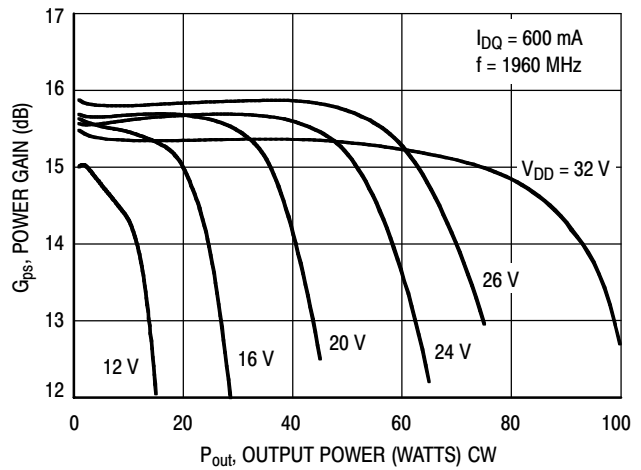
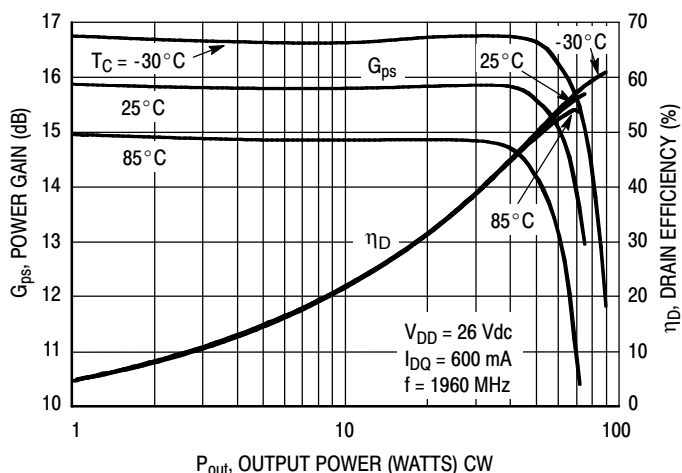
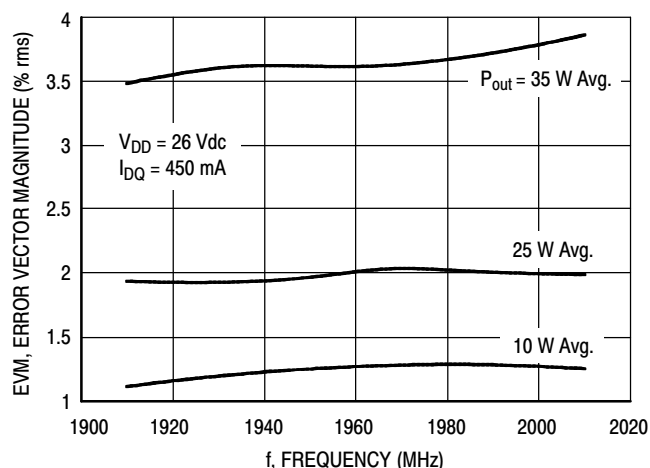


Figure 6. Power Gain versus Output Power

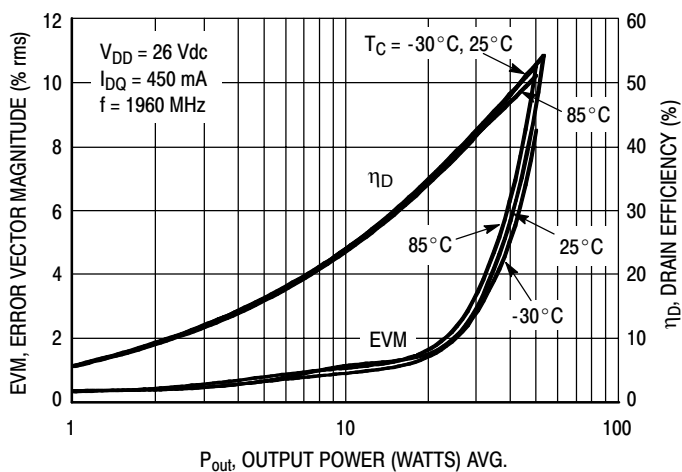
## TYPICAL CHARACTERISTICS — 1900 MHz



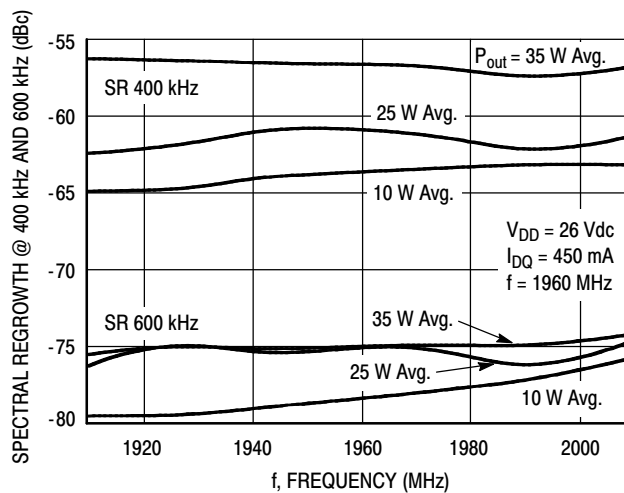
**Figure 7. Power Gain and Drain Efficiency versus CW Output Power**



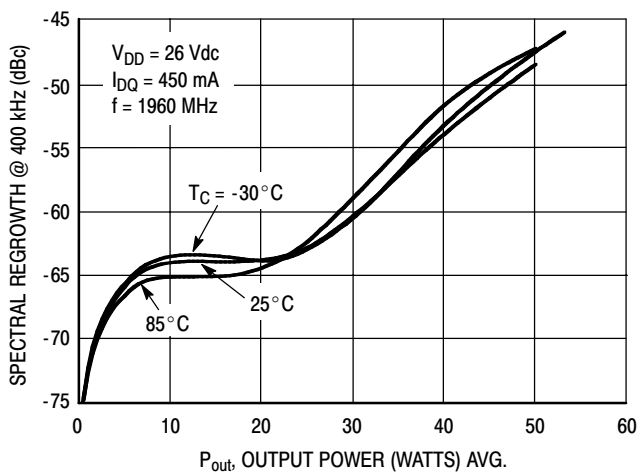
**Figure 8. Error Vector Magnitude versus Frequency**



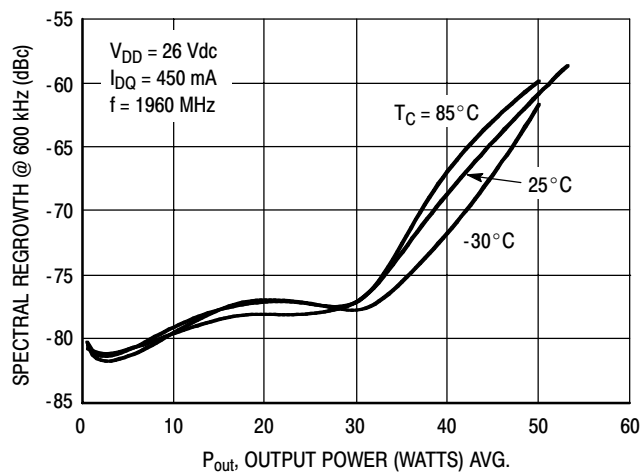
**Figure 9. Error Vector Magnitude and Drain Efficiency versus Output Power**



**Figure 10. Spectral Regrowth at 400 kHz and 600 kHz versus Frequency**



**Figure 11. Spectral Regrowth at 400 kHz versus Output Power**

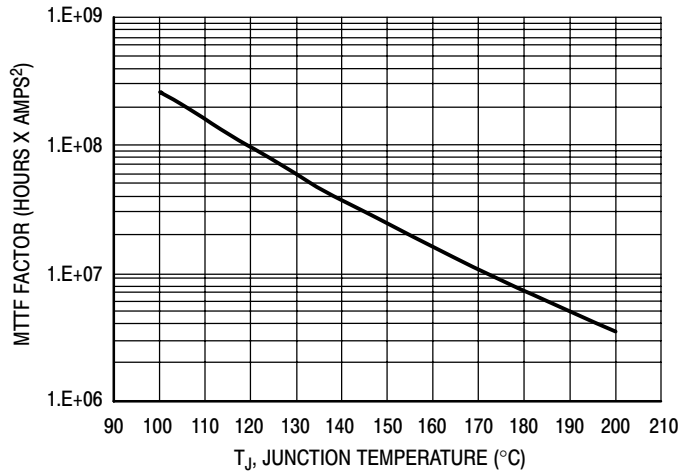


**Figure 12. Spectral Regrowth at 600 kHz versus Output Power**

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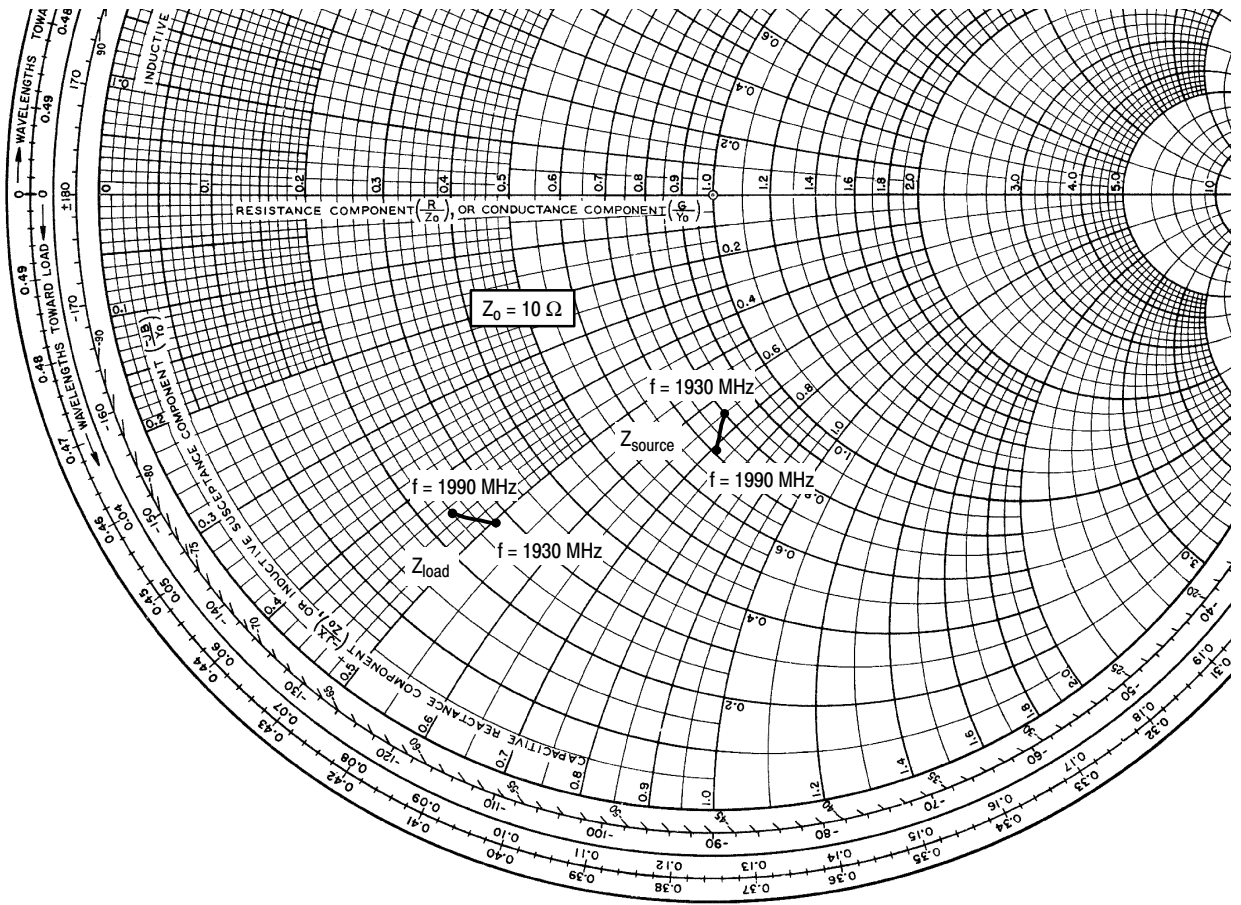
**TYPICAL CHARACTERISTICS**



This above graph displays calculated MTTF in hours x ampere<sup>2</sup> drain current. Life tests at elevated temperatures have correlated to better than ±10% of the theoretical prediction for metal failure. Divide MTTF factor by  $I_D^2$  for MTTF in a particular application.

**Figure 13. MTTF Factor versus Junction Temperature**





$V_{DD} = 26 \text{ Vdc}$ ,  $I_{DQ} = 600 \text{ mA}$ ,  $P_{out} = 60 \text{ W CW}$

f MHz	$Z_{source}$ $\Omega$	$Z_{load}$ $\Omega$
1930	8.00 - j6.48	2.83 - j5.13
1960	7.57 - j6.82	2.63 - j4.84
1990	7.06 - j7.06	2.44 - j4.54

$Z_{source}$  = Test circuit impedance as measured from gate to ground.

$Z_{load}$  = Test circuit impedance as measured from drain to ground.

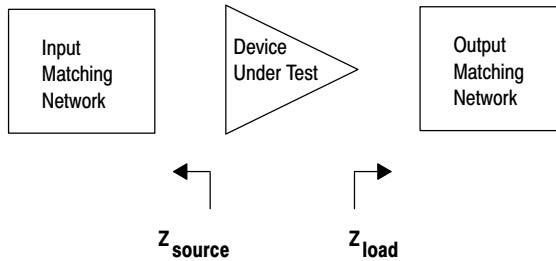
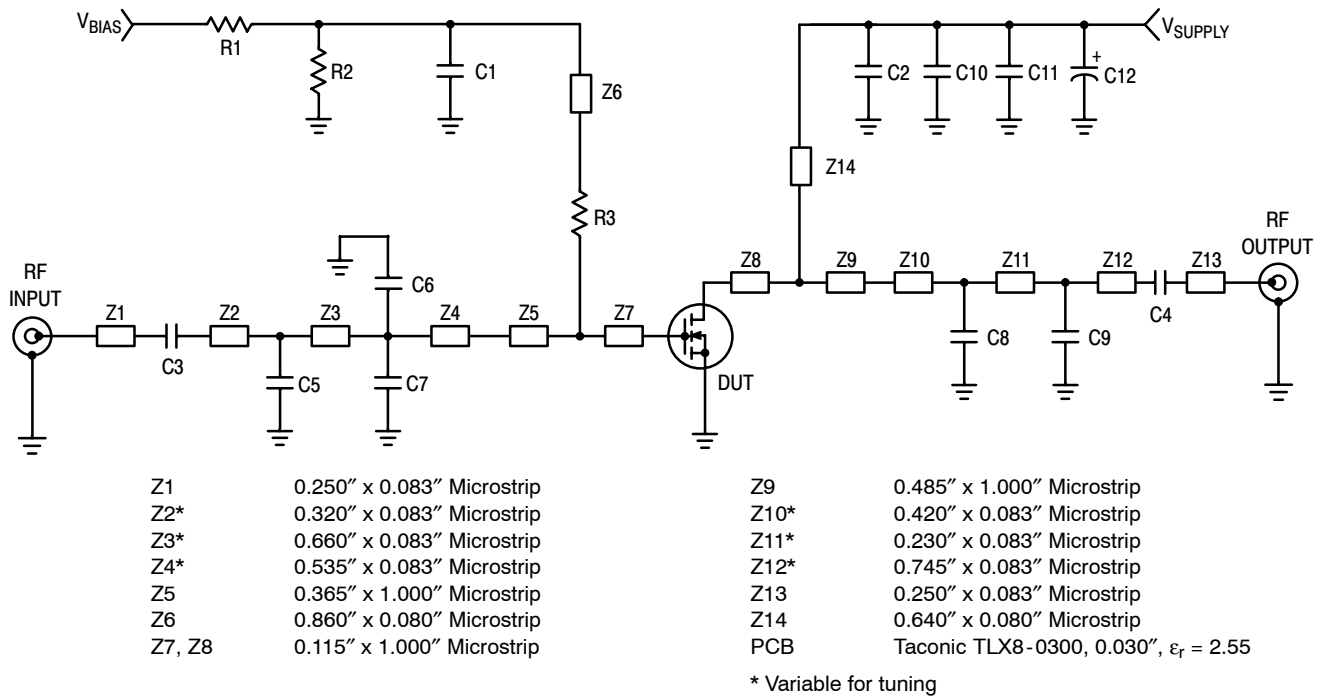


Figure 14. Series Equivalent Source and Load Impedance — 1900 MHz



**Figure 15. MRF6S18060MR1 (MBR1) Test Circuit Schematic — 1800 MHz**

**Table 7. MRF6S18060MR1 (MBR1) Test Circuit Component Designations and Values — 1800 MHz**

Part	Description	Part Number	Manufacturer
C1, C2, C3, C4	6.8 pF 100B Chip Capacitors	100B6R8CW	ATC
C5	0.8 pF 600B Chip Capacitor	600B0R8BW	ATC
C6, C9	0.5 pF 600B Chip Capacitors	600B0R5BW	ATC
C7	2.2 pF 200B Chip Capacitor	200B2R2BW	ATC
C8	1.5 pF 600B Chip Capacitor	600B1R5BW	ATC
C10, C11	10 $\mu$ F Chip Capacitors (2220)	C5750X5R1H106MT	TDK
C12	220 $\mu$ F, 63 V Electrolytic Capacitor, Radial	13668221	Philips
R1, R2	10 k $\Omega$ , 1/4 W Chip Resistors (1206)		
R3	10 $\Omega$ , 1/4 W Chip Resistor (1206)		

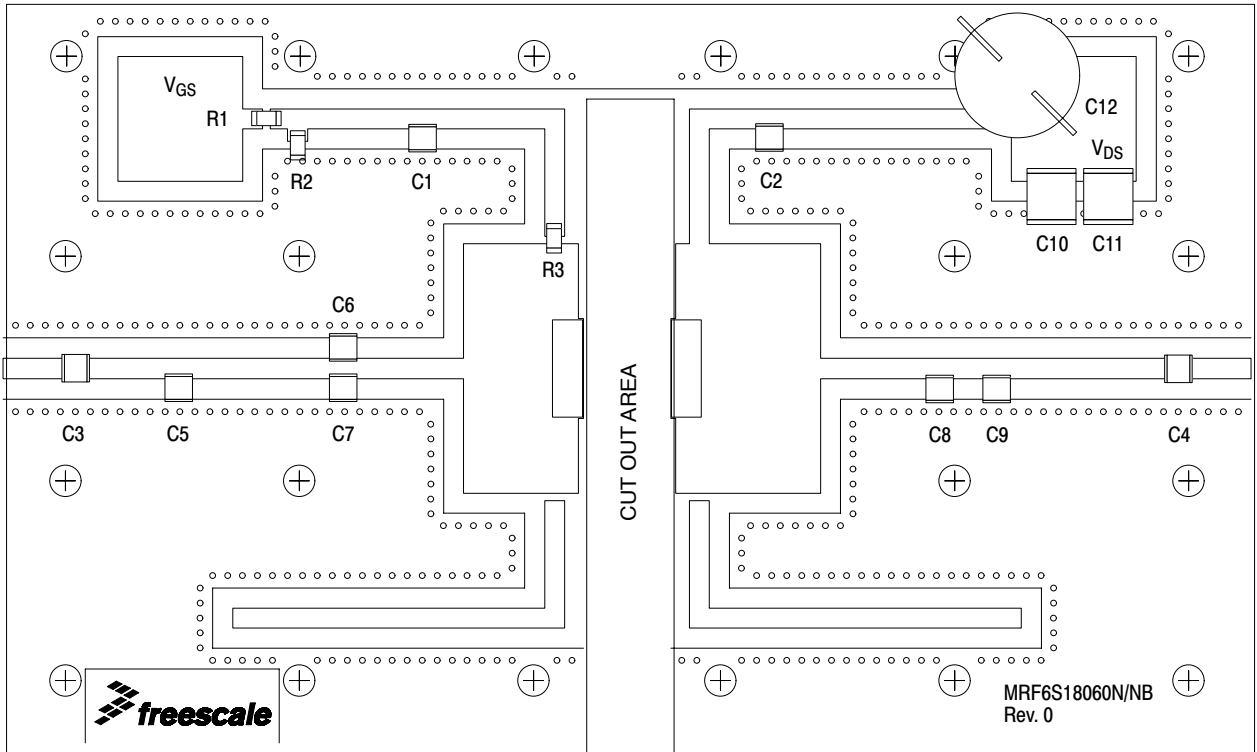
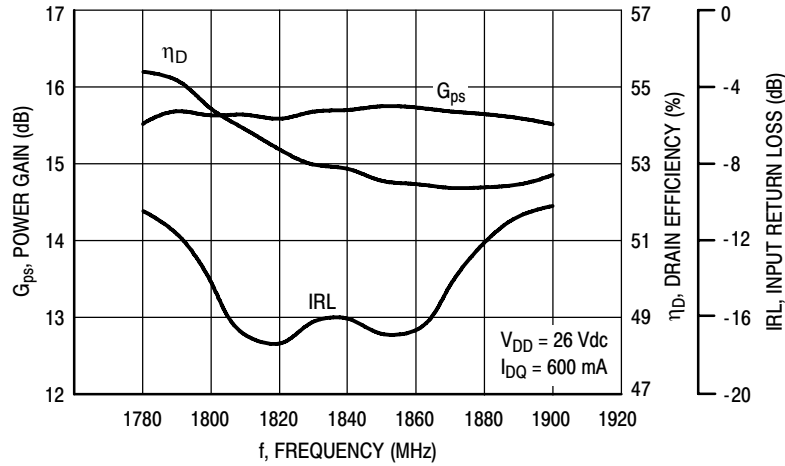
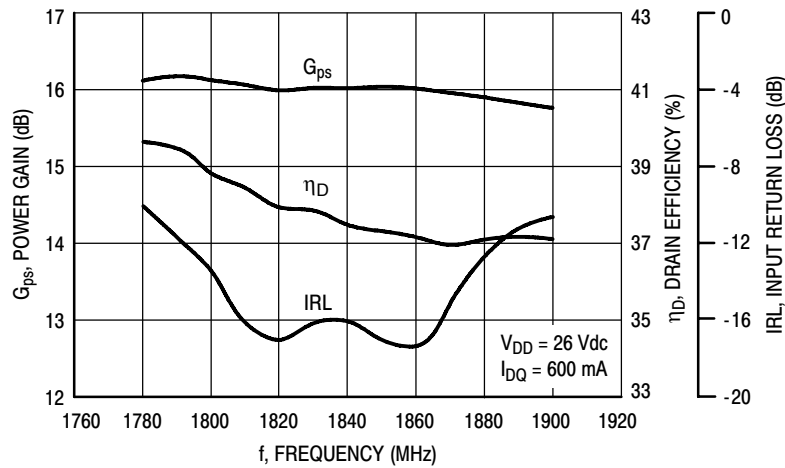


Figure 16. MRF6S18060MR1(MBR1) Test Circuit Component Layout — 1800 MHz

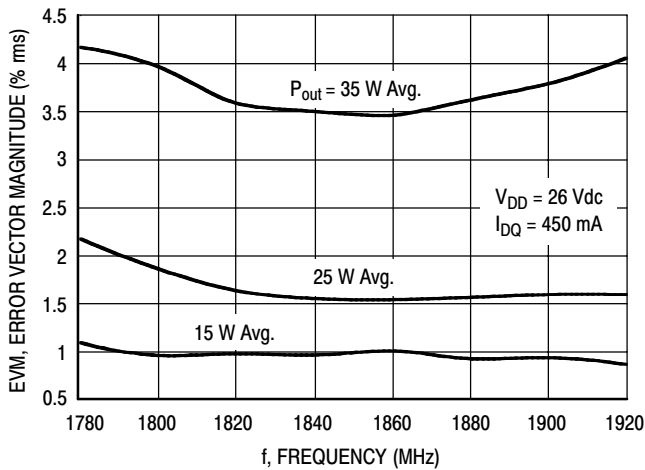
**TYPICAL CHARACTERISTICS — 1800 MHz**



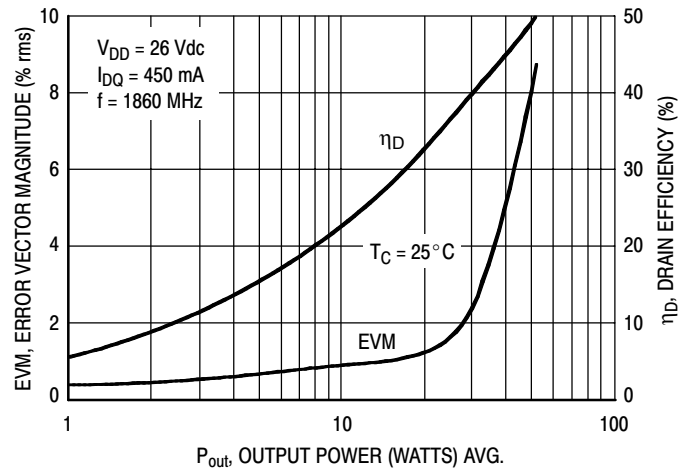
**Figure 17. Power Gain, Input Return Loss and Drain Efficiency versus Frequency @ P<sub>out</sub> = 60 Watts**



**Figure 18. Power Gain, Input Return Loss and Drain Efficiency versus Frequency @ P<sub>out</sub> = 30 Watts**



**Figure 19. Error Vector Magnitude versus Frequency**



**Figure 20. Error Vector Magnitude and Drain Efficiency versus Output Power**

TYPICAL CHARACTERISTICS — 1800 MHz

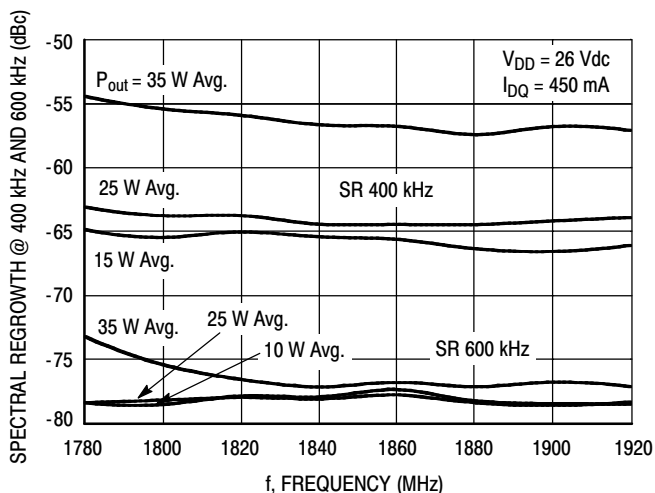


Figure 21. Spectral Regrowth at 400 kHz and 600 kHz versus Frequency

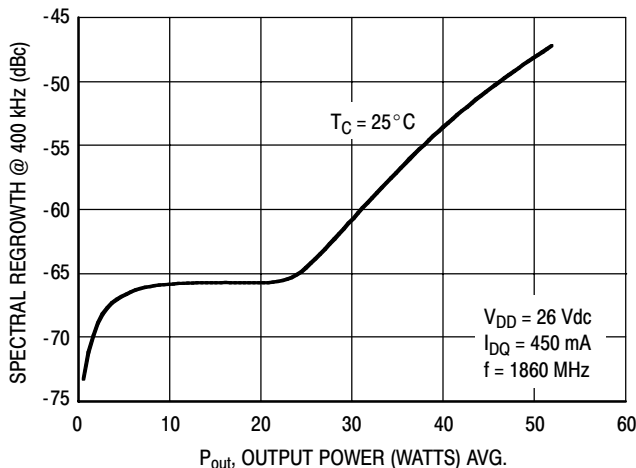


Figure 22. Spectral Regrowth at 400 kHz versus Output Power

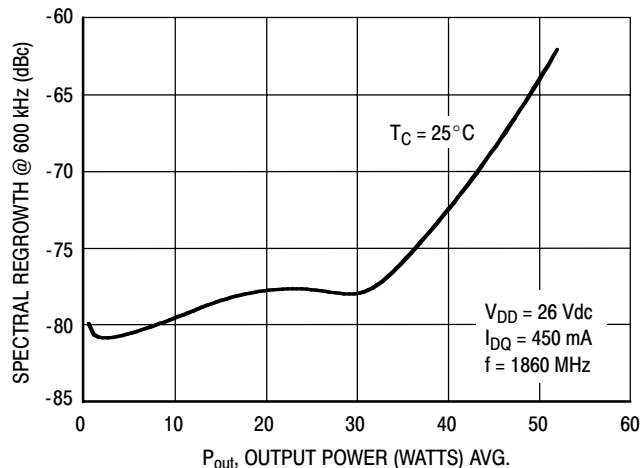
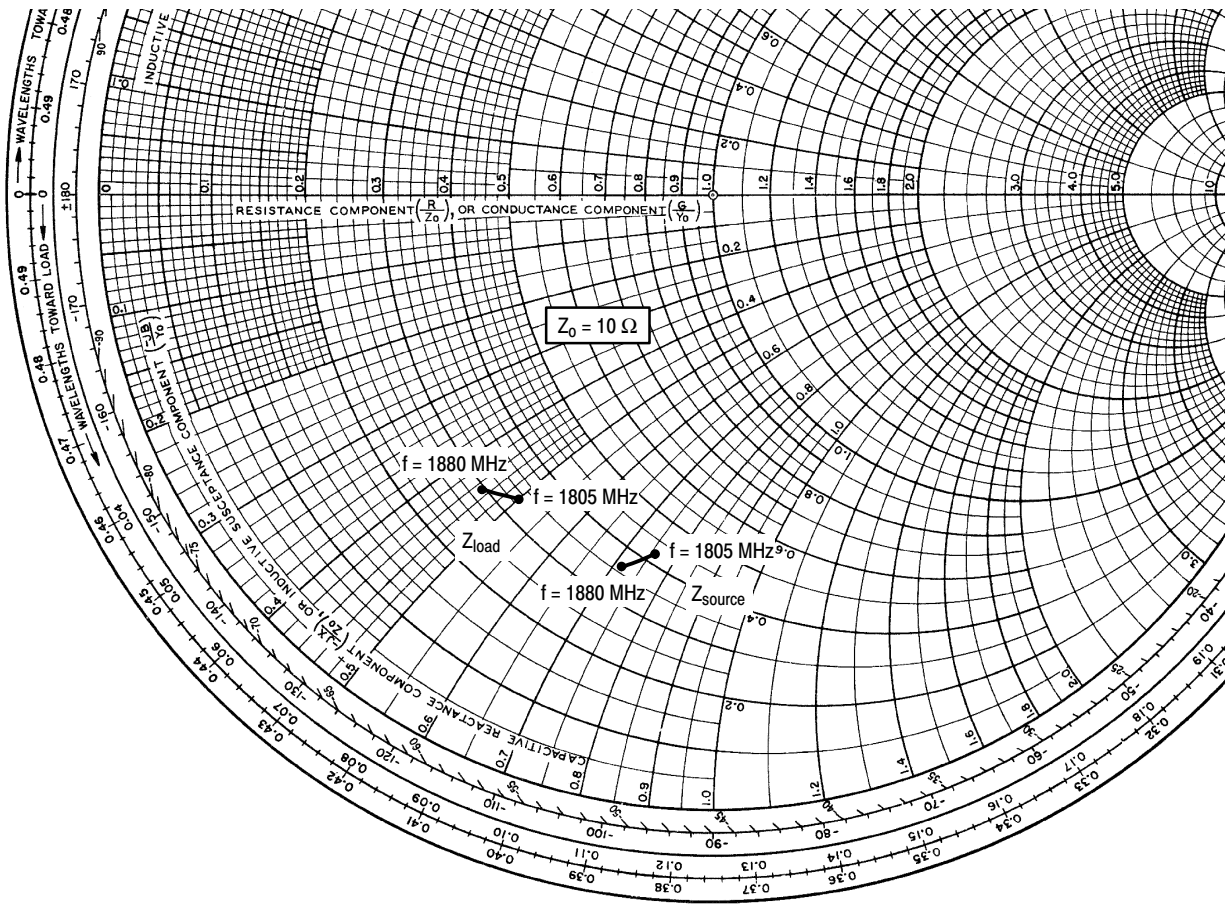


Figure 23. Spectral Regrowth at 600 kHz versus Output Power

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$V_{DD} = 26 \text{ Vdc}$ ,  $I_{DQ} = 600 \text{ mA}$ ,  $P_{out} = 65 \text{ W CW}$

f MHz	$Z_{source}$ $\Omega$	$Z_{load}$ $\Omega$
1805	$4.16 - j7.56$	$3.29 - j4.91$
1840	$3.89 - j7.40$	$3.10 - j4.69$
1880	$3.56 - j7.21$	$2.88 - j4.45$

$Z_{source}$  = Test circuit impedance as measured from gate to ground.

$Z_{load}$  = Test circuit impedance as measured from drain to ground.

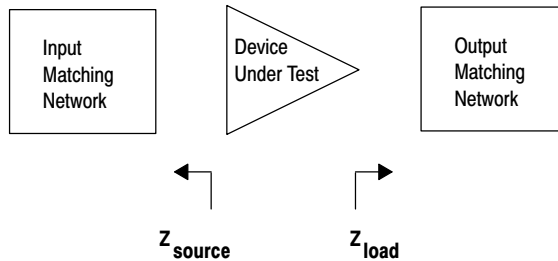
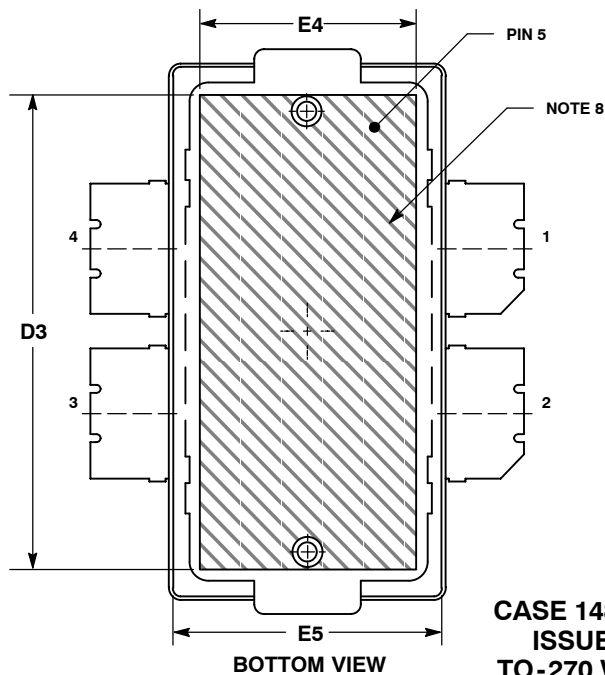
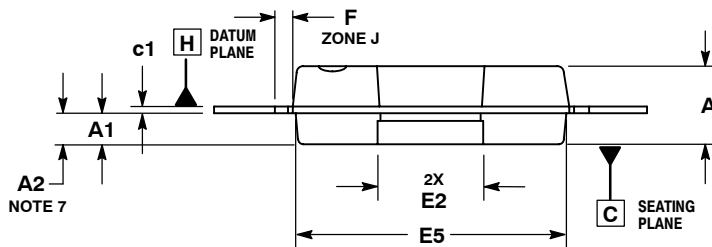
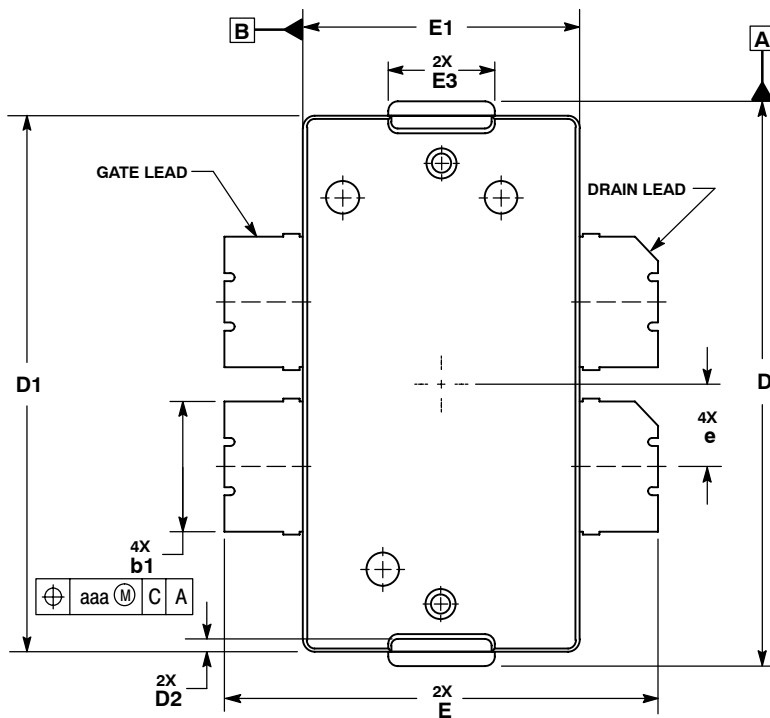


Figure 24. Series Equivalent Source and Load Impedance — 1800 MHz

# NOTES

# PACKAGE DIMENSIONS



## NOTES:

1. CONTROLLING DIMENSION: INCH.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M - 1994.
3. DATUM PLANE -H- IS LOCATED AT THE TOP OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE TOP OF THE PARTING LINE.
4. DIMENSIONS "D" AND "E1" DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS .006 PER SIDE. DIMENSIONS "D" AND "E1" DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -H-.
5. DIMENSION "b1" DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE .005 TOTAL IN EXCESS OF THE "b1" DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. DATUMS -A- AND -B- TO BE DETERMINED AT DATUM PLANE -H-.
7. DIMENSION A2 APPLIES WITHIN ZONE "J" ONLY.
8. HATCHING REPRESENTS THE EXPOSED AREA OF THE HEAT SLUG.

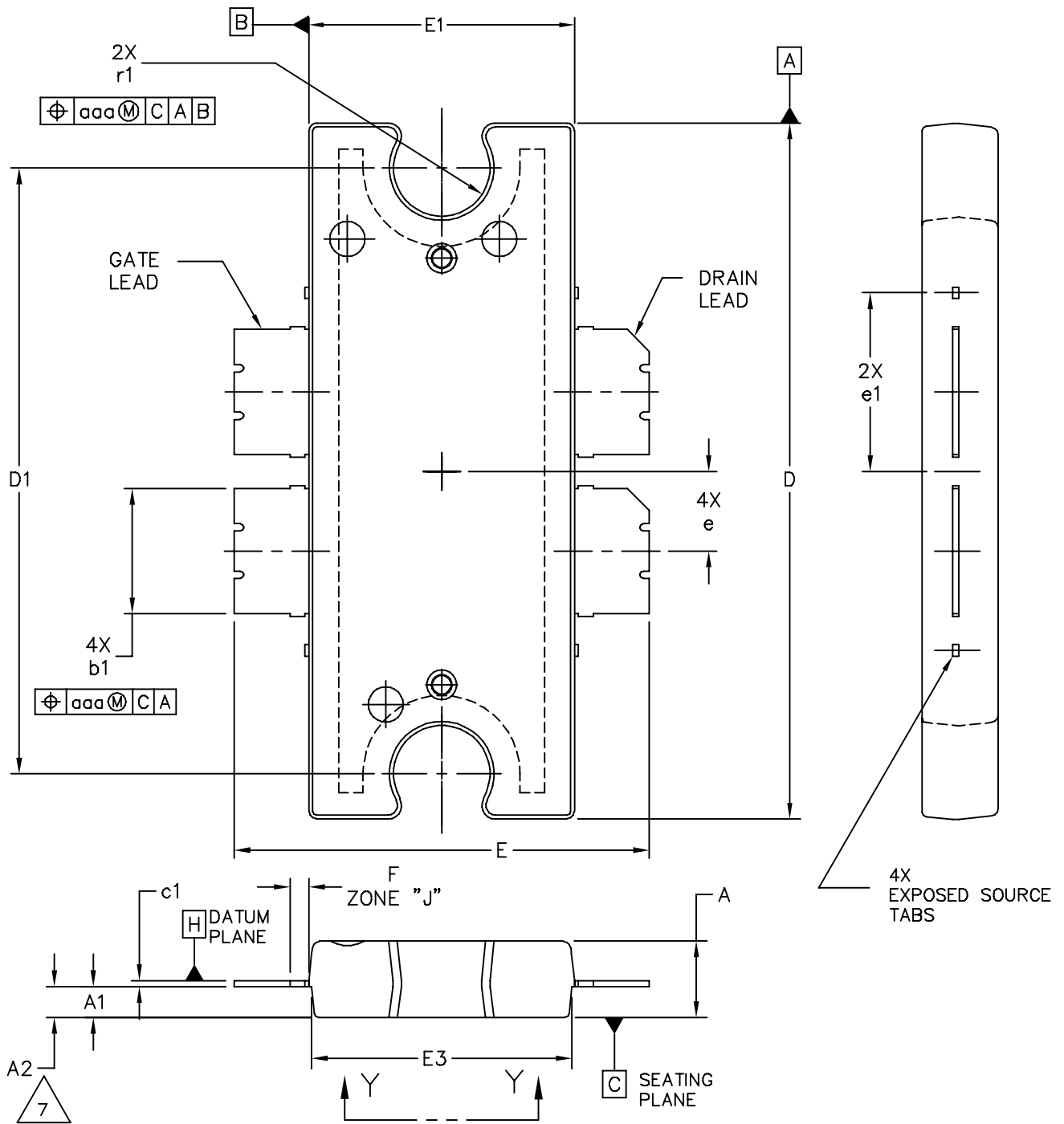
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.100	.104	2.54	2.64
A1	.039	.043	0.99	1.09
A2	.040	.042	1.02	1.07
D	.712	.720	18.08	18.29
D1	.688	.692	17.48	17.58
D2	.011	.019	0.28	0.48
D3	.600	---	15.24	---
E	.551	.559	14	14.2
E1	.353	.357	8.97	9.07
E2	.132	.140	3.35	3.56
E3	.124	.132	3.15	3.35
E4	.270	---	6.86	---
E5	.346	.350	8.79	8.89
F	.025 BSC		0.64 BSC	
b1	.164	.170	4.17	4.32
c1	.007	.011	0.18	0.28
e	.106 BSC		2.69 BSC	
aaa	.004		0.10	

## STYLE 1:

1. DRAIN
2. DRAIN
3. GATE
4. GATE
5. SOURCE

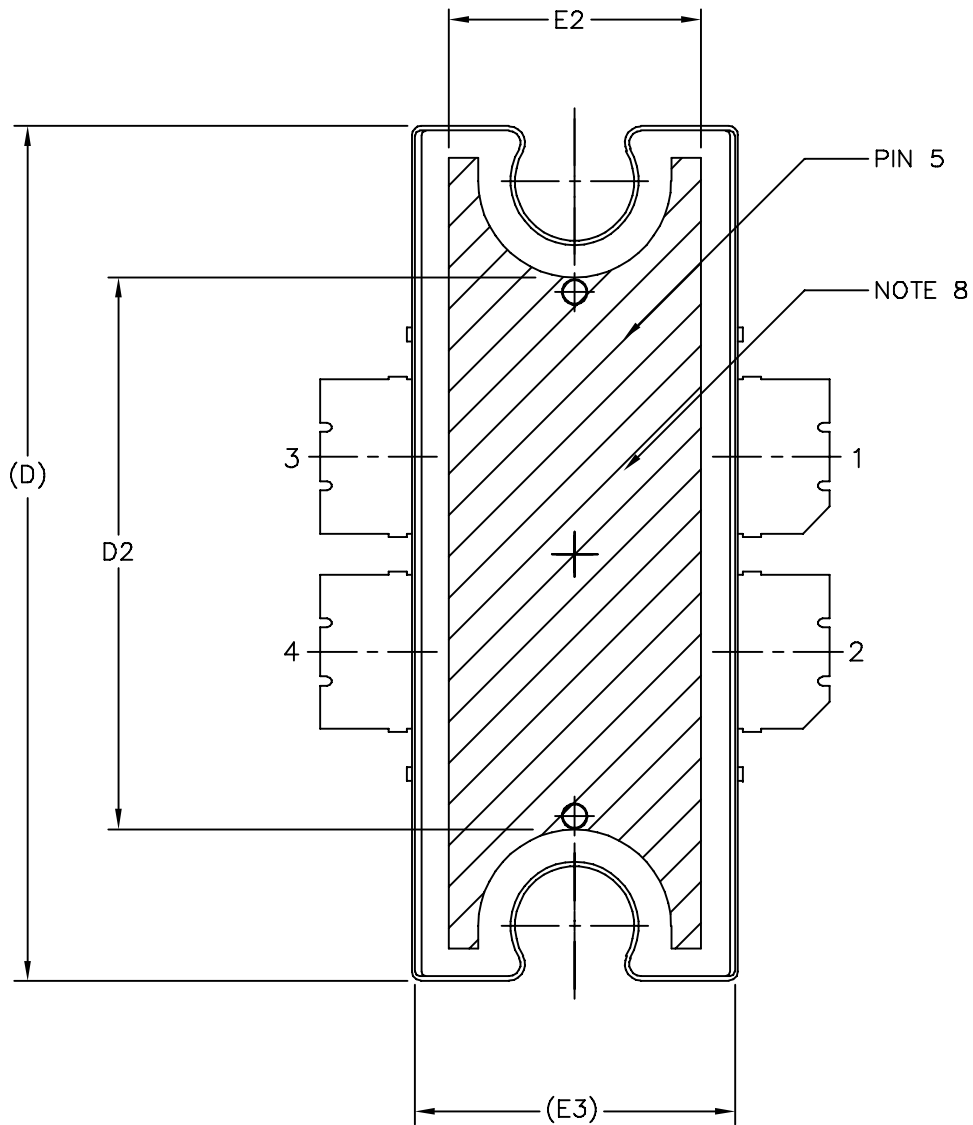
**CASE 1486-03  
ISSUE C  
TO-270 WB-4  
PLASTIC  
MRF6S18060MR1**





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TITLE:  TO-272 4 LEAD, WIDE BODY			DOCUMENT NO: 98ASA10575D		REV: D
			CASE NUMBER: 1484-04		05 APR 2006
			STANDARD: NON-JEDEC		

MRF6S18060MR1 MRF6S18060MBR1



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TITLE: TO-272 4 LEAD, WIDE BODY	DOCUMENT NO: 98ASA10575D	REV: D	
	CASE NUMBER: 1484-04	05 APR 2006	
	STANDARD: NON-JEDEC		

NOTES:

1. CONTROLLING DIMENSION: INCH
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M-1994.
3. DATUM PLANE H IS LOCATED AT THE TOP OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE TOP OF THE PARTING LINE.
4. DIMENSIONS "D" AND "E1" DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS .006 PER SIDE. DIMENSIONS "D" AND "E1" DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
5. DIMENSIONS "b1" DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE .005 TOTAL IN EXCESS OF THE "b1" DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. DATUM A AND B TO BE DETERMINED AT DATUM PLANE H.
7. DIMENSION A2 APPLIES WITHIN ZONE "J" ONLY.
8. HATCHING REPRESENTS EXPOSED AREA OF THE HEAT SLUG. HATCHED AREA SHOWN IS ON THE SAME PLANE.

STYLE 1:

PIN 1 - DRAIN      PIN 2 - DRAIN  
 PIN 3 - GATE      PIN 4 - GATE  
 PIN 5 - SOURCE

DIM	INCH		MILLIMETER		DIM	INCH		MILLIMETER	
	MIN	MAX	MIN	MAX		MIN	MAX	MIN	MAX
A	.100	.104	2.54	2.64	b1	.164	.170	4.17	4.32
A1	.039	.043	0.99	1.09	c1	.007	.011	.18	.28
A2	.040	.042	1.02	1.07	r1	.063	.068	1.60	1.73
D	.928	.932	23.57	23.67	e	.106 BSC		2.69 BSC	
D1	.810 BSC		20.57 BSC		e1	.239 INFO ONLY		6.07 INFO ONLY	
D2	.600	---	15.24	---	aaa	.004		.10	
E	.551	.559	14	14.2					
E1	.353	.357	8.97	9.07					
E2	.270	---	6.86	---					
E3	.346	.350	8.79	8.89					
F	.025 BSC		0.64 BSC						

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PRINT VERSION NOT TO SCALE

TITLE:

TO-272  
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DOCUMENT NO: 98ASA10575D

REV: D

CASE NUMBER: 1484-04

05 APR 2006

STANDARD: NON-JEDEC

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