To all our customers

Regarding the change of names mentioned in the document, such as Mitsubishi Electric and Mitsubishi XX, to Renesas Technology Corp.

The semiconductor operations of Hitachi and Mitsubishi Electric were transferred to Renesas Technology Corporation on April 1st 2003. These operations include microcomputer, logic, analog and discrete devices, and memory chips other than DRAMs (flash memory, SRAMs etc.) Accordingly, although Mitsubishi Electric, Mitsubishi Electric Corporation, Mitsubishi Semiconductors, and other Mitsubishi brand names are mentioned in the document, these names have in fact all been changed to Renesas Technology Corp. Thank you for your understanding. Except for our corporate trademark, logo and corporate statement, no changes whatsoever have been made to the contents of the document, and these changes do not constitute any alteration to the contents of the document itself.

Note : Mitsubishi Electric will continue the business operations of high frequency & optical devices and power devices.

EOL announced

Renesas Technology Corp.
Customer Support Dept.
April 1, 2003

Downloaded from Elcodis.com electronic components distributor

MITSUBISHI 8-BIT SINGLE-CHIP MICROCOMPUTER
740 FAMILY / 38000 SERIES

3819

User's Manual

Group

EOL announced

RENESAS
Renesas Technology Corp.

Downloaded from Elcodis.com electronic components distributor

keep safety first in your circuit designs !

- Mitsubishi Electric Corporation puts the maximum effort into making semiconductor products better and more reliable, but there is always the possibility that trouble may occur with them. Trouble with semiconductors may lead to personal injury, fire or property damage. Remember to give due consideration to safety when making your circuit designs, with appropriate measures such as (i) placement of substitutive, auxiliary circuits, (ii) use of non-flammable material or (iii) prevention against any malfunction or mishap.

Notes regarding these materials

- These materials are intended as a reference to assist our customers in the selection of the Mitsubishi semiconductor product best suited to the customer's application; they do not convey any license under any intellectual property rights, or any other rights, belonging to Mitsubishi Electric Corporation or a third party.

- Mitsubishi Electric Corporation assumes no responsibility for any damage, or infringement of any third-party's rights, originating in the use of any product data, diagrams, charts or circuit application examples contained in these materials.

- All information contained in these materials, including product data, diagrams and charts, represent information on products at the time of publication of these materials, and are subject to change by Mitsubishi Electric Corporation without notice due to product improvements or other reasons. It is therefore recommended that customers contact Mitsubishi Electric Corporation or an authorized Mitsubishi Semiconductor product distributor for the latest product information before purchasing a product listed herein.

- Mitsubishi Electric Corporation semiconductors are not designed or manufactured for use in a device or system that is used under circumstances in which human life is potentially at stake. Please contact Mitsubishi Electric Corporation or an authorized Mitsubishi Semiconductor product distributor when considering the use of a product contained herein for any specific purposes, such as apparatus or systems for transportation, vehicular, medical, aerospace, nuclear, or undersea repeater use.

- The prior written approval of Mitsubishi Electric Corporation is necessary to reprint or reproduce in whole or in part these materials.

- If these products or technologies are subject to the Japanese export control restrictions, they must be exported under a license from the Japanese government and cannot be imported into a country other than the approved destination.
  Any diversion or reexport contrary to the export control laws and regulations of JAPAN and/or the country of destination is prohibited.

- Please contact Mitsubishi Electric Corporation or an authorized Mitsubishi Semiconductor product distributor for further details on these materials or the products contained therein.

EOL announced

Downloaded from Elcodis.com electronic components distributor

Preface

This user's manual describes Mitsubishi's CMOS 8-bit microcomputers 3819 Group.
After reading this manual, the user should have a through knowledge of the functions and features of the 3819 Group, and should be able to fully utilize the product. The manual starts with specifications and ends with application examples.
For details of software, refer to the "740 Family Software MANUAL".

EOL announced

Downloaded from Elcodis.com electronic components distributor

BEFORE USING THIS USER'S MANUAL

This user's manual consists of the following three chapters. Refer to the chapter appropriate to your conditions, such as hardware design or software development.

1. Organization

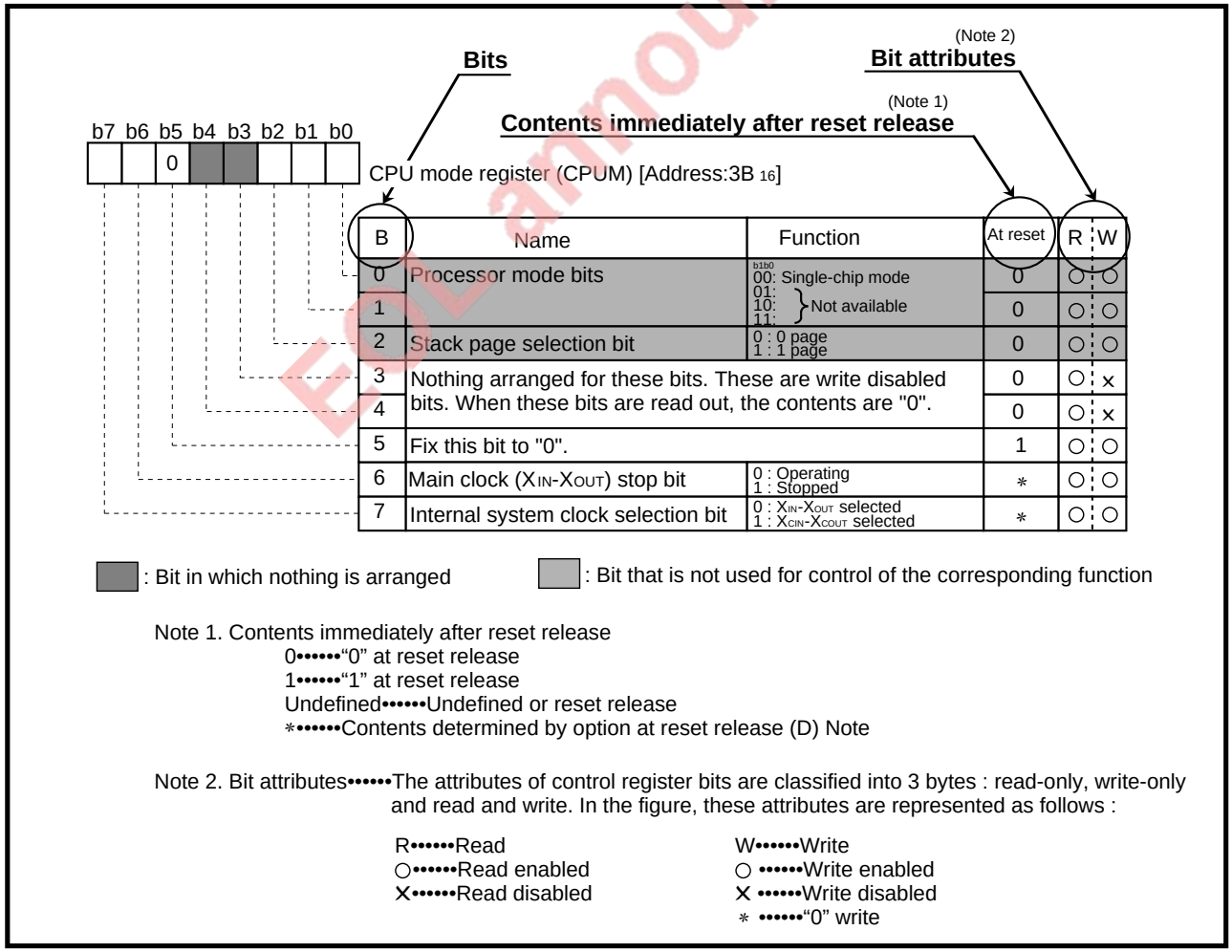
● CHAPTER 1 HARDWARE
This chapter describes features of the microcomputer, operation of each peripheral function and electric characteristics.

● CHAPTER 2 APPLICATION
This chapter describes usage and application examples of peripheral functions, based mainly on setting examples of related registers.

● CHAPTER 3 APPENDIX
This chapter includes precautions for systems development using the microcomputer, a list of control registers, the masking confirmation (mask ROM version), and mark specifications which are to be submitted when ordering.

2. Structure of register

The figure of each register structure describes its functions, contents at reset, and attributes as follows :



Note 1. Contents immediately after reset release
0••••••"0" at reset release
1••••••"1" at reset release
Undefined••••••Undefined or reset release
∗••••••Contents determined by option at reset release (D) Note

Note 2. Bit attributes••••••The attributes of control register bits are classified into 3 bytes : read-only, write-only and read and write. In the figure, these attributes are represented as follows :

R••••••Read
○••••••Read enabled
×••••••Read disabled

W••••••Write
○ ••••••Write enabled
× ••••••Write disabled
∗ ••••••"0" write

EOL announced

Downloaded from Elcodis.com electronic components distributor

Table of contents

CHAPTER 1. HARDWARE

EOL announced

Downloaded from Elcodis.com electronic components distributor

Table of contents

EOL announced

CHAPTER 2. APPLICATION

Downloaded from Elcodis.com electronic components distributor

CHAPTER 3. APPENDIX

Pre-announced

Downloaded from Elcodis.com electronic components distributor

List of figures

CHAPTER 1. HARDWARE

Not announced

Downloaded from Elcodis.com electronic components distributor

CHAPTER 2. APPLICATION

Not announced

Downloaded from Elcodis.com electronic components distributor

Table of contents

PCL announced

Downloaded from Elcodis.com electronic components distributor

Not recommended

Downloaded from Elcodis.com electronic components distributor

Table of contents

EOL announced

Downloaded from Elcodis.com electronic components distributor

List of tables

CHAPTER 1. HARDWARE

CHAPTER 2. APPLICATION

CHAPTER 3. APPENDIX

EOL announced

Downloaded from Elcodis.com electronic components distributor

CHAPTER 1

HARDWARE

EOL announced

Downloaded from Elcodis.com electronic components distributor

DESCRIPTION

The 3819 group is a 8-bit microcomputer based on the 740 family core technology.

The 3819 group has a flourescent display automatic display circuit and an 16-channel 8-bit A-D converter as additional functions.

The various microcomputers in the 3819 group include variations of internal memory size and packaging. For details, refer to the section on part numbering.

For details on availability of microcomputers in the 3819 group, refer to the section on group expansion.

FEATURES

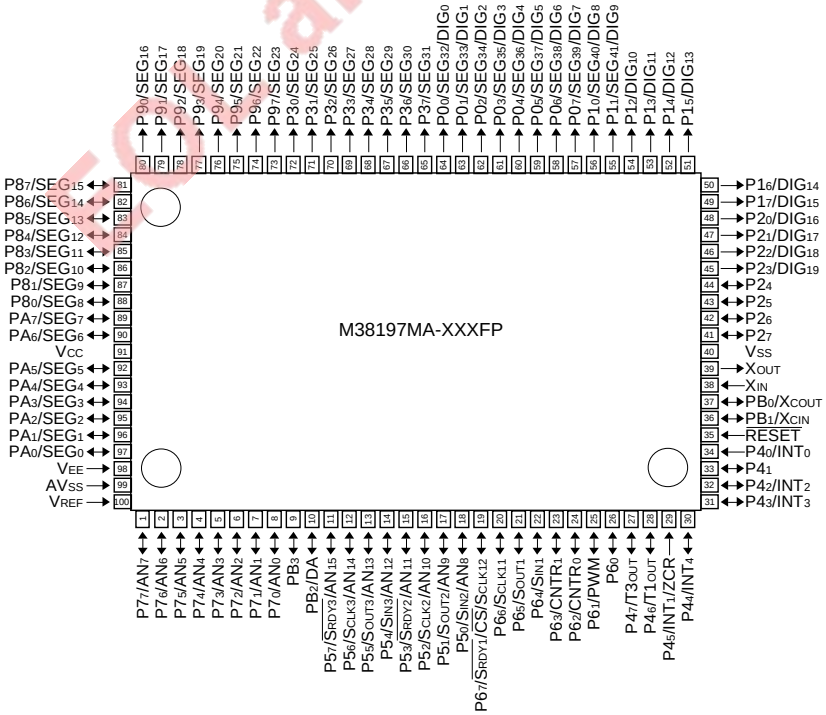
- Basic machine-language instructions 71
- The minimum instruction execution time ..... 0.48 µs
  (at 8.4 MHz oscillation frequency)
- Memory size .....
  ROM ..... 4K to 60 K bytes
  RAM ..... 192 to 2048 bytes
- Programmable input/output ports 54
- High-breakdown-voltage output ports 52
- Interrupts ..... 20 sources, 16 vectors
- Timers ..... 8-bit × 6
- Serial I/O (Serial I/O1 has an automatic transfer function)
  ..... 8-bit × 3(clock-synchronized)
- PWM output circuit ..... 8-bit × 1(also functions as timer 6)
- A-D converter ..... 8-bit × 16 channels
- D-A converter ..... 8-bit × 1 channels
- Zero cross detection input ..... 1 channel
- Fluorescent display function
  Segments ..... 16 to 42
  Digits ..... 6 to 16
- 2 Clock generating circuit
  Clock (X_{IN}-X_{OUT}) ..... Internal feedback resistor
  Sub-clock (X_{CIN}-X_{COUT}) ..... Without internal feedback resistor
  (connect to external ceramic resonator or quartz-crystal oscillator)
- Power source voltage
  In high-speed mode ..... 4.0 to 5.5 V
  (at 8.4 MHz oscillation frequency and high-speed selected)
  In middle-speed mode ..... 2.8 to 5.5 V
  (at 8.4 MHz oscillation frequency)
  In low-speed mode ..... 2.8 to 5.5 V
  (at 32 kHz oscillation frequency)
- Power dissipation
  In high-speed mode ..... 35 mW
  (at 8.4 MHz oscillation frequency)
  In low-speed mode ..... 60 µW
  (at 3 V power source voltage and 32 kHz oscillation frequency)
- Operating temperature range ..... –10 to 85°C

APPLICATION

Musical Instruments, household appliance, etc.

Discontinued

PIN CONFIGURATION (TOP VIEW)

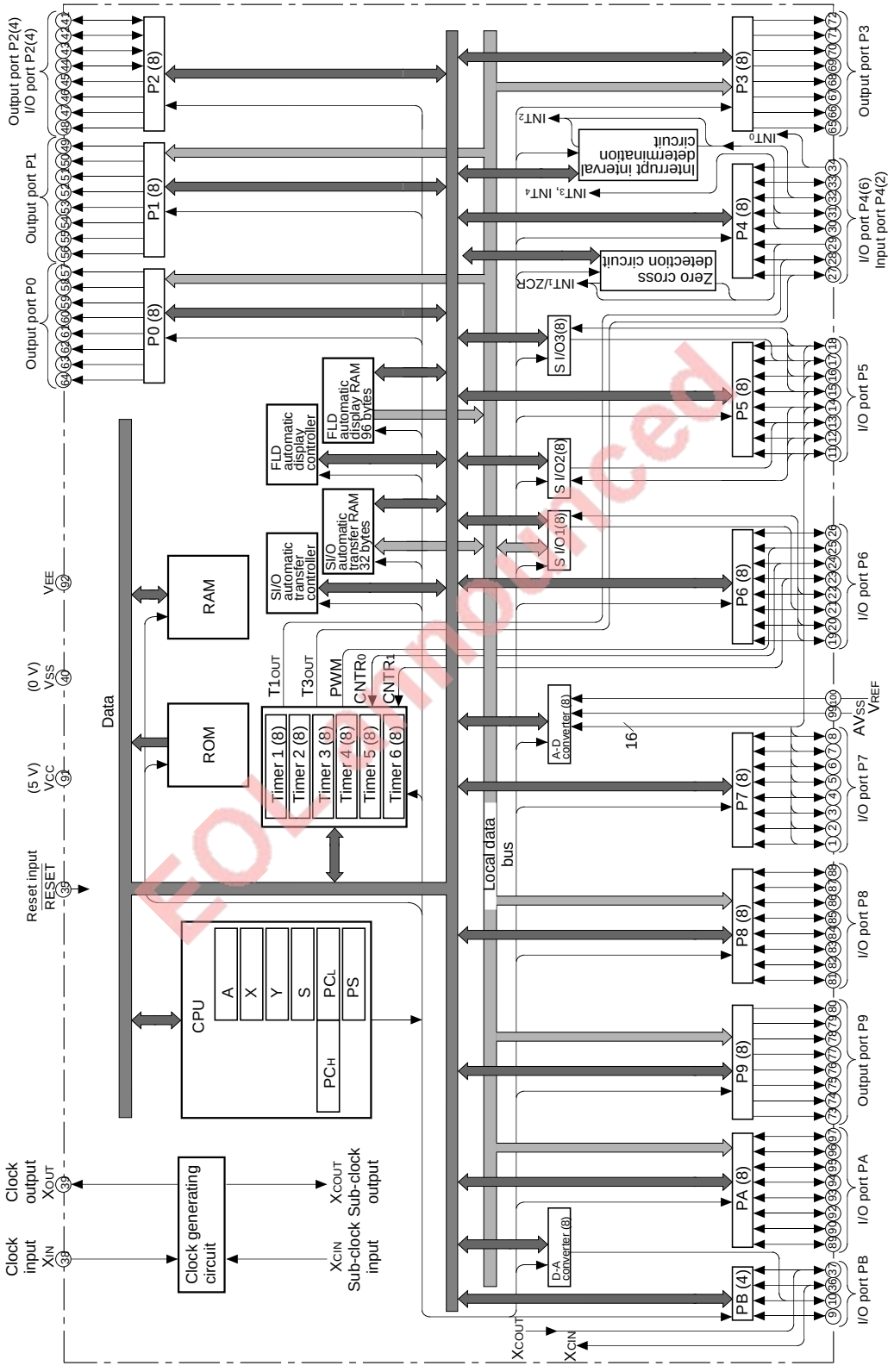


Package type : 100P6S-A
100-pin plastic-molded QFP

Renesas Technology Corp.

Downloaded from Elcodis.com electronic components distributor

FUNCTIONAL BLOCK DIAGRAM (Package : 100P6S-A)



Eol announced

Downloaded from Elcodis.com electronic components distributor

PIN DESCRIPTION

Pin	Name	Function	Function except a port function
V_{CC}, V_{SS}	Power source	•Apply voltage of 4.0 to 5.5 V to V_{CC}, and 0 V to V_{SS}.	
V_{EE}	Pull-down Power source	•Applies voltage supplied to pull-down resistors of ports P0, P1, $P2_0$–$P2_3$, P3, and P9.	
V_{REF}	Analog reference voltage	•Reference voltage input pin for A-D converter and D-A converter	
AV_{SS}	Analog power source	•GND input pin for A-D converter and D-A converter •Connect AV_{SS} to V_{SS}.	
$\overline{RESET}$	Reset input	•Reset input pin for active “L”	
X_{IN}	Clock input	•Input and output pins for the main clock generating circuit •Feedback resistor is built in between X_{IN} pin and X_{OUT} pin. •Connect a ceramic resonator or a quartz-crystal oscillator between the X_{IN} pin and X_{OUT} pin to set oscillation frequency. •If an external clock is used, connect the clock source to the X_{IN} pin and leave the X_{OUT} pin open. •This clock is used as the oscillating source of system clock.	
X_{OUT}	Clock output		
$P0_0$/SEG_{32}/ DIG_0–$P0_7$/ SEG_{39}/DIG_7	Output port P0	•8-bit output port •This port builds in pull-down resistor between port P0 and the V_{EE} pin. •At reset this port is set to V_{EE} level. •The high-breakdown-voltage P-channel open-drain	FLD automatic display pins
$P1_0$/SEG_{40}/ DIG_8–$P1_7$/ DIG_{15}	Output port P1	•8-bit output port with the same function as port P0	FLD automatic display pins
$P2_0$/DIG_{16}– $P2_3$/DIG_{19}	Output port P2	•4-bit output port with the same function as port P0	FLD automatic display pins
$P2_4$–$P2_7$	I/O port P2	•4-bit I/O port •I/O direction register allows each pin to be individually programmed as either input or output. •At reset this port is set to input mode. •TTL input level •CMOS 3-state output	
$P3_0$/SEG_{24}– $P3_7$/SEG_{31}	Output port P3	•8-bit output port with the same function as port P0	FLD automatic display pins
$P4_0$/INT_0, $P4_5$/INT_1/ ZCR	Input port P4	•2-bit input port •CMOS compatible input level	External interrupt input pins A zero cross detection circuit input pin ($P4_5$)
$P4_2$/INT_2– $P4_4$/INT_4	I/O port P4	•6-bit CMOS I/O port with the same function as ports $P2_4$–$P2_7$ •CMOS compatible input level •CMOS 3-state output	
$P4_1$			
$P4_6$/$T1_{OUT}$, $P4_7$/$T3_{OUT}$			Timer output pins

E.O.L announced

Downloaded from Elcodis.com electronic components distributor

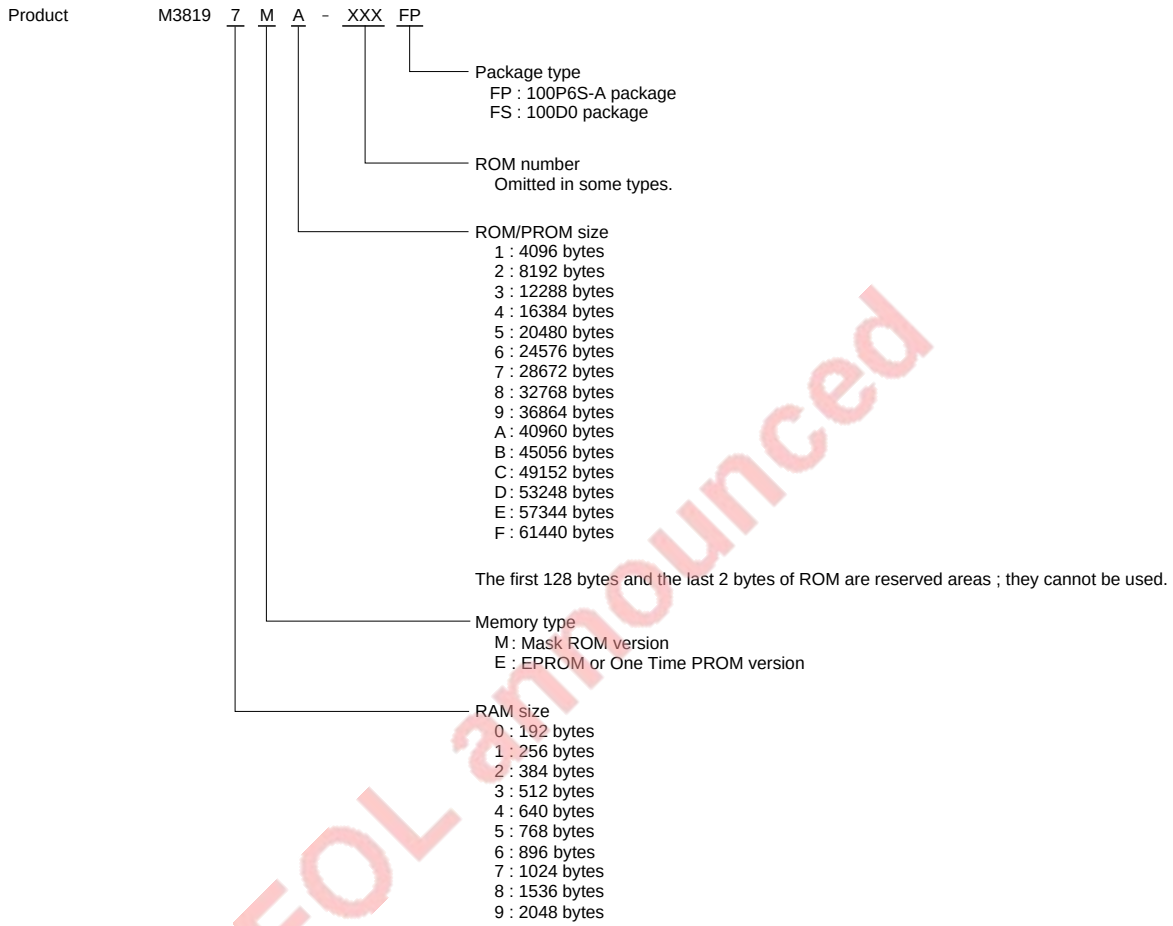
PIN DESCRIPTION (Continued)

Pin	Name	Function	Function except a port function
P5$_0$/SIN$_2$/AN$_8$, P5$_1$/SOUT$_2$/AN$_9$, P5$_2$/SCLK$_2$/AN$_{10}$, P5$_3$/SRDY$_2$/AN$_{11}$	I/O port P5	•8-bit CMOS I/O port with the same function as ports P2$_4$–P2$_7$ •CMOS compatible input level •CMOS 3-state output	Serial I/O2 function pins A-D conversion input pins
P5$_4$/SIN$_3$/AN$_{12}$, P5$_5$/SOUT$_3$/AN$_{13}$, P5$_6$/SCLK$_3$/AN$_{14}$, P5$_7$/SRDY$_3$/AN$_{15}$			Serial I/O3 function pins A-D conversion input pins
P6$_0$	I/O port P6	•8-bit CMOS I/O port with the same function as ports P2$_4$–P4$_7$ •CMOS compatible input level •CMOS 3-state output	
P6$_1$/PWM			PWM output pin (Timer output pin)
P6$_2$/CNTR$_0$, P6$_3$/CNTR$_1$			Timer input pins
P6$_4$/SIN$_1$, P6$_5$/SOUT$_1$, P6$_6$/SCLK$_{11}$, P6$_7$/SRDY$_1$/CS/ SCLK$_{12}$			Serial I/O1 function pins
P7$_0$/AN$_0$–P7$_7$/AN$_7$	I/O port P7	•8-bit CMOS I/O port with the same function as ports P2$_4$–P2$_7$ •CMOS compatible input level •CMOS 3-state output	A-D conversion input pins
P8$_0$/SEG$_8$–P8$_7$/SEG$_{15}$	I/O port P8	•8-bit I/O port with the same function as ports P2$_4$–P2$_7$ •CMOS compatible input level •The high-breakdown-voltage P-channel open-drain	FLD automatic display pins
P9$_0$/SEG$_{16}$–P9$_7$/SEG$_{23}$	Output port P9	•8-bit output port with the same function as port P0	
PA$_0$/SEG$_0$–PA$_7$/SEG$_7$	I/O port PA	•8-bit I/O port with the same function as ports P2$_4$–P2$_7$ •CMOS compatible input level •The high-breakdown voltage P-channel open-drain	
PB$_0$/XCOUT, PB$_1$/XCIN	I/O port PB	•4-bit CMOS I/O port with the same function as ports P2$_4$–P2$_7$ •CMOS compatible input level •CMOS 3-state output	I/O pins for sub-clock generating circuit (connect a ceramic resonator or a quarts-crystal oscillator)
PB$_2$/DA			D-A conversion output pin
PB$_3$			

EOL announced

Downloaded from Elcodis.com electronic components distributor

PART NUMBERING



EOL announced

Downloaded from Elcodis.com electronic components distributor

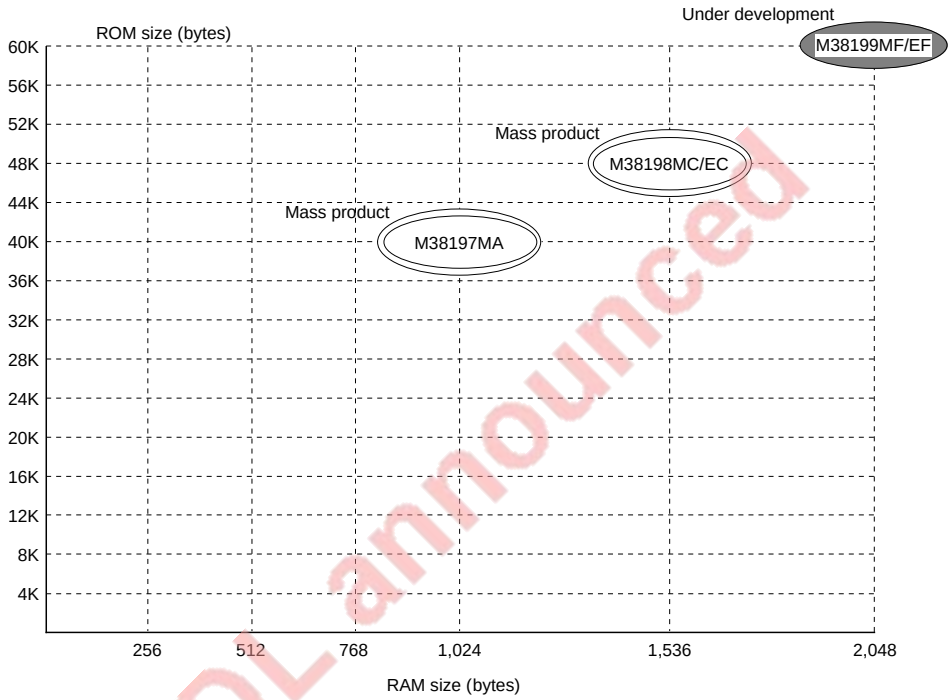
GROUP EXPANSION

Mitsubishi plans to expand the 3819 group as follows:

(1) Support for mask ROM, One Time PROM, and EPROM versions
ROM/PROM capacity ..... 40 K to 60 K bytes
RAM capacity ..... 1024 to 2048 bytes

(2) Packages
100P6S-A ..... 0.65 mm-pitch plastic molded QFP
100D0 ..... Ceramic LCC(built-in EPROM version)

Memory Expansion Plan



Products under development : the development schedule and specifications may be revised without notice.

Currently supported products are listed below. As of May 1996

Product	(P) ROM size (bytes) ROM size for User in ( )	RAM size (bytes)	Package	Remarks
M38197MA-XXXFP	40960 (40830)	1024	100P6S-A	Mask ROM version
M38197MA-XXXKP			100P6P-E	Mask ROM version
M38198MC-XXXKP				Mask ROM version
M38199MF-XXXKP				Mask ROM version
M38198MC-XXXFP	49152 (49022)	1536	100P6S-A	Mask ROM version
M38198EC-XXXFP				One Time PROM version
M38198ECFP				One Time PROM version (blank)
M38198ECFS			100D0	EPROM version
M38199MF-XXXFP	61440 (61310)	2048	100P6S-A	Mask ROM version
M38199EF-XXXFP				One Time PROM version
M38199EFFP				One Time PROM version (blank)
M38199EFFS			100D0	EPROM version

EOL announced

Downloaded from Elcodis.com electronic components distributor

FUNCTIONAL DESCRIPTION
Central Processing Unit (CPU)

The 3819 group uses the standard 740 family instruction set. Refer to the table of 740 family addressing modes and machine instructions or the 740 Family Software Manual for details on the instruction set.

Machine-resident 740 family instructions are as follows:

The FST, SLW instruction cannot be used.

The MUL, DIV, WIT and STP instruction can be used.

CPU Mode Register

The CPU mode register is allocated at address 003B16. The CPU mode register contains the stack page selection bit and the internal system clock selection bit.

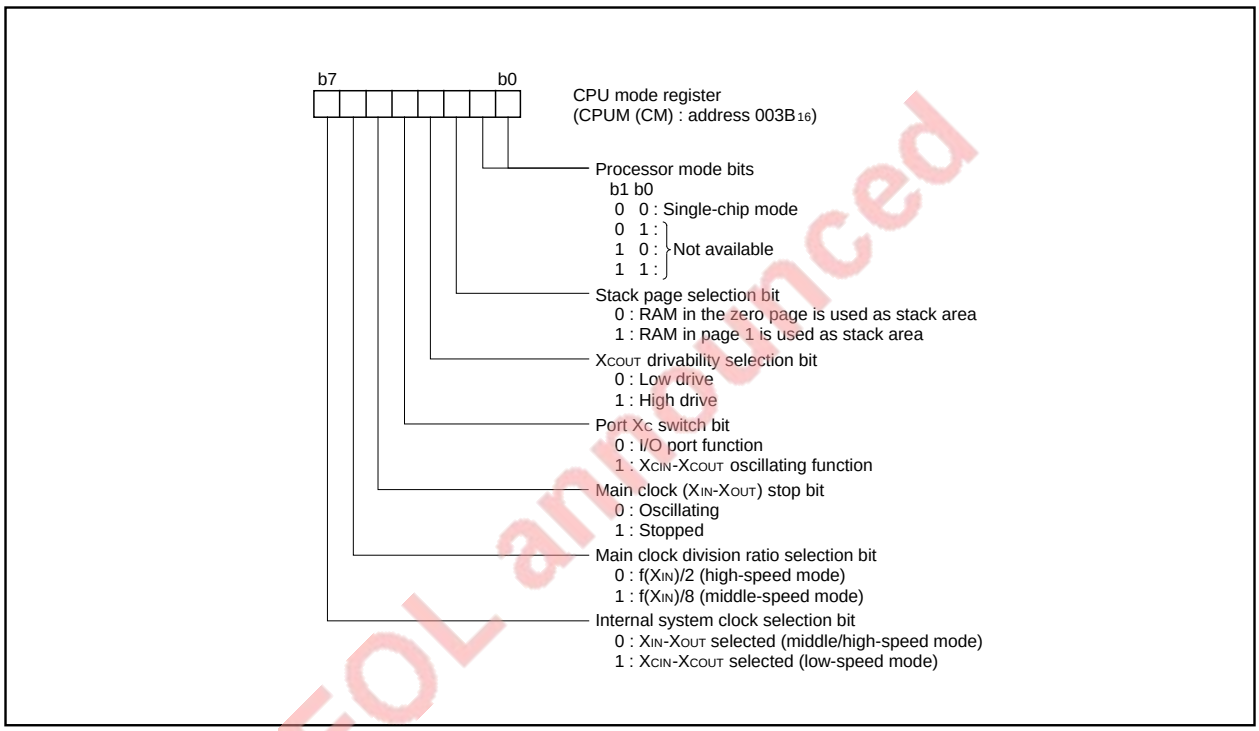


Fig. 1 Structure of CPU mode register

EOL announced

Downloaded from Elcodis.com electronic components distributor

Memory
Special function register (SFR) area
The special function register (SFR) area in the zero page contains control registers such as I/O ports and timers.

RAM
RAM is used for data storage and for stack area of subroutine calls and interrupts.

ROM
The first 128 bytes and the last 2 bytes of ROM are reserved for device testing and the reset is user area for storing programs.

Interrupt vector area
The interrupt vector area contains reset and interrupt vectors.

Zero page
The 256 bytes from addresses 0000_{16} to $00FF_{16}$ are called the zero page area. The internal RAM and the special function registers (SFR) are allocated to this area.
The zero page addressing mode can be used to specify memory and register addresses in the zero page area. Access to this area with only 2 bytes is possible in the zero page addressing mode.

Special page
The 256 bytes from addresses $FF00_{16}$ to $FFFF_{16}$ are called the special page area. The special page addressing mode can be used to specify memory addresses in the special page area. Access to this area with only 2 bytes is possible in the special page addressing mode.

EOL announced

RAM area

RAM capacity (bytes)	Address XXXX$_{16}$
192	00FF$_{16}$
256	013F$_{16}$
384	01BF$_{16}$
512	023F$_{16}$
640	02BF$_{16}$
768	033F$_{16}$
896	03BF$_{16}$
1024	043F$_{16}$
1536	063F$_{16}$
2048	083F$_{16}$

ROM area

ROM capacity (bytes)	Address YYYY$_{16}$	Address ZZZZ$_{16}$
4096	F000$_{16}$	F080$_{16}$
8192	E000$_{16}$	E080$_{16}$
12288	D000$_{16}$	D080$_{16}$
16384	C000$_{16}$	C080$_{16}$
20480	B000$_{16}$	B080$_{16}$
24576	A000$_{16}$	A080$_{16}$
28672	9000$_{16}$	9080$_{16}$
32768	8000$_{16}$	8080$_{16}$
36864	7000$_{16}$	7080$_{16}$
40960	6000$_{16}$	6080$_{16}$
45056	5000$_{16}$	5080$_{16}$
49152	4000$_{16}$	4080$_{16}$
53248	3000$_{16}$	3080$_{16}$
57344	2000$_{16}$	2080$_{16}$
61440	1000$_{16}$	1080$_{16}$

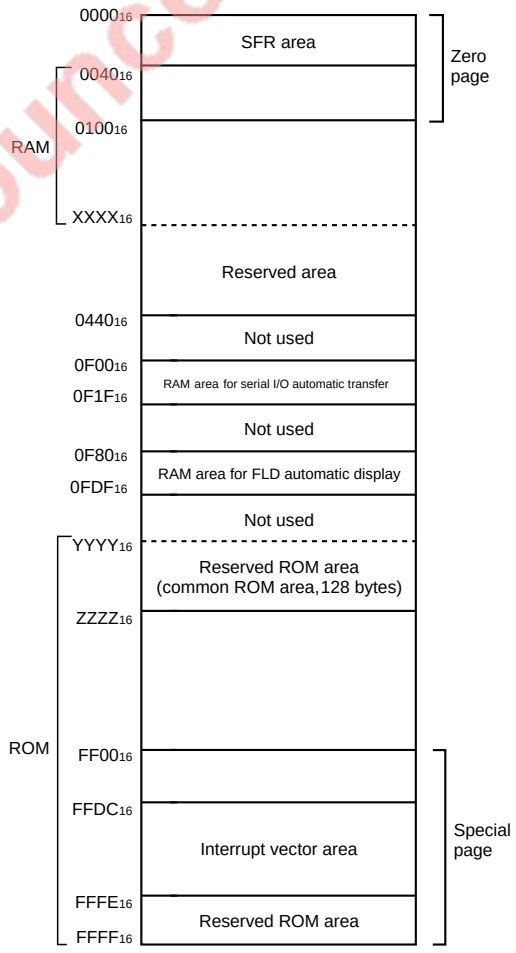


Fig. 2 Memory map

Downloaded from Elcodis.com electronic components distributor

0000₁₆	Port P0 (P0)
0001₁₆	
0002₁₆	Port P1 (P1)
0003₁₆	
0004₁₆	Port P2 (P2)
0005₁₆	Port P2 direction register (P2D)
0006₁₆	Port P3 (P3)
0007₁₆	
0008₁₆	Port P4 (P4)
0009₁₆	Port P4 direction register (P4D)
000A₁₆	Port P5 (P5)
000B₁₆	Port P5 direction register (P5D)
000C₁₆	Port P6 (P6)
000D₁₆	Port P6 direction register (P6D)
000E₁₆	Port P7 (P7)
000F₁₆	Port P7 direction register (P7D)
0010₁₆	Port P8 (P8)
0011₁₆	Port P8 direction register (P8D)
0012₁₆	Port P9 (P9)
0013₁₆	
0014₁₆	Port PA (PA)
0015₁₆	Port PA direction register (PAD)
0016₁₆	Port PB (PB)
0017₁₆	Port PB direction register (PBD)
0018₁₆	Serial I/O automatic transfer data pointer (SIODP)
0019₁₆	Serial I/O1 control register (SIO1CON)
001A₁₆	Serial I/O automatic transfer control register (SIOAC)
001B₁₆	Serial I/O1 register (SIO1)
001C₁₆	Serial I/O automatic transfer interval register (SIOAI)
001D₁₆	Serial I/O2 control register (SIO2CON)
001E₁₆	Serial I/O3 control register (SIO3CON)
001F₁₆	Serial I/O2 register (SIO2)

0020₁₆	Timer 1 (T1)
0021₁₆	Timer 2 (T2)
0022₁₆	Timer 3 (T3)
0023₁₆	Timer 4 (T4)
0024₁₆	Timer 5 (T5)
0025₁₆	Timer 6 (T6)
0026₁₆	Serial I/O3 register (SIO3)
0027₁₆	Timer 6 PWM register (T6PWM)
0028₁₆	Timer 12 mode register (T12M)
0029₁₆	Timer 34 mode register (T34M)
002A₁₆	Timer 56 mode register (T56M)
002B₁₆	D-A conversion register (DA)
002C₁₆	AD-DA control register (ADCON)
002D₁₆	A-D conversion register (AD)
002E₁₆	
002F₁₆	
0030₁₆	Interrupt interval determination register (IID)
0031₁₆	Interrupt interval determination control register (IIDCON)
0032₁₆	Port P0 segment/digit switch register (P0SDR)
0033₁₆	Port P2 digit/port switch register (P2DPR)
0034₁₆	Port P8 segment/port switch register (P8SPR)
0035₁₆	Port PA segment/port switch register (PASPR)
0036₁₆	FLDC mode register 1 (FLDM1)
0037₁₆	FLDC mode register 2 (FLDM2)
0038₁₆	FLD data pointer (FLDDP)
0039₁₆	Zero cross detection control register (ZCRCON)
003A₁₆	Interrupt edge selection register (INTEDGE)
003B₁₆	CPU mode register (CPUM)
003C₁₆	Interrupt request register 1 (IREQ1)
003D₁₆	Interrupt request register 2 (IREQ2)
003E₁₆	Interrupt control register 1 (ICON1)
003F₁₆	Interrupt control register 2 (ICON2)

Fig. 3 Memory map of special function register (SFR)

EOL announced

Downloaded from Elcodis.com electronic components distributor

I/O PORTS

Direction Registers

The 3819 group has 54 programmable I/O pins arranged in 8 I/O ports (ports $P2_4$–$P2_7$, $P4_1$–$P4_4$, $P4_6$, $P4_7$, P5–P8, PA, and PB). The I/O ports have direction registers which determine the input/output direction of each individual pin. Each bit in a direction register corresponds to one pin, each pin can be set to be input or output.

When "0" is written to the bit corresponding to a pin, that pin becomes an input pin. When "1" is written to that bit, that pin becomes an output pin.

If data is read from a pin which is set for output, the value of the port latch is read, not the value of the pin itself. A pin which is set for input the value of the pin itself is read because the pin is in floating state. If a pin set for input is written to, only the port latch is written to and the pin remains floating.

High-Breakdown-Voltage Output Ports

The 3819 group microprocessors have 7 ports with high-breakdown-voltage pins (ports P0, P1, $P2_0$–$P2_3$, P3, P8, P9, PA). The high-breakdown-voltage ports have P-channel open-drain output with V_{CC} –40 V of breakdown voltage.

Each pin in ports P0, P1, $P2_0$–$P2_3$, P3, and P9 has an internal pull-down resistor connected to V_{EE}. Ports P8 and PA have no internal pull-down resistors, so that connect an external resistor to each port. At reset, the P-channel output transistor of each port latch is turned off, so it becomes V_{EE} level ("L") by the pull-down resistor.

Writing "1" (weak drivability) to bit 7 of the FLDC mode register 1 (address 0036_{16}) shows the rising transition of the output transistors for reducing transient noise. At reset, bit 7 of the FLDC mode register 1 is set to "0" (strong drivability).

Pin	Name	Input/Output	I/O Format	Non-Port Function	Related SFRs	Diagram No.
$P0_0$/SEG_{32}/DIG_0–$P0_7$/SEG_{39}/DIG_7	Port P0	Output	High-breakdown-voltage P-channel open-drain output with pull-down resistor	FLD automatic display function	FLDC mode register 1 FLDC mode register 2 Port P0 segment/digit switch register	(1)
$P1_0$/SEG_{40}/DIG_8–$P1_7$/DIG_{15}	Port P1	Output	High-breakdown-voltage P-channel open-drain output with pull-down resistor	FLD automatic display function	FLDC mode register 1 FLDC mode register 2	(1) (2)
$P2_0$/DIG_{16}–$P2_3$/DIG_{19}	Port P2	Output	High-breakdown-voltage P-channel open-drain output with pull-down resistor	FLD automatic display function	FLDC mode register 1 FLDC mode register 2 Port P2 digit/port switch register	(3)
$P2_4$–$P2_7$		Input/output, individual bits	TTL level input CMOS 3-state output			(4)
$P3_0$/SEG_{24}–$P3_7$/SEG_{31}	Port P3	Output	High-breakdown-voltage P-channel open-drain output with pull-down resistor	FLD automatic display function	FLDC mode register 1 FLDC mode register 2	(5)
$P4_0$/INT_0 $P4_5$/INT_1/ZCR	Port P4	Input	CMOS compatible input level	External interrupt input Zero cross detection circuit input ($P4_5$)	Interrupt edge selection register Zero cross detection control register	(6)
$P4_2$/INT_2–$P4_4$/INT_4		Input/output, individual bits	CMOS compatible input level CMOS 3-state output			(7)
$P4_1$						(4)
$P4_6$/$T1_{OUT}$, $P4_7$/$T3_{OUT}$				Timer output	Timer 12 mode register Timer 34 mode register	(8)

EOL Announced

Downloaded from Elcodis.com electronic components distributor

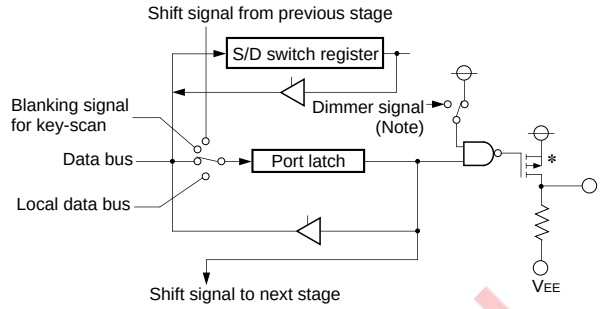
Pin	Name	Input/Output	I/O Format	Non-Port Function	Related SFRs	Diagram No.
P50/SIN2/AN8	Port P5	Input/output, individual bits	CMOS compatible input level CMOS 3-state output	Serial I/O2 function I/O A-D conversion input	Serial I/O2 control register AD/DA control register	(9)
P51/SOUT2/AN9, P52/SCLK2/AN10						(10)
P53/$\overline{\text{SRDY2}}$/AN11						(11)
P54/SIN3/AN12				Serial I/O3 function I/O A-D conversion input	Serial I/O3 control register AD/DA control register	(9)
P55/SOUT3/AN13, P56/SCLK3/AN14						(10)
P57/$\overline{\text{SRDY3}}$/AN15						(11)
P60	Port P6		CMOS compatible input level CMOS 3-state output			(4)
P61/PWM				PWM (timer) output	Timer 56 mode register	(8)
P62/CNTR0, P63/CNTR1				Timer input	Interrupt edge selection register	(7)
P64/SIN1				Serial I/O1 function I/O	Serial I/O1 control register Serial I/O automatic transfer control register	(9)
P65/SOUT1, P66/SCLK11						(10)
P67/$\overline{\text{SRDY1}}$/$\overline{\text{CS}}$/SCLK12						(11)
P70/AN0–P77/AN7	Port P7		CMOS compatible input level CMOS 3-state output	A-D conversion input	AD/DA control register	(12)
P80/SEG8–P87/SEG15	Port P8		CMOS compatible input level High-breakdown-voltage P-channel open-drain output with pull-down resistor	FLD automatic display function	FLDC mode register Segment/port switch register	(13)
P90/SEG16–P97/SEG23	Port P9	Output	High-breakdown-voltage P-channel open-drain output with pull-down resistor		FLDC mode register	(5)
PA0/SEG0–PA7/SEG7	Port PA	Input/output, individual bits	CMOS compatible input level High-breakdown-voltage P-channel open-drain output		FLDC mode register Segment/port switch register	(13)
PB0/XCOUT, PB1/XCIN	Port PB	Input/output, individual bits	CMOS compatible input level CMOS 3-state output	I/O for sub-clock generating circuit	CPU mode register	(14) (15)
PB2/DA				D-A conversion output	AD/DA control register	(16)
PB3						(4)

Note : Make sure that the input level at each pin is either 0 V or VCC during execution of the STP instruction. When an input level is at an intermediate potential, a current will flow from VCC to VSS through the input-stage gate.

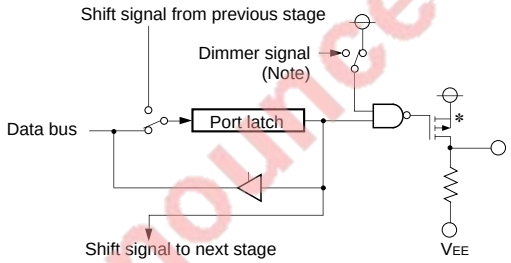
EOL announced

Downloaded from Elcodis.com electronic components distributor

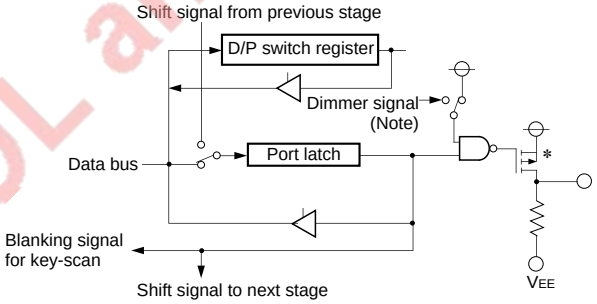
(1) Ports P0, P1$_0$, P1$_1$



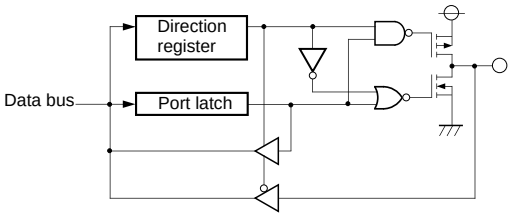
(2) Ports P1$_2$–P1$_7$



(3) Ports P2$_0$–P2$_3$



(4) Ports P2$_4$–P2$_7$, P4$_1$, P6$_0$, PB$_3$



∗ : High-breakdown-voltage P-channel transistor

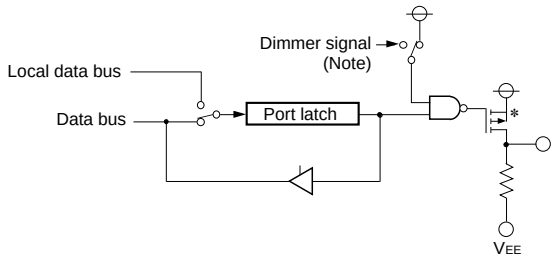
Note: The dimmer signal sets the Toff timing.

Fig. 4 Port block diagram (1)

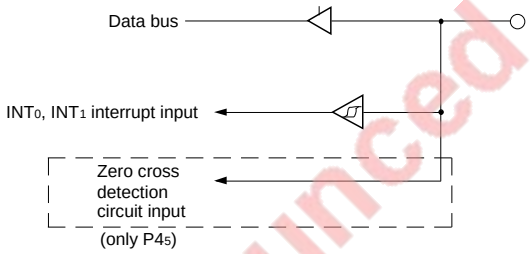
EOL announced

Downloaded from Elcodis.com electronic components distributor

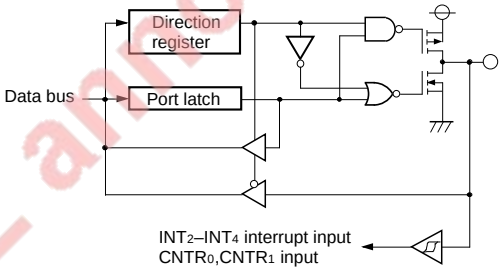
(5) Ports P3, P9



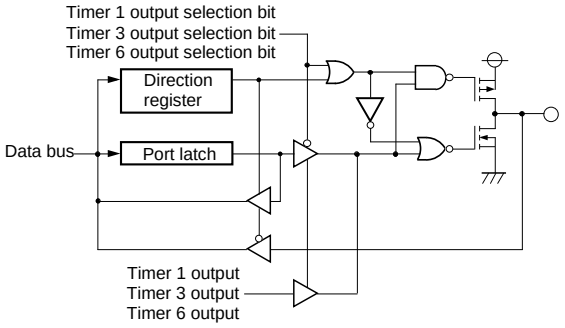
(6) Ports $P4_0$, $P4_5$



(7) Ports $P4_2$–$P4_4$, $P6_2$, $P6_3$



(8) Ports $P4_6$, $P4_7$, $P6_1$



✻ : High-breakdown-voltage P-channel transistor

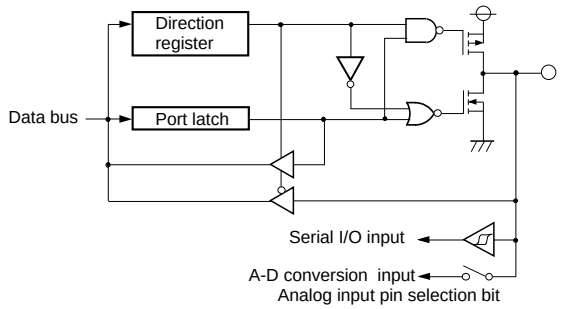
Note: The dimmer signal sets the Toff timing.

Fig. 5 Port block diagram (2)

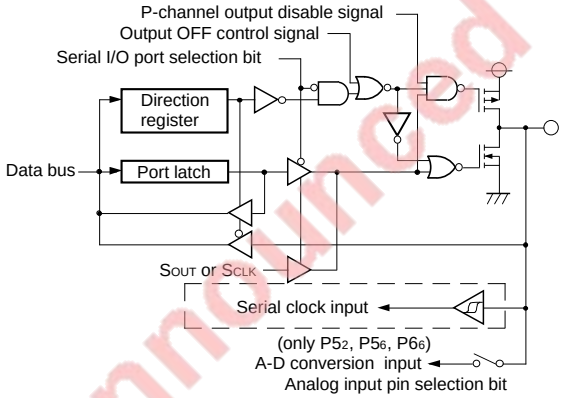
EOL announced

Downloaded from Elcodis.com electronic components distributor

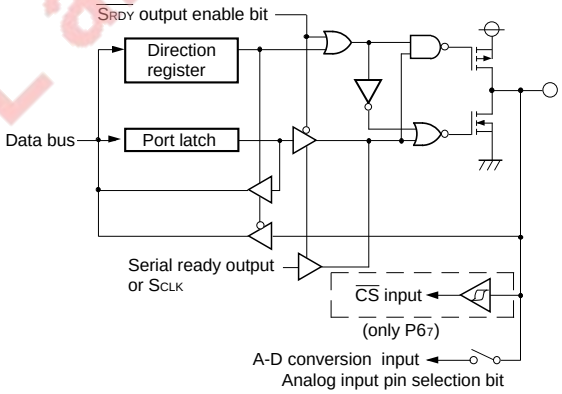
(9) Ports $P5_0$, $P5_4$, $P6_4$



(10) Ports $P5_1$, $P5_2$, $P5_5$, $P5_6$, $P6_5$, $P6_6$



(11) Ports $P5_3$, $P5_7$, $P6_7$



(12) Port P7

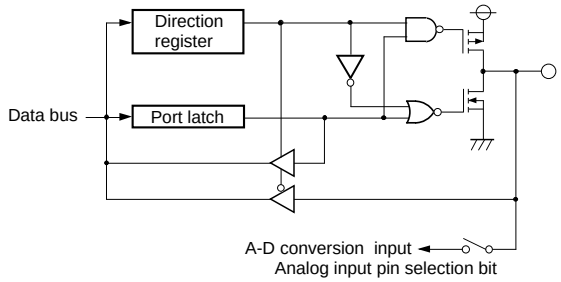
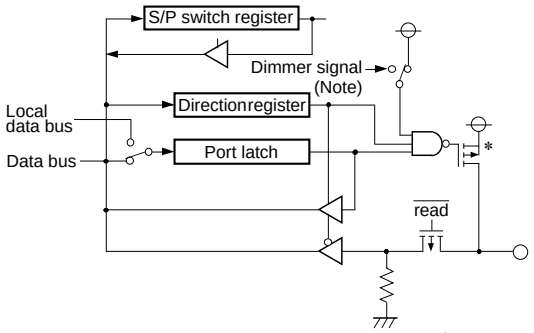


Fig. 6 Port block diagram (3)

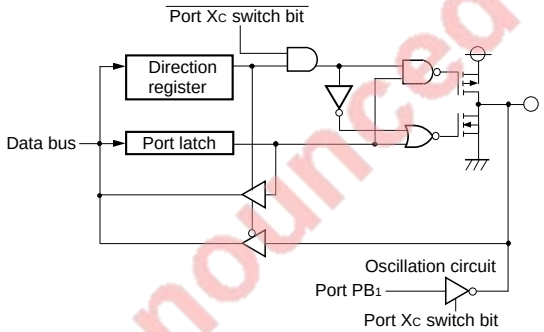
EOL announced

Downloaded from Elcodis.com electronic components distributor

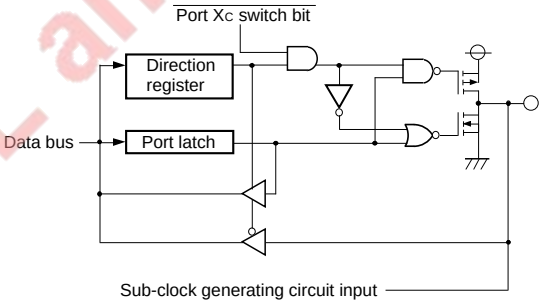
(13) Ports P8, PA



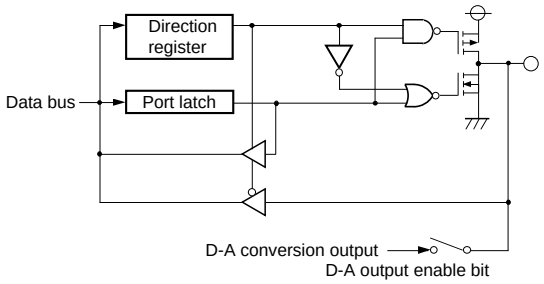
(14) Port PB_0



(15) Port PB_1



(16) Port PB_2



∗ : High-breakdown-voltage P-channel transistor

Note: The dimmer signal sets the Toff timing.

Fig. 7 Port block diagram (4)

EOL announced

Downloaded from Elcodis.com electronic components distributor

INTERRUPTS

Interrupts occur by 20 sources: 5 external, 14 internal, and 1 software.

Interrupt Control

Each interrupt is controlled by an interrupt request bit, an interrupt enable bit, and the interrupt disable flag except for the software interrupt set by the BRK instruction. An interrupt occurs if the corresponding interrupt request and enable bits are "1" and the interrupt disable flag is "0".

Interrupt enable bits can be set or cleared by software.

Interrupt request bits can be cleared by software, but cannot be set by software.

The BRK instruction cannot be disabled with any flag or bit.

The I (interrupt disable) flag disables all interrupts except the BRK instruction interrupt.

Interrupt Operation

When an interrupt is received, the contents of the program counter and processor status register are automatically stored into the stack. The interrupt disable flag is set to inhibit other interrupts from interfering. The corresponding interrupt request bit is cleared and the interrupt jump destination address is read from the vector table into the program counter.

Notes on Use

When the active edge of an external interrupt (INT_0 to INT_4) is changed or when switching interrupt sources in the same vector address, the corresponding interrupt request bit may also be set. Therefore, please take following sequence;

(1) Disable the external interrupt which is selected.

(2) Change the active edge.

(3) Clear the interrupt request bit which is selected to "0".

(4) Enable the external interrupt which is selected.

Table 1. Interrupt vector addresses and priority

Interrupt Source	Priority	Vector Addresses (Note 1)		Interrupt Request Generating Conditions	Remarks
		High	Low		
Reset (Note 2)	1	$FFFD_{16}$	$FFFC_{16}$	At reset	Non-maskable
INT_0	2	$FFFB_{16}$	$FFFA_{16}$	At detection of either rising or falling edge of INT_0 input	External interrupt (active edge selectable)
INT_1/ZCR	3	$FFF9_{16}$	$FFF8_{16}$	At detection of either rising or falling edge of INT_1/ZCR input	External interrupt (active edge selectable)
INT_2	4	$FFF7_{16}$	$FFF6_{16}$	At detection of either rising or falling edge of INT_2 input	External interrupt (active edge selectable)
Remote control/ counter overflow				At 8-bit counter overflow	Valid when interrupt interval determination is operating
Serial I/O1	5	$FFF5_{16}$	$FFF4_{16}$	At completion of data transfer	Valid when serial I/O ordinary mode is selected
Serial I/O automatic transfer				At completion of the last data transfer	Valid when serial I/O automatic transfer mode is selected
Serial I/O2	6	$FFF3_{16}$	$FFF2_{16}$	At completion of data transfer	Valid when serial I/O2 is selected
Serial I/O3	7	$FFF1_{16}$	$FFF0_{16}$	At completion of data transfer	Valid when serial I/O3 is selected
Timer 1	8	$FFEF_{16}$	$FFEE_{16}$	At timer 1 underflow	STP release timer underflow
Timer 2	9	$FFED_{16}$	$FFEC_{16}$	At timer 2 underflow	
Timer 3	10	$FFEB_{16}$	$FFEA_{16}$	At timer 3 underflow	
Timer 4	11	$FFE9_{16}$	$FFE8_{16}$	At timer 4 underflow	
Timer 5	12	$FFE7_{16}$	$FFE6_{16}$	At timer 5 underflow	
Timer 6	13	$FFE5_{16}$	$FFE4_{16}$	At timer 6 underflow	
INT_3	14	$FFE3_{16}$	$FFE2_{16}$	At detection of either rising or falling edge of INT_3 input	External interrupt (active edge selectable)
INT_4	15	$FFE1_{16}$	$FFE0_{16}$	At detection of either rising or falling edge of INT_4 input	Valid when INT_4 interrupt is selected External interrupt (active edge selectable)
A-D conversion				At completion of A-D conversion	Valid when A-D conversion interrupt is selected
FLD blanking	16	$FFDF_{16}$	$FFDE_{16}$	At falling edge of the last digit immediately before blanking period starts	Valid when FLD blanking interrupt is selected
FLD digit				At rising edge of each digit	Valid when FLD digit interrupt is selected
BRK instruction	17	$FFDD_{16}$	$FFDC_{16}$	At BRK instruction execution	Non-maskable software interrupt

Notes 1 : Vector addresses contain interrupt jump destination addresses.
2 : Reset function in the same way as an interrupt with the highest priority.

EOL announced

Downloaded from Elcodis.com electronic components distributor

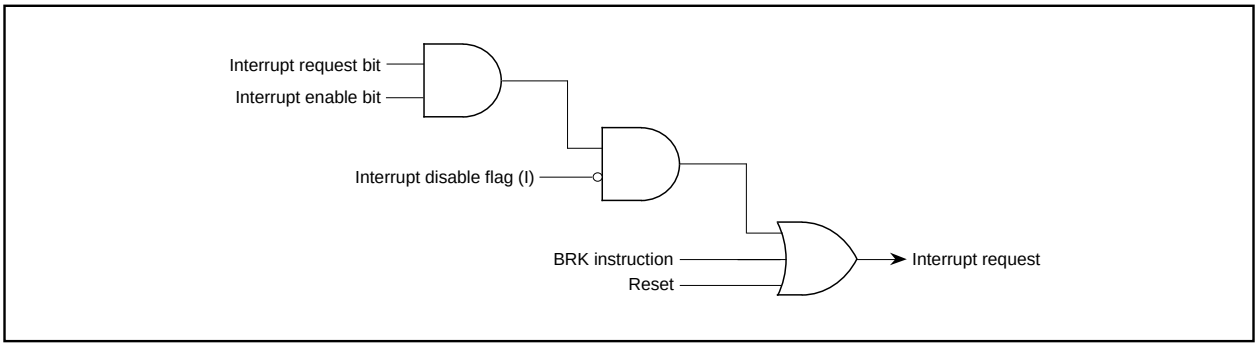


Fig. 8 Interrupt control

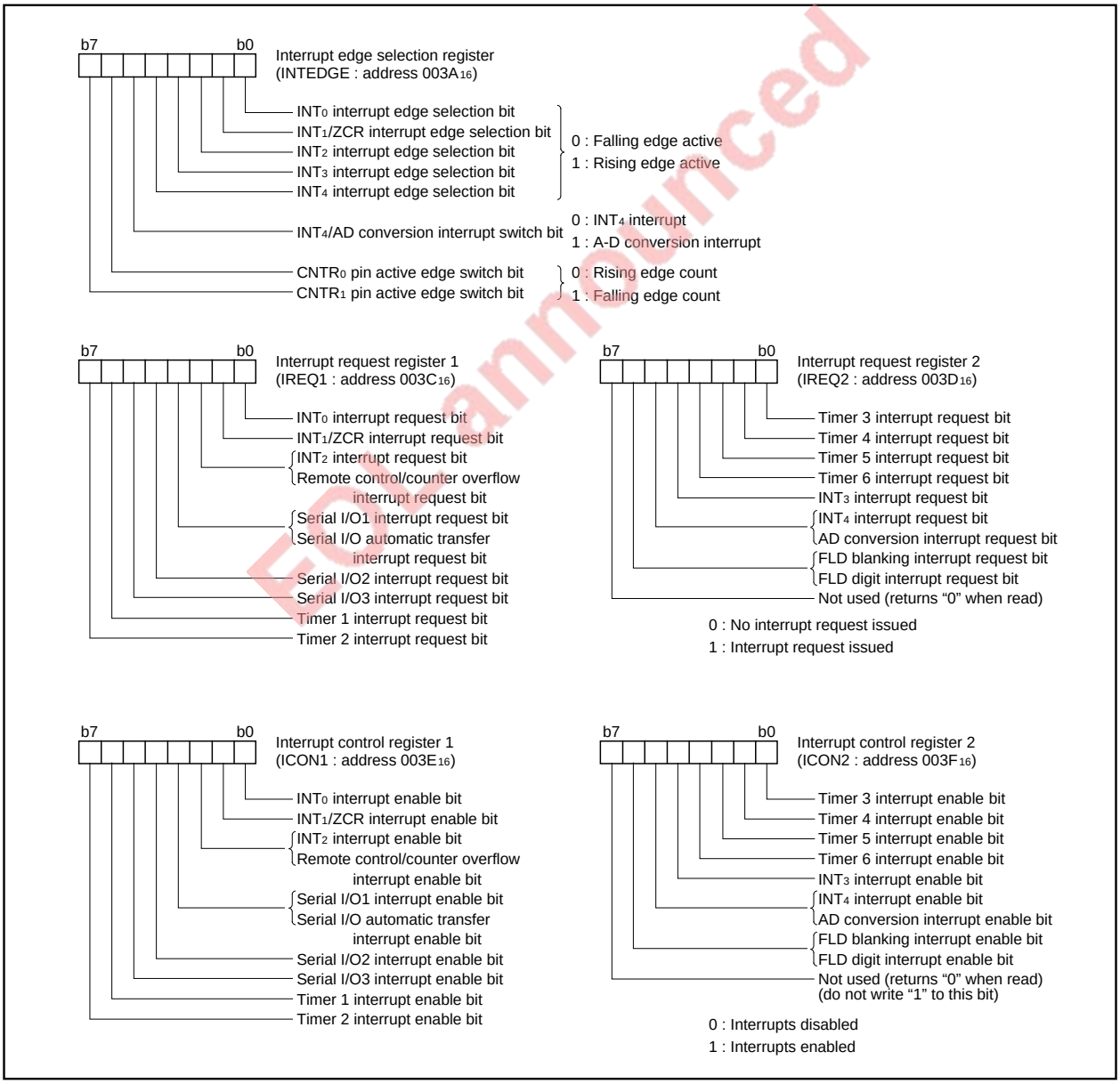


Fig. 9 Structure of interrupt-related registers

Renesas Technology Corp.

Downloaded from Elcodis.com electronic components distributor

TIMERS

The 3819 group has 6 built-in timers: timer 1, timer 2, timer 3, timer 4, timer 5, and timer 6.

Each timer has the 8-bit timer latch. The timers count down.

Once a timer reaches 00_{16}, at the next count pulse the contents of each timer latch is loaded into the corresponding timer, and sets the corresponding interrupt request bit to "1".

The count can be stopped by setting the stop bit of each timer to "1". The internal clock ϕ can be set to either the high-speed mode or low-speed mode with the CPU mode register. At the same time, timer internal count source is switched to either f(XIN) or f(XCIN).

Timer 1 and Timer 2

The count sources of timer 1 and timer 2 can be selected by setting the timer 12 mode register. A rectangular waveform of timer 1 underflow signal divided by 2 is output from the $P4_6$/T1OUT pin. The waveform polarity changes each time timer 1 overflows. The active edge of the external clock $CNTR_0$ can be switched with the bit 6 of the interrupt edge selection register.

At reset or when executing the STP instruction, all bits of the timer 12 mode register are cleared to "0", timer 1 is set to "FF_{16}", and timer 2 is set to "01_{16}".

Timer 3 and Timer 4

The count sources of timer 3 and timer 4 can be selected by setting the timer 34 mode register. A rectangular waveform of timer 3 underflow signal divided by 2 is output from the $P4_7$/T3OUT pin. The waveform polarity changes each time timer 3 overflows.

The active edge of the external clock $CNTR_1$ can be switched with the bit 7 of the interrupt edge selection register.

Timer 5 and Timer 6

The count sources of timer 5 and timer 6 can be selected by setting the timer 56 mode register.

A rectangular waveform of timer 6 underflow signal divided by 2 is output from the $P6_1$/PWM pin. The waveform polarity changes each time timer 6 overflows.

Timer 6 PWM Mode

Timer 6 can output a rectangular waveform with duty cycle n/(n + m) from the $P6_1$/PWM pin by setting the timer 56 mode register (refer to fig. 12). The n is the value set in timer 6 latch (address 0025_{16}) and m is the value in the timer 6 PWM register (address 0027_{16}). If n is "0", the PWM output is "L", if m is "0", the PWM output is "H"(n=0 is prior than m=0). In the PWM mode, interrupts occur at the rising edge of the PWM output.

EOL announced

Downloaded from Elcodis.com electronic components distributor

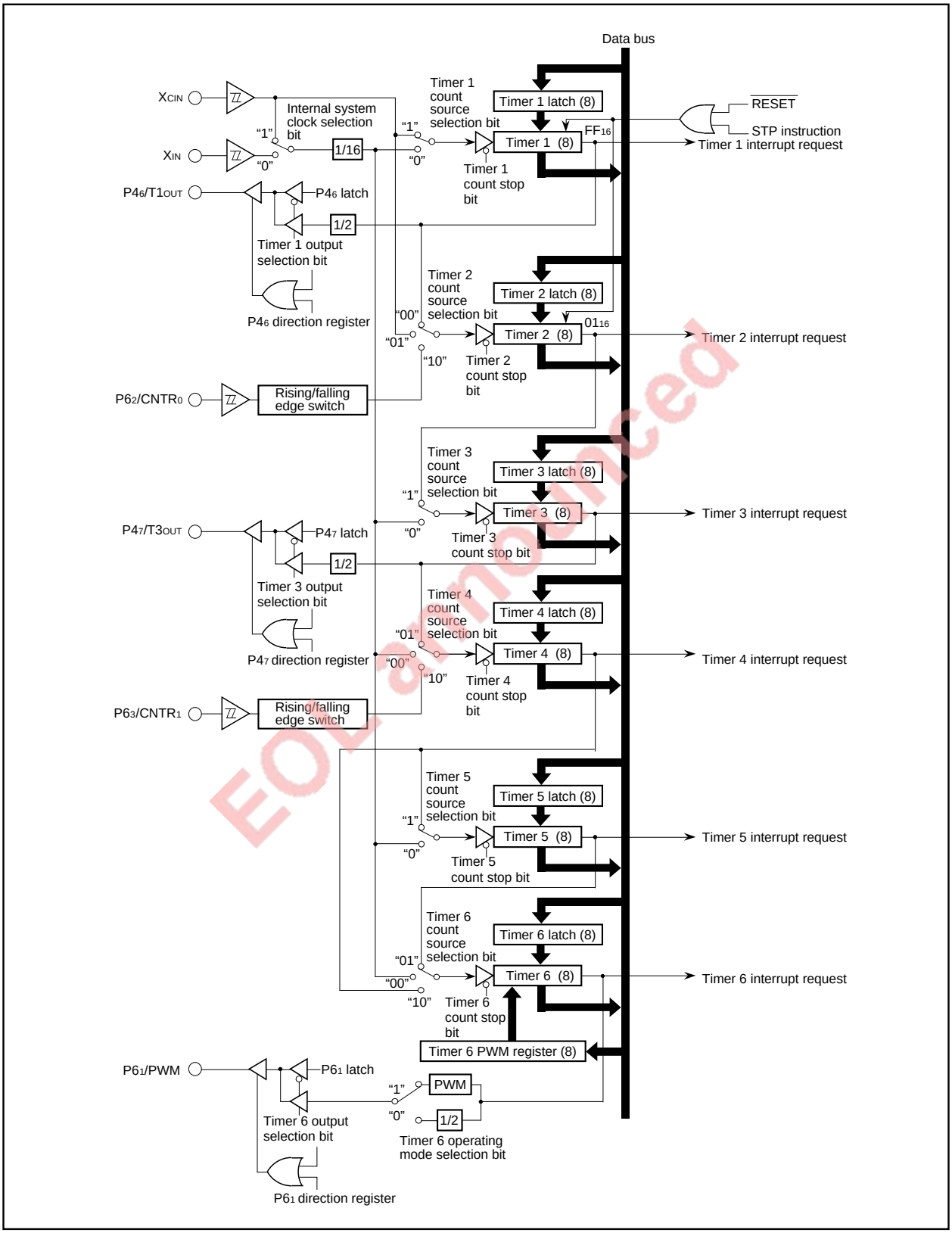


Fig. 10 Timer block diagram

EOL announced

Downloaded from Elcodis.com electronic components distributor

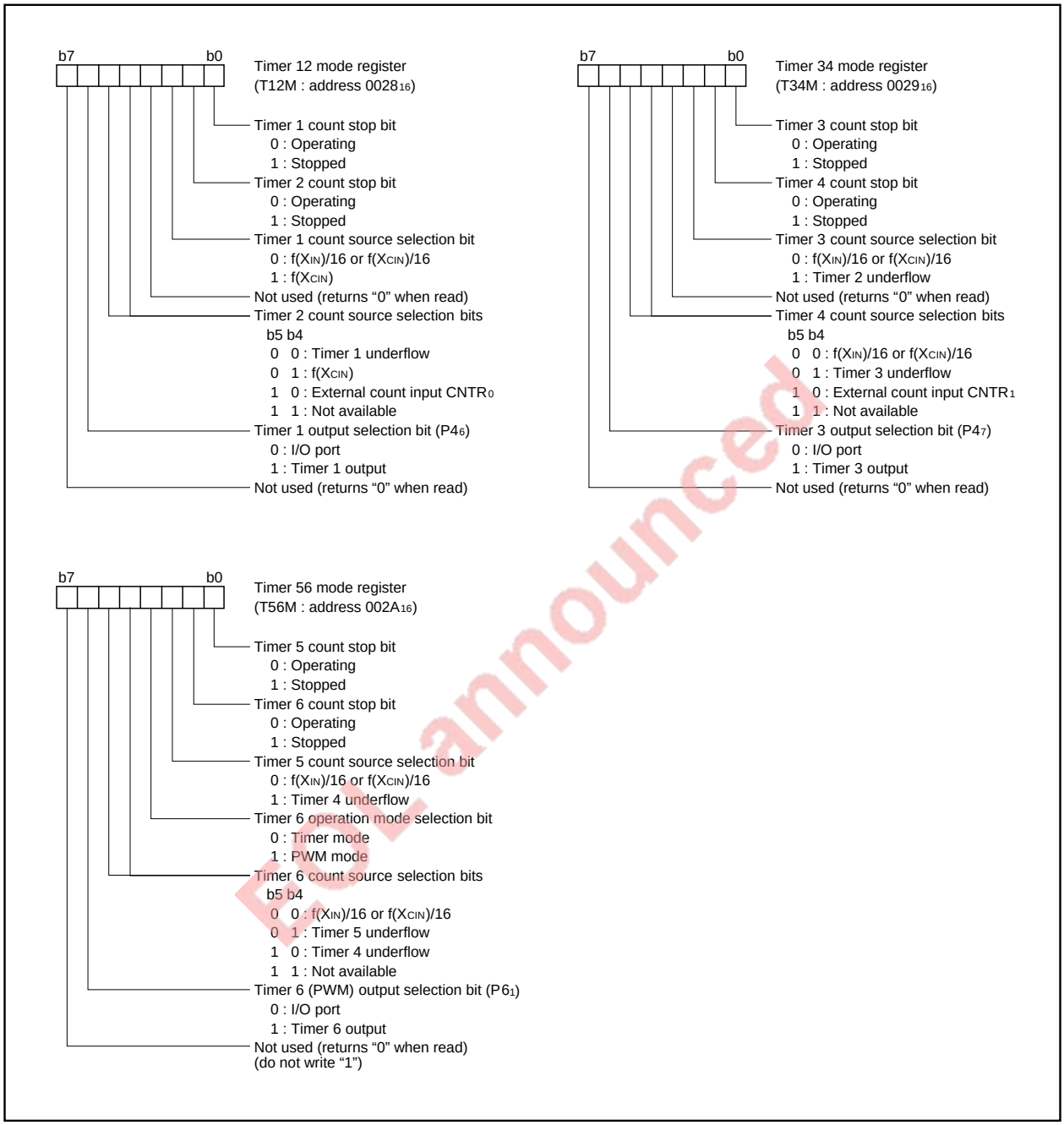
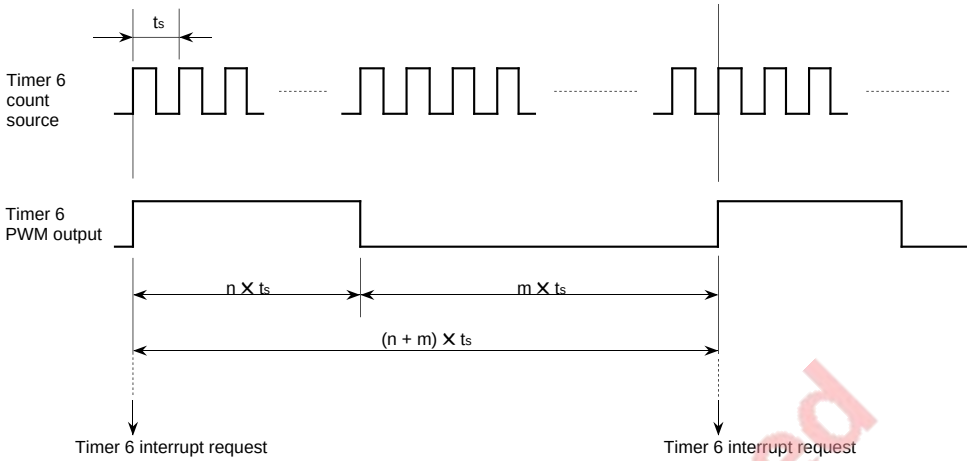


Fig. 11 Structure of timer-related registers

For announced

Downloaded from Elcodis.com electronic components distributor



Note: If the value set in timer 6 is n and the value set in the timer 6 PWM register is m, a PWM waveform with duty cycle n/(n + m) and period (n + m) 5 ts (ts : the frequency of the timer 6 count source) is output.

Fig. 12 Timing in timer 6 PWM mode

EOL announced

Downloaded from Elcodis.com electronic components distributor

SERIAL I/O

The 3819 group has built-in 8-bit clock synchronized serial I/O × 3 channels (serial I/O1, serial I/O2, and serial I/O3).

Serial I/O1 builds in the automatic transfer function. The function can be switched to the serial I/O ordinary mode with the serial I/O automatic transfer control register (address $001A_{16}$).

Serial I/O2 and Serial I/O3 can be used only in the serial I/O ordinary mode.

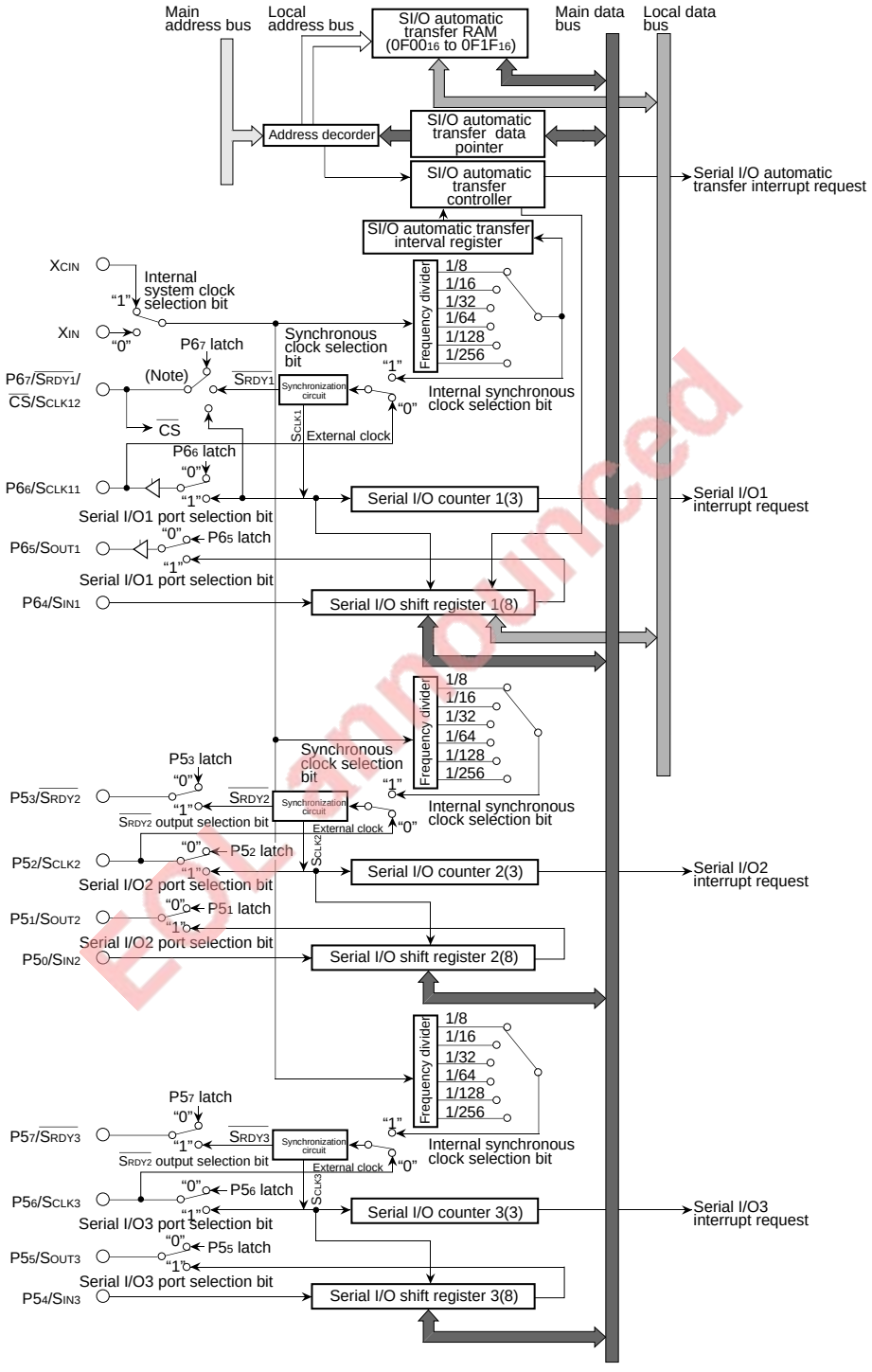
The I/O pins of the serial I/O function are also used as I/O ports P5 and $P6_4$–$P6_7$, and their operation is selected with the serial I/O control registers (addresses 0019_{16}, $001D_{16}$, and $001E_{16}$).

Serial I/O Control Registers (SIO1CON, SIO2CON, SIO3CON) 0019_{16}, $001D_{16}$, $001E_{16}$

Each of the serial I/O control registers (addresses 0019_{16}, $001D_{16}$, and $001E_{16}$) consists of 8 selection bits which control the serial I/O function.

EOL announced

Downloaded from Elcodis.com electronic components distributor



Note: Selected with the synchronous clock selection bit, $\overline{SRDY1}$ output selection bit, serial I/O1 port selection bit (these 3 bits are of the serial I/O1 control register), automatic transfer control bit, and synchronous clock output pin selection bit (these 2 bits are ofthe serial I/O automatic transfer register).

Fig. 13 Serial I/O block diagram

Downloaded from Elcodis.com electronic components distributor

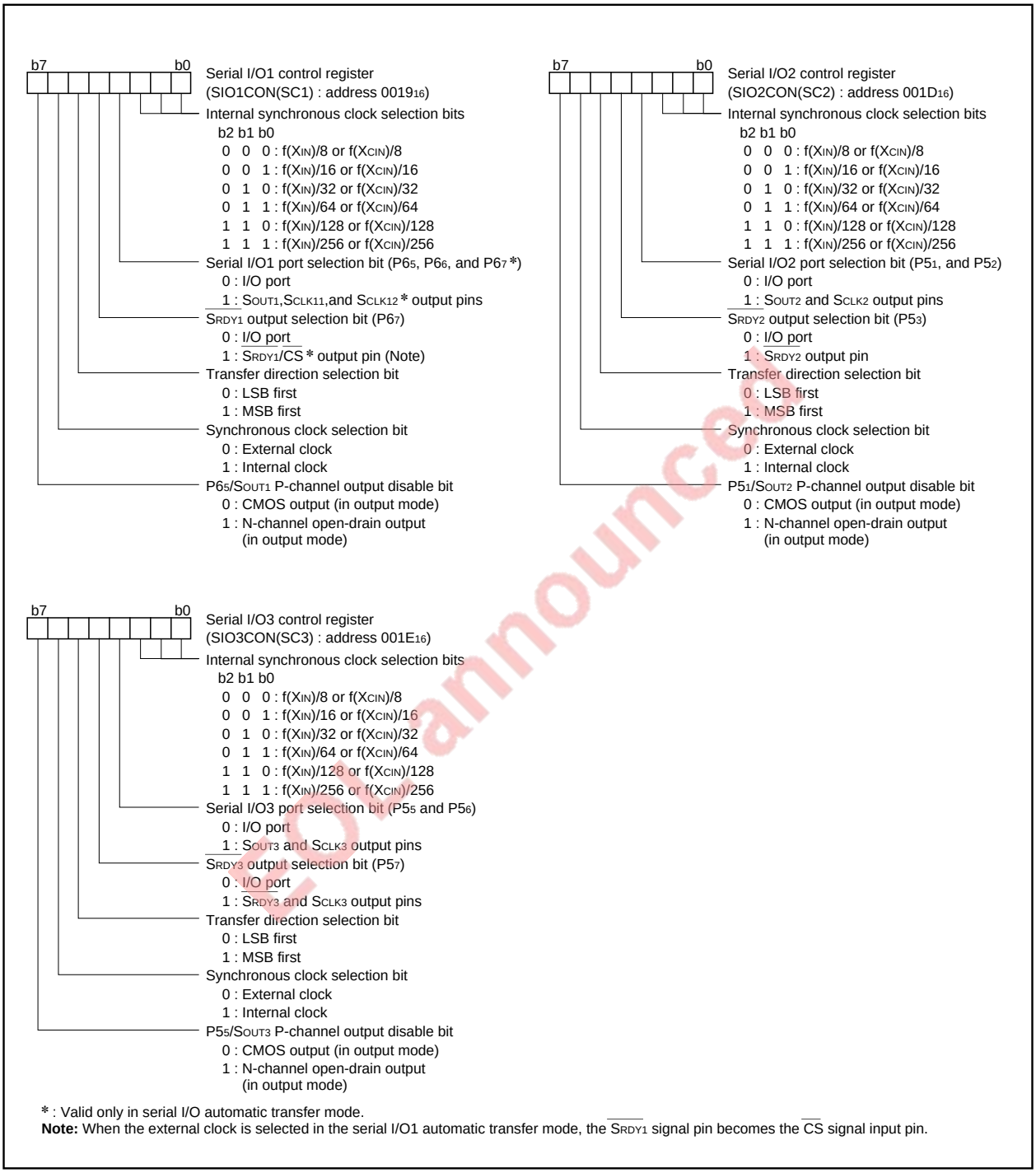


Fig. 14 Structure of serial I/O control registers

Eol announced

Downloaded from Elcodis.com electronic components distributor

(1) Serial I/O Ordinary Mode

Either an internal clock or an external clock can be selected as the synchronous clock for serial I/O transfer. A dedicated divider is built in as the internal clock for selecting of 6 clocks. If internal clock is selected, transfer starts with a write signal to a serial I/O register (addresses 001B16, 001F16, or 002616). After 8 bits have been transferred, the SOUT pin goes to high impedance state.

If external clock is selected, control the clock externally because the contents of the serial I/O register continue to shift during inputting the transfer clock. In this case, note that the SOUT pin does not go to high impedance state at the completion of data transfer.

The interrupt request bit is set at the completion of the transfer of 8 bits, regardless of whether the internal or external clock is selected.

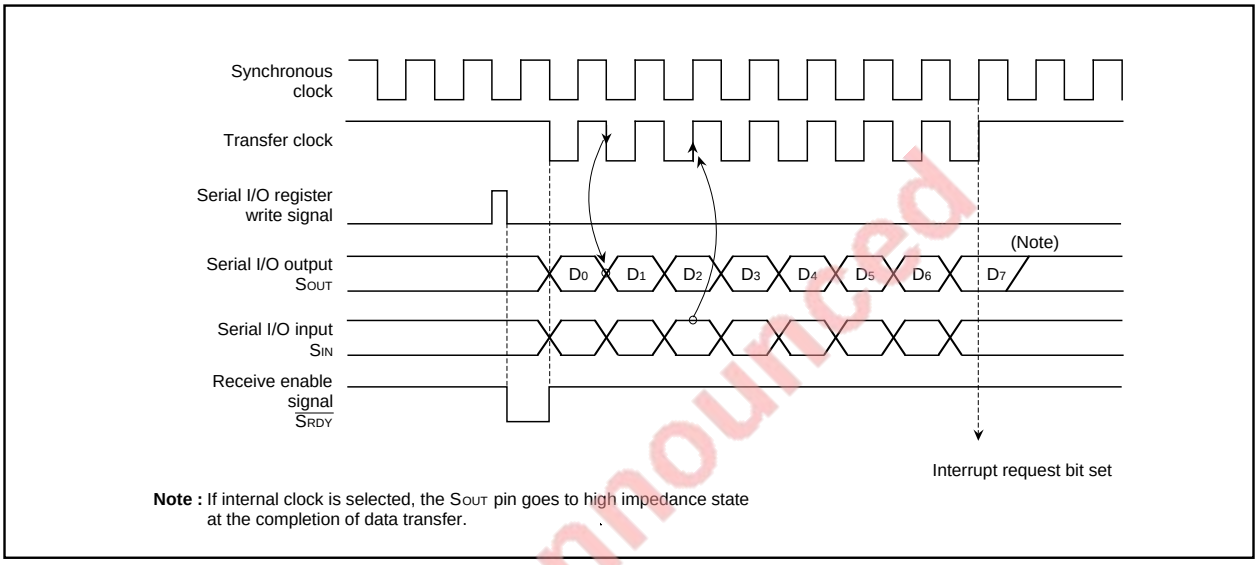


Fig. 15 Serial I/O timing in the serial I/O ordinary mode (for LSB first)

(2) Serial I/O Automatic Transfer Mode

The serial I/O1 has the automatic transfer function. For automatic transfer, switch to the automatic transfer mode by setting the serial I/O automatic transfer control register (address 001A16).

The following memory spaces and registers used to enable automatic transfer mode:

- 32-byte serial I/O automatic transfer RAM
- A serial I/O automatic transfer control register
- A serial I/O automatic transfer interval register
- A serial I/O automatic transfer data pointer

When using serial I/O automatic transfer, set the serial I/O1 control register (address 001916) in the same way as the serial I/O ordinary mode. However, note that when external clock is selected, port P67 becomes the $\overline{CS}$ input pin by setting the bit 4 (the $\overline{SRDY1}$ output selection bit) of the serial I/O1 control register to "1".

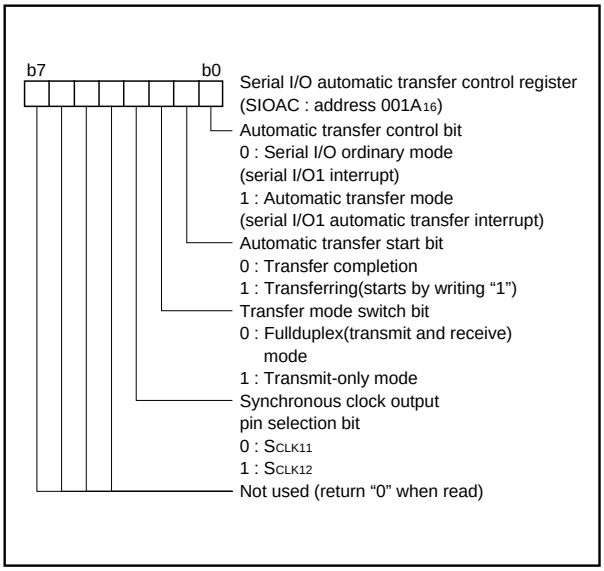


Fig. 16 Structure of serial I/O automatic transfer control register

Serial I/O Automatic Transfer Control Register (SIOAC) 001A16

The serial I/O automatic transfer control register (address 001A16) consists of 4 bits which control automatic transfer.

EOL announced

Downloaded from Elcodis.com electronic components distributor

Serial I/O Automatic Transfer Data Pointer (SIODP) 001816

The serial I/O automatic transfer data pointer (address 001816) consists of 5 bits which indicate addresses in serial I/O automatic transfer RAM (the value which adds 0F0016 to the serial I/O automatic transfer data pointer is actual address in memory).
Set the value (the number of transfer data-1) to the serial I/O automatic transfer data pointer for specifying the storage address of first data.

● Serial I/O Automatic Transfer RAM

The serial I/O automatic transfer RAM is the 32 bytes from address 0F0016 to address 0F1F16.

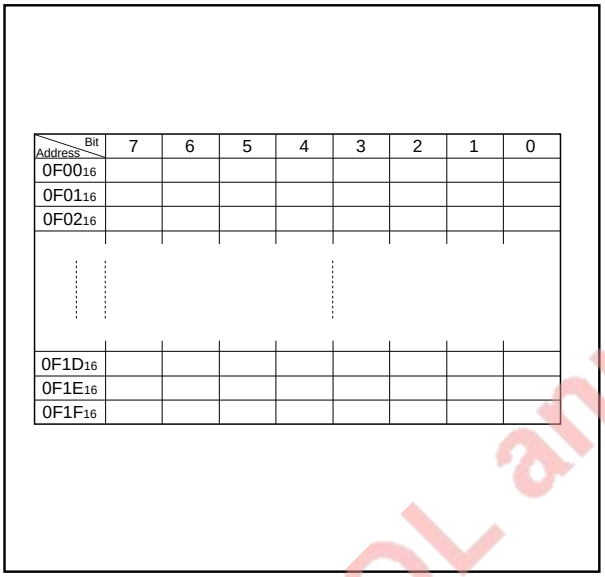


Fig. 17 Bit allocation of serial I/O automatic transfer RAM

● Setting of Serial I/O Automatic Transfer Data

When data is stored in the serial I/O automatic transfer RAM, store the first data at the address set with the serial I/O automatic transfer data pointer so that the last data can be stored at address 0F0016.

Serial I/O Automatic Transfer Interval Register (SIOAI) 001C16

The serial I/O automatic transfer interval register (address 001C16) consists of a 5-bit counter that determines the transfer interval Ti during automatic transfer.
When writing the value n to the serial I/O automatic transfer interval register, Ti=(n+2) × Tc (Tc: the length of one bit of the transfer clock) occurs. However, note that this transfer interval setting is valid only when selecting the internal clock as the clock source.

EOL announced

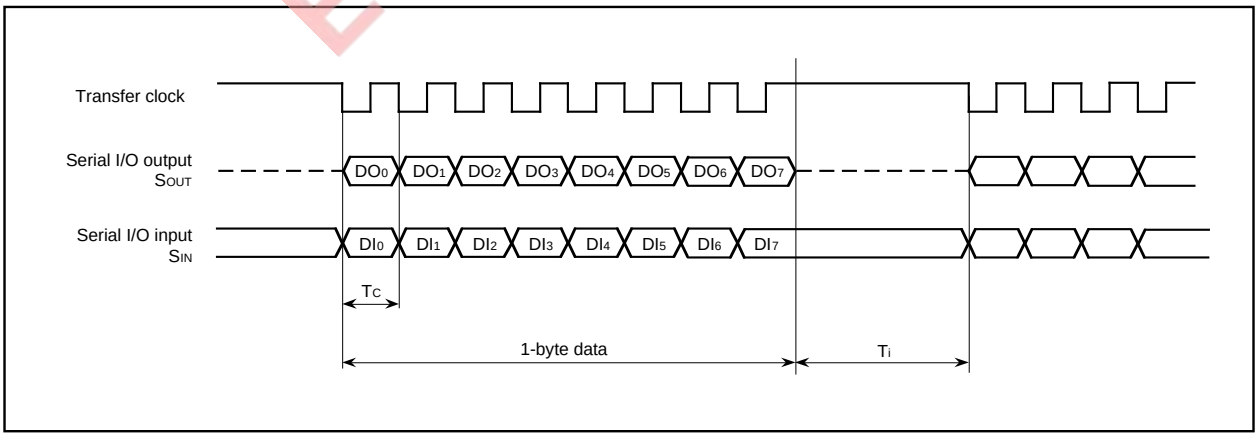


Fig. 18 Serial I/O automatic transfer interval timing

Downloaded from Elcodis.com electronic components distributor

● Setting of Serial I/O Automatic Transfer Timing

The timing of serial I/O automatic transfer is set with the serial I/O1 control register (address 0019_{16}) and the serial I/O automatic transfer interval register (address $001C_{16}$).

The serial I/O1 control register sets the transfer clock speed, and the serial I/O automatic transfer interval register sets the serial I/O automatic transfer interval. This setting of transfer interval is valid only when selecting the internal clock as the clock source.

● Start of Serial I/O Automatic Transfer

Automatic transfer mode is set by writing "1" to the bit 0 of the serial I/O automatic transfer control register (address $001A_{16}$), then automatic transfer starts by writing "1" to the bit 1.

The bit 1 of the serial I/O automatic transfer control register is always "1" during automatic transfer; writing "0" can complete the serial I/O automatic transfer.

● Operation in Serial I/O Automatic Transfer Modes

There are two modes for serial I/O automatic transfer: full duplex mode and transmit-only mode. Either internal or external clock can be selected for each of these modes.

(2.1) Operation in Full Duplex Mode

In full duplex mode, data can be transmitted and received at the same time. Data in the automatic transfer RAM is transmitted in sequence in accordance with the serial I/O automatic transfer data pointer and simultaneously reception data is written to the automatic transfer RAM.

The transfer timing of each bit is the same as that in ordinary operation mode, and the transfer clock stops at "H" after eight transfer clocks are counted.

When selecting the internal clock, the transfer clock remains at "H" for the time set with the serial I/O automatic transfer interval register, then the data at the next address (the address is indicated with the serial I/O automatic transfer data pointer) are transferred.

If when selecting the external clock, the setting of the automatic transfer interval register is invalid, so control the transfer clock externally.

The last data transfer completes when the contents of the serial I/O automatic transfer pointer reach "00_{16}". At that point, the serial I/O automatic transfer interrupt request bit is set to "1" and the bit 1 of the serial I/O automatic transfer control register is cleared to "0" to complete the serial I/O automatic transfer.

(2.2) Operation in Transmit-Only Mode

The operation in transmit-only mode is the same as that in full duplex mode, except for that data is not transferred from the serial I/O1 register to the serial I/O automatic transfer RAM.

EOL announced

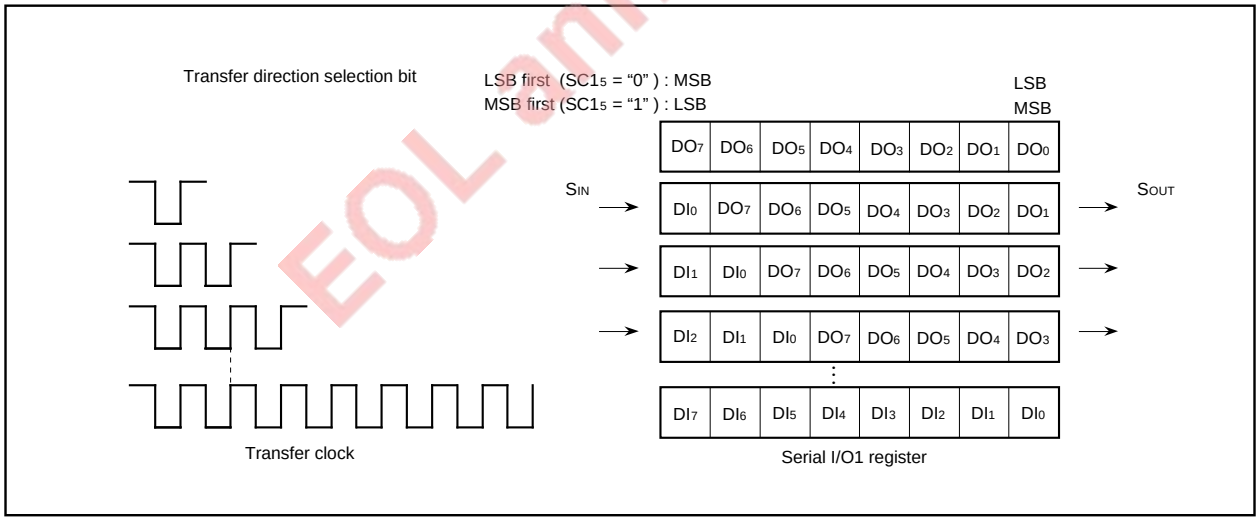


Fig. 19 Serial I/O1 register transfer operation in full duplex mode

Renesas Technology Corp.
Downloaded from Elcodis.com electronic components distributor

(2.3) When Selecting the Internal Clock

When selecting the internal clock, the P67/$\overline{\text{SRDY1}}$/$\overline{\text{CS}}$/SCLK12 pin can be used as the $\overline{\text{SRDY1}}$ pin by setting SC14 to "1".

When selecting the internal clock, the P67 pin can be used as the synchronous clock output pin SCLK12 by setting SIOAC3 to "1". In this case, the SCLK11 pin goes to high impedance state.

Select the function of the P67/$\overline{\text{SRDY1}}$/$\overline{\text{CS}}$/SCLK12 and P66/SCLK11 with the following registers (refer to Table 2):

- the bit 3 (SC13), the bit 4(SC14), and the bit 6(SC16) of the serial I/O1 control register
- the bit 3 (SIOAC3) of the serial I/O automatic transfer control register

When using both the SCLK11 and SCKL12 by switching, switch the P67/$\overline{\text{SRDY1}}$/$\overline{\text{CS}}$/SCLK12 to the P67 (SC14=0) and set the P67 direction register to input mode. Note that switch SIOAC3 during "H" of transfer clock at the completion of automatic transfer.

Table 2. SCLK11 and SCLK12 selection

SC16	SC14	SC33	SIOAC3	P66/SCLK11	P67/SCLK12
1	0	1	0	SCLK11	P67
			1	High impedance	SCLK12

Note : SC13: Serial I/O1 port selection bit
SC14: $\overline{\text{SRDY1}}$ output selection bit
SC16: Synchronous clock selection bit
SIOAC3: Synchronous clock output pin selection bit

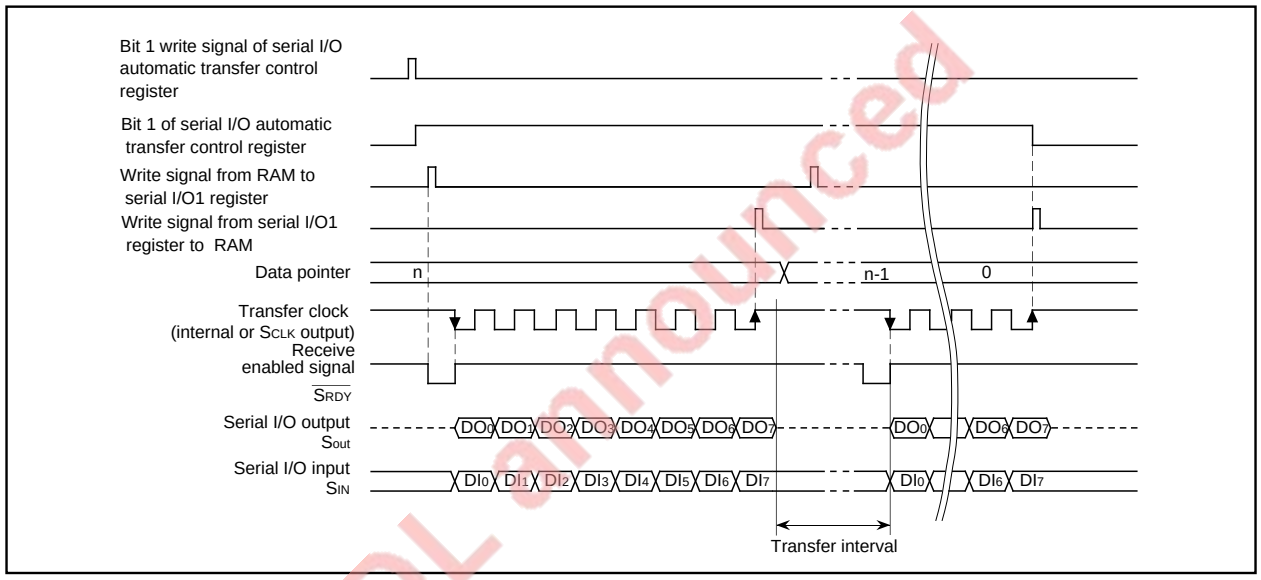


Fig. 20 Timing diagram during serial I/O automatic transfer (internal clock selected, $\overline{\text{SRDY}}$ used)

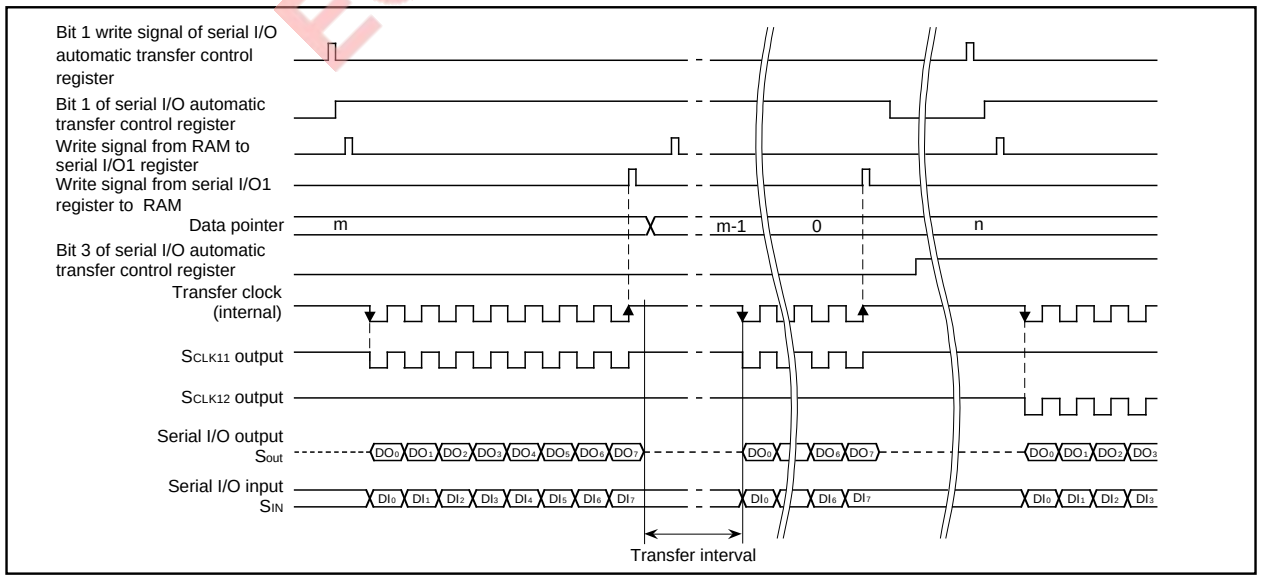


Fig. 21 Timing during serial I/O automatic transfer (internal clock selected, SCLK11 and SCLK12 used)

EOL announced

Downloaded from Elcodis.com electronic components distributor

(2.4) When Selecting the External Clock

When selecting the external clock, the internal clock and the setting of transfer interval with the serial I/O automatic transfer interval register are invalid, but the serial I/O output pin SOUT1 and the internal transfer clock can be controlled from the outside by setting the $\overline{\text{SRDY1}}$ pin to the $\overline{\text{CS}}$ (input) pin.

When the $\overline{\text{CS}}$ input is "L", the SOUT1 pin and the internal transfer clock are enabled.

When the $\overline{\text{CS}}$ input is "H", the SOUT1 pin goes to high impedance state and the internal transfer clock goes to "H".

Select the function of the P67/$\overline{\text{SRDY1}}$/$\overline{\text{CS}}$/SCLK12 with the following registers (refer to Table GA-2):

- the bit 4 (SC14) and the bit 6 (SC16) of the serial I/O1 control register
- the bit 0 (SIOAC0) of the serial I/O automatic transfer control register

Switch the $\overline{\text{CS}}$ pin from "L" to "H" or from "H" to "L" during "H" of the transfer clock (SCLK11 input) after transferring 1-byte data.

When selecting the external clock, set the external clock to "L" after 9 cycles or more of the internal clock ϕ after setting the start bit. After transferring 1-byte data, leave 11 cycles or more of the internal clock ϕ free for the transfer interval.

When not using the $\overline{\text{CS}}$ input, note that the SOUT pin will not go to high impedance state, even after transfer is completed.

When not using the $\overline{\text{CS}}$ input, or when $\overline{\text{CS}}$ is "L", control the external clock because the data in the serial I/O register will continue to shift while the external clock is input, even after the completion of automatic transfer (Note that the automatic transfer interrupt request bit is set and the bit 1 of the serial I/O automatic transfer register is cleared at the point when the specified number of bytes of data have been transferred.)

Table 3. P67/$\overline{\text{SRDY1}}$/$\overline{\text{CS}}$ selection

SC16	SC14	SIOAC0	P67/$\overline{\text{SRDY1}}$/$\overline{\text{CS}}$
0	0	×	P67
	1	0	$\overline{\text{SRDY1}}$
		1	$\overline{\text{CS}}$

Note : SC14: $\overline{\text{SRDY1}}$ output selection bit
SC16: Synchronous clock selection bit
SIOAC0: Automatic transfer control bit

EOL announced

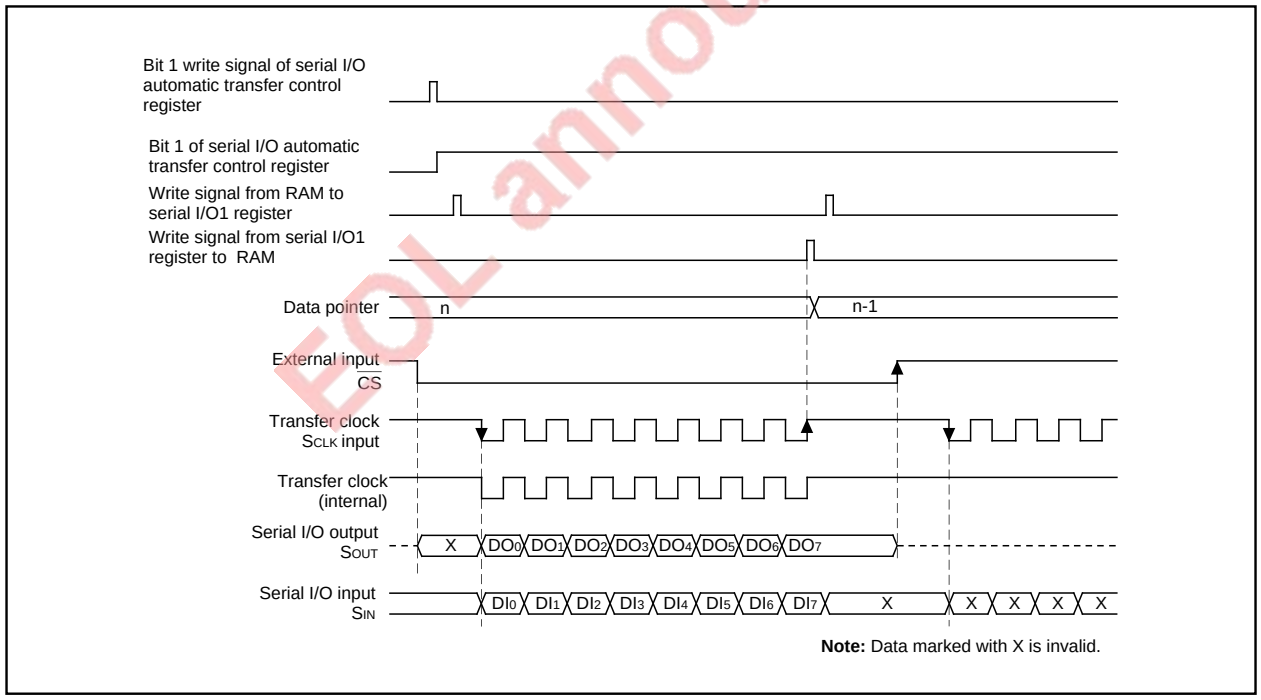


Fig. 22 Timing during serial I/O automatic transfer (external clock selected)

Renesas Technology Corp.
Downloaded from Elcodis.com electronic components distributor

A-D CONVERTER

The functional blocks of the A-D converter are described below.

A-D Conversion Register (AD) 002D16

The A-D conversion register is a read-only register that stores the result of an A-D conversion. This register should not be read during A-D conversion.

AD/DA Control Register (ADCON) 002C16

The AD/DA control register controls the A-D and the D-A conversion process. Bits 0 to 3 of this register select analog input pins. Bit 4 is the AD conversion completion bit. The value of this bit remains at "0" during an A-D conversion, then changes to "1" when the A-D conversion is completed.

The A-D conversion starts by writing "0" to this bit. Bit 6 controls the output of D-A converter.

Comparison Voltage Generator

The comparison voltage generator divides the voltage between AVSS and VREF by 256, and outputs the divided voltages.

Channel Selector

The channel selector selects one of the input ports P77/AN7–P70/AN0, P57/$\overline{\text{SRDY3}}$/AN15–P50/SIN2/AN8, and inputs to the comparator.

Comparator and Control Circuit

The comparator and control circuit compares an analog input voltage with the comparison voltage and stores the result in the A-D conversion register. When an A-D conversion is completed, the control circuit sets the AD conversion completion bit and the AD conversion interrupt request bit to "1".

Note that the comparator is constructed linked to a capacitor, so set f(XIN) to 500 kHz or more during A-D conversion.

Note : When using the A-D conversion interrupt, set the INT4/AD conversion interrupt switch bit (the bit 5 of the interrupt selection register) to "1".

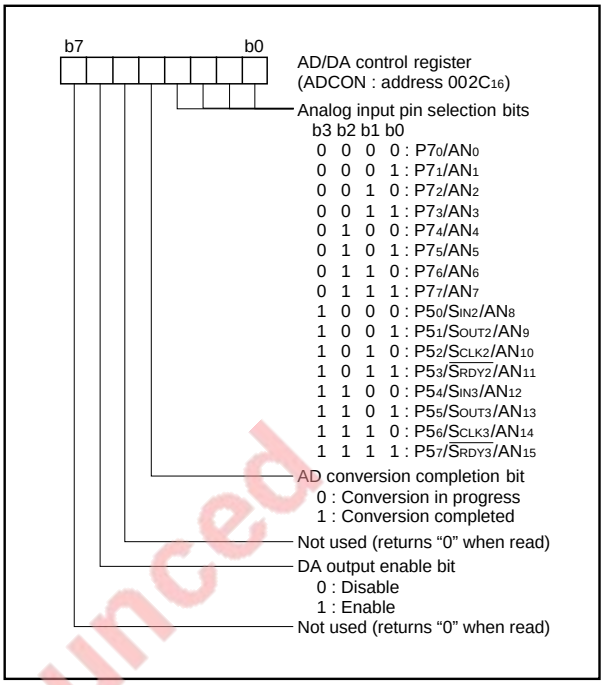


Fig. 23 Structure of A-D control register

EOL announced

Downloaded from Elcodis.com electronic components distributor

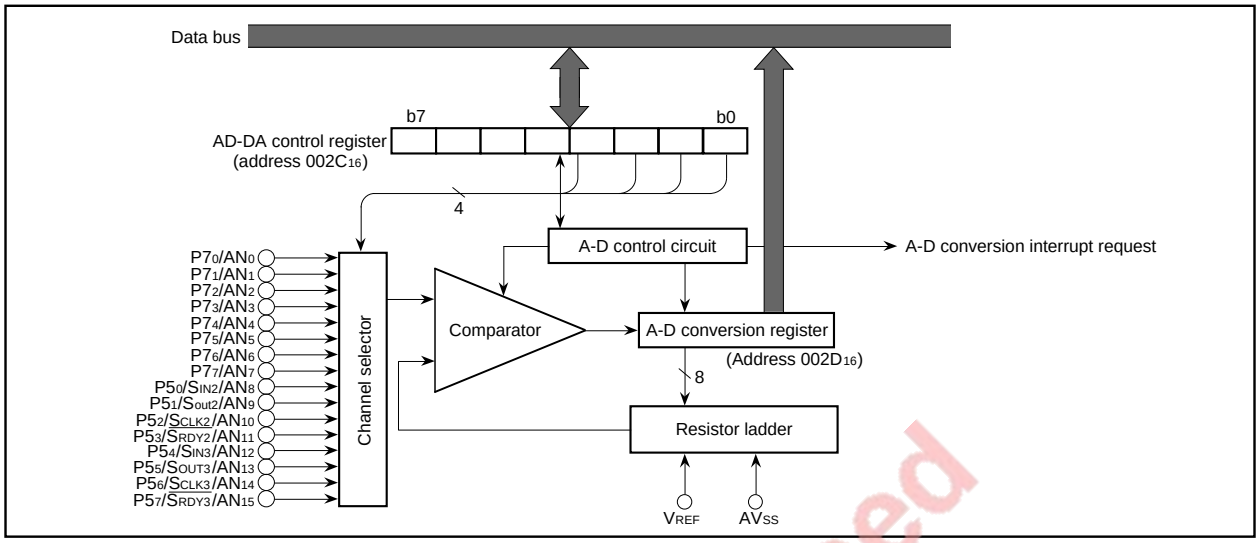


Fig. 24 A-D converter block diagram

D-A CONVERTER

The 3819 group has internal D-A converter with 8-bit resolutions × 1 channel.

D-A conversion is performed by setting the value in the D-A conversion register. The result of D-A conversion is output from the DA pin by setting the DA output enable bit to “1” . At this time, the corresponding bit (PB2/DA) of the port PB direction register should be set to “0” (input status).

The output analog voltage V is determined with the value n (n: decimal number) in the D-A conversion register as follows:

$V = V_{REF} \times n/256$ (n=0 to 255)

✻V_{REF}: the reference voltage

At reset, the D-A conversion register is cleared to “00_{16}”, the DA output enable bits are cleared to “0”, and the PB2/DA pin goes to high impedance state. The D-A output does not build in a buffer, so connect an external buffer when driving a low-impedance load.

Set V_{CC} to 3.0 V or more when using the D-A converter.

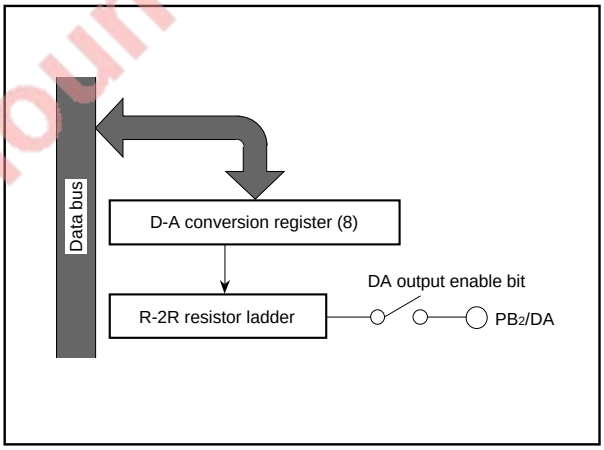


Fig. 25 D-A converter block diagram

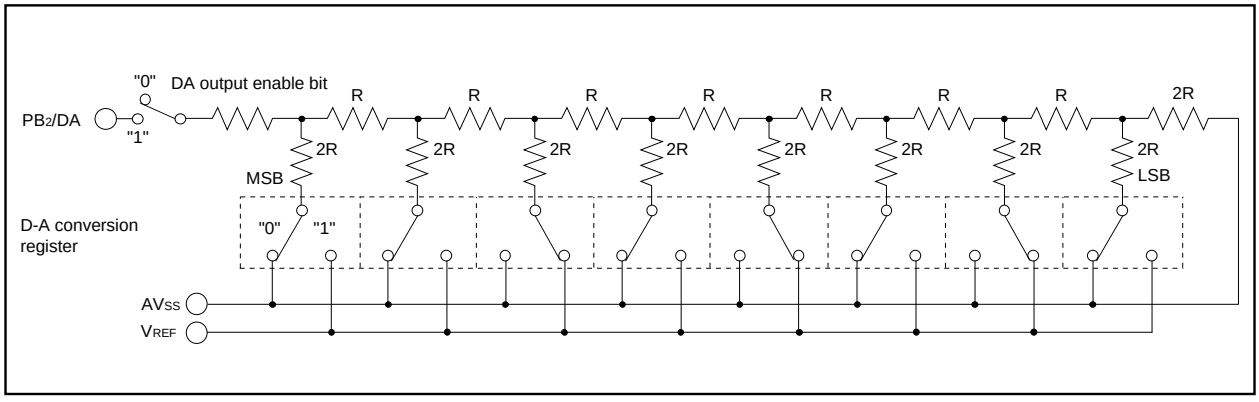


Fig. 26 Equivalent connection circuit of D-A converter

EOL announced

Downloaded from Elcodis.com electronic components distributor

FLD CONTROLLER

The 3819 group has fluorescent display (FLD) drive and control circuits.

The FLD controller consists of the following components:

- 42 pins for segments
- 20 pins for digits
- FLDC mode register 1
- FLDC mode register 2
- FLD data pointer
- FLD data pointer reload register
- Port P0 segment/digit switch register
- Port P2 digit/port switch register
- Port PA segment/port switch register
- Port P8 segment/port switch register
- 96-byte FLD automatic display RAM

The segment pins can be used from 16 up to 42 pins (maximum) and the digit pins can be used from 6 up to 16 pins (maximum). The segment and the digit pins can be used up to 52 pins (maximum) in total.

In the FLD automatic display mode ports P12 to P17 become digit pins DIG10 to DIG15 automatically.

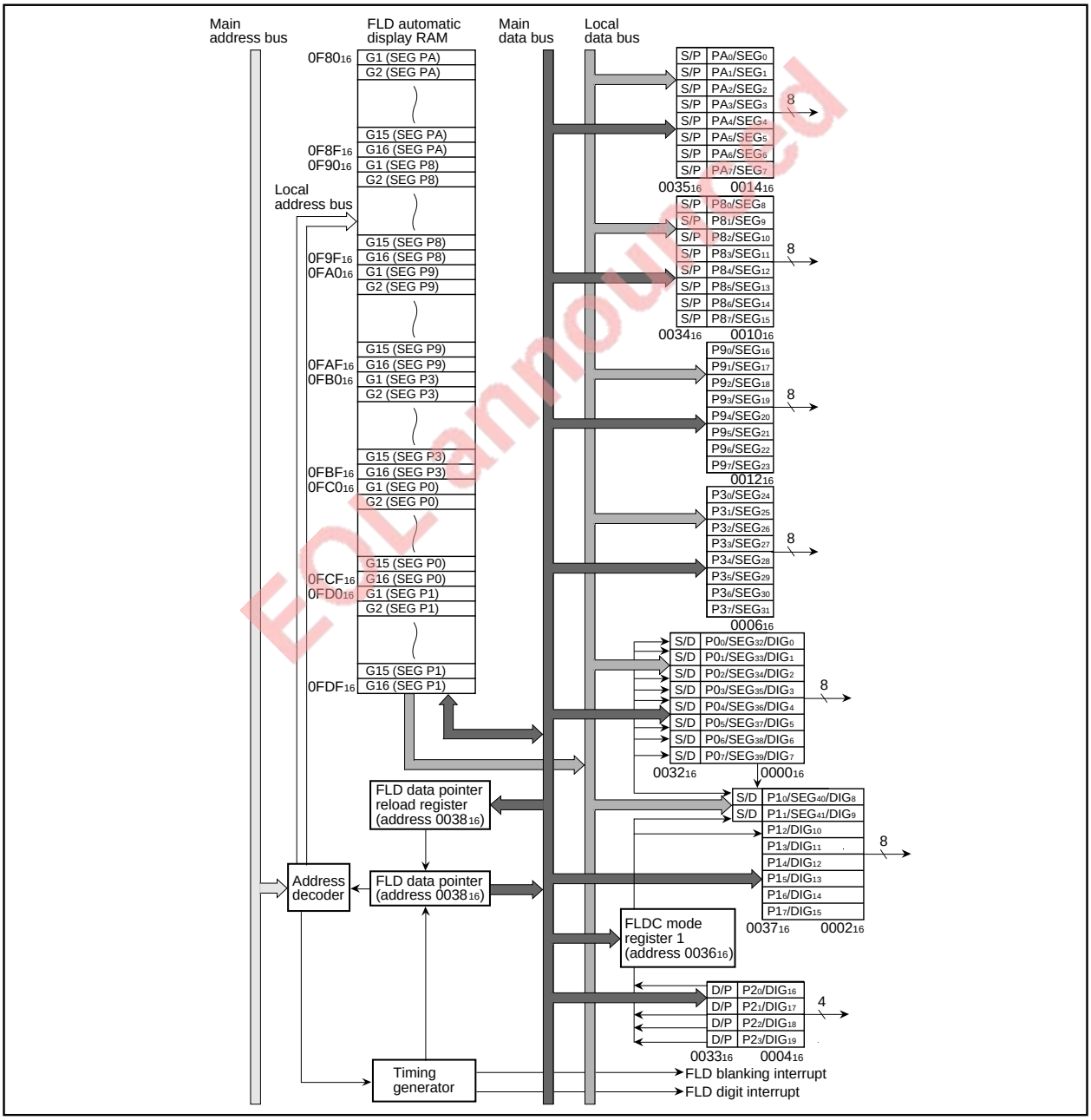


Fig. 27 FLD control circuit block diagram

EOL announced

Downloaded from Elcodis.com electronic components distributor

FLDC Mode Registers (FLDM 1, FLDM 2) 0036₁₆, 0037₁₆

The FLDC mode register 1 (address 0036₁₆) and FLDC mode register 2 (address 0037₁₆) are a seven bit register and an eight bit register respectively which are used to control the FLD automatic display and set the blanking time T_{scan} for key-scan.

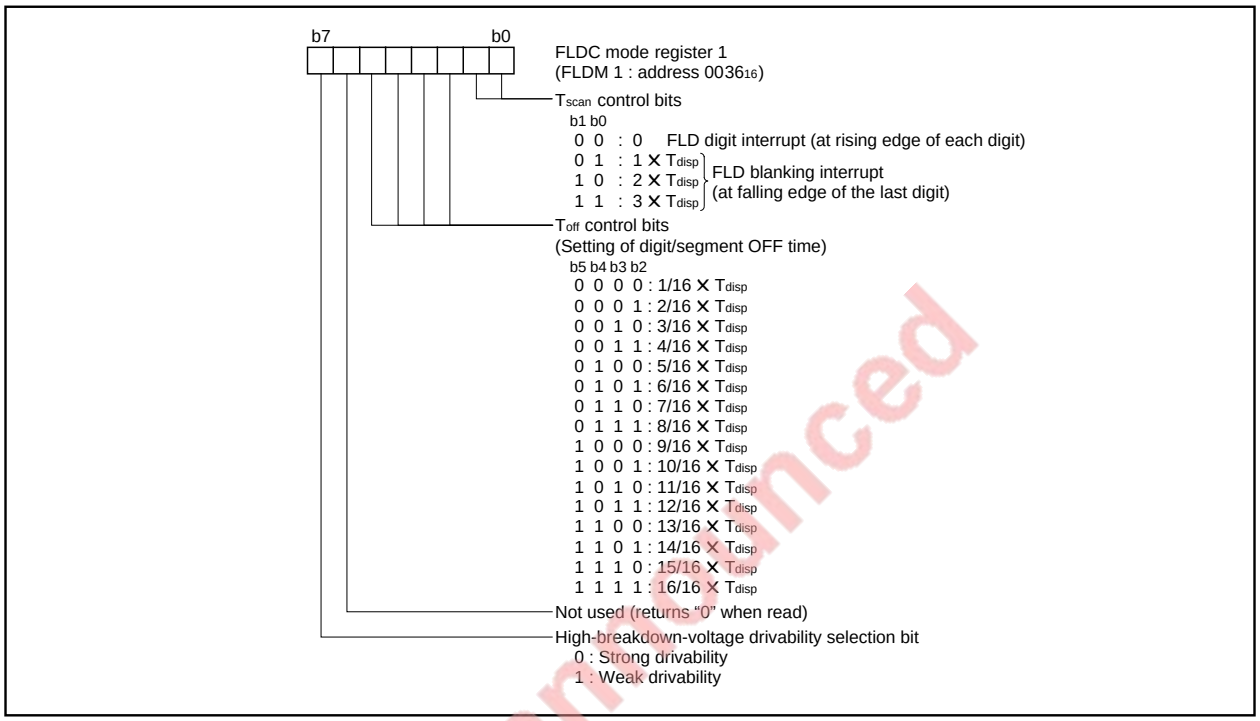


Fig. 28 Structure of FLDC mode register 1

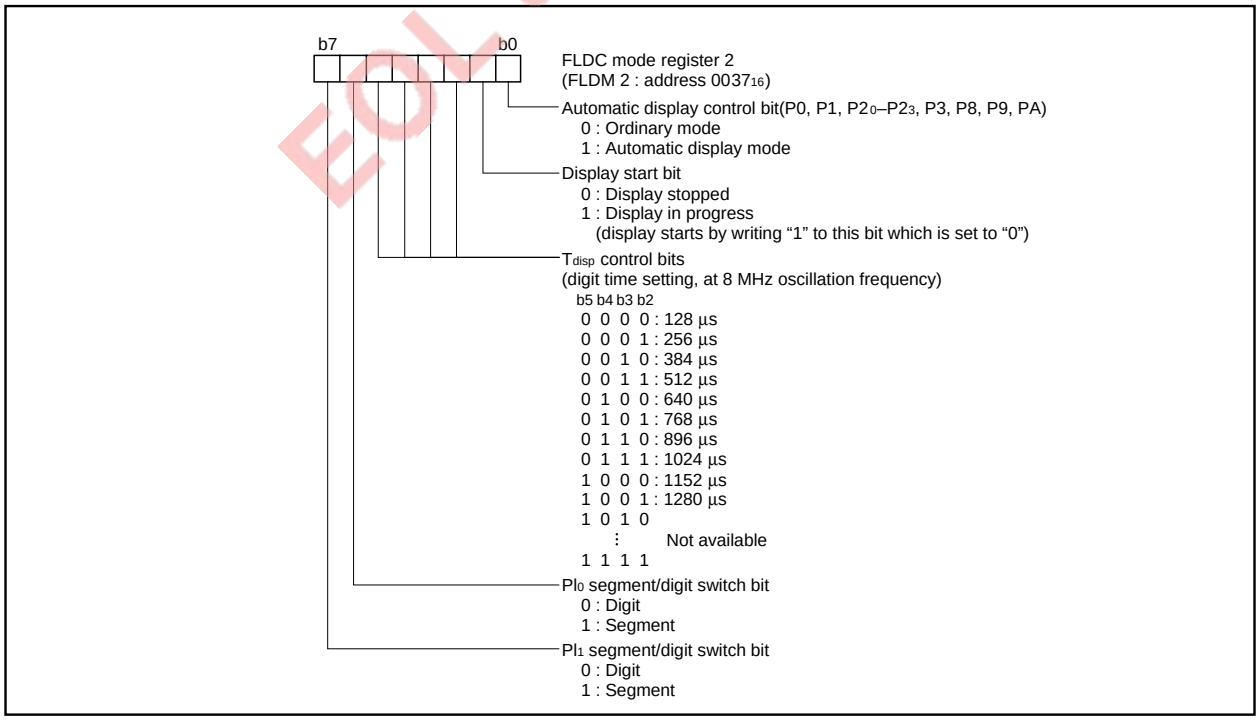


Fig. 29 Structure of FLDC mode register 2

EOL announced

Downloaded from Elcodis.com electronic components distributor

● Pins for FLD Automatic Display

Ports P0, P1, P20–P23, P3, P8, P9, and PA is selected for the FLD automatic display function by setting the automatic display control bit of the FLDC mode register 2 (address 003716) to "1".

When using the FLD automatic display mode, set the number of segments and digits for each port.

Table 4. Pins in FLD automatic display mode

Port Name	Automatic Display Pins	Setting Method
PA0–PA7	SEG0–SEG7 or PA0–PA7	The individual bits of the segment/port switch register (address 003516) can be set each pin to either segment ("1") or general-purpose I/O port ("0").
P80–P87	SEG8–SEG15 or P80–P87	The individual bits of the segment/port switch register (address 003416) can be used to set each pin to either segment ("1") or general-purpose I/O port ("0").
P90–P97	SEG16–SEG23	None (segment only)
P30–P37	SEG24–SEG31	None (segment only)
P00–P07 P10, P11	SEG32–SEG41 or DIG0–DIG9	The individual bits of the segment/digit switch register (address 003216) and the bit 6, 7 of the FLDC mode register 2 can be used to set each pin to segment ("1") or digit ("0"). (Note)
P12–P17	DIG10–DIG15	None (digit only)
P20–P23	DIG16–DIG19 or P20–P23	The individual bits of the digit/port switch register (address 003316) can be used to set each pin to digit ("1") or general-purpose output port ("0"). (Note)

Note : Be sure to set digits in sequence.

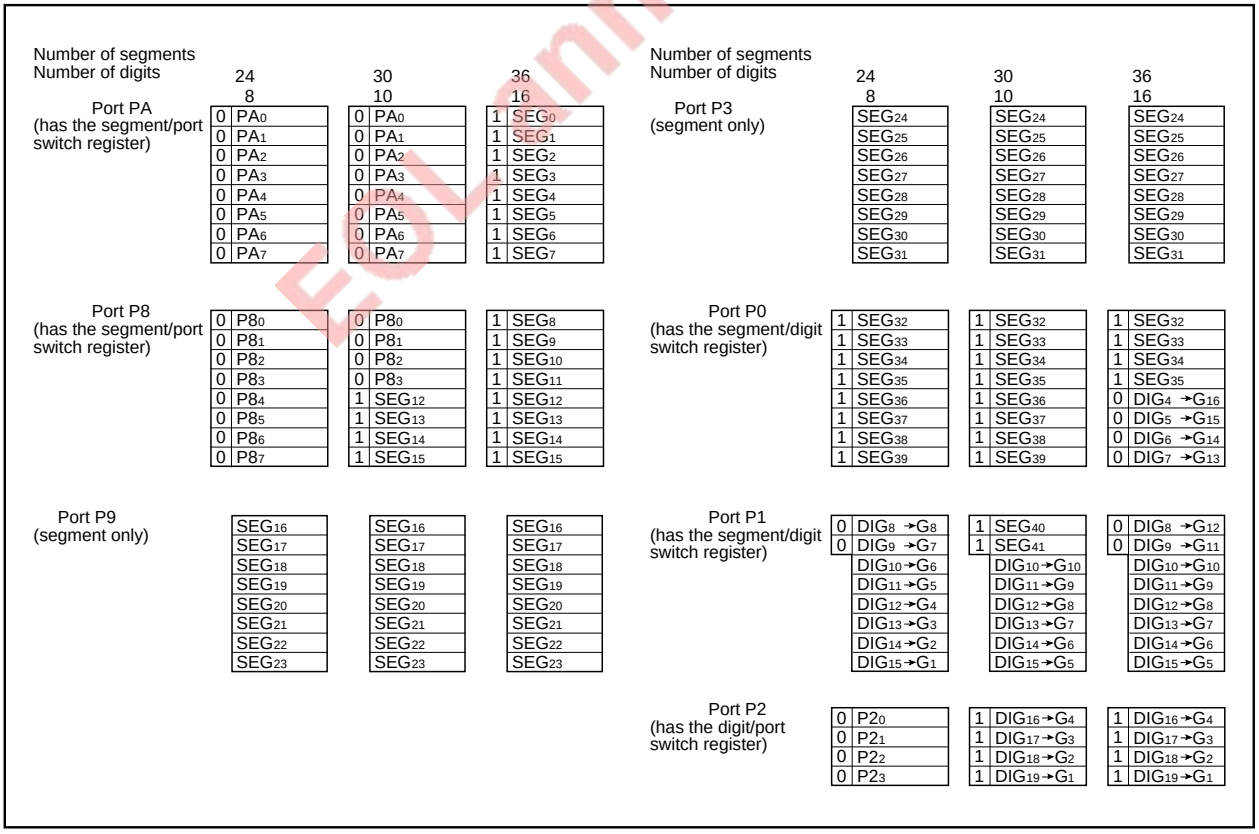


Fig. 30 Segment/digit setting example

Renesas Technology Corp.

Downloaded from Elcodis.com electronic components distributor

● FLD Automatic Display RAM

The FLD automatic display RAM area is the 96 bytes from addresses $0F80_{16}$ to $0FDF_{16}$. The FLD automatic display RAM area can store 6-byte segment data up to 16 digits (maximum). Addresses $0F80_{16}$ to $0F8F_{16}$ are used for PA segment data, addresses $0F90_{16}$ to $0F9F_{16}$ are used for P8 segment data, addresses $0FA0_{16}$ to $0FAF_{16}$ are used for P9 segment data, addresses $0FB0_{16}$ to $0FBF_{16}$ are used for P3 segment data, addresses $0FC0_{16}$ to $0FCF_{16}$ are used for P0 segment data, and addresses 0FD0 to $0FDF_{16}$ are used for P1 segment data.

FLD Data Pointer and FLD Data Pointer Reload Register

(FLDDP) 0038_{16}

Both the FLD data pointer and FLD data pointer reload register are 7-bit registers allocated at address 0038_{16}. When writing data to this address, the data is written to the FLD data pointer reload register, when reading data from this address, the value in the FLD data pointer is read.

The FLD data pointer indicates the data address in the FLD automatic display RAM to be transferred to a segment. The FLD data pointer reload register indicates the first digit address of the most significant segment.

The value which adds $0F80_{16}$ to these data is actual address in memory.

The contents of the FLD data pointer indicate the first address of segment P1(the contents of the FLD data pointer reload register) at the start of automatic display. The FLDC data pointer content changes repeatedly as follows: when transferring the segment P1 data to the segment, the content decreases by –16; when transferring the segment P0 data, it decreases by –16; when transferring the segment P3 data, it decreases by –16; when transferring the segment P9 data, it decreases by –16; when transferring the segment P8 data, it decreases by –16; when transferring the segment PA data, it increases by +79. Once it reaches “00”, at the next timing the value in the FLD data pointer reload register is transferred to the FLD data pointer. In this way, the 6-byte data of P1, P0, P3, P9, P8 and PA segments for 1 digit are transferred.

EOL announced

Downloaded from Elcodis.com electronic components distributor

Address \ Bit	7	6	5	4	3	2	1	0	
$0F80_{16}$	SEG_7	SEG_6	SEG_5	SEG_4	SEG_3	SEG_2	SEG_1	SEG_0	← The last digit (The last data of segment PA)
$0F81_{16}$	SEG_7	SEG_6	SEG_5	SEG_4	SEG_3	SEG_2	SEG_1	SEG_0	
⋮	⋮			⋮					Segment PA data area
$0F8E_{16}$	SEG_7	SEG_6	SEG_5	SEG_4	SEG_3	SEG_2	SEG_1	SEG_0	
$0F8F_{16}$	SEG_7	SEG_6	SEG_5	SEG_4	SEG_3	SEG_2	SEG_1	SEG_0	
$0F90_{16}$	SEG_{15}	SEG_{14}	SEG_{13}	SEG_{12}	SEG_{11}	SEG_{10}	SEG_9	SEG_8	← The last digit (The last data of segment P8)
$0F91_{16}$	SEG_{15}	SEG_{14}	SEG_{13}	SEG_{12}	SEG_{11}	SEG_{10}	SEG_9	SEG_8	
⋮	⋮			⋮					Segment P8 data area
$0F9E_{16}$	SEG_{15}	SEG_{14}	SEG_{13}	SEG_{12}	SEG_{11}	SEG_{10}	SEG_9	SEG_8	
$0F9F_{16}$	SEG_{15}	SEG_{14}	SEG_{13}	SEG_{12}	SEG_{11}	SEG_{10}	SEG_9	SEG_8	
$0FA0_{16}$	SEG_{23}	SEG_{22}	SEG_{21}	SEG_{20}	SEG_{19}	SEG_{18}	SEG_{17}	SEG_{16}	← The last digit (The last data of segment P9)
$0FA1_{16}$	SEG_{23}	SEG_{22}	SEG_{21}	SEG_{20}	SEG_{19}	SEG_{18}	SEG_{17}	SEG_{16}	
⋮	⋮			⋮					Segment P9 data area
$0FAE_{16}$	SEG_{23}	SEG_{22}	SEG_{21}	SEG_{20}	SEG_{19}	SEG_{18}	SEG_{17}	SEG_{16}	
$0FAF_{16}$	SEG_{23}	SEG_{22}	SEG_{21}	SEG_{20}	SEG_{19}	SEG_{18}	SEG_{17}	SEG_{16}	
$0FB0_{16}$	SEG_{31}	SEG_{30}	SEG_{29}	SEG_{28}	SEG_{27}	SEG_{26}	SEG_{25}	SEG_{24}	← The last digit (The last data of segment P3)
$0FB1_{16}$	SEG_{31}	SEG_{30}	SEG_{29}	SEG_{28}	SEG_{27}	SEG_{26}	SEG_{25}	SEG_{24}	
⋮	⋮			⋮					Segment P3 data area
$0FBE_{16}$	SEG_{31}	SEG_{30}	SEG_{29}	SEG_{28}	SEG_{27}	SEG_{26}	SEG_{25}	SEG_{24}	
$0FBF_{16}$	SEG_{31}	SEG_{30}	SEG_{29}	SEG_{28}	SEG_{27}	SEG_{26}	SEG_{25}	SEG_{24}	
$0FC0_{16}$	SEG_{39}	SEG_{38}	SEG_{37}	SEG_{36}	SEG_{35}	SEG_{34}	SEG_{33}	SEG_{32}	← The last digit (The last data of segment P0)
$0FC1_{16}$	SEG_{39}	SEG_{38}	SEG_{37}	SEG_{36}	SEG_{35}	SEG_{34}	SEG_{33}	SEG_{32}	
⋮	⋮			⋮					Segment P0 data area
$0FCE_{16}$	SEG_{39}	SEG_{38}	SEG_{37}	SEG_{36}	SEG_{35}	SEG_{34}	SEG_{33}	SEG_{32}	
$0FCF_{16}$	SEG_{39}	SEG_{38}	SEG_{37}	SEG_{36}	SEG_{35}	SEG_{34}	SEG_{33}	SEG_{32}	
$0FD0_{16}$							SEG_{41}	SEG_{40}	← The last digit (The last data of segment P1)
$0FD1_{16}$							SEG_{41}	SEG_{40}	
⋮	⋮			⋮					Segment P1 data area
$0FDE_{16}$							SEG_{41}	SEG_{40}	
$0FDF_{16}$							SEG_{41}	SEG_{40}	

EOL announced

Fig. 31 FLD automatic display RAM and bit allocation

Downloaded from Elcodis.com electronic components distributor

● Data Setup

When data is stored in the FLD automatic display RAM, the last data of segment PA is stored at address 0F80$_{16}$, the last data of segment P8 is stored at address 0F90$_{16}$, the last data of segment P9 is stored at address 0FA0$_{16}$, the last data of segment P3 is stored at address 0FB0$_{16}$, the last data of segment P0 is stored at address 0FC0$_{16}$, and the last data of segment P1 is stored at address 0FD0$_{16}$ to allocate in sequence from the last data respectively. The first data of the segment PA, P8, P9, P3, P0, and P1 is stored at an address which adds the value of (the digit number–1) to the corresponding address 0F80$_{16}$, 0F90$_{16}$, 0FA0$_{16}$, 0FB0$_{16}$, 0FC0$_{16}$, and 0FD0$_{16}$.

Set the low-order 4 bits of the FLD data pointer reload register to the value given by the number of digits–1. "1" is always written to bit 6 and bit 4, and "0" is always written to bit 5. Note that "0" is always read from bits 6, 5 and 4 when reading.

For 30 segments and 15 digits
(FLD data pointer reload register = 14)

Address \ Bit	7	6	5	4	3	2	1	0
0F80$_{16}$	▨	▨	▨	▨	▨	▨	▨	▨
0F81$_{16}$	▨	▨	▨	▨	▨	▨	▨	▨
0F82$_{16}$	▨	▨	▨	▨	▨	▨	▨	▨
0F83$_{16}$	▨	▨	▨	▨	▨	▨	▨	▨
0F84$_{16}$	▨	▨	▨	▨	▨	▨	▨	▨
0F85$_{16}$	▨	▨	▨	▨	▨	▨	▨	▨
0F86$_{16}$	▨	▨	▨	▨	▨	▨	▨	▨
0F87$_{16}$	▨	▨	▨	▨	▨	▨	▨	▨
0F88$_{16}$	▨	▨	▨	▨	▨	▨	▨	▨
0F89$_{16}$	▨	▨	▨	▨	▨	▨	▨	▨
0F8A$_{16}$	▨	▨	▨	▨	▨	▨	▨	▨
0F8B$_{16}$	▨	▨	▨	▨	▨	▨	▨	▨
0F8C$_{16}$	▨	▨	▨	▨	▨	▨	▨	▨
0F8D$_{16}$	▨	▨	▨	▨	▨	▨	▨	▨
0F8E$_{16}$	▨	▨	▨	▨	▨	▨	▨	▨
0F8F$_{16}$								
0F90$_{16}$	▨	▨	▨	▨	▨	▨	▨	▨
0F91$_{16}$	▨	▨	▨	▨	▨	▨	▨	▨
0F92$_{16}$	▨	▨	▨	▨	▨	▨	▨	▨
0F93$_{16}$	▨	▨	▨	▨	▨	▨	▨	▨
0F94$_{16}$	▨	▨	▨	▨	▨	▨	▨	▨
0F95$_{16}$	▨	▨	▨	▨	▨	▨	▨	▨
0F96$_{16}$	▨	▨	▨	▨	▨	▨	▨	▨
0F97$_{16}$	▨	▨	▨	▨	▨	▨	▨	▨
0F98$_{16}$	▨	▨	▨	▨	▨	▨	▨	▨
0F99$_{16}$	▨	▨	▨	▨	▨	▨	▨	▨
0F9A$_{16}$	▨	▨	▨	▨	▨	▨	▨	▨
0F9B$_{16}$	▨	▨	▨	▨	▨	▨	▨	▨
0F9C$_{16}$	▨	▨	▨	▨	▨	▨	▨	▨
0F9D$_{16}$	▨	▨	▨	▨	▨	▨	▨	▨
0F9E$_{16}$	▨	▨	▨	▨	▨	▨	▨	▨
0F9F$_{16}$								
0FA0$_{16}$	▨	▨	▨	▨	▨	▨	▨	▨
0FA1$_{16}$	▨	▨	▨	▨	▨	▨	▨	▨
0FA2$_{16}$	▨	▨	▨	▨	▨	▨	▨	▨
0FA3$_{16}$	▨	▨	▨	▨	▨	▨	▨	▨
0FA4$_{16}$	▨	▨	▨	▨	▨	▨	▨	▨
0FA5$_{16}$	▨	▨	▨	▨	▨	▨	▨	▨
0FA6$_{16}$	▨	▨	▨	▨	▨	▨	▨	▨
0FA7$_{16}$	▨	▨	▨	▨	▨	▨	▨	▨
0FA8$_{16}$	▨	▨	▨	▨	▨	▨	▨	▨
0FA9$_{16}$	▨	▨	▨	▨	▨	▨	▨	▨
0FAA$_{16}$	▨	▨	▨	▨	▨	▨	▨	▨
0FAB$_{16}$	▨	▨	▨	▨	▨	▨	▨	▨
0FAC$_{16}$	▨	▨	▨	▨	▨	▨	▨	▨
0FAD$_{16}$	▨	▨	▨	▨	▨	▨	▨	▨
0FAE$_{16}$	▨	▨	▨	▨	▨	▨	▨	▨
0FAF$_{16}$								

For 30 segments and 15 digits
(FLD data pointer reload register = 14)

Address \ Bit	7	6	5	4	3	2	1	0
0FB0$_{16}$			▨	▨	▨	▨	▨	▨
0FB1$_{16}$			▨	▨	▨	▨	▨	▨
0FB2$_{16}$			▨	▨	▨	▨	▨	▨
0FB3$_{16}$			▨	▨	▨	▨	▨	▨
0FB4$_{16}$			▨	▨	▨	▨	▨	▨
0FB5$_{16}$			▨	▨	▨	▨	▨	▨
0FB6$_{16}$			▨	▨	▨	▨	▨	▨
0FB7$_{16}$			▨	▨	▨	▨	▨	▨
0FB8$_{16}$			▨	▨	▨	▨	▨	▨
0FB9$_{16}$			▨	▨	▨	▨	▨	▨
0FBA$_{16}$			▨	▨	▨	▨	▨	▨
0FBB$_{16}$			▨	▨	▨	▨	▨	▨
0FBC$_{16}$			▨	▨	▨	▨	▨	▨
0FBD$_{16}$			▨	▨	▨	▨	▨	▨
0FBE$_{16}$			▨	▨	▨	▨	▨	▨
0FBF$_{16}$								
0FC0$_{16}$								
0FC1$_{16}$								
0FC2$_{16}$								
0FC3$_{16}$								
0FC4$_{16}$								
0FC5$_{16}$								
0FC6$_{16}$								
0FC7$_{16}$								
0FC8$_{16}$								
0FC9$_{16}$								
0FCA$_{16}$								
0FCB$_{16}$								
0FCC$_{16}$								
0FCD$_{16}$								
0FCE$_{16}$								
0FCF$_{16}$								
0FD0$_{16}$								
0FD1$_{16}$								
0FD2$_{16}$								
0FD3$_{16}$								
0FD4$_{16}$								
0FD5$_{16}$								
0FD6$_{16}$								
0FD7$_{16}$								
0FD8$_{16}$								
0FD9$_{16}$								
0FDA$_{16}$								
0FDB$_{16}$								
0FDC$_{16}$								
0FDD$_{16}$								
0FDE$_{16}$								
0FDF$_{16}$								

Note : ▨ Shaded areas are used.

EOL announced

Fig. 32 Example of using the FLD automatic display RAM (1)

Downloaded from Elcodis.com electronic components distributor

For 42 segments and 8 digits
(FLD data pointer reload register = 7)

Address \ Bit	7	6	5	4	3	2	1	0
0F80₁₆								
0F81₁₆								
0F82₁₆								
0F83₁₆								
0F84₁₆								
0F85₁₆								
0F86₁₆								
0F87₁₆								
0F88₁₆								
0F89₁₆								
0F8A₁₆								
0F8B₁₆								
0F8C₁₆								
0F8D₁₆								
0F8E₁₆								
0F8F₁₆								
0F90₁₆								
0F91₁₆								
0F92₁₆								
0F93₁₆								
0F94₁₆								
0F95₁₆								
0F96₁₆								
0F97₁₆								
0F98₁₆								
0F99₁₆								
0F9A₁₆								
0F9B₁₆								
0F9C₁₆								
0F9D₁₆								
0F9E₁₆								
0F9F₁₆								
0FA0₁₆								
0FA1₁₆								
0FA2₁₆								
0FA3₁₆								
0FA4₁₆								
0FA5₁₆								
0FA6₁₆								
0FA7₁₆								
0FA8₁₆								
0FA9₁₆								
0FAA₁₆								
0FAB₁₆								
0FAC₁₆								
0FAD₁₆								
0FAE₁₆								
0FAF₁₆								

For 42 segments and 8 digits
(FLD data pointer reload register = 7)

Address \ Bit	7	6	5	4	3	2	1	0
0FB0₁₆								
0FB1₁₆								
0FB2₁₆								
0FB3₁₆								
0FB4₁₆								
0FB5₁₆								
0FB6₁₆								
0FB7₁₆								
0FB8₁₆								
0FB9₁₆								
0FBA₁₆								
0FBB₁₆								
0FBC₁₆								
0FBD₁₆								
0FBE₁₆								
0FBF₁₆								
0FC0₁₆								
0FC1₁₆								
0FC2₁₆								
0FC3₁₆								
0FC4₁₆								
0FC5₁₆								
0FC6₁₆								
0FC7₁₆								
0FC8₁₆								
0FC9₁₆								
0FCA₁₆								
0FCB₁₆								
0FCC₁₆								
0FCD₁₆								
0FCE₁₆								
0FCF₁₆								
0FD0₁₆								
0FD1₁₆								
0FD2₁₆								
0FD3₁₆								
0FD4₁₆								
0FD5₁₆								
0FD6₁₆								
0FD7₁₆								
0FD8₁₆								
0FD9₁₆								
0FDA₁₆								
0FDB₁₆								
0FDC₁₆								
0FDD₁₆								
0FDE₁₆								
0FDF₁₆								

Note : ▨ Shaded areas are used.

EOL announced

Fig. 33 Example of using the FLD automatic display RAM (2) (continued)

Downloaded from Elcodis.com electronic components distributor

● Timing Setting

The digit time (T_{disp}) can be set with the FLDC mode register 2 (address 0037_{16}). The T_{scan} and digit/segment OFF time (T_{off}) can be set with the FLDC mode register 1 (address 0036_{16}). Note that flickering will occur if the repetition frequency (1/(T_{disp} × number of digits + T_{scan})) is an integral multiple of the digit timing T_{disp}.

● FLD Automatic Display Start

To perform FLD automatic display, set the following registers.

- Port P0 segment/digit switch register
- Port P2 digit/port switch register
- Port P8 segment/port switch register
- Port PA segment/port switch register
- FLDC mode register 1
- FLDC mode register 2
- FLD data pointer

Automatic display mode is selected by writing "1" to the bit 0 of the FLDC mode register 2 (address 0037_{16}), and the automatic display is started by writing "1" to the bit 1.

During automatic display bit 1 of the FLDC mode register 2 always keeps "1", automatic display can be interrupted by writing "0" to the bit 1.

● Key-scan

If key-scan is performed with the segment during the key-scan blanking period T_{scan}, take the following sequence:

1. Write "0" to the bit 0 (automatic display control bit) of the FLDC mode register 2 (address 0037_{16}).
2. Set the port corresponding to the segment for key-scan to the output port.
3. Perform the key-scan.
4. After the key-scan is performed, write "1" (automatic display mode) to the bit 0 of FLDC mode register 2 (address 0037_{16}).

Note on performance of key-scan in the above 1 to 4 sequence.

1. Do not write "0" to the bit 1 of FLDC mode register 2 (address 0037_{16}).
2. Do not write "1" to the port corresponding to the digit.

EOL announced

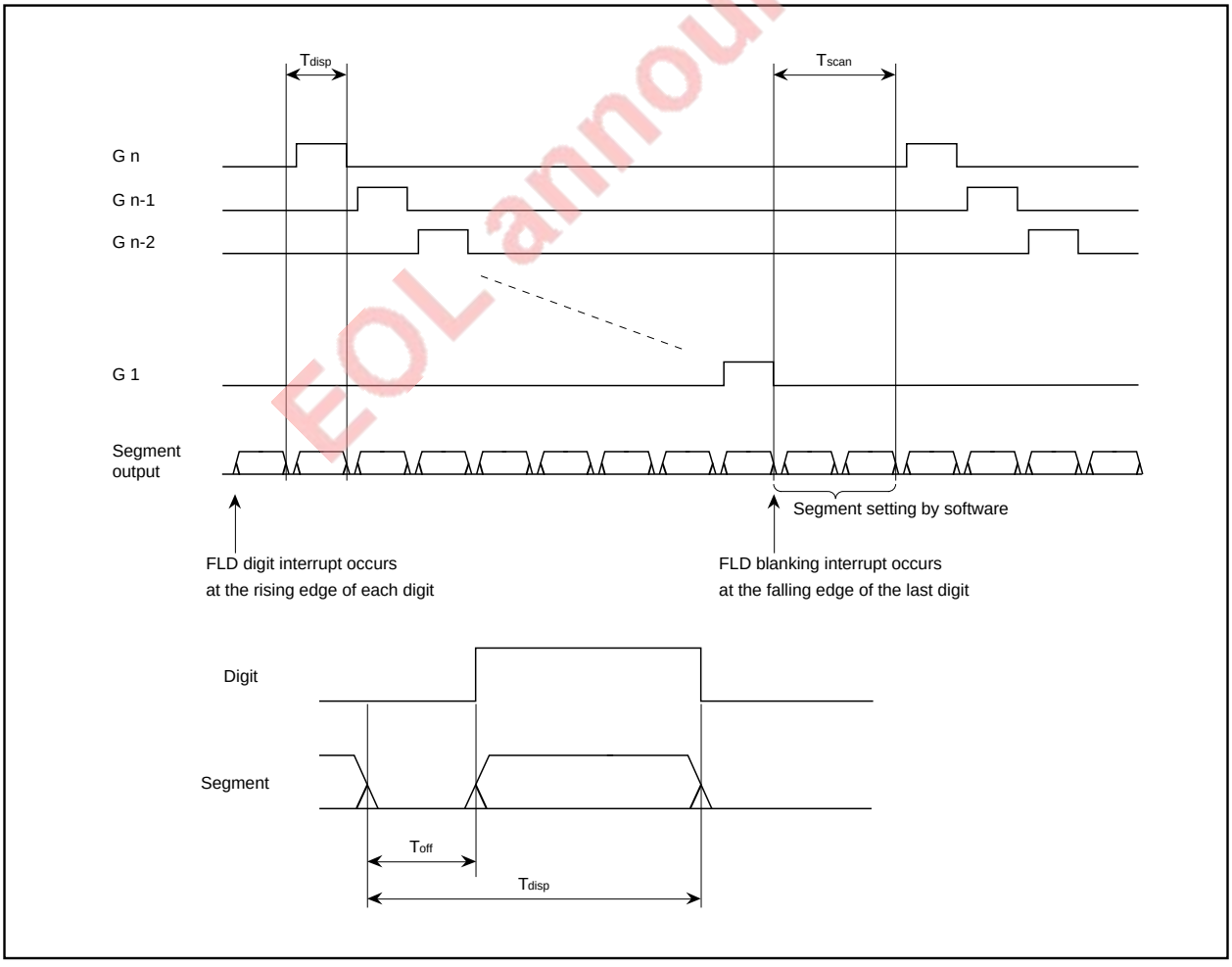


Fig. 34 FLDC timing

Renesas Technology Corp.

Downloaded from Elcodis.com electronic components distributor

INTERRUPT INTERVAL DETERMINATION FUNCTION

The 3819 group builds in an interrupt interval determination circuit. This interrupt interval determination circuit has an 8-bit binary up counter. Using this counter, it determines a duration of time from the rising transition (falling transition) of an input signal pulse on the P42/INT2 pin to the rising transition (falling transition) of the signal pulse that is input next.

How to determine the interrupt interval is described below.

① Enable the INT2 interrupt by setting the bit 2 of the interrupt control register 1 (address 003E16). Select the rising interval or falling interval by setting the bit 2 of the interrupt edge selection register (address 003A16).

② Set the bit 0 of the interrupt interval determination control register (address 003116) to "1" (interrupt interval determination operating).

③ Select the sampling clock of 8-bit binary up counter by setting the bit 1 of the interrupt interval determination control register. When writing "0", f(XIN)/256 is selected (the sampling interval: 32 µs at f(XIN) = 8.38 MHz) ; when "1", f(XIN)/512 is selected (the sampling interval: 64 µs at f(XIN) = 8.38 MHz).

④ When the signal of polarity which is set on the INT2 pin (rising or falling transition) is input, the 8-bit binary up counter starts counting up of the selected counter sampling clock.

⑤ When the signal of polarity above ④ is input again, the value of the 8-bit binary up counter is transferred to the interrupt interval determination register (address 003016), and the remote control interrupt request occurs. Immediately after that, the 8-bit binary up counter is cleared to "0016". The 8-bit binary up counter continues to count up again from "0016".

⑥ When count value reaches "FF16", the 8-bit binary up counter stops counting up. Then, simultaneously when the next counter sampling clock is input, the counter sets value "FF16" to the interrupt interval determination register to generate the counter overflow interrupt request.

Noise filter

The P42/INT2 pin builds in the noise filter.

The noise filter operation is described below.

① Select the sampling clock of the input signal with the bits 2 and 3 of the interrupt interval determination control register. When not using the noise filter, set "002".

② The P42/INT2 input signal is sampled in synchronization with the selected clock. When sampling the same level signal in series, the signal is recognized as the interrupt signal, and the interrupt request occurs.

When setting the bit 4 of interrupt interval determination control register to "1", the interrupt request can occur at both rising and falling edges.

When using the noise filter, set the minimum pulse width of the INT2 input signal to 2 cycles or more.

Note : In the low-speed mode (CM7=1), the interrupt interval determination function can not operate.

EOL announced

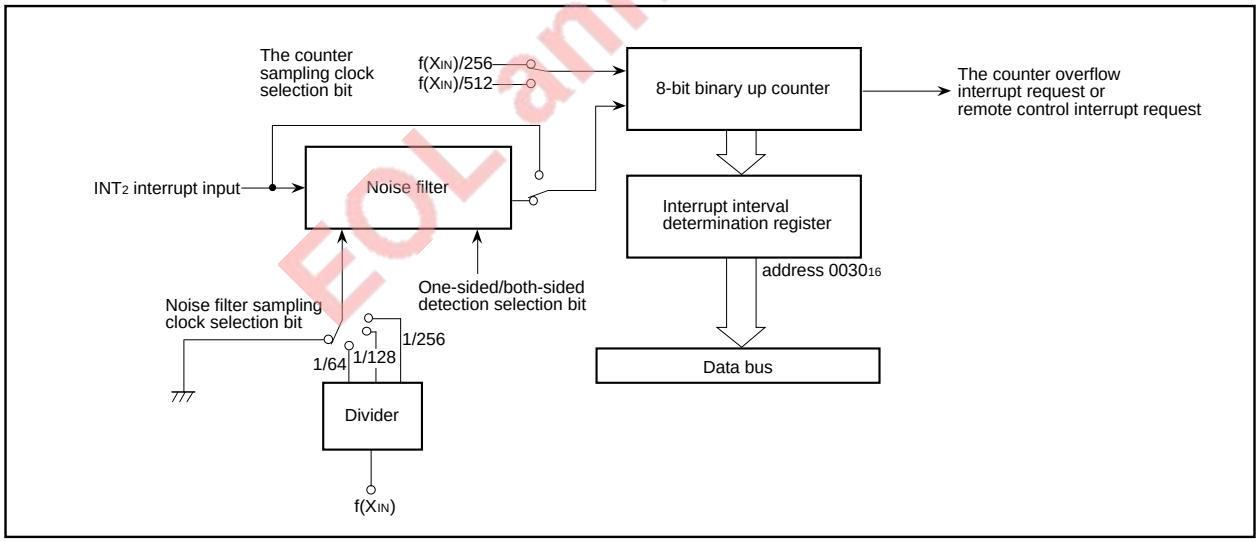


Fig. 35 Block diagram of interrupt interval datermination circuit

Downloaded from Elcodis.com electronic components distributor

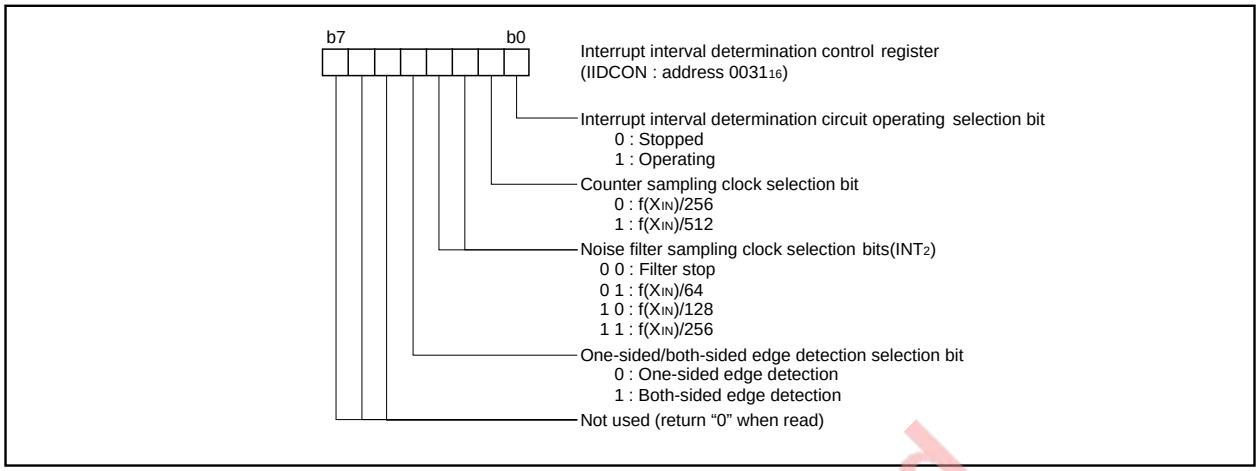


Fig. 36 Structure of interrupt interval determination control register

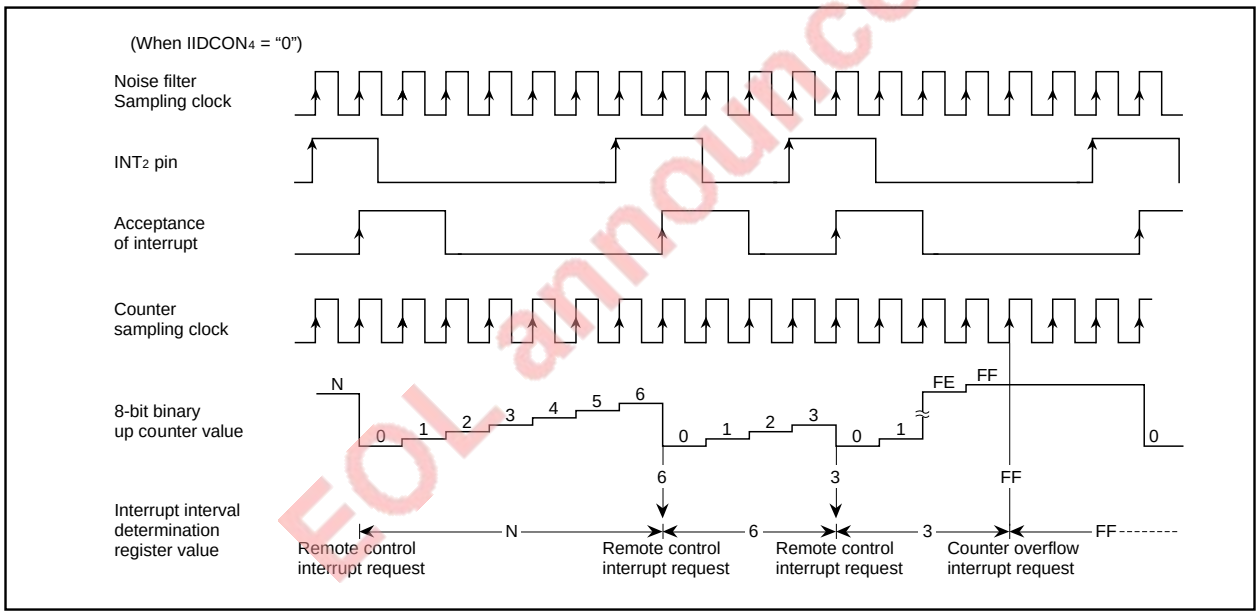


Fig. 37 Interrupt interval determination operation example (at rising edge active)

EOL announced

Renesas Technology Corp.
Downloaded from Elcodis.com electronic components distributor

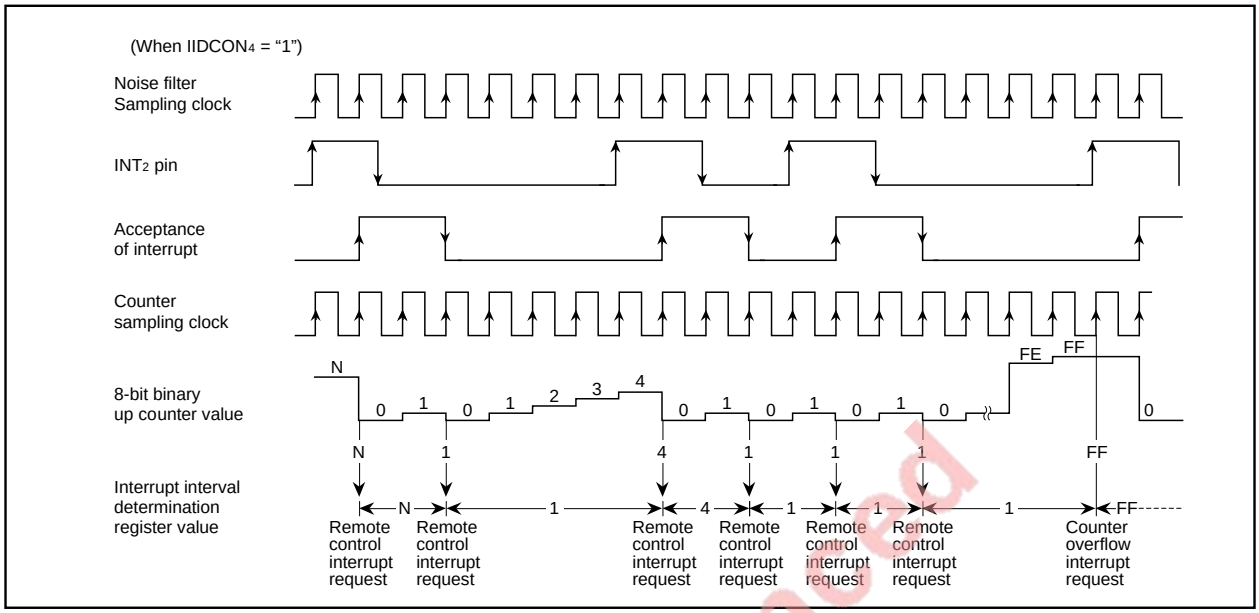


Fig. 38 Interrupt interval determination operation example (at both-sided edge active)

EOL announced

Downloaded from Elcodis.com electronic components distributor

ZERO CROSS DETECTION CIRCUIT

The zero cross detection circuit compares the voltage applied to P45/INT1/ZCR pin and VSS. The result can be read from the zero cross detection circuit input bit (bit 7) of the zero cross detection control register. It is set to "1" when the input voltage is higher than VSS and to "0" when it is lower than VSS. The input signal to P45/INT1/ZCR pin can select to either pass through the zero cross detection comparator or not to do.

When using 100 V AC as input signal, insert an external circuit between it and P45/INT1/ZCR pin. Set the input current limiting resistors used in the external circuit to a value which satisfies the absolute maximum rating of port P45.

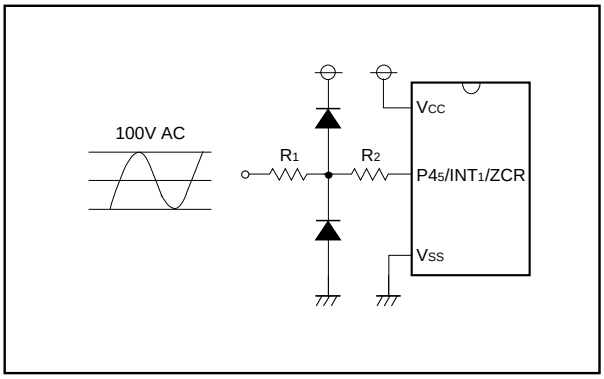


Fig. 39 External circuit example for zero cross detection

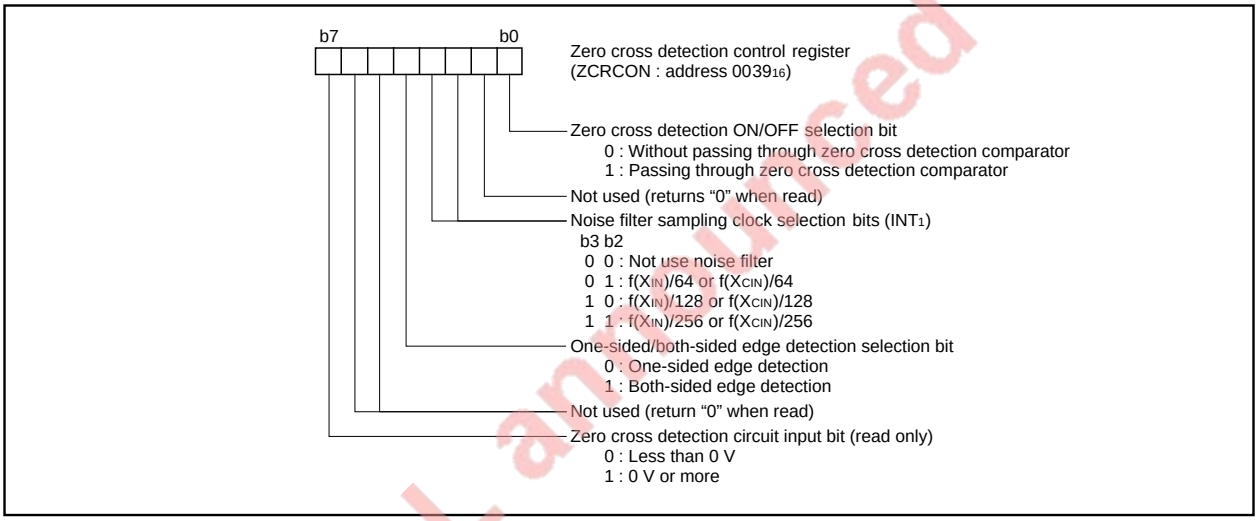


Fig. 40 Structure of zero cross detection control register

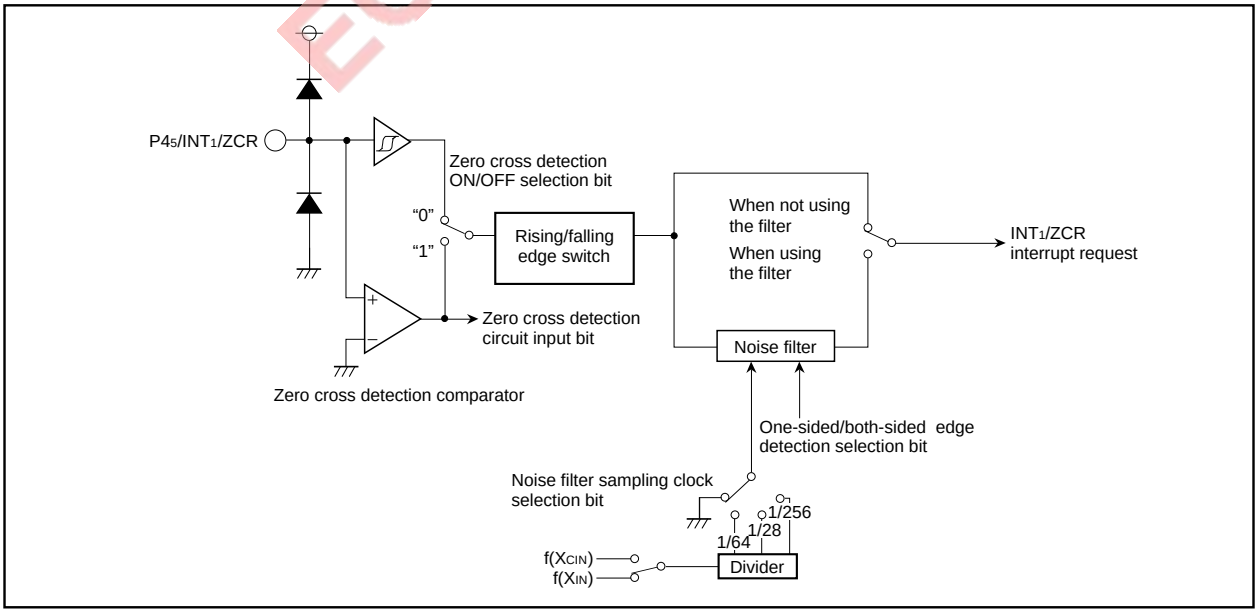


Fig. 41 Block diagram of zero cross detection circuit

EOL announced

RENESAS
Renesas Technology Corp.

Downloaded from Elcodis.com electronic components distributor

NOISE FILTER

The noise filter uses a sampling clock to remove the noise component digitally from the input signal of P45/INT1/ZCR pin. The sampling clock can be selected from 8 µs, 16 µs, or 32 µs (at f(XIN)= 8.38 MHz) and this is used to change the noise component to be removed. It is also possible to generate an internal trigger and INT1/ZCR interrupt request directly without passing through the noise filter. When passing through the noise filter, either both-sided edge detection or one-sided edge detection can be selected as the interrupt request generating source. The zero cross detection control register is used for this selection. Furthermore, switch between rising edge and falling edge is performed with the bit 1 of the interrupt edge selection register (address 003A16).

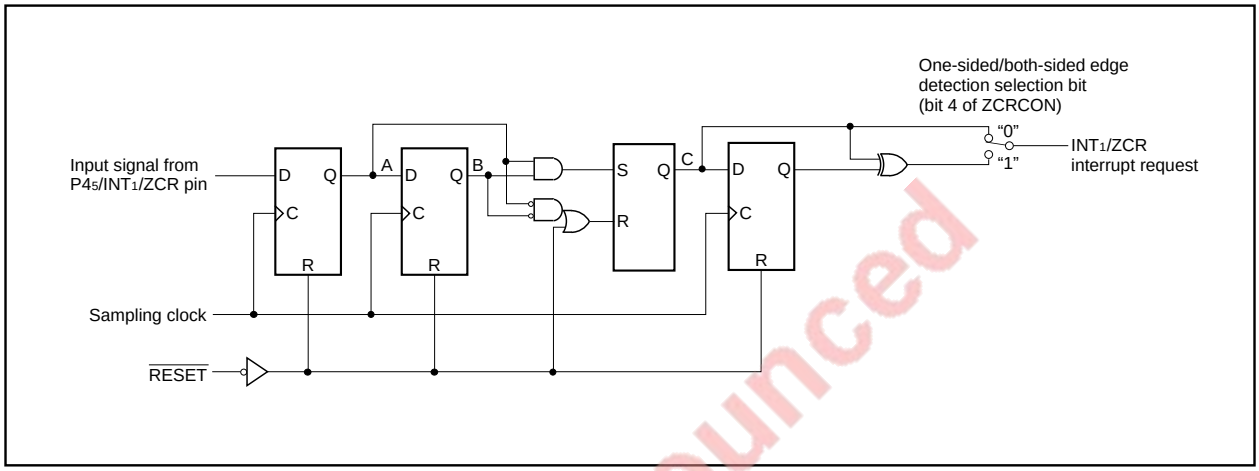


Fig. 42 Noise filter circuit diagram

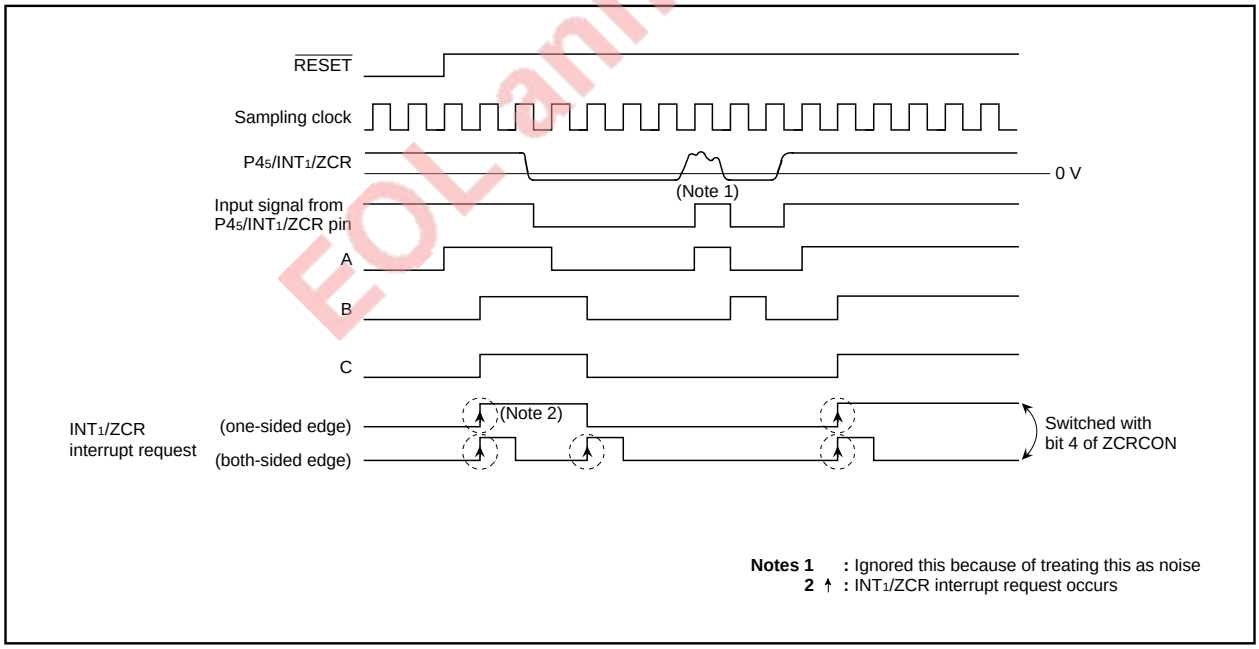


Fig. 43 Timing of noise filter circuit

EOL announced

Downloaded from Elcodis.com electronic components distributor

RESET CIRCUIT

To reset the microcomputer, $\overline{\text{RESET}}$ pin should be held at an "L" level for 2 µs or more. Then the $\overline{\text{RESET}}$ pin is returned to an "H" level (the power source voltage should be between 2.8 V and 5.5 V, and X_{IN} oscillation is stable), reset is released. In order to give the X_{IN} clock time to stabilize, internal operation does not begin until after about 4000 X_{IN} clock cycles (256 cycles of f(X_{IN})/16) are completed. After the reset is completed, the program starts from the address contained in address $FFFD_{16}$ (high-order) and address $FFFC_{16}$ (low-order). Make sure that the reset input voltage is 0.5 V or less for 2.8 V of V_{CC}.

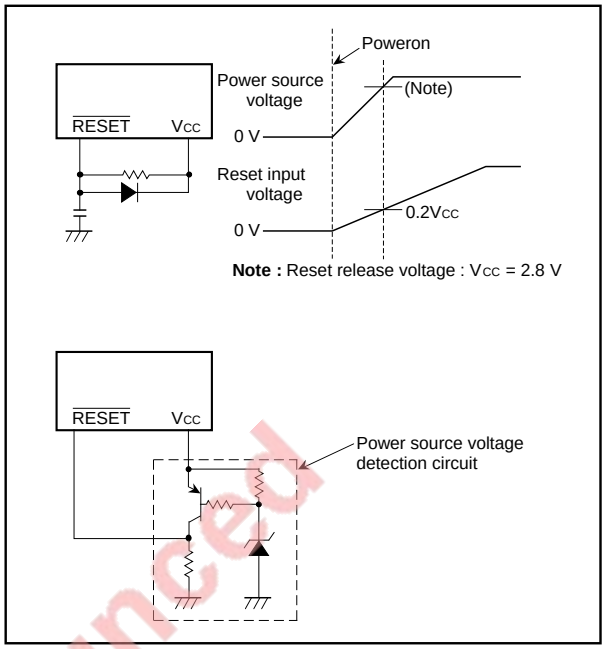


Fig. 44 Example of reset circuit

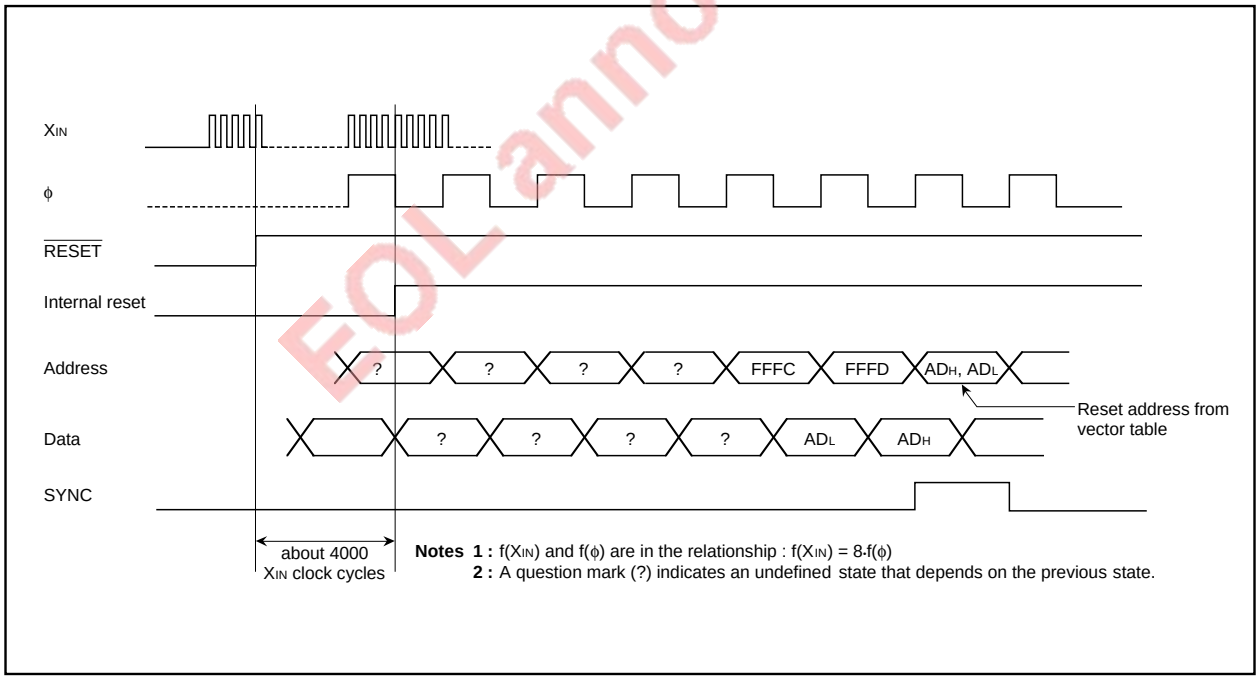


Fig. 45 Reset sequence

EOL announced

Downloaded from Elcodis.com electronic components distributor

	Address	Register contents
(1) Port P0	(0000_{16})···	00_{16}
(2) Port P1	(0002_{16})···	00_{16}
(3) Port P2	(0004_{16})···	00_{16}
(4) Port P2 direction register	(0005_{16})···	$0F_{16}$
(5) Port P3	(0006_{16})···	00_{16}
(6) Port P4	(0008_{16})···	00_{16}
(7) Port P4 direction register	(0009_{16})···	00_{16}
(8) Port P5	($000A_{16}$)···	00_{16}
(9) Port P5 direction register	($000B_{16}$)···	00_{16}
(10) Port P6	($000C_{16}$)···	00_{16}
(11) Port P6 direction register	($000D_{16}$)···	00_{16}
(12) Port P7	($000E_{16}$)···	00_{16}
(13) Port P7 direction register	($000F_{16}$)···	00_{16}
(14) Port P8	(0010_{16})···	00_{16}
(15) Port P8 direction register	(0011_{16})···	00_{16}
(16) Port P9	(0012_{16})···	00_{16}
(17) Port PA	(0014_{16})···	00_{16}
(18) Port PA direction register	(0015_{16})···	00_{16}
(19) Port PB	(0016_{16})···	00_{16}
(20) Port PB direction register	(0017_{16})···	00_{16}
(21) Serial I/O1 control register	(0019_{16})···	00_{16}
(22) Serial I/O automatic transfer control register	($001A_{16}$)···	00_{16}
(23) Serial I/O automatic transfer interval register	($001C_{16}$)···	00_{16}
(24) Serial I/O2 control register	($001D_{16}$)···	00_{16}
(25) Serial I/O3 control register	($001E_{16}$)···	00_{16}
(26) Timer 1	(0020_{16})···	FF_{16}
(27) Timer 2	(0021_{16})···	01_{16}
(28) Timer 3	(0022_{16})···	FF_{16}
(29) Timer 4	(0023_{16})···	FF_{16}
(30) Timer 5	(0024_{16})···	FF_{16}

	Address	Register contents
(31) Timer 6	(0025_{16})···	FF_{16}
(32) Timer 12 mode register	(0028_{16})···	00_{16}
(33) Timer 34 mode register	(0029_{16})···	00_{16}
(34) Timer 56 mode register	($002A_{16}$)···	00_{16}
(35) D-A conversion register	($002B_{16}$)···	00_{16}
(36) AD/DA control register	($002C_{16}$)···	10_{16}
(37) Interrupt interval determination control register	(0031_{16})···	00_{16}
(38) Port P0 segment/digit switch register	(0032_{16})···	00_{16}
(39) Port P2 digit/port switching register	(0033_{16})···	00_{16}
(40) Port P8 segment/port switch register	(0034_{16})···	00_{16}
(41) Port PA segment/port switch	(0035_{16})···	00_{16}
(42) FLDC mode register 1	(0036_{16})···	00_{16}
(43) FLDC mode register 2	(0037_{16})···	00_{16}
(44) Zero cross detection control register	(0039_{16})···	00_{16}
(45) Interrupt edge selection register	($003A_{16}$)···	00_{16}
(46) CPU mode register	($003B_{16}$)···	0 1 0 0 1 0 0 0
(47) Interrupt request register 1	($003C_{16}$)···	00_{16}
(48) Interrupt request register 2	($003D_{16}$)···	00_{16}
(49) Interrupt control register 1	($003E_{16}$)···	00_{16}
(50) Interrupt control register 2	($003F_{16}$)···	00_{16}
(51) Processor status register	(PS)···	X X X X X 1 X X
(52) Program counter	(PC_H)···	Contents of address $FFFD_{16}$
	(PC_L)···	Contents of address $FFFC_{16}$

Note : X : Undefined
The contents of all other registers and RAM are undefined at reset, so set their initial values.

Fig. 46 Internal status at reset

EOL announced

Downloaded from Elcodis.com electronic components distributor

CLOCK GENERATING CIRCUIT

The 3819 group has two built-in oscillation circuits. An oscillation circuit can be formed by connecting a resonator between XIN and XOUT (XCIN and XCOUT). Use the circuit constants in accordance with the resonator manufacturer's recommended values. No external resistor is needed between XIN and XOUT since a feed-back resistor exists on-chip. However, an external feed-back resistor is needed between XCIN and XCOUT.

Immediately after poweron, only the XIN oscillation circuit starts oscillation, and XCIN and XCOUT pins function as I/O ports.

Frequency Control

Middle-speed mode

The internal clock ϕ is the frequency of XIN divided by 8. After reset, this mode is selected.

High-speed mode

The internal clock ϕ is half the frequency of XIN.

Low-speed mode

The internal clock ϕ is half the frequency of XCIN.

Note : If you switch the mode between middle/high-speed and low-speed, stabilize both XIN and XCIN oscillations. The sufficient time is required for the XCIN oscillation to stabilize, especially immediately after poweron and at returning from stop mode. When switching the mode between middle/high-speed and low-speed, set the frequency on condition that f(XIN) > 3·f(XCIN).

Low-power dissipation mode

When stopping the main clock XIN in the low-speed mode, the low-power dissipation operation starts. To stop the main clock, set the bit 5 of the CPU mode register to "1". When the main clock XIN is restarted, set enough time for oscillation to stabilize by programming.

The low-power dissipation operation 200 µA or less (at f(XIN) = 32 kHz) can be realized by reducing the XCIN–XCOUT drivability. To reduce the XCIN–XCOUT drivability, clear the bit 3 of the CPU mode register to "0". At reset or when executing the STP instruction, this bit is set to "1" and strong drivability is selected to help the oscillation to start.

Oscillation Control

Stop mode

If the STP instruction is executed, the internal clock ϕ stops at an "H" level, and XIN and XCIN oscillators stop. Timer 1 is set to "FF16" and timer 2 is set to "0116". Either XIN or XCIN divided by 16 is input to timer 1, and the output of timer 1 is connected to timer 2. The bits of the timer 12 mode register are cleared to "0". Set the timer 1 and timer 2 interrupt enable bits to disabled ("0") before executing the STP instruction.

Oscillator restarts at reset or when an external interrupt is received, but the internal clock ϕ is not supplied to the CPU until timer 1 underflows. When using an external resonator, it is necessary for oscillating to stabilize.

Wait mode

If the WIT instruction is executed, the internal clock ϕ stops at an "H" level. The states of XIN and XCIN are the same as the state before executing the WIT instruction. The internal clock restarts at reset or when an interrupt is received. Since the oscillator does not stop, normal operation can be started immediately after the clock is restarted.

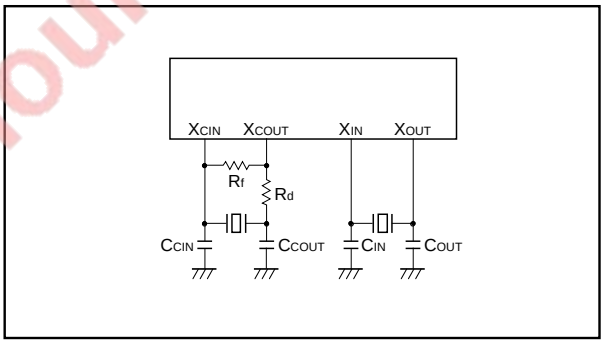


Fig. 47 Ceramic resonator external circuit

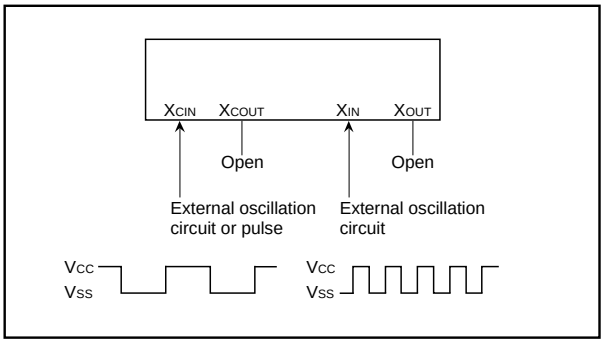
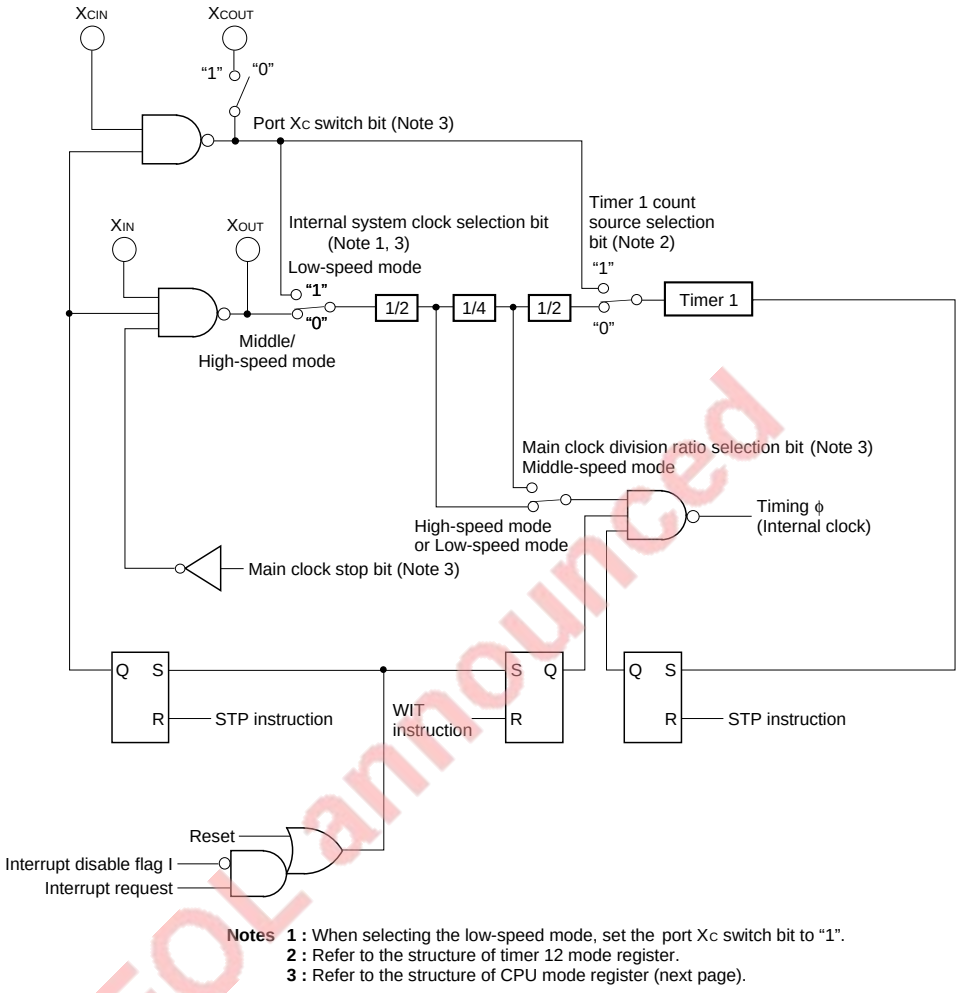


Fig. 48 External clock input circuit

End announced

Renesas Technology Corp.

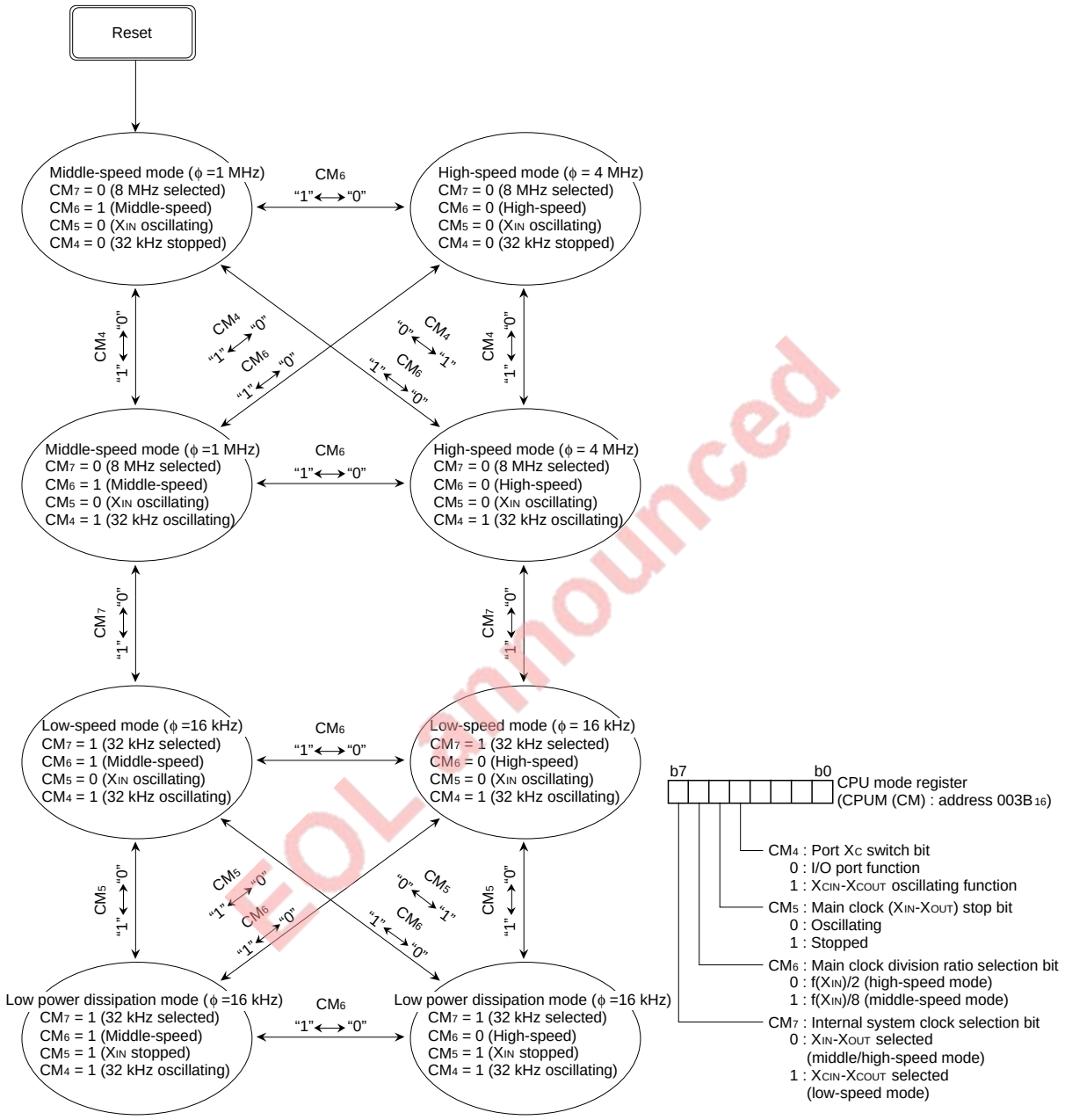
Downloaded from Elcodis.com electronic components distributor



EOL announced

Fig. 49 Clock generating circuit block diagram

Downloaded from Elcodis.com electronic components distributor



EOL announced

Notes 1 : Switch the mode by the allows shown between the mode blocks. (Do not switch between the mode directly without an allow.)
2 : The all modes can be switched to the stop mode or the wait mode and return to the source mode when the stop mode or the wait mode is ended.
Timer operates in the wait mode.
3 : When the stop mode is released in middle/high-speed mode, a delay of approximately 0.5 ms occurs automatically by timer 1.
4 : When the stop mode is released in low-speed mode, a delay of approximately 0.125 s occurs automatically by timer 1.
5 : The example assumes that 8 MHz is being applied to the XIN pin and 32 kHz to the XCIN pin. ϕ indicates the internal clock.

Fig. 50 State transitions of system clock

Downloaded from Elcodis.com electronic components distributor

NOTES ON PROGRAMMING

Processor Status Register

The contents of the processor status register (PS) after a reset are undefined, except for the interrupt disable flag (I) which is "1". After a reset, initialize flags which affect program execution. In particular, it is essential to initialize the index X mode (T) and the decimal mode (D) flags because of their effect on calculations.

Interrupts

The contents of the interrupt request bits do not change immediately after they have been written. After writing to an interrupt request register, execute at least one instruction before performing a BBC or BBS instruction.

Decimal Calculations

- To calculate in decimal notation, set the decimal mode flag (D) to "1", then execute an ADC or SBC instruction. Only the ADC and SBC instructions yield proper decimal results. After executing an ADC or SBC instruction, execute at least one instruction before executing a SEC, CLC, or CLD instruction.
- In decimal mode, the values of the negative (N), overflow (V), and zero (Z) flag are invalid.
  The carry flag can be used to indicate whether a carry or borrow has occurred. Initialize the carry flag before each calculation. Clear the carry flag before an ADC and set the flag before an SBC.

Timers

If a value n (between 0 and 255) is written to a timer latch, the frequency division ratio is 1/(n+1).

Multiplication and Division Instructions

- The index X mode (T) and the decimal mode (D) flags do not affect the MUL and DIV instruction.
- The execution of these instructions does not change the contents of the processor status register.

Ports

The contents of the port direction registers cannot be read. The following cannot be used:

- the data transfer instruction (LDA, etc.)
- the operation instruction when the index X mode flag (T) is "1"
- the addressing mode which uses the value of a direction register as an index
- the bit-test instruction (BBC or BBS, etc.) to a direction register
- the read-modify-write instructions (ROR, CLB, or SEB, etc.) to a direction register.

Use instructions such as LDM and STA, etc., to set the port direction registers.

Serial I/O

When using an external clock, input "H" to the external clock input pin and clear the serial I/O interrupt request bit before executing serial I/O transfer and serial I/O automatic transfer.
When using the internal clock, set the synchronous clock to internal clock, then clear the serial I/O interrupt request bit before executing a serial I/O transfer and serial I/O automatic transfer.

A-D Converter

The comparator uses internal capacitors whose charge will be lost if the clock frequency is too low.
Make sure that f(XIN) is 500 kHz or more during an A-D conversion.
Do not execute the STP or WIT instruction during an A-D conversion.

Instruction Execution Time

The instruction execution time is obtained by multiplying the frequency of the internal clock ϕ by the number of cycles needed to execute an instruction.
The number of cycles required to execute an instruction is shown in the list of machine instructions. The frequency of the internal clock ϕ is half of the XIN or XCIN frequency.

At the STP Instruction Release

At the STP instruction release, all bits of the timer 12 mode register are cleared.
The XCOUT drivability selection bit (the CPU mode register) is set to "1" (high drive) in order to start oscillating.

EOL announced

Downloaded from Elcodis.com electronic components distributor

DATA REQUIRED FOR MASK ORDERS

The following are necessary when ordering a mask ROM production:

(1) Mask ROM Order Confirmation Form
(2) Mark Specification Form
(3) Data to be written to ROM, in EPROM form (three identical copies)

PROM PROGRAMMING METHOD

The built-in PROM of the blank One Time PROM version and built-in EPROM version can be read or programmed with a general-purpose PROM programmer using a special programming adapter.

Package	Name of Programming Adapter
100P6S-A	PCA4738F-100A
100D0	PCA4738L-100A

Set the address of PROM programmer in the user ROM area.
The PROM of the blank One Time PROM version is not tested or screened in the assembly process and following processes. To ensure proper operation after writing, the procedure shown in Figure 51 is recommended to verify programming.

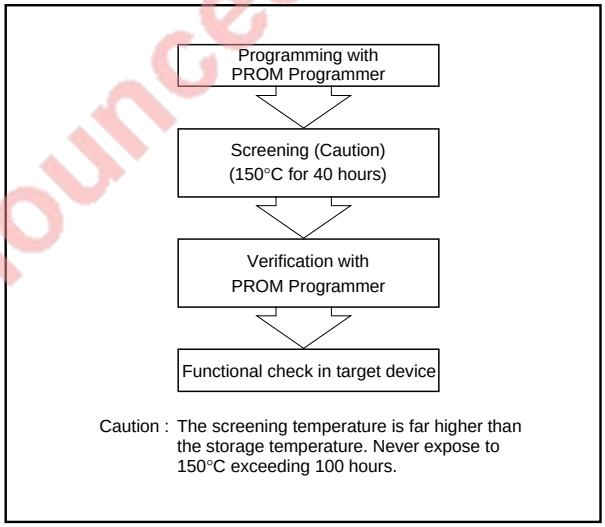


Fig. 51 Programming and testing of One Time PROM version

EOL announced

Downloaded from Elcodis.com electronic components distributor

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Power source voltage	All voltages are based on V_{SS}. Output transistors are cut off.	–0.3 to 7.0	V
V_{EE}	Pull-down power source voltage		V_{CC} –40 to V_{CC} +0.3	V
V_I	Input voltage $P2_4$–$P2_7$, $P4_1$–$P4_4$, $P4_6$, $P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_7$, $P7_0$–$P7_7$, PB_0–PB_3		–0.3 to V_{CC} +0.3	V
V_I	Input voltage $P4_0$, $P4_5$		–0.3 to V_{CC} +0.3	V
V_I	Input voltage $P8_0$–$P8_7$, PA_0–PA_7		V_{CC} –40 to V_{CC} +0.3	V
V_I	Input voltage $\overline{RESET}$, X_{IN}		–0.3 to V_{CC} +0.3	V
V_I	Input voltage X_{CIN}		–0.3 to V_{CC} +0.3	V
V_O	Output voltage $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_3$, $P3_0$–$P3_7$, $P8_0$–$P8_7$, $P9_0$–$P9_7$, PA_0–PA_7		V_{CC} –40 to V_{CC} +0.3	V
V_O	Output voltage $P2_4$–$P2_7$, $P4_1$–$P4_4$, $P4_6$, $P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_7$, $P7_0$–$P7_7$, PB_0–PB_3, X_{OUT}, X_{COUT}		–0.3 to V_{CC} +0.3	V
P_d	Power dissipation	T_a = 25°C	600	mW
T_{opr}	Operating temperature		–10 to 85	°C
T_{stg}	Storage temperature		–40 to 125	°C

RECOMMENDED OPERATING CONDITIONS

(V_{CC} = 4.0 to 5.5 V, T_a = –10 to 85°C, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min.	Typ.	Max.	
V_{CC}	Power source voltage	High-speed mode	4.0	5.0	5.5	V
		Middle/Low-speed mode	2.8	5.0	5.5	V
V_{SS}	Power source voltage			0		V
V_{EE}	Pull-down power source voltage		V_{CC}–38		V_{CC}	V
V_{REF}	Analog reference voltage (when using A-D converter)		2.0		V_{CC}	V
	Analog reference voltage (when using D-A converter)		3.0		V_{CC}	V
AV_{SS}	Analog power source voltage			0		V
V_{IA}	Analog input voltage AN_0–AN_{15}		0		V_{CC}	V
V_{IH}	“H” input voltage $P4_0$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_7$, $P7_0$–$P7_7$, PB_0–PB_3		0.75V_{CC}		V_{CC}	V
V_{IH}	“H” input voltage $P2_4$–$P2_7$		0.4V_{CC}		V_{CC}	V
V_{IH}	“H” input voltage $P8_0$–$P8_7$, PA_0–PA_7		0.8V_{CC}		V_{CC}	V
V_{IH}	“H” input voltage $\overline{RESET}$		0.8V_{CC}		V_{CC}	V
V_{IH}	“H” input voltage X_{IN}, X_{CIN}		0.8V_{CC}		V_{CC}	V
V_{IL}	“L” input voltage $P4_0$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_7$, $P7_0$–$P7_7$, PB_0–PB_3		0		0.25V_{CC}	V
V_{IL}	“L” input voltage $P2_4$–$P2_7$		0		0.16V_{CC}	V
V_{IL}	“L” input voltage $P8_0$–$P8_7$, PA_0–PA_7		0		0.2V_{CC}	V
V_{IL}	“L” input voltage $\overline{RESET}$		0		0.2V_{CC}	V
V_{IL}	“L” input voltage X_{IN}, X_{CIN}		0		0.2V_{CC}	V

Not announced

Downloaded from Elcodis.com electronic components distributor

RECOMMENDED OPERATING CONDITIONS (Vcc = 4.0 to 5.5 V, Ta = –10 to 85°C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
$\Sigma I_{OH(peak)}$	"H" total peak output current (Note 1) $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$–$P3_7$, $P8_0$–$P8_7$, $P9_0$–$P9_7$, PA_6, PA_7			–240	mA
	"H" total peak output current (Note 1) $P4_1$–$P4_4$, $P4_6$, $P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_7$, $P7_0$–$P7_7$, PA_0–PA_5, PB_0–PB_3			–60	mA
$\Sigma I_{OL(peak)}$	"L" total peak output current (Note 1) $P2_4$–$P2_7$, $P4_1$–$P4_4$, $P4_6$, $P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_7$, $P7_0$–$P7_7$, PB_0–PB_3			100	mA
$\Sigma I_{OH(avg)}$	"H" total average output current (Note 1) $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$–$P3_7$, $P8_0$–$P8_7$, $P9_0$–$P9_7$, PA_6, PA_7			–120	mA
	"H" total average output current (Note 1) $P4_1$–$P4_4$, $P4_6$, $P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_7$, $P7_0$–$P7_7$, PA_0–PA_5, PB_0–PB_3			–30	mA
$\Sigma I_{OL(avg)}$	"L" total average output current (Note 1) $P2_4$–$P2_7$, $P4_1$–$P4_4$, $P4_6$, $P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_7$, $P7_0$–$P7_7$, PB_0–PB_3			50	mA
$I_{OH(peak)}$	"H" peak output current (Note 2) $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_3$, $P3_0$–$P3_7$, $P8_0$–$P8_7$, $P9_0$–$P9_7$, PA_0–PA_7			–40	mA
$I_{OH(peak)}$	"H" peak output current (Note 2) $P2_4$–$P2_7$, $P4_1$–$P4_4$, $P4_6$, $P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_7$, $P7_0$–$P7_7$, PB_0–PB_3			–10	mA
$I_{OL(peak)}$	"L" peak output current (Note 3) $P2_4$–$P2_7$, $P4_1$–$P4_4$, $P4_6$, $P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_7$, $P7_0$–$P7_7$, PB_0–PB_3			10	mA
$I_{OH(avg)}$	"H" average output current (Note 3) $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_3$, $P3_0$–$P3_7$, $P8_0$–$P8_7$, $P9_0$–$P9_7$, PA_0–PA_7			–18	mA
$I_{OH(avg)}$	"H" average output current (Note 3) $P2_4$–$P2_7$, $P4_1$–$P4_4$, $P4_6$, $P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_7$, $P7_0$–$P7_7$, PB_0–PB_3			–5.0	mA
$I_{OL(avg)}$	"L" average output current (Note 3) $P2_4$–$P2_7$, $P4_1$–$P4_4$, $P4_6$, $P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_7$, $P7_0$–$P7_7$, PB_0–PB_3			5.0	mA
$f(CNTR_0)$ $f(CNTR_1)$	Clock input frequency for timers 2 and 4 (duty cycle 50%)			250	kHz
$f(X_{IN})$	Main clock input oscillation frequency (Note 4)			8.4	MHz
$f(X_{CIN})$	Sub-clock input oscillation frequency (Note 4, 5)		32.768	50	kHz

Notes 1 : The total output current is the sum of all the currents flowing through all the applicable ports.The total average current is an average value measured over 100 ms. The total peak current is the peak value of all the currents.
2 : The peak output current is the peak current flowing in each port.
3 : The average output current in an average value measured over 100 ms.
4 : When the oscillation frequency has a 50% duty cycle.
5 : When using the microcomputer in low-speed operation mode, set the sub-clock input oscillation frequency on condition that $f(X_{CIN}) < f(X_{IN})/3$.

EOL announced

Downloaded from Elcodis.com electronic components distributor

ELECTRICAL CHARACTERISTICS (Vcc = 4.0 to 5.5 V, Ta = –10 to 85°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
VOH	"H" output voltage P00–P07, P10–P17, P20–P23, P30–P37, P80–P87, P90–P97, PA0–PA7	IOH=–18 mA	Vcc–2.0			V
VOH	"H" output voltage P24–P27, P41–P44, P46, P47, P50–P57, P60–P67, P70–P77, PB0–PB3	IOH=–10 mA	Vcc–2.0			V
VOL	"L" output voltage P24–P27, P41–P44, P46, P47, P50–P57, P60–P67, P70–P77, PB0–PB3	IOL=10 mA			2.0	V
VT+–VT–	Hysteresis $\overline{INT0}$–$\overline{INT4}$, SIN1, SIN2, SIN3, SCLK11, SCLK2, SCLK3, $\overline{CS}$, CNTR0, CNTR1	When using a non-port function		0.4		V
VT+–VT–	Hysteresis $\overline{RESET}$, XIN			0.5		V
VT+–VT–	Hysteresis XCIN			0.5		V
IH	"H" input current P24–P27, P40–P47, P50–P57, P60–P67, P70–P77, PB0–PB3	VI=VCC			5.0	µA
IH	"H" input current P80–P87, PA0–PA7 (Note)	VI=VCC			5.0	µA
IH	"H" input current $\overline{RESET}$, XCIN	VI=VCC			5.0	µA
IH	"H" input current XIN	VI=VCC		4.0		µA
IL	"L" input current P24–P27, P40–P47, P50–P57, P60–P67, P70–P77, PB0–PB3	VI=VSS			–5.0	µA
IL	"L" input current P80–P87, PA0–PA7 (Note)	VI=VSS			–5.0	µA
IL	"L" input current $\overline{RESET}$, XCIN	VI=VSS			–5.0	µA
IL	"L" input current XIN	VI=VSS		–4.0		µA
ILOAD	Output load current P00–P07, P10–P17, P20–P23, P30–P37, P90–P97	VEE=VCC–36 V, VOL=VCC, Output transistors "off"	150	500	900	µA
ILEAK	Output leakage current P00–P07, P10–P17, P20–P23, P30–P37, P80–P87, P90–P97, PA0–PA7	VEE=VCC–38 V, VOL=VCC–38 V, Output transistors "off"			–10	µA
VRAM	RAM hold voltage	When clock is stopped	2		5.5	V

Note : Except when reading ports P8 or PA.

EOL announced

Downloaded from Elcodis.com electronic components distributor

ELECTRICAL CHARACTERISTICS (V_{CC} = 4.0 to 5.5 V, T_a = –10 to 85°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
I_{CC}	Power source current	• High-speed mode $f(X_{IN})$ = 8.4 MHz $f(X_{CIN})$ = 32 kHz Output transistors “off”		7.5	15	mA
		• High-speed mode $f(X_{IN})$ = 8.4 MHz (in WIT state) $f(X_{CIN})$ = 32 kHz Output transistors “off”		1		mA
		• Middle-speed mode $f(X_{IN})$ = 8.4 MHz $f(X_{CIN})$ = stopped Output transistors “off”		3		mA
		• Middle-speed mode $f(X_{IN})$ = 8.4 MHz (in WIT state) $f(X_{CIN})$ = stopped Output transistors “off”		1		mA
		• Low-speed mode $f(X_{IN})$ = stopped, $f(X_{CIN})$ = 32 kHz Low-power dissipation mode set (CM_3) = 0 Output transistors “off”		60	200	µA
		• Low-speed mode $f(X_{IN})$ = stopped $f(X_{CIN})$ = 32 kHz (in WIT state) Low-power dissipation mode set (CM_3) = 0 Output transistors “off”		20	40	µA
		Increase at A-D converter operating $f(X_{IN})$ = 8.4 MHz		0.6		mA
		Increase at zero cross detection ($P4_5$ = V_{CC})		1		mA
		All oscillation stopped (in STP state) Output transistors “off” T_a = 25°C		0.1	1	µA
		All oscillation stopped (in STP state) Output transistors “off” T_a = 85°C			10	µA

EOL announced

Downloaded from Elcodis.com electronic components distributor

ZERO CROSS DETECTION INPUT CHARACTERISTICS

(V_{CC} = 4.0 to 5.5 V, V_{SS} = 0 V, T_a = –10 to 85°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
f_{ZCR}	Input frequency of zero cross detection			50, 60	1000	Hz
ΔV_T	Voltage error of zero cross detection distinction	50 Hz or 60 Hz	–100	0	100	mV

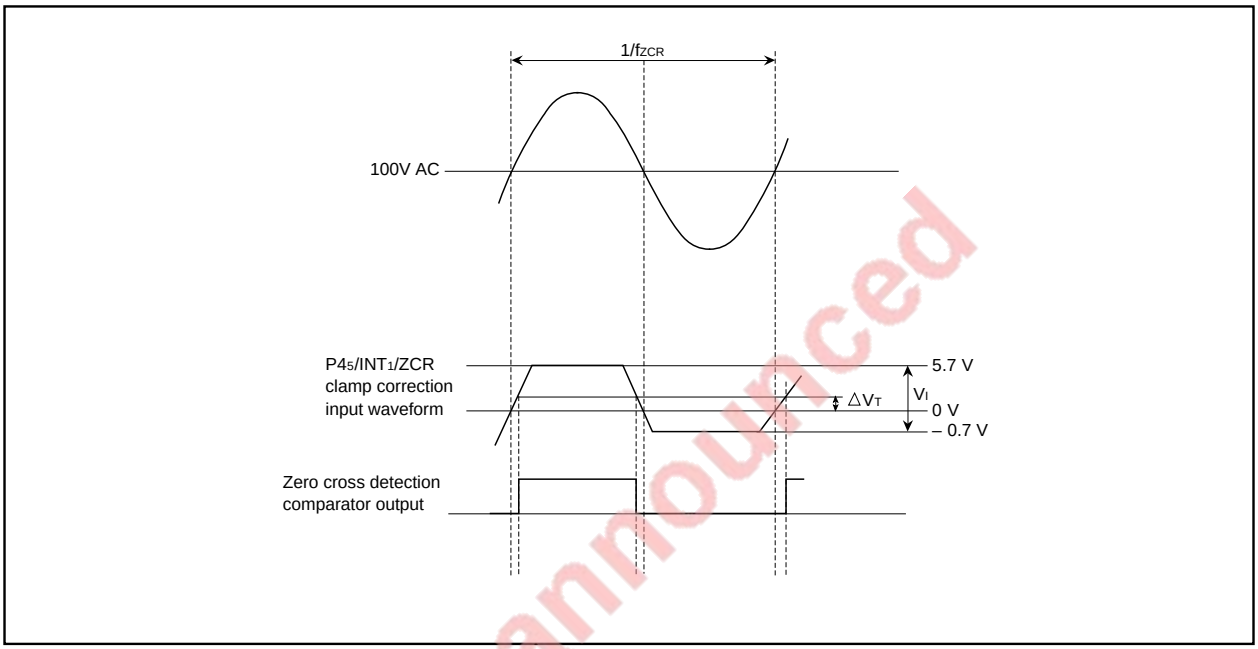


Fig. 52 Zero cross detection input characteristics

A-D CONVERTER CHARACTERISTICS

(V_{CC} = 4.0 to 5.5 V, V_{SS} = 0 V, T_a = –10 to 85°C, high-speed operation mode f(X_{IN}) = 500 kHz to 8.4 MHz, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
–	Resolution				8	Bits
–	Absolute accuracy (excluding quantization error)	V_{CC} = V_{REF} = 5.12 V		±1	±2.5	LSB
T_{CONV}	Conversion time		49		50	t_c (ϕ)
I_{VREF}	Reference power source input current	V_{REF} = 5 V	50	150	200	µA
I_{IA}	Analog port input current			0.5	5.0	µA
R_{LADDER}	Ladder resistor			35		kΩ

D-A CONVERTER CHARACTERISTICS

(V_{CC} = 4.0 to 5.5 V, V_{SS} = AV_{SS} = 0 V, V_{REF} = 3.0 to V_{CC}, T_a = –10 to 85°C, unless otherwise noted)

Symbol	Parameter		Test conditions	Limits			Unit
				Min.	Typ.	Max.	
–	Resolution					8	Bits
–	Absolute accuracy	V_{CC} = 4.0 to 5.5 V				1.0	%
		V_{CC} = 3.0 to 5.5 V				2.5	%
T_{su}	Setting time					3	µs
R_O	Output resistor			1	2.5	4	kΩ
I_{VREF}	Reference power source input current (Note)					3.2	mA

Note : Exclude currents flowing through the A-D converter ladder resistor

ECL announced

Downloaded from Elcodis.com electronic components distributor

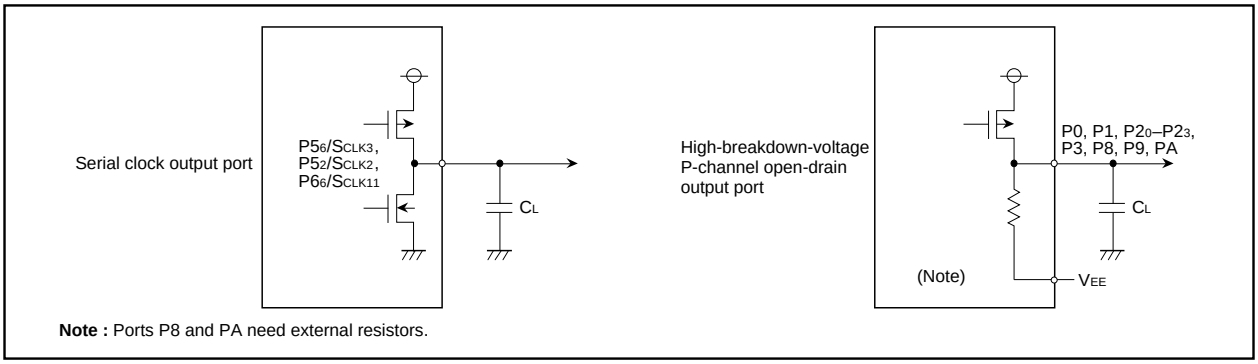
TIMING REQUIREMENTS (V_{CC} = 4.0 to 5.5 V, V_{SS} = 0 V, T_a = –10 to 85°C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
$t_{W(\overline{RESET})}$	Reset input “L” pulse width	2.0			µs
$t_{C(X_{IN})}$	Main clock input cycle time (X_{IN} input)	119			ns
$t_{WH(X_{IN})}$	Main clock input “H” pulse width	30			ns
$t_{WL(X_{IN})}$	Main clock input “L” pulse width	30			ns
$t_{C(X_{CIN})}$	Sub-clock input cycle time (X_{CIN} input)	20			µs
$t_{WH(X_{CIN})}$	Sub-clock input “H” pulse width	5.0			µs
$t_{WL(X_{CIN})}$	Sub-clock input “L” pulse width	5.0			µs
$t_{C(CNTR)}$	$CNTR_0$, $CNTR_1$ input cycle time	4.0			µs
$t_{WH(CNTR)}$	$CNTR_0$, $CNTR_1$ input “H” pulse width	1.6			µs
$t_{WL(CNTR)}$	$CNTR_0$, $CNTR_1$ input “L” pulse width	1.6			µs
$t_{WH(INT)}$	INT_0–INT_4 input “H” pulse width	80			ns
$t_{WL(INT)}$	INT_0–INT_4 input “L” pulse width	80			ns
$t_{C(S_{CLK})}$	Serial I/O clock input cycle time	1.0			µs
$t_{WH(S_{CLK})}$	Serial I/O clock input “H” pulse width	400			ns
$t_{WL(S_{CLK})}$	Serial I/O clock input “L” pulse width	400			ns
$t_{su(S_{CLK}–S_{IN})}$	Serial I/O input setup time	200			ns
$t_{h(S_{CLK}–S_{IN})}$	Serial I/O input hold time	200			ns

SWITCHING CHARACTERISTICS (V_{CC} = 4.0 to 5.5 V, V_{SS} = 0 V, T_a = –10 to 85°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
$t_{WH(S_{CLK})}$	Serial I/O clock output “H” pulse width	C_L = 100 pF	$t_{C(S_{CLK})}$ /2–160			ns
$t_{WL(S_{CLK})}$	Serial I/O clock output “L” pulse width	C_L = 100 pF	$t_{C(S_{CLK})}$ /2–160			ns
$t_{d(S_{CLK}–S_{OUT})}$	Serial I/O output delay time				$0.2t_{C(S_{CLK})}$	ns
$t_{v(S_{CLK}–S_{OUT})}$	Serial I/O output hold time		0			ns
$t_{r(S_{CLK})}$	Serial I/O clock output rising time	C_L = 100 pF			40	ns
$t_{f(S_{CLK})}$	Serial I/O clock output falling time	C_L = 100 pF			40	ns
$t_{r(Pch–strg)}$	High-breakdown-voltage P-channel open-drain output rising time (Note 1)	C_L = 100 pF V_{EE} = V_{CC} –36 V		55		ns
$t_{f(Pch–weak)}$	High-breakdown-voltage P-channel open-drain output falling time (Note 2)	C_L = 100 pF V_{EE} = V_{CC} –36 V		1.8		µs

Notes 1: When the bit 7 of the FLDC mode register 1 (address 003616) is at “0”.
2: When the bit 7 of the FLDC mode register 1 (address 003616) is at “1”.



Note : Ports P8 and PA need external resistors.

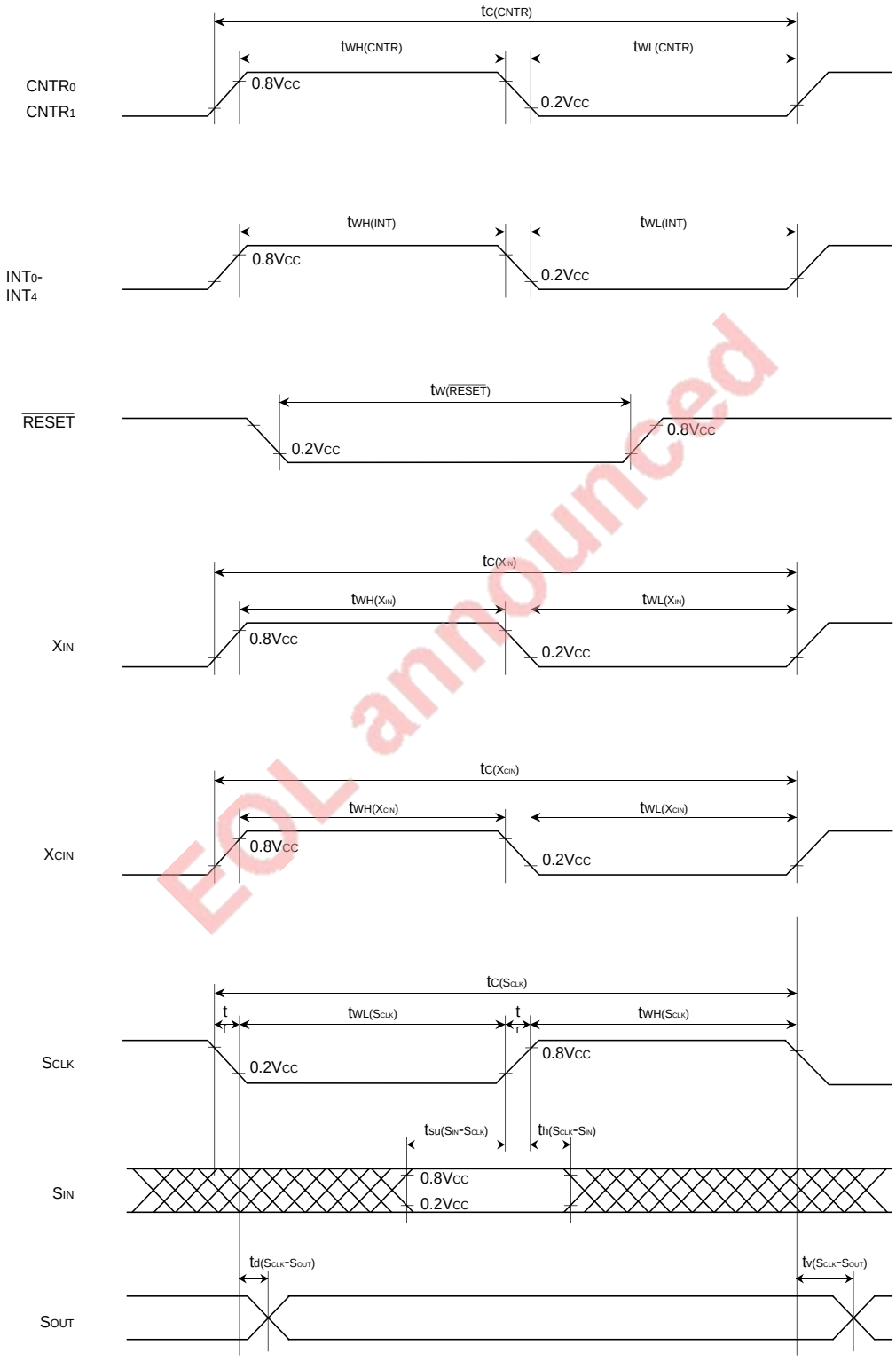
Fig. 53 Circuit for measuring output switching characteristics

Final announced

RENESAS
Renesas Technology Corp.

Downloaded from Elcodis.com electronic components distributor

TIMING DIAGRAM



EOL announced

Downloaded from Elcodis.com electronic components distributor

Power source current characteristic examples

Figures 54 and 55 show power source current characteristic examples.

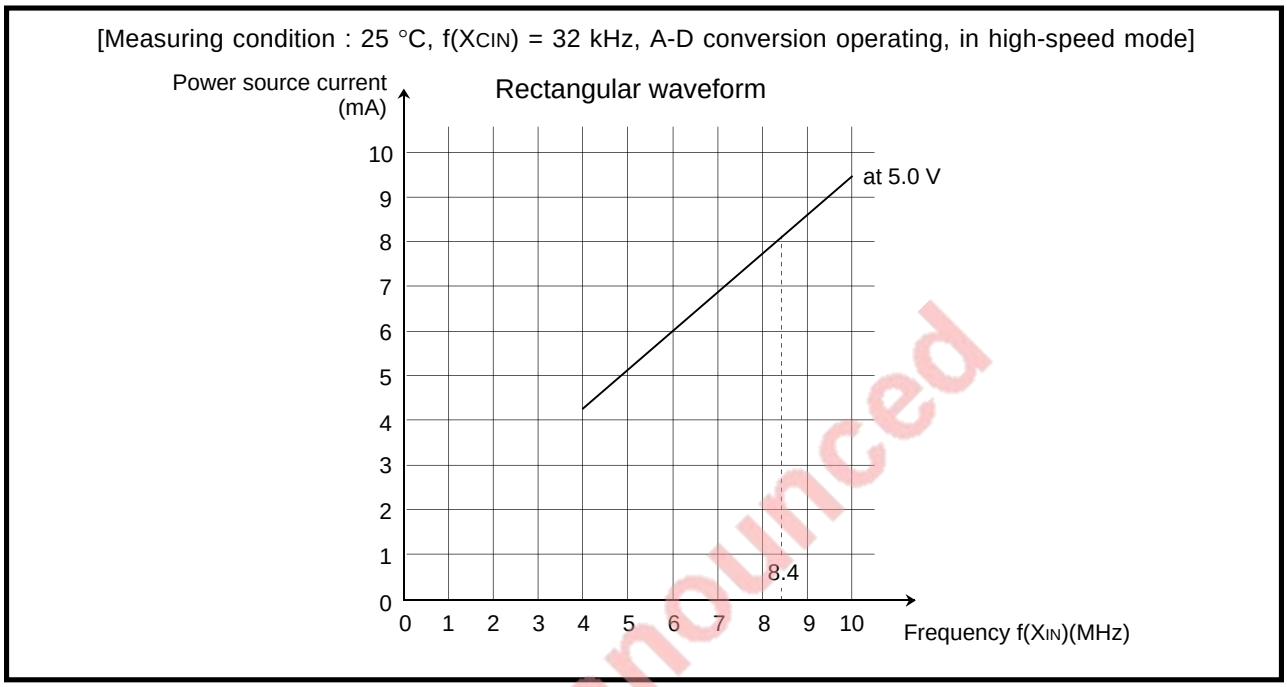


Fig. 54 Power source current characteristic example

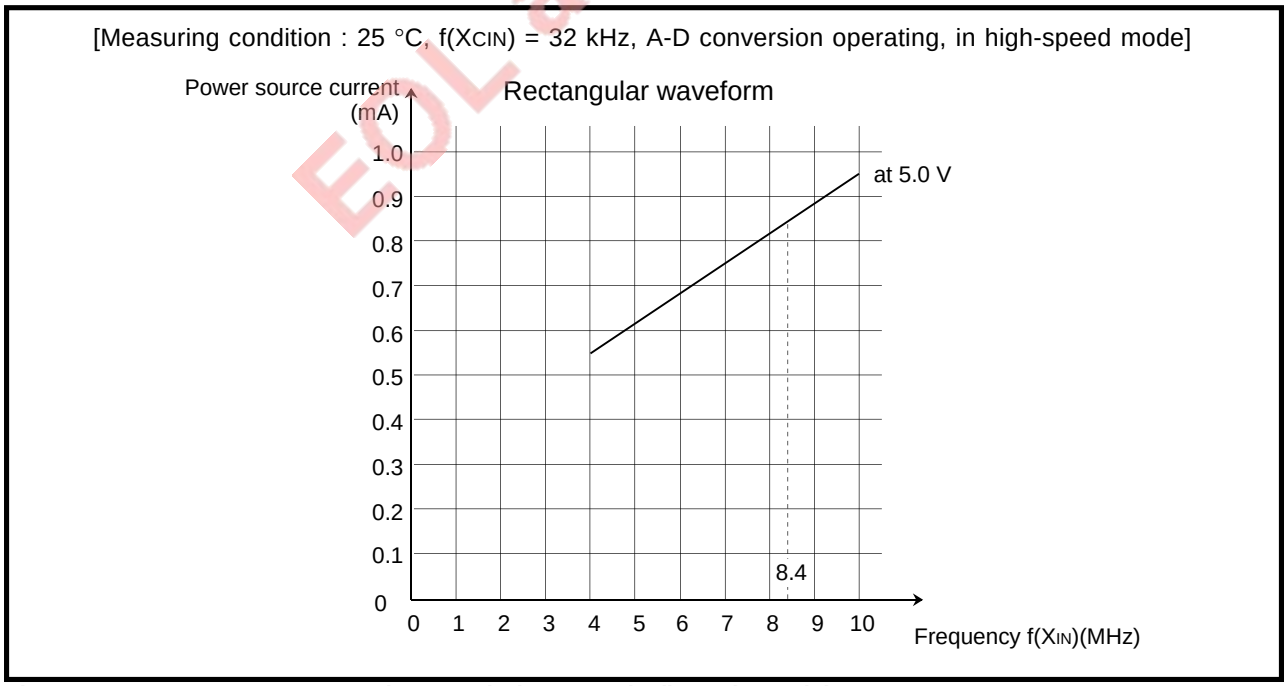


Fig. 55 Power source current characteristic example (in wait mode)

EOL announced

Downloaded from Elcodis.com electronic components distributor

Port standard characteristic examples

Figures 56, 57, and 58 show port standard characteristic examples.

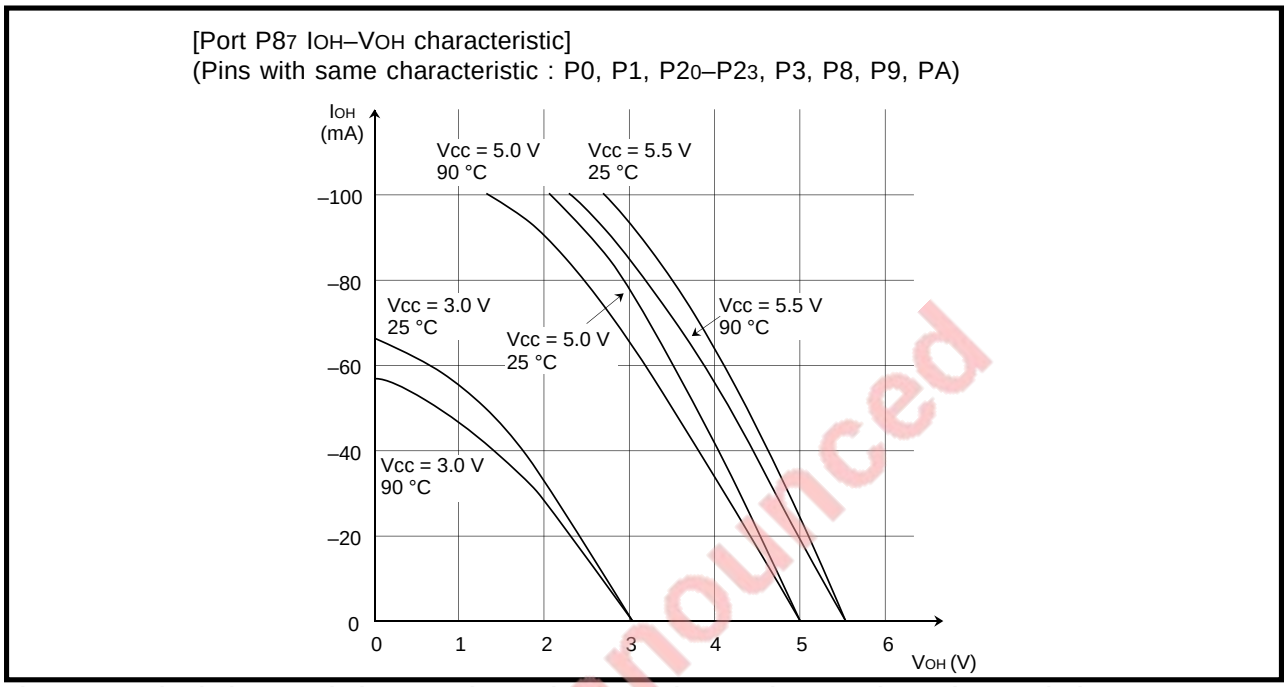


Fig. 56 Standard characteristic example of High-breakdown-voltage P-channel open-drain output port

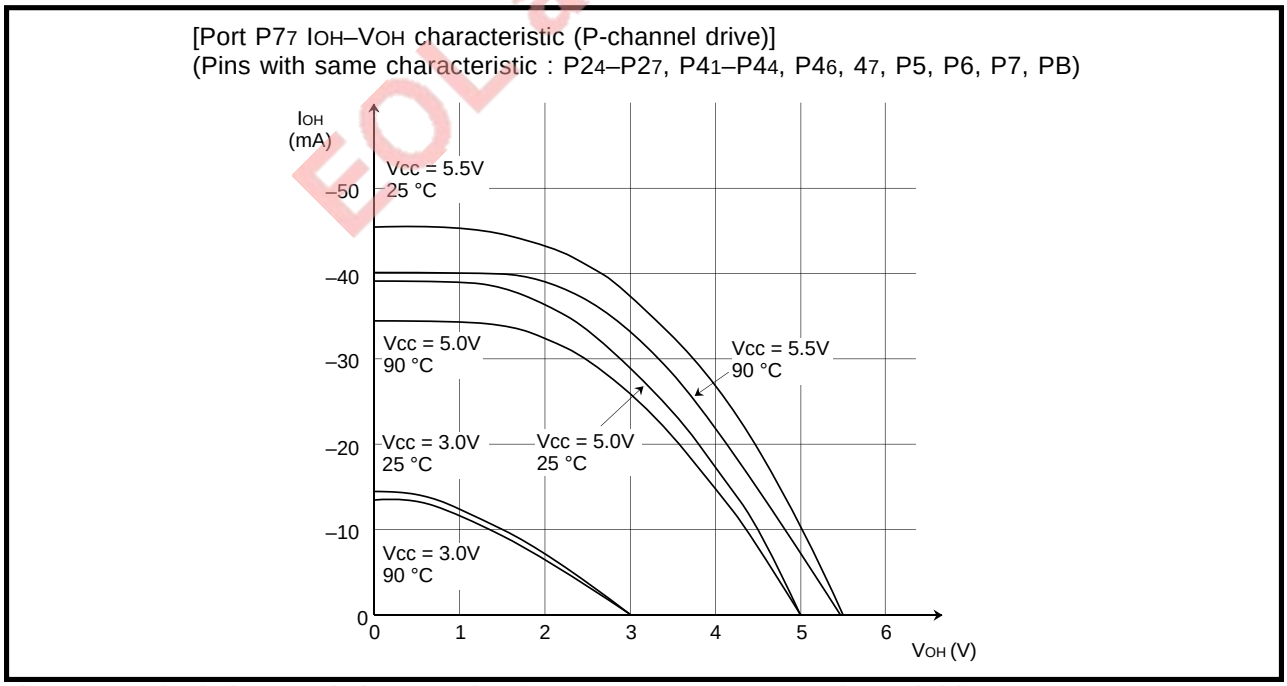


Fig. 57 Standard characteristic example of CMOS output port at P-channel drive

EOL announced

Downloaded from Elcodis.com electronic components distributor

[Port P77 IOL–VOL characteristic (N-channel drive)]
(Pins with same characteristic : P24–P27, P41–P44, P46, 47, P5, P6, P7, PB)

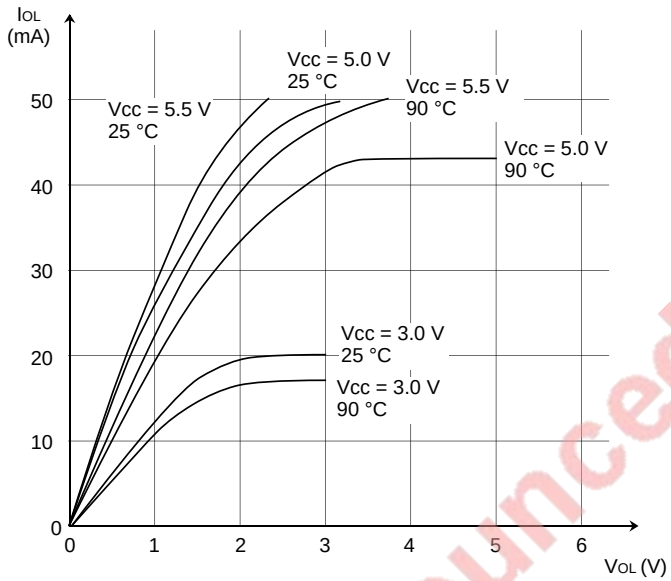


Fig. 58 Standard characteristic example of CMOS output port at N-channel drive

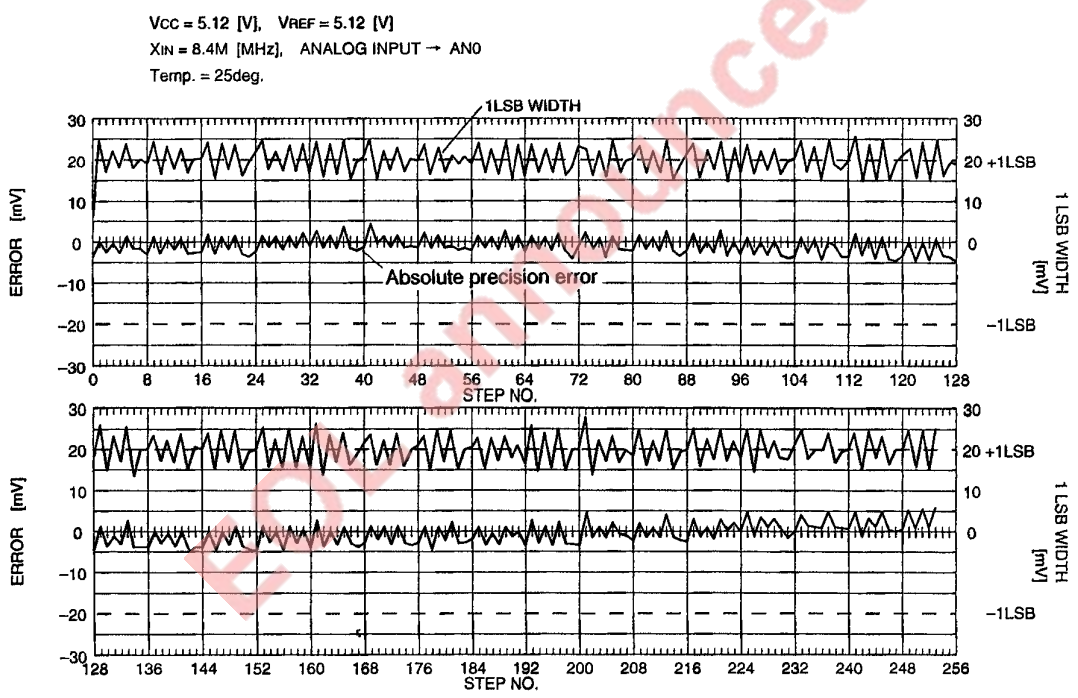
EOL announced

Downloaded from Elcodis.com electronic components distributor

A-D conversion standard characteristics

Figure 59 shows the A-D conversion standard characteristics.
The lower-side line on the graph indicates the absolute precision error. It represents the deviation from the ideal value. For example, the conversion of output code from 00_{16} to 01_{16} occurs ideally at the point of AN_0 = 10 mV, but the measured value is –4 mV. Accordingly, the measured point of conversion is represented as "10 – 4 = 6 mV".
The upper-side line on the graph indicates the width of input voltages equivalent to output codes. For example, the measured width of the input voltage for output code 49_{16} is 23 mV, so the differential nonlinear error is represented as "23 – 20 = 3 mV" (0.1 LSB).

M38197MA-000FP A-D CONVERTER STEP WIDTH MEASUREMENT



EOL announced

Measured when a power source voltage is stable in the high-speed mode

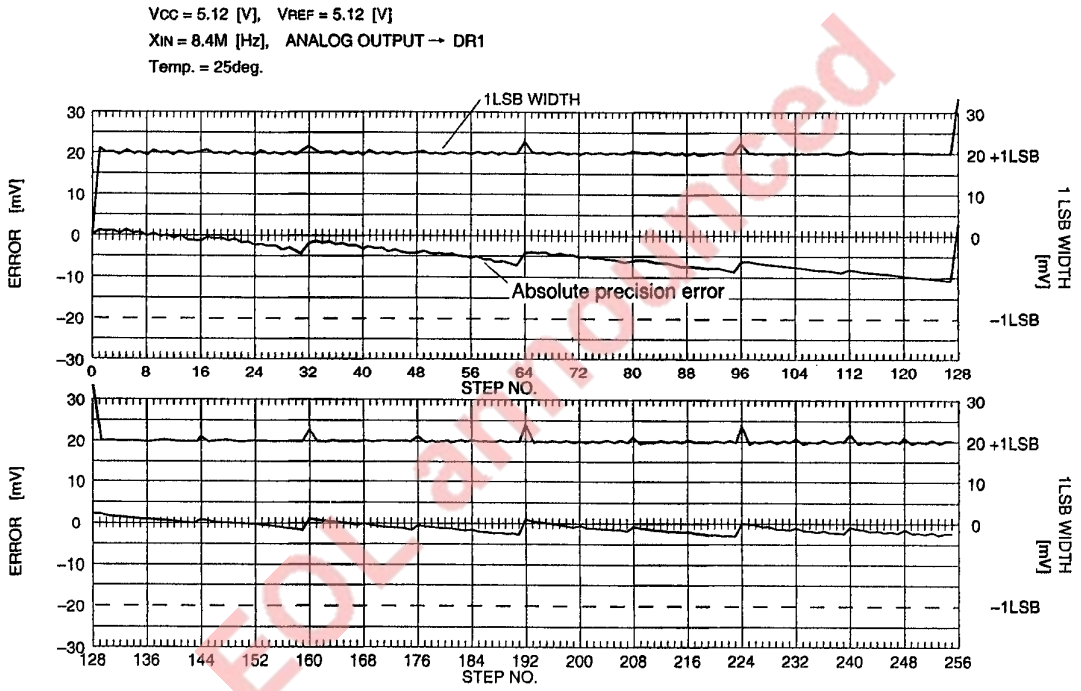
Fig. 59 A-D conversion standard characteristics

Downloaded from Elcodis.com electronic components distributor

D-A conversion standard characteristics

Figure 60 shows the D-A conversion standard characteristics. The lower-side line on the graph indicates the absolute precision error. In this case, it represents the difference between the ideal analog output value for an input code and the measured value.
The upper-side line on the graph indicates the change width of output analog value to a one-bit change of input code.

M38197EAFP D-A CONVERTER STEP WIDTH MEASUREMENT



Measured when a power source voltage is stable in the high-speed mode

Fig. 60 D-A conversion standard characteristics

EOL announced

Downloaded from Elcodis.com electronic components distributor

Functional description supplement

Interrupt

3819 group permits interrupts on the basis of 20 sources. It is vector interrupts with a fixed priority system. Accordingly, when two or more interrupt requests occur during the same sampling, the higher-priority interrupt is accepted first. This priority is determined by hardware, but variety of priority processing can be performed by software, using an interrupt enable bit and an interrupt disable flag.
For interrupt sources, vector addresses and interrupt priority, refer to **"Table 5."**

Table 5. Interrupt sources, vector addresses and interrupt priority

Priority	Interrupt sources	Vector addresses		Remarks
		High-order	Low-order	
1	Reset (Note)	FFFD16	FFFC16	Non-maskable
2	INT0 interrupt	FFFB16	FFFA16	External interrupt (active edge selectable)
3	INT1/ZCR interrupt	FFF916	FFF816	External interrupt (active edge selectable)
4	INT2 interrupt	FFF716	FFF616	External interrupt (active edge selectable)
	Remote control/counter overflow interrupt			Valid when interrupt interval determination operates
5	Serial I/O 1 interrupt	FFF516	FFF416	Valid when serial I/O ordinary mode is selected
	Serial I/O 1 automatic transfer interrupt			Valid when serial I/O automatic transfer mode is selected
6	Serial I/O 2 interrupt	FFF316	FFF216	Valid when serial I/O 2 is selected
7	Serial I/O 3 interrupt	FFF116	FFF016	Valid when serial I/O 3 is selected
8	Timer 1 interrupt	FFEF16	FFEE16	STP release timer underflow
9	Timer 2 interrupt	FFED16	FFEC16	
10	Timer 3 interrupt	FFEB16	FFEA16	
11	Timer 4 interrupt	FFE916	FFE816	
12	Timer 5 interrupt	FFE716	FFE616	
13	Timer 6 interrupt	FFE516	FFE416	
14	INT3 interrupt	FFE316	FFE216	External interrupt (active edge selectable)
15	INT4 interrupt	FFE116	FFE016	Valid when INT4 interrupt is selected External interrupt (active edge selectable)
	A-D conversion interrupt			Valid when A-D converter interrupt is selected
16	FLD blanking interrupt	FFDF16	FFDE16	Valid when FLD blanking interrupt is selected
	FLD digit interrupt			Valid when FLD digit interrupt is selected
17	BRK instruction interrupt	FFDD16	FFDC16	Non-maskable software interrupt

Note : Reset functions in the same way as an interrupt with the highest priority.

EOL announced

Downloaded from Elcodis.com electronic components distributor

Timing after interrupt

The interrupt processing routine begins with the machine cycle following the completion of the instruction that is currently in execution.
Figure 61 shows a timing chart after an interrupt occurs, and figure 62 shows the time up to execution of the interrupt processing routine.

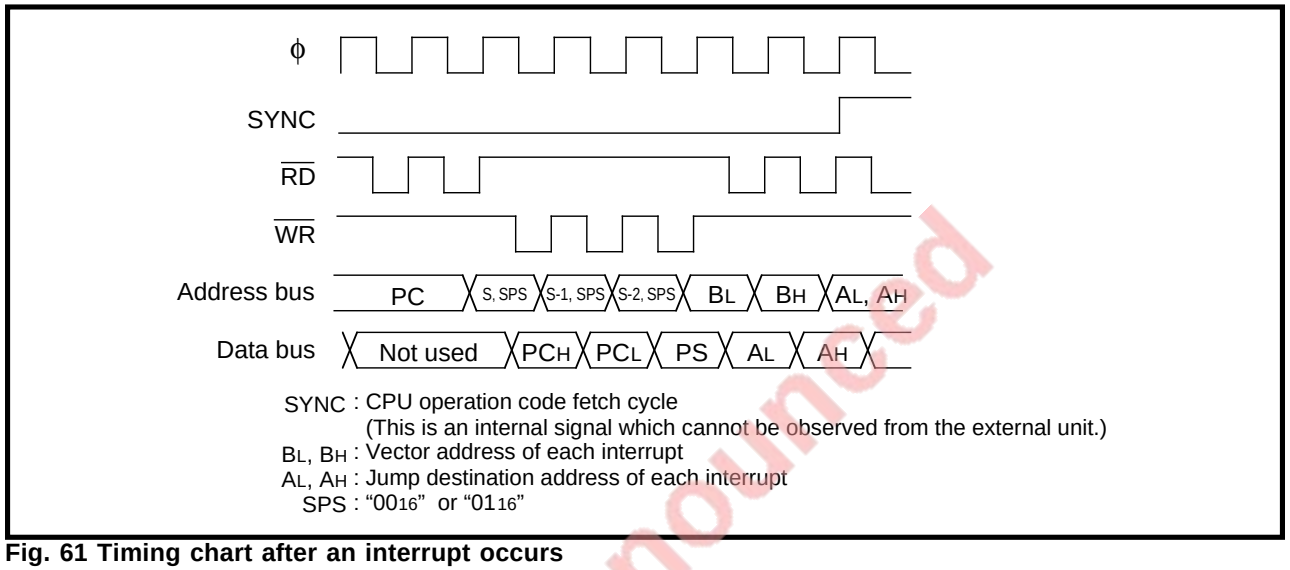


Fig. 61 Timing chart after an interrupt occurs

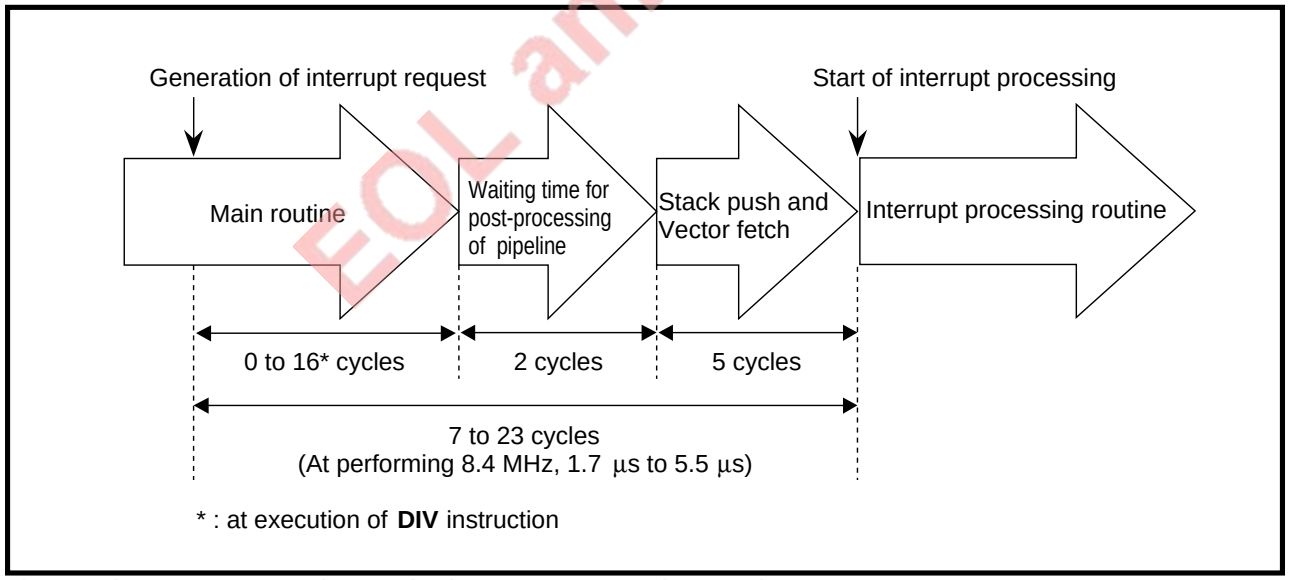


Fig. 62 Time up to execution of the interrupt processing routine

EOL announced

Downloaded from Elcodis.com electronic components distributor

A-D converter

A-D conversion is started by setting A-D conversion completion bit to "0". During A-D conversion, internal operations are performed as follows.

1. After the start of A-D conversion, A-D conversion register goes to "00$_{16}$."
2. The highest-order bit of A-D conversion register is set to "1", and the comparison voltage Vref is input to the comparator. Then, Vref is compared with analog input voltage V_{IN}.
3. As a result of comparison, when Vref < V_{IN}, the highest-order bit of A-D conversion register becomes "1." When Vref > V_{IN}, the highest-order bit becomes "0."

By repeating the above operations up to the lowest-order bit of the A-D conversion register, an analog value converts into a digital value.

A-D conversion completes at 50 clock cycles (11.9 µs at f(X_{IN}) = 8.4 MHz) after it is started, and the result of the conversion is stored into the A-D conversion register.

Concurrently with the completion of A-D conversion, A-D conversion interrupt request occurs, so that the A-D conversion interrupt request bit is set to "1".

Relative formula for a reference voltage V_{REF} of A-D converter and Vref

When n = 0 Vref = 0

When n = 1 to 255 $Vref = \frac{V_{REF}}{256} \times (n-0.5)$

n : the value of A-D converter (decimal numeral)

Table 6. Change of A-D conversion register during A-D conversion

	Change of A-D conversion register	Value of comparison voltage (Vref)
At start of conversion	0 0 0 0 0 0 0 0	0
First comparison	1 0 0 0 0 0 0 0	$\frac{V_{REF}}{2} - \frac{V_{REF}}{512}$
Second comparison	*1 1 0 0 0 0 0 0	$\frac{V_{REF}}{2} \pm \frac{V_{REF}}{4} - \frac{V_{REF}}{512}$
Third comparison	*1 *2 1 0 0 0 0 0	$\frac{V_{REF}}{2} \pm \frac{V_{REF}}{4} \pm \frac{V_{REF}}{8} - \frac{V_{REF}}{512}$
After completion of eighth comparison	A result of A-D conversion: *1 *2 *3 *4 *5 *6 *7 *8	

*1 : A result of the first comparison
*2 : A result of the second comparison
*3 : A result of the third comparison
*4 : A result of the fourth comparison
*5 : A result of the fifth comparison
*6 : A result of the sixth comparison
*7 : A result of the seventh comparison
*8 : A result of the eighth comparison

EOL announced

Downloaded from Elcodis.com electronic components distributor

Figures 63 shows A-D conversion equivalent circuit, and figure 64 shows A-D conversion timing chart.

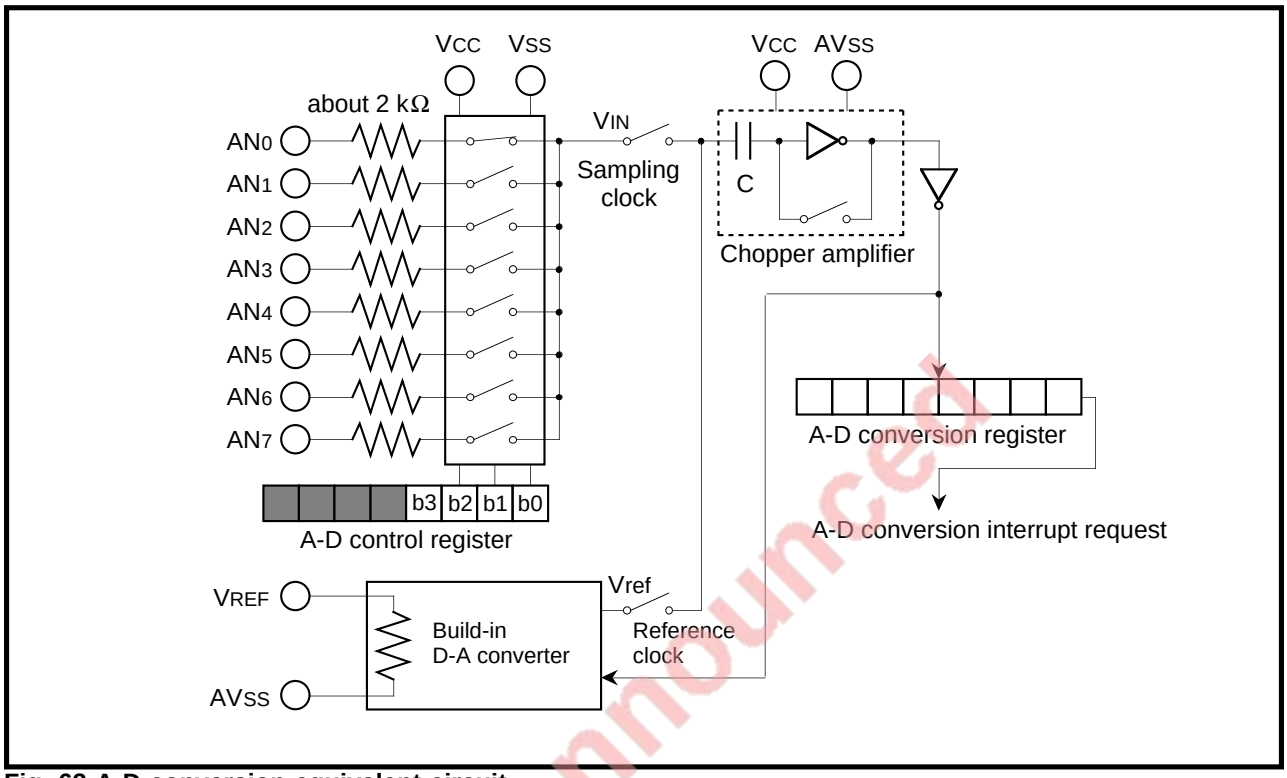


Fig. 63 A-D conversion equivalent circuit

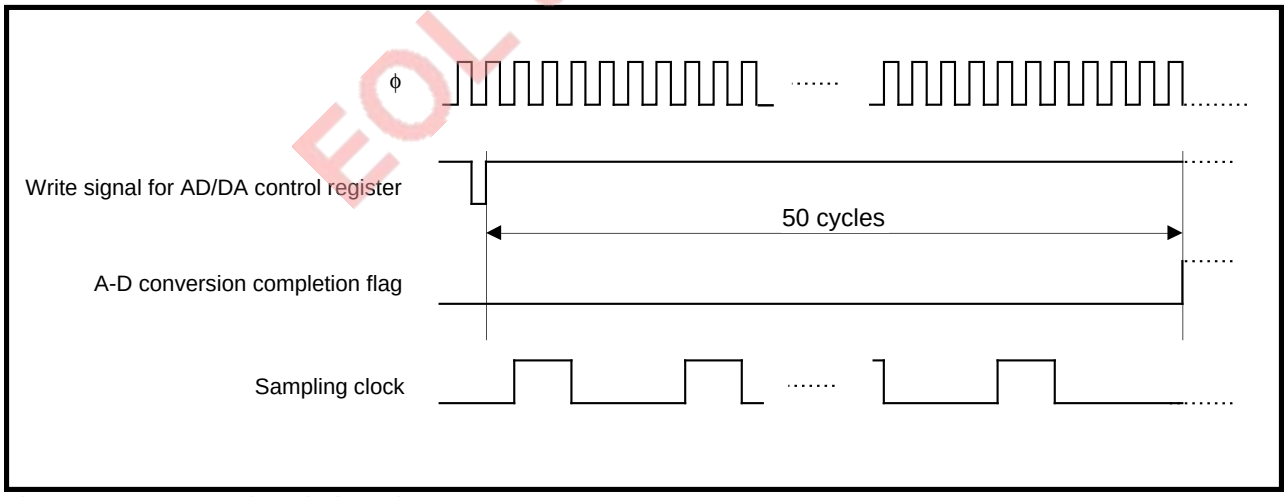


Fig. 64 A-D conversion timing chart

EOL announced

Renesas Technology Corp.

Downloaded from Elcodis.com electronic components distributor

CHAPTER 2

APPLICATION

EOL announced

Downloaded from Elcodis.com electronic components distributor

2. APPLICATION

2.1 I/O Port

2.1.1 Related registers

Port Pi

b7 b6 b5 b4 b3 b2 b1 b0

Port Pi (Pi) (i = 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, A, B)
[Address:00 16, 02 16, 04 16, 06 16, 08 16, 0A 16, 0C 16, 0E 16, 10 16, 12 16, 14 16, 16 16]

B	Name	Function	At reset	R	W
0	Port Pi_0	• In output mode Write } Port latch Read • In input mode Write : Port latch Read : Value of pins (Note)	0	○	○
1	Port Pi_1		0	○	○
2	Port Pi_2		0	○	○
3	Port Pi_3		0	○	○
4	Port Pi_4		0	○	○
5	Port Pi_5		0	○	○
6	Port Pi_6		0	○	○
7	Port Pi_7		0	○	○

Note : Port PB register [Address:16 16]
Port PB is a four-bit port (PB_0 to PB_3). Accordingly, when bits 4 to 7 are read out, the contents are "0."

Fig. 2.1.1 Structure of Port Pi (i = 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, A, B)

Port P2 direction register

b7 b6 b5 b4 b3 b2 b1 b0

Port P2 direction register (P2D) [Address:05 16]

B	Name	Function	At reset	R	W
0	Because $P2_0$ to $P2_3$ are output ports, these bits do not have a direction register function and nothing is allocated.		1	×	×
1			1	×	×
2			1	×	×
3			1	×	×
4	Port P2 direction register	0 : Port $P2_4$ input mode 1 : Port $P2_4$ output mode	0	×	○
5		0 : Port $P2_5$ input mode 1 : Port $P2_5$ output mode	0	×	○
6		0 : Port $P2_6$ input mode 1 : Port $P2_6$ output mode	0	×	○
7		0 : Port $P2_7$ input mode 1 : Port $P2_7$ output mode	0	×	○

Fig. 2.1.2 Structure of Port P2 direction register

EOL announced

Downloaded from Elcodis.com electronic components distributor

2. APPLICATION

Port Pi direction register

b7 b6 b5 b4 b3 b2 b1 b0

Port Pi direction register (PiD) (i = 4, 5, 6, 7, 8, A, B)
[Address:09 16, 0B16, 0D16, 0F16, 1116, 1516, 1716]

B	Name	Function	At reset	R	W
0	Port Pi direction register	0 : Port Pi0 input mode 1 : Port Pi0 output mode (**Note**)	0	×	○
1		0 : Port Pi1 input mode 1 : Port Pi1 output mode	0	×	○
2		0 : Port Pi2 input mode 1 : Port Pi2 output mode	0	×	○
3		0 : Port Pi3 input mode 1 : Port Pi3 output mode	0	×	○
4		0 : Port Pi4 input mode 1 : Port Pi4 output mode	0	×	○
5		0 : Port Pi5 input mode 1 : Port Pi5 output mode (**Note**)	0	×	○
6		0 : Port Pi6 input mode 1 : Port Pi6 output mode	0	×	○
7		0 : Port Pi7 input mode 1 : Port Pi7 output mode	0	×	○

Note : Port P4 direction register [Address:09 16]
Ports P40 and P45 are input ports. Accordingly, these bits do not have a direction register function.

Fig. 2.1.3 Structure of Port Pi direction register (i = 4, 5, 6, 7, 8, A, B)

2.1.2 Handling of unused pins

Table 2.1.1 Handling of unused pins

Name of Pins/Ports	Handling
P0, P1, P20–P23, P3, P9	Open
P24–P27, P41–P44, P46, P47, P5, P6, P7, P8, PA, PB	• Set to the input mode and connect to VCC or VSS through each resistor. • Set to the output mode and open at "L" or "H."
P40	Connect to VSS(GND) through the resistor.
P45	Connect to VCC through the resistor.
VEE, AVSS	Connect to VSS(GND).
VREF	Connect to VSS(GND) through the resistor.

EOL announced

Downloaded from Elcodis.com electronic components distributor

2. APPLICATION

2.2 Timer

2.2.1 Related registers

Timer i

b7	b6	b5	b4	b3	b2	b1	b0

Timer i (Ti) (i = 1, 3, 4, 5, 6)
[Address:20_{16}, 22_{16}, 23_{16}, 24_{16}, 25_{16}]

B	Function	At reset	R	W
0	● The count value of the Timer i is set. ● The value set in this register is written to both the Timer i and the Timer i latch at the same time. ● When the Timer i is read out, the value (count value) of the Timer i is read out.	1	○	○
1		1	○	○
2		1	○	○
3		1	○	○
4		1	○	○
5		1	○	○
6		1	○	○
7		1	○	○

Fig. 2.2.1 Structure of Timer i (i = 1, 3, 4, 5, 6)

Timer 2

b7	b6	b5	b4	b3	b2	b1	b0

Timer 2 (T2) [Address:21_{16}]

B	Function	At reset	R	W
0	● The count value of the Timer 2 is set. ● The value set in this register is written to both the Timer 2 and the Timer 2 latch at the same time. ● When the Timer 2 is read out, the value (count value) of the Timer 2 is read out.	1	○	○
1		0	○	○
2		0	○	○
3		0	○	○
4		0	○	○
5		0	○	○
6		0	○	○
7		0	○	○

Fig. 2.2.2 Structure of Timer 2

EOL announced

Downloaded from Elcodis.com electronic components distributor

2. APPLICATION

Timer 6 PWM register

b7	b6	b5	b4	b3	b2	b1	b0

Timer 6 PWM register (T6PWM) [Address:27_{16}]

B	Function	At reset	R	W
0	● In Timer 6 PWM mode Set the width of "L" of the PWM rectangular waveform. ● Duty of the PWM rectangular waveform : n/(n + m) Cycle : (n + m) × ts n = a set value of the Timer 6 m = a set value of the Timer 6 PWM register ts = a cycle of the Timer 6 count source ● Selection of the Timer 6 PWM mode Set the Timer 6 operation mode selection bit of the Timer 56 mode register (Address : $2A_{16}$) to "1".	?	○	○
1		?	○	○
2		?	○	○
3		?	○	○
4		?	○	○
5		?	○	○
6		?	○	○
7		?	○	○

Fig. 2.2.3 Structure of Timer 6 PWM register

Timer 12 mode register

b7	b6	b5	b4	b3	b2	b1	b0

Timer 12 mode register (T12M) [Address:28_{16}]

B	Name	Function	At reset	R	W
0	Timer 1 count stop bit	0 : Operating 1 : Stopped	0	○	○
1	Timer 2 count stop bit	0 : Operating 1 : Stopped	0	○	○
2	Timer 1 count source selection bit	0 : $f(X_{IN})/16$ or $f(X_{CIN})/16$ 1 : $f(X_{CIN})$	0	○	○
3	Nothing is allocated for this bit. It is a write disabled bit. When this bit is read out, the value is "0. "		0	○	×
4	Timer 2 count source selection bits	b5 b4 00 : Timer 1 underflow 01 : $f(X_{CIN})$ 10 : External count input $CNTR_0$ 11 : Not available	0	○	○
5			0	○	○
6	Timer 1 output selection bit ($P4_6$)	0 : I/O port 1 : Timer 1 output	0	○	○
7	Nothing is allocated for this bit. It is a write disabled bit. When this bit is read out, the value is "0. "		0	○	×

Fig. 2.2.4 Structure of Timer 12 mode register

EOL announced

Downloaded from Elcodis.com electronic components distributor

2. APPLICATION

Timer 34 mode register

b7 b6 b5 b4 b3 b2 b1 b0

Timer 34 mode register (T34M) [Address:29$_{16}$]

B	Name	Function	At reset	R	W
0	Timer 3 count stop bit	0 : Operating 1 : Stopped	0	○	○
1	Timer 4 count stop bit	0 : Operating 1 : Stopped	0	○	○
2	Timer 3 count source selection bit	0 : f(X$_{IN}$)/16 or f(X$_{CIN}$)/16 1 : Timer 2 underflow	0	○	○
3	Nothing is allocated for this bit. It is a write disabled bit. When this bit is read out, the value is "0. "		0	○	×
4	Timer 4 count source selection bits	b5 b4 00 : f(X$_{IN}$)/16 or f(X$_{CIN}$)/16 01 : Timer 3 underflow 10 : External count input CNTR$_1$ 11 : Not available	0	○	○
5			0	○	○
6	Timer 3 output selection bit (P4$_7$)	0 : I/O port 1 : Timer 3 output	0	○	○
7	Nothing is allocated for this bit. It is a write disabled bit. When this bit is read out, the value is "0. "		0	○	×

Fig. 2.2.5 Structure of Timer 34 mode register

Timer 56 mode register

b7 b6 b5 b4 b3 b2 b1 b0

0

Timer 56 mode register (T56M) [Address:2A$_{16}$]

B	Name	Function	At reset	R	W
0	Timer 5 count stop bit	0 : Operating 1 : Stopped	0	○	○
1	Timer 6 count stop bit	0 : Operating 1 : Stopped	0	○	○
2	Timer 5 count source selection bit	0 : f(X$_{IN}$)/16 or f(X$_{CIN}$)/16 1 : Timer 4 underflow	0	○	○
3	Timer 6 operation mode selection bit	0 : Timer mode 1 : PWM mode	0	○	○
4	Timer 6 count source selection bits	b5 b4 00 : f(X$_{IN}$)/16 or f(X$_{CIN}$)/16 01 : Timer 5 underflow 10 : Timer 4 underflow 11 : Not available	0	○	○
5			0	○	○
6	Timer 6 (PWM) output selection bit (P6$_1$)	0 : I/O port 1 : Timer 6 output	0	○	○
7	Fix this bit to "0."		0	○	○

Fig. 2.2.6 Structure of Timer 56 mode register

EOL announced

Downloaded from Elcodis.com electronic components distributor

2. APPLICATION

Interrupt request register 1

b7 b6 b5 b4 b3 b2 b1 b0

Interrupt request register 1 (IREQ1) [Address:3C16]

B	Name	Function	At reset	R	W
0	INT0 interrupt request bit	0 : No interrupt request 1 : Interrupt request	0	○	*
1	INT1/ZCR interrupt request bit	0 : No interrupt request 1 : Interrupt request	0	○	*
2	• INT2 interrupt request bit • Remote control/counter overflow interrupt request bit	0 : No interrupt request 1 : Interrupt request	0	○	*
3	• Serial I/O 1 interrupt request bit • Serial I/O automatic transfer interrupt request bit	0 : No interrupt request 1 : Interrupt request	0	○	*
4	Serial I/O 2 interrupt request bit	0 : No interrupt request 1 : Interrupt request	0	○	*
5	Serial I/O 3 interrupt request bit	0 : No interrupt request 1 : Interrupt request	0	○	*
6	Timer 1 interrupt request bit	0 : No interrupt request 1 : Interrupt request	0	○	*
7	Timer 2 interrupt request bit	0 : No interrupt request 1 : Interrupt request	0	○	*

* "0" is set by software, but not "1."

Fig. 2.2.7 Structure of Interrupt request register 1

Interrupt request register 2

b7 b6 b5 b4 b3 b2 b1 b0

Interrupt request reigster 2 (IREQ2) [Address:3D16]

b	Name	Function	At reset	R	W
0	Timer 3 interrupt request bit	0 : No interrupt request 1 : Interrupt request	0	○	*
1	Timer 4 interrupt request bit	0 : No interrupt request 1 : Interrupt request	0	○	*
2	Timer 5 interrupt request bit	0 : No interrupt request 1 : Interrupt request	0	○	*
3	Timer 6 interrupt request bit	0 : No interrupt request 1 : Interrupt request	0	○	*
4	INT3 interrupt request bit	0 : No interrupt request 1 : Interrupt request	0	○	*
5	• INT4 interrupt request bit • A-D conversion interrupt request bit	0 : No interrupt request 1 : Interrupt request	0	○	*
6	• FLD blanking interrupt request bit • FLD digit interrupt request bit	0 : No interrupt request 1 : Interrupt request	0	○	*
7	Nothing is allocated for this bit. This is a write disabled bit. When this bit is read out, the value is "0."		0	○	*

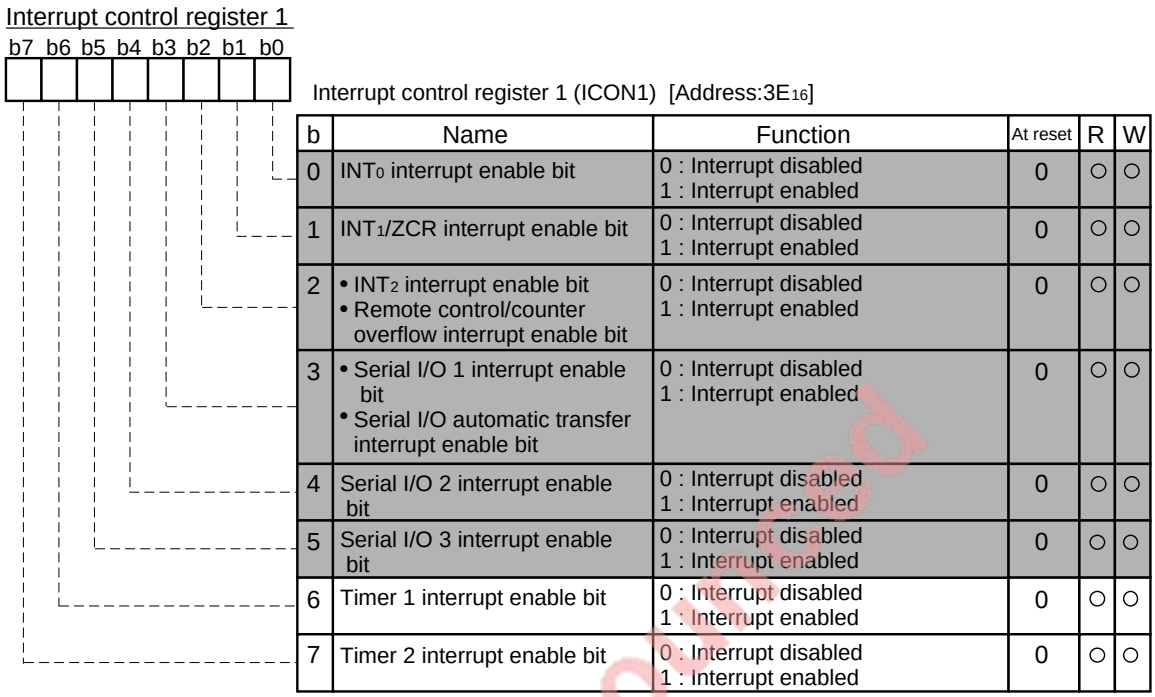
* "0" is set by software, but not "1."

Fig. 2.2.8 Structure of Interrupt request register 2

EOL announced

Downloaded from Elcodis.com electronic components distributor

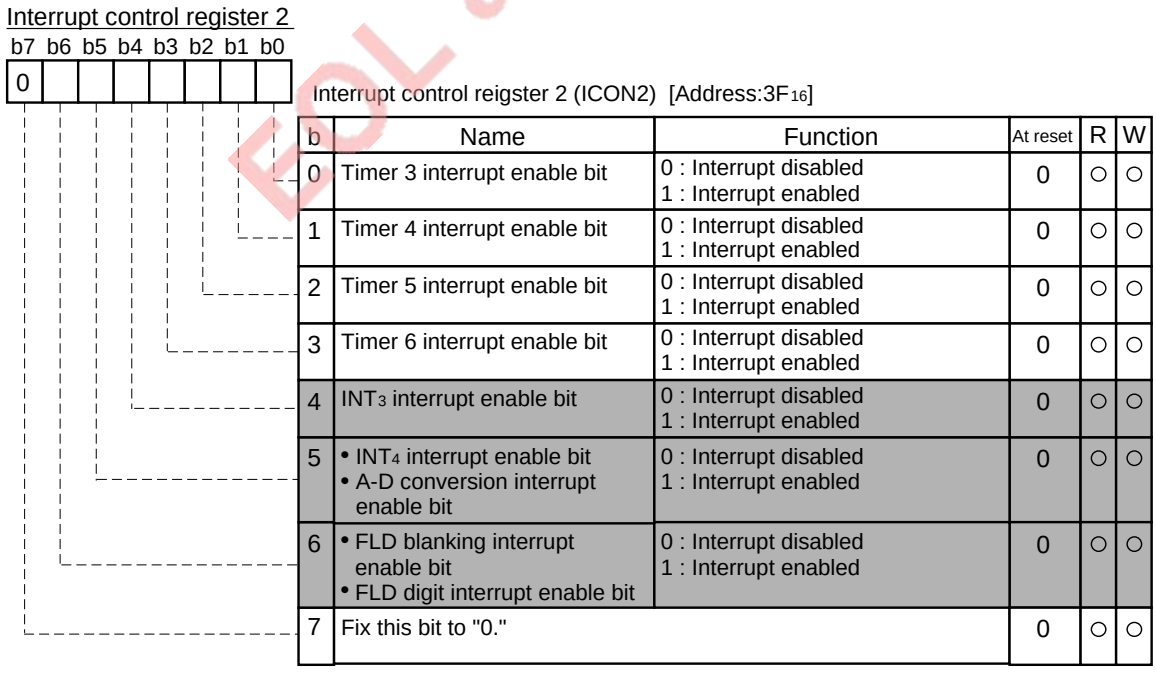
2. APPLICATION



Interrupt control register 1 (ICON1) [Address:3E16]

b	Name	Function	At reset	R	W
0	INT_0 interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	○	○
1	INT_1/ZCR interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	○	○
2	• INT_2 interrupt enable bit • Remote control/counter overflow interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	○	○
3	• Serial I/O 1 interrupt enable bit • Serial I/O automatic transfer interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	○	○
4	Serial I/O 2 interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	○	○
5	Serial I/O 3 interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	○	○
6	Timer 1 interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	○	○
7	Timer 2 interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	○	○

Fig. 2.2.9 Structure of Interrupt control register 1



Interrupt control reigster 2 (ICON2) [Address:3F16]

b	Name	Function	At reset	R	W
0	Timer 3 interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	○	○
1	Timer 4 interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	○	○
2	Timer 5 interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	○	○
3	Timer 6 interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	○	○
4	INT_3 interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	○	○
5	• INT_4 interrupt enable bit • A-D conversion interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	○	○
6	• FLD blanking interrupt enable bit • FLD digit interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	○	○
7	Fix this bit to "0."		0	○	○

Fig. 2.2.10 Structure of Interrupt control register 2

EOL announced

Downloaded from Elcodis.com electronic components distributor

2. APPLICATION

2.2.2 Timer application examples

(1) Basic functions and uses

[Function 1] Control of Event interval (Timers 1 to 6)

The Timer count stop bit is set to "0" after setting a count value to a timer. Then a timer interrupt request occurs after a certain period.

[Use] • Generation of an output signal timing
• Generation of a waiting time

[Function 2] Control of Cyclic operation : Generation of synchronous timing (Timers 1 to 6)

The value of a timer latch is automatically written to a timer each time a timer underflows, and a timer interrupt request occurs.

[Use] • Generation of cyclic interrupts
• Clock function (measurement of one second) → Application example 1
• Control of a main routine cycle

[Function 3] Output of Rectangular waveform (Timers 1 and 3)

The output level of the TOUT pin is inverted every time a timer underflows. To output long-interval rectangular waveforms (when division of 8 bits or more is necessary), the Timers 2 and 3 are connected .

[Use] • A piezoelectric buzzer output → Application example 2
• Generation of the remote-control carrier waveforms

[Function 4] Count of External pulse (Timers 2 and 4)

External pulses input to the CNTR pin are selected as a timer count source.

[Use] • Measurement of frequency (judging if the Video synchronization signal exits) → Application example 3
• Division of external pulses and generation of interrupts in a cycle based on an external pulse.
(count of a reel pulse)

[Function 5] Output of PWM signal (Timer 6)

The pulses with each specified intervals of "H" and "L" are output.

[Use] • Control of an electronic volume (connected with VCA)

EOL announced

Downloaded from Elcodis.com electronic components distributor

2. APPLICATION

(2) Timer application example 1: Clock function (measurement of one second)

Outline : The input clock is divided by a timer so that the clock counts up every second.

Specifications :
- The clock f(XIN) = 4.19 MHz (2^{22}) is divided by a timer.
- The Timer 3 interrupt request bit is checked in the main routine, and the clock is counted up when an interrupt request occurs.
- Another interrupt processing is executed in a parallel, so a timer interrupt occurs every 244 µs.

Figure 2.2.11 shows a connection of timers and a setting of division ratios, Figures 2.2.12 and 2.2.13 show a setting of related registers, and Figure 2.2.14 shows a control procedure.

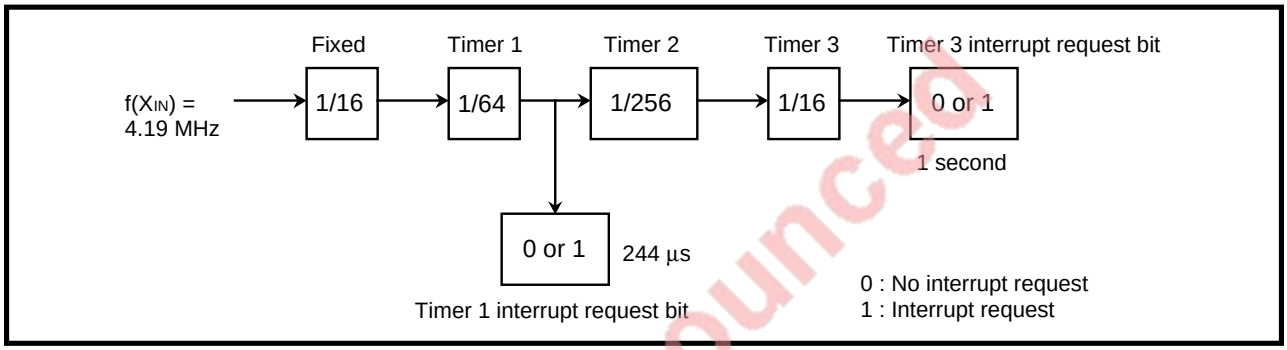


Fig. 2.2.11 Connection of timers and setting of division ratios [Clock function]

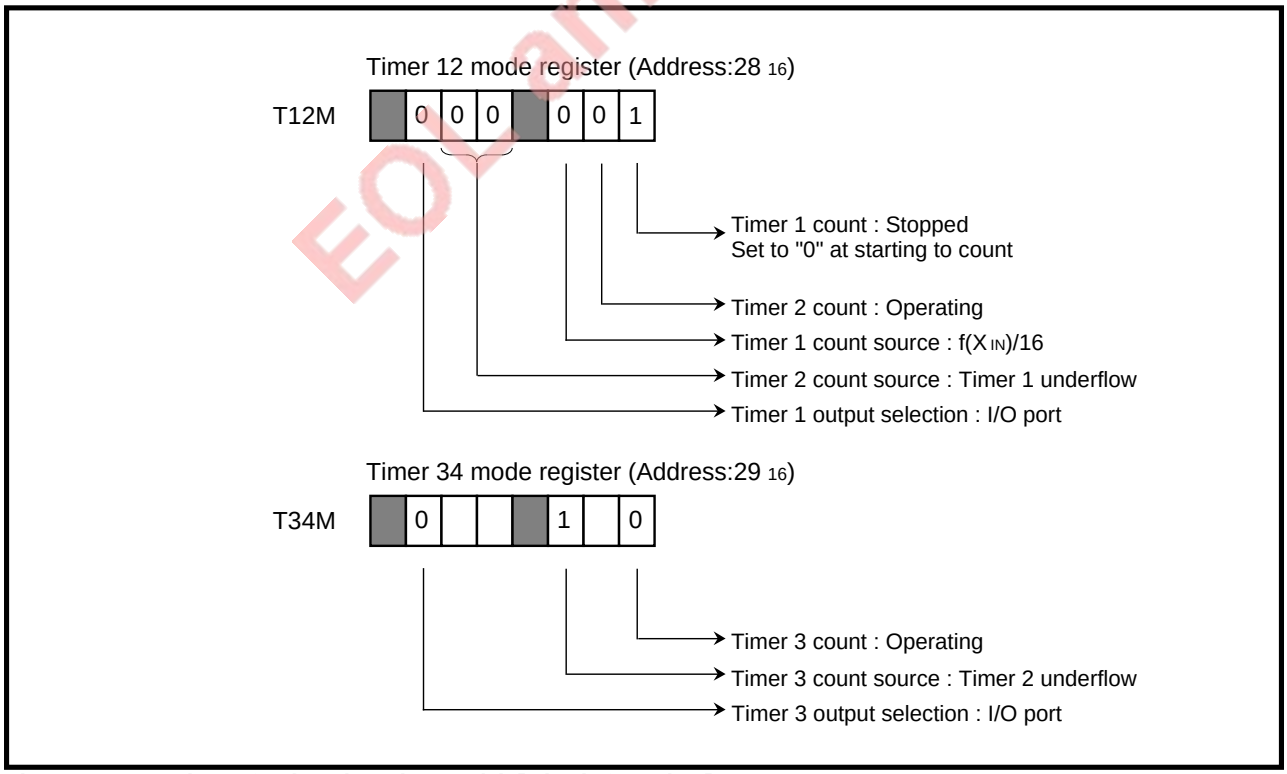
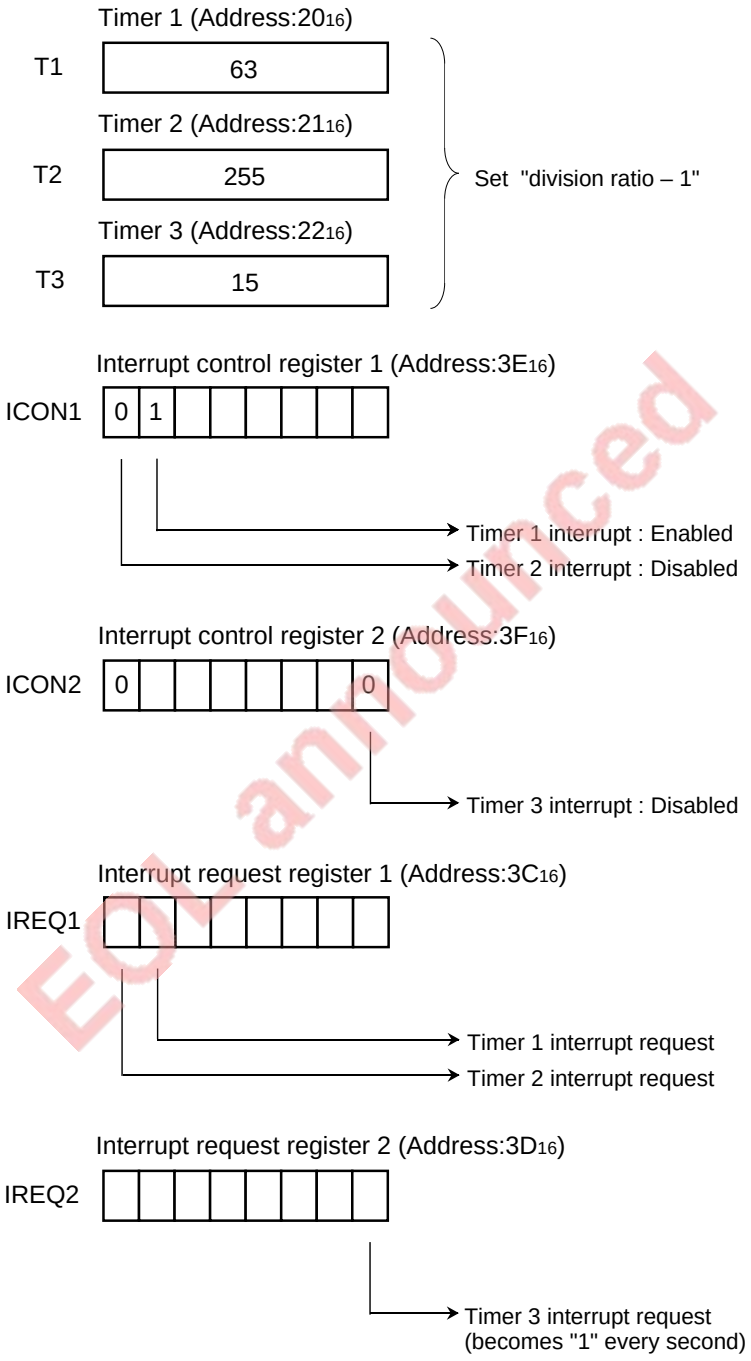


Fig. 2.2.12 Setting of related registers (1) [Clock function]

EOL announced

Downloaded from Elcodis.com electronic components distributor

2. APPLICATION



EOL announced

Fig. 2.2.13 Setting of related registers (2) [Clock function]

Downloaded from Elcodis.com electronic components distributor

2. APPLICATION

Control procedure :
Figure 2.2.14 shows a control procedure.

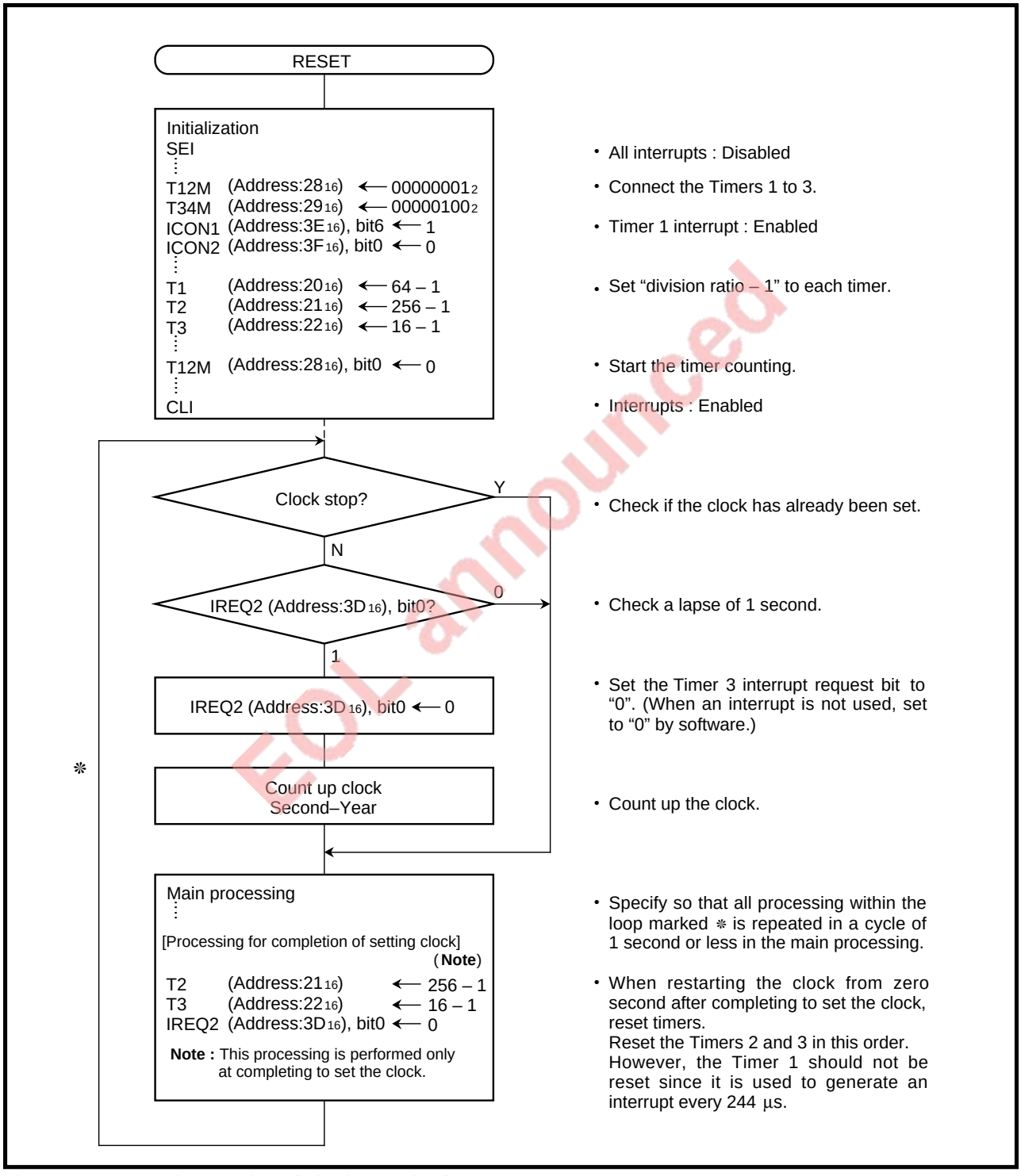


Fig. 2.2.14 Control procedure [Clock function]

EOL announced

Downloaded from Elcodis.com electronic components distributor

2. APPLICATION

(3) Timer application example 2: Piezoelectric buzzer output

Outline : The rectangular waveform output function of a timer is applied for a piezoelectric buzzer output.

Specifications : • The rectangular waveform, 2 kHz (2048 Hz) which is divided clock f(XIN) = 4.19 MHz is output from the T3OUT pin.
• The level of the T3OUT pin fixes to "H" while a piezoelectric buzzer output is stopped.

Figure 2.2.15 shows an example of a peripheral circuit, and Figure 2.2.16 shows a connection of the timer and setting of the division ratio.

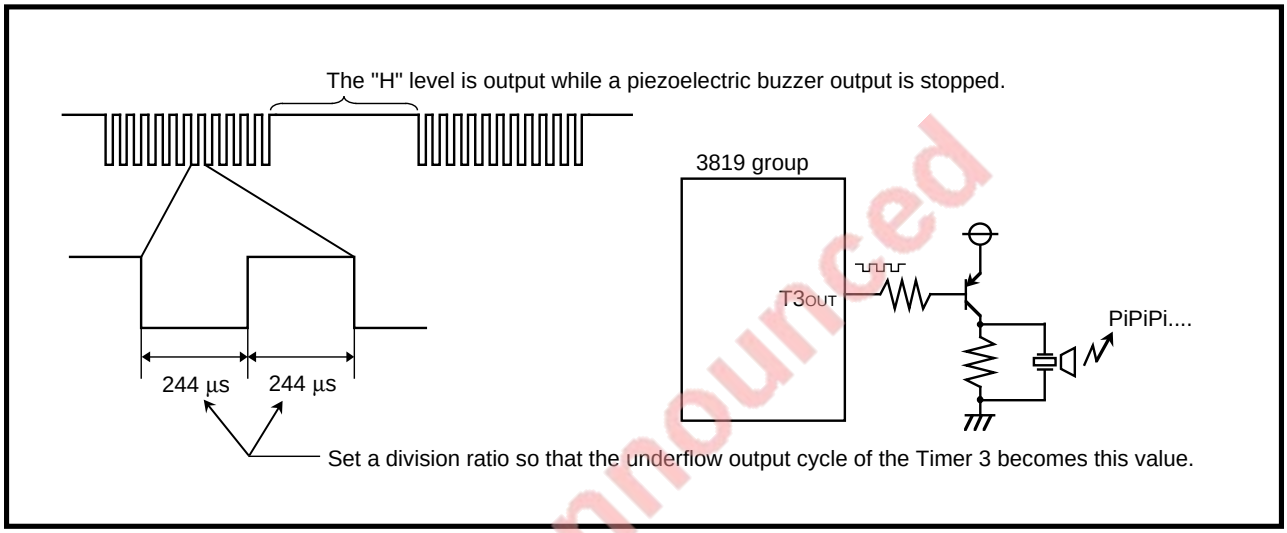


Fig. 2.2.15 Example of a peripheral circuit

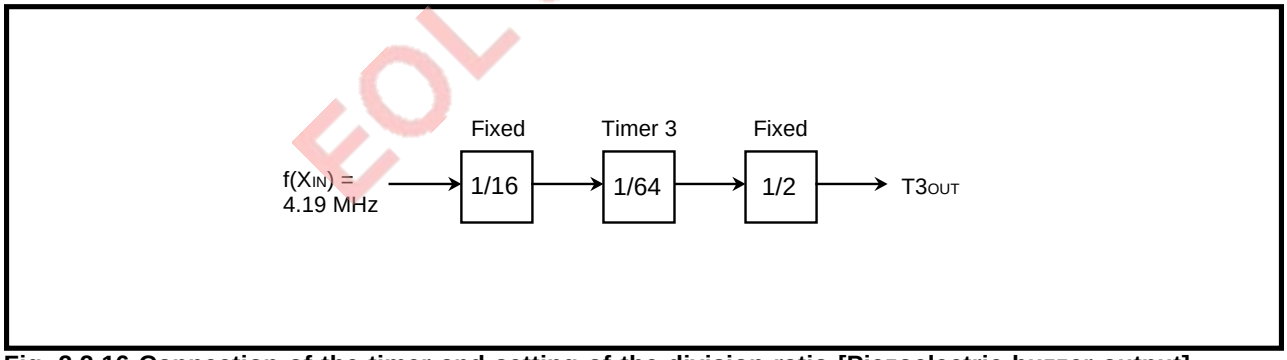


Fig. 2.2.16 Connection of the timer and setting of the division ratio [Piezoelectric buzzer output]

EOL announced

Downloaded from Elcodis.com electronic components distributor

2. APPLICATION

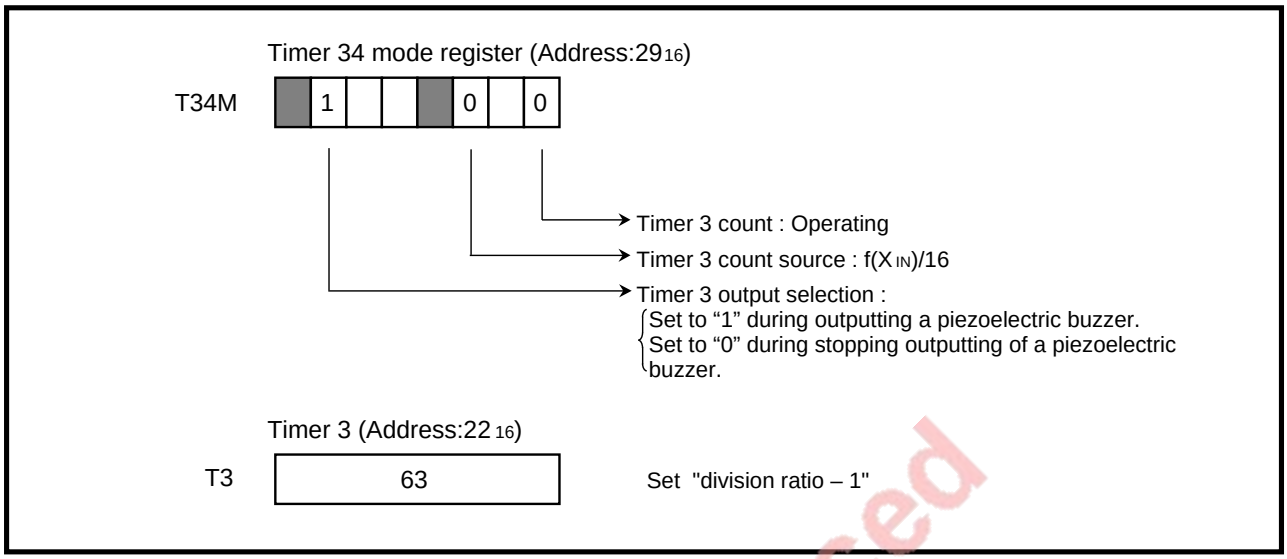


Fig. 2.2.17 Setting of related registers [Piezoelectric buzzer output]

Control procedure :

Figure 2.2.18 shows a control procedure.

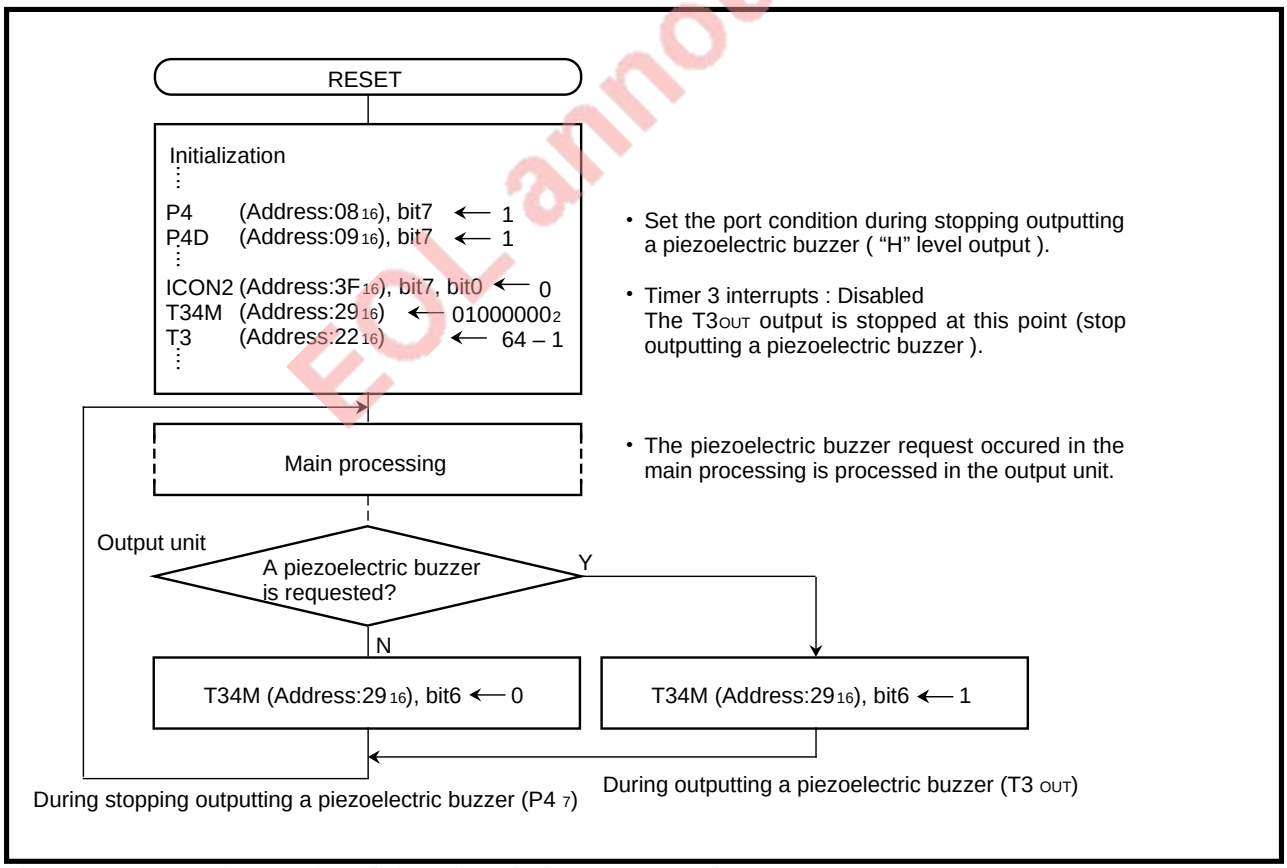


Fig. 2.2.18 Control procedure [Piezoelectric buzzer output]

EOL announced

Downloaded from Elcodis.com electronic components distributor

2. APPLICATION

(4) Timer application example 3 : Measurement of frequency (judging if Video synchronization signal exists)

Outline : The pulses input to the External count input pin (CNTR) are counted by a timer to judge if the frequency is within a certain range.

Specifications :
- The Video synchronization signal is input to the $CNTR_1$ pin and counted by the Timer 4.
- A count value is read out at the interval of about 2 ms (Timer 1 interrupt interval : 244 µs × 8). When the count value is 28 to 40, it is regarded as the existence of the Video synchronization signal.
- Because the timer is a down-counter, the count value is compared with 227 to 215.*

*227 to 215 = 255 (initialized value of counter) – 28 to 40 (the number of valid value).

Figure 2.2.19 shows a method for judging if Video synchronization signal exists, and Figure 2.2.20 shows a setting of related registers.

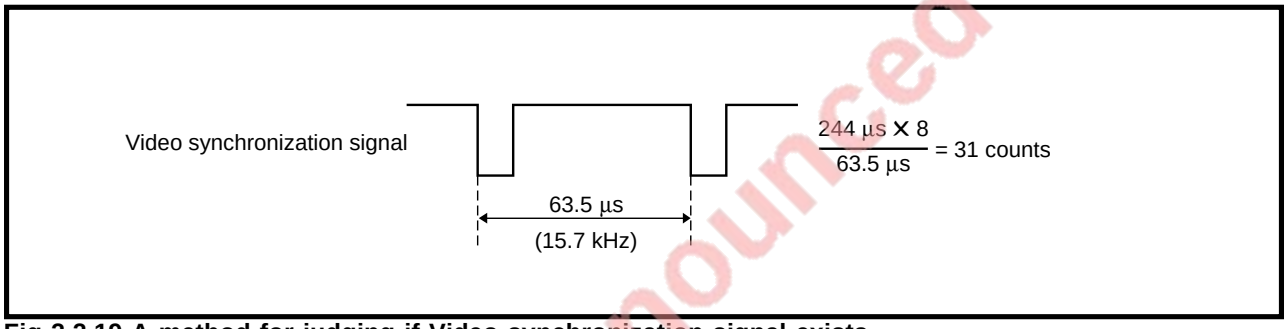
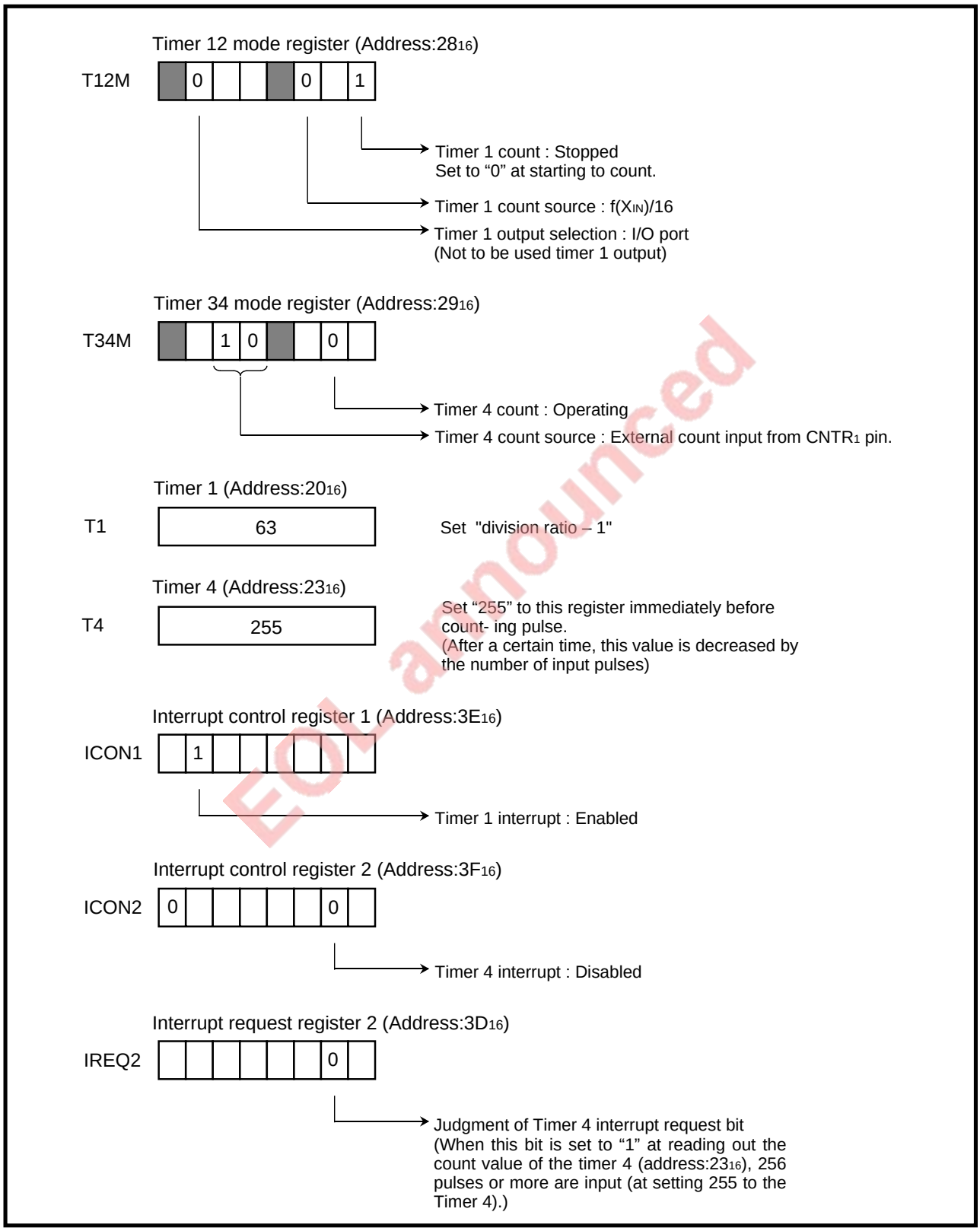


Fig 2.2.19 A method for judging if Video synchronization signal exists

EOL announced

Downloaded from Elcodis.com electronic components distributor

2. APPLICATION



EOL announced

Fig. 2.2.20 Setting of related registers [Measurement of frequency]

Downloaded from Elcodis.com electronic components distributor

2. APPLICATION

Control procedure :

Figure 2.2.21 shows a control procedure.

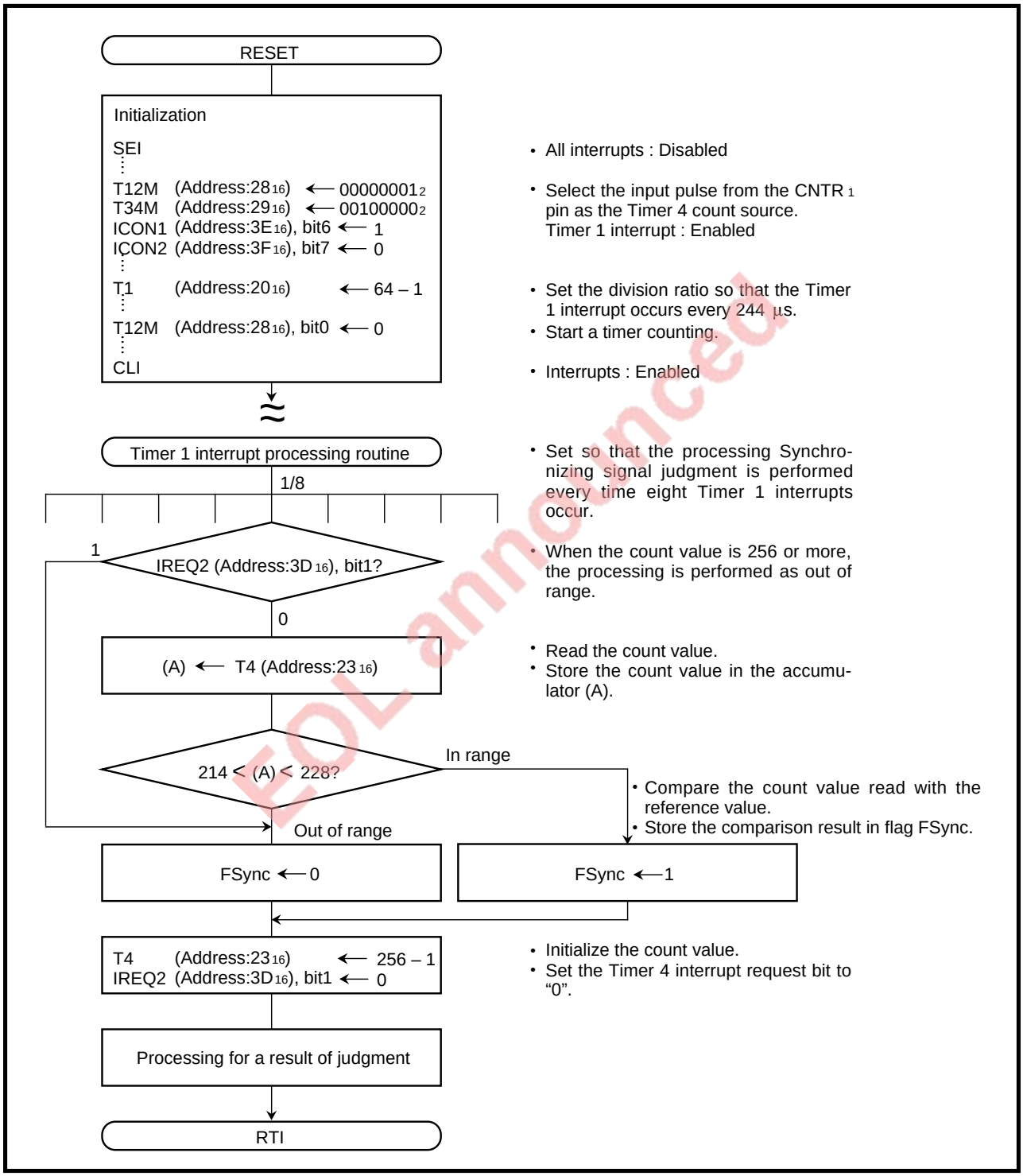


Fig. 2.2.21 Control procedure [Measurement of frequency]

EOL announced

Downloaded from Elcodis.com electronic components distributor

2. APPLICATION

2.3 Serial I/O

2.3.1 Related registers

Serial I/O automatic transfer data pointer

b7 b6 b5 b4 b3 b2 b1 b0

Serial I/O automatic transfer data pointer (SIODP) [Address:18$_{16}$]

B	Function	At reset	R	W
0	Indicate an address of Serial I/O automatic transfer RAM.	?	○	○
1		?	○	○
2		?	○	○
3		?	○	○
4		?	○	○
5	Nothing is allocated for these bits. These are write disabled bits. When these bits are read out, the values are "0."	0	○	×
6		0	○	×
7		0	○	×

Fig. 2.3.1 Structure of Serial I/O automatic transfer data pointer

Serial I/O 1 control register

b7 b6 b5 b4 b3 b2 b1 b0

Serial I/O 1 control register (SIO1CON) [Address:19$_{16}$]

B	Name	Function	At reset	R	W
0	Internal synchronous clock selection bits	b2 b1b0 000 : f(X$_{IN}$)/8 or f(X$_{CIN}$)/8 001 : f(X$_{IN}$)/16 or f(X$_{CIN}$)/16 010 : f(X$_{IN}$)/32 or f(X$_{CIN}$)/32 011 : f(X$_{IN}$)/64 or f(X$_{CIN}$)/64 110 : f(X$_{IN}$)/128 or f(X$_{CIN}$)/128 111 : f(X$_{IN}$)/256 or f(X$_{CIN}$)/256	0	○	○
1			0	○	○
2			0	○	○
3	Serial I/O 1 port selection bit (P6$_5$,P6$_6$,P6$_7$*)	0 : I/O port 1 : S$_{OUT1}$, S$_{CLK11}$, S$_{CLK12}$* signal pins	0	○	○
4	$\overline{S_{RDY1}}$ output selection bit (P6$_7$)	0 : I/O port 1 : $\overline{S_{RDY1}}$/$\overline{CS}$* signal pin (**Note**)	0	○	○
5	Transfer direction selection bit	0 : LSB first 1 : MSB first	0	○	○
6	Synchronous clock selection bit	0 : External clock 1 : Internal clock	0	○	○
7	P6$_5$/S$_{OUT1}$ P-channel output disable bit	0 : CMOS output (in output mode) 1 : N-channel open-drain output (in output mode)	0	○	○

* Valid only in the Serial I/O automatic transfer mode

Note : When an external clock is selected in the serial I/O 1 automatic transfer mode, the $\overline{S_{RDY1}}$ signal pin is used as the $\overline{CS}$ signal input pin.

Fig. 2.3.2 Structure of Serial I/O 1 control register

EOL announced

Downloaded from Elcodis.com electronic components distributor

2. APPLICATION

Serial I/O automatic transfer control register

b7 b6 b5 b4 b3 b2 b1 b0

Serial I/O automatic transfer control register (SIOAC) [Address:1A16]

B	Name	Function	At reset	R	W
0	Automatic transfer control bit	0 : Serial I/O ordinary mode (serial I/O 1 interrupt) 1 : Automatic transfer mode (serial I/O automatic transfer interrupt)	0	○	○
1	Automatic transfer start bit	0 : Transfer completion 1 : Transferring (starts by writing "1")	0	○	○
2	Transfer mode switch bit	0 : Fullduplex (transmit / receive) mode 1 : Transmit-only mode	0	○	○
3	Synchronous clock output pin selection bit	0 : S_{CLK11} 1 : S_{CLK12}	0	○	○
4	Nothing is allocated for these bits. These are write disabled bits. When these bits are read out, the values are "0."		0	○	×
5			0	○	×
6			0	○	×
7			0	○	×

Fig. 2.3.3 Structure of Serial I/O automatic transfer control register

Serial I/O 1 register

b7 b6 b5 b4 b3 b2 b1 b0

Serial I/O 1 register (SIO1) [Address:1B16]

B	Function	At reset	R	W
0	A shift register for serial transmission and reception. ● At transmitting : Set a transmission data. ● At receiving : Store a reception data.	?	○	○
1		?	○	○
2		?	○	○
3		?	○	○
4		?	○	○
5		?	○	○
6		?	○	○
7		?	○	○

Fig. 2.3.4 Structure of Serial I/O 1 register

EOL announced

Downloaded from Elcodis.com electronic components distributor

2. APPLICATION

Serial I/O automatic transfer interval register

b7 b6 b5 b4 b3 b2 b1 b0

Serial I/O automatic transfer interval register (SIOAI) [Address:1C16]

B	Function	At reset	R	W
0	Ti = (n + 2) × Tc Ti = a length of transfer interval n = a setting value Tc = a length of a bit of transfer clock	0	○	○
1		0	○	○
2		0	○	○
3		0	○	○
4		0	○	○
5	Nothing is allocated for these bits. These are write disabled bits. When these bits are read out, the values are "0."	0	○	×
6		0	○	×
7		0	○	×

Fig. 2.3.5 Structure of Serial I/O automatic transfer interval register

Serial I/O 2 control register

b7 b6 b5 b4 b3 b2 b1 b0

Serial I/O 2 control register (SIO2CON) [Address:1D16]

B	Name	Function	At reset	R	W
0	Internal synchronous clock selection bits	b2 b1b0 000 : f(XIN)/8 or f(XCIN)/8 001 : f(XIN)/16 or f(XCIN)/16 010 : f(XIN)/32 or f(XCIN)/32 011 : f(XIN)/64 or f(XCIN)/64 110 : f(XIN)/128 or f(XCIN)/128 111 : f(XIN)/256 or f(XCIN)/256	0	○	○
1			0	○	○
2			0	○	○
3	Serial I/O 2 port selection bit (P51,P52)	0 : I/O port 1 : SOUT2, SCLK2 signal pins	0	○	○
4	$\overline{SRDY2}$ output selection bit (P53)	0 : I/O port 1 : $\overline{SRDY2}$ signal pin	0	○	○
5	Transfer direction selection bit	0 : LSB first 1 : MSB first	0	○	○
6	Synchronous clock selection bit	0 : External clock 1 : Internal clock	0	○	○
7	P51/SOUT2 P-channel output disable bit	0 : CMOS output (in output mode) 1 : N-channel open-drain output (in output mode)	0	○	○

Fig. 2.3.6 Structure of Serial I/O 2 control register

EOL announced

Downloaded from Elcodis.com electronic components distributor

2. APPLICATION

Serial I/O 3 control register

b7 b6 b5 b4 b3 b2 b1 b0

Serial I/O 3 control register (SIO3CON) [Address:1E16]

B	Name	Function	At reset	R	W
0	Internal synchronous clock selection bits	b2 b1b0 000 : f(XIN)/8 or f(XCIN)/8 001 : f(XIN)/16 or f(XCIN)/16 010 : f(XIN)/32 or f(XCIN)/32 011 : f(XIN)/64 or f(XCIN)/64 110 : f(XIN)/128 or f(XCIN)/128 111 : f(XIN)/256 or f(XCIN)/256	0	○	○
1			0	○	○
2			0	○	○
3	Serial I/O 3 port selection bit (P55,P56)	0 : I/O port 1 : SOUT3, SCLK3 signal pins	0	○	○
4	$\overline{S_{RDY3}}$ output selection bit (P57)	0 : I/O port 1 : $\overline{S_{RDY3}}$ signal pin	0	○	○
5	Transfer direction selection bit	0 : LSB first 1 : MSB first	0	○	○
6	Synchronous clock selection bit	0 : External clock 1 : Internal clock	0	○	○
7	P55/SOUT3 P-channel output disable bit	0 : CMOS output (in output mode) 1 : N-channel open-drain output (in output mode)	0	○	○

Fig. 2.3.7 Structure of Serial I/O 3 control register

Interrupt request register 1

b7 b6 b5 b4 b3 b2 b1 b0

Interrupt request reigster 1 (IREQ1) [Address:3C16]

B	Name	Function	At reset	R	W
0	INT0 interrupt request bit	0 : No interrupt request 1 : Interrupt request	0	○	*
1	INT1/ZCR interrupt request bit	0 : No interrupt request 1 : Interrupt request	0	○	*
2	• INT2 interrupt request bit • Remote control/counter overflow interrupt request bit	0 : No interrupt request 1 : Interrupt request	0	○	*
3	• Serial I/O 1 interrupt request bit • Serial I/O automatic transfer interrupt request bit	0 : No interrupt request 1 : Interrupt request	0	○	*
4	Serial I/O 2 interrupt request bit	0 : No interrupt request 1 : Interrupt request	0	○	*
5	Serial I/O 3 interrupt request bit	0 : No interrupt request 1 : Interrupt request	0	○	*
6	Timer 1 interrupt request bit	0 : No interrupt request 1 : Interrupt request	0	○	*
7	Timer 2 interrupt request bit	0 : No interrupt request 1 : Interrupt request	0	○	*

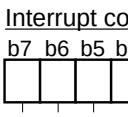
* "0" is set by software, but not "1."

Fig. 2.3.8 Structure of Interrupt request register 1

EOL announced

Downloaded from Elcodis.com electronic components distributor

2. APPLICATION



Interrupt control register 1 (ICON1) [Address:3E16]

B	Name	Function	At reset	R	W
0	INT_0 interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	○	○
1	INT_1/ZCR interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	○	○
2	• INT_2 interrupt enable bit • Remote control/counter overflow interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	○	○
3	• Serial I/O1 interrupt enable bit • Serial I/O automatic transfer interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	○	○
4	Serial I/O 2 interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	○	○
5	Serial I/O 3 interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	○	○
6	Timer 1 interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	○	○
7	Timer 2 interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	○	○

Fig. 2.3.9 Structure of Interrupt control register 1

EOL announced

Downloaded from Elcodis.com electronic components distributor

2. APPLICATION

2.3.2 Serial I/O connection examples

(1) Control of peripheral IC equipped with CS pin

In any application, the automatic transfer function is available.

Figure 2.3.10 shows connection examples of a peripheral IC equipped with the CS pin.

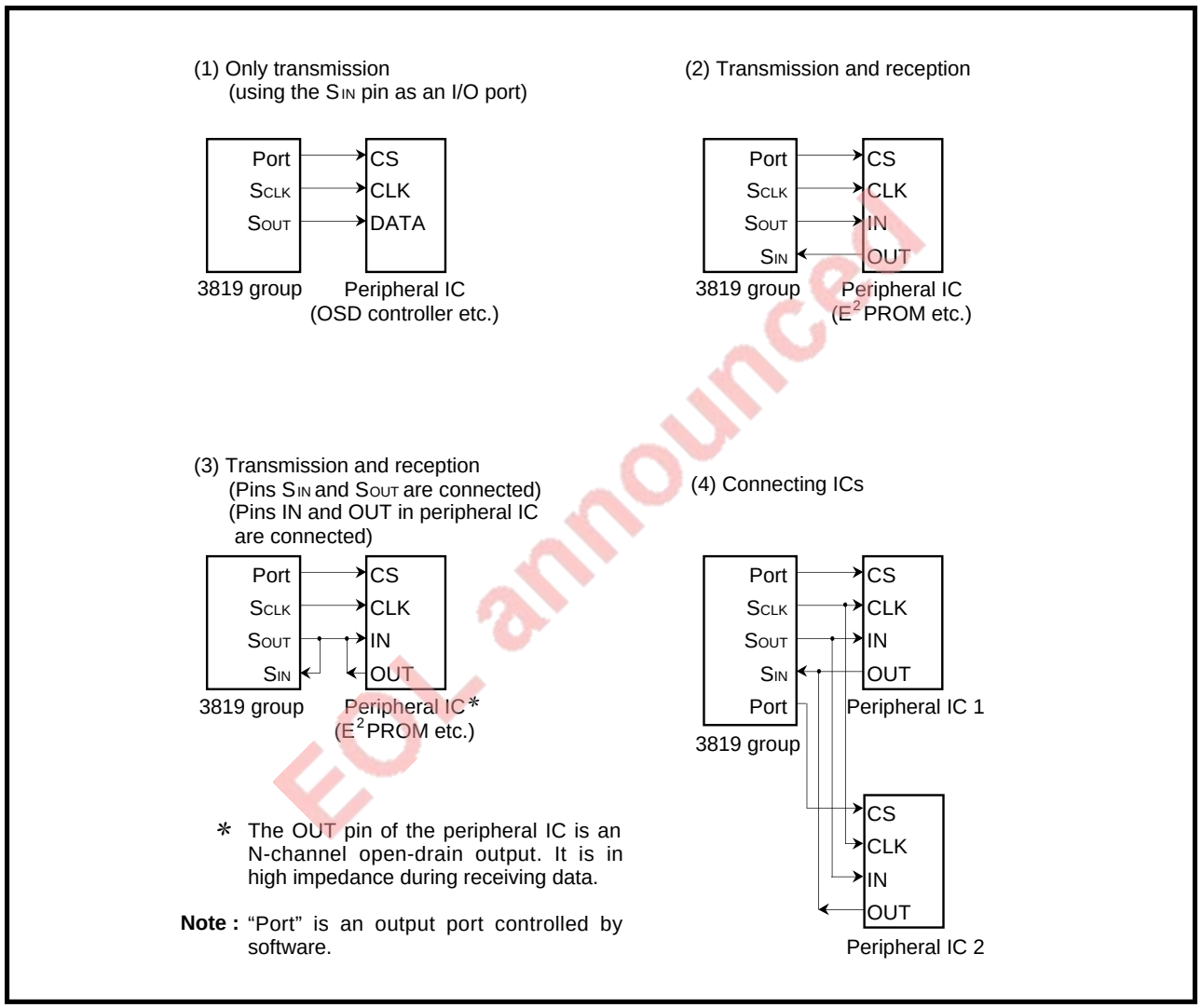


Fig. 2.3.10 Serial I/O connection examples (1)

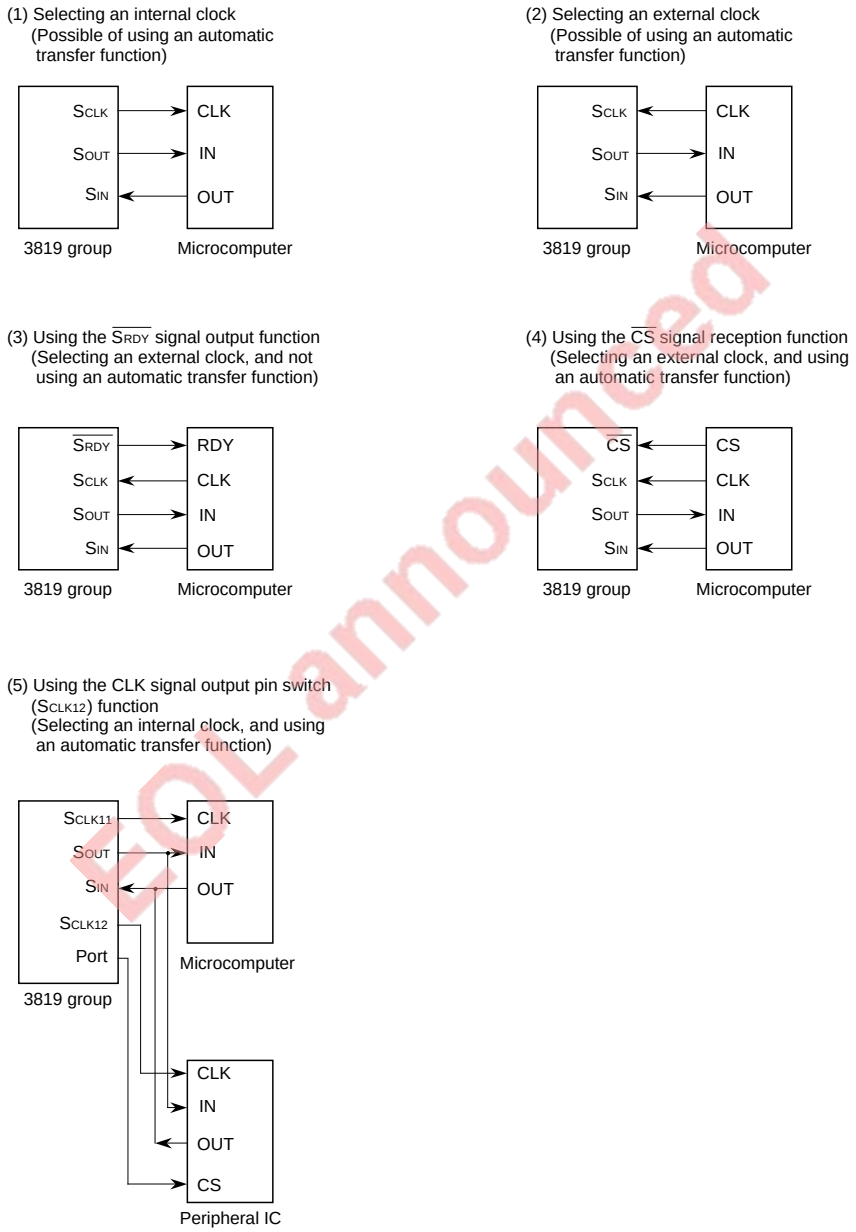
EOL announced

Downloaded from Elcodis.com electronic components distributor

2. APPLICATION

(2) Connection with microcomputer

Figure 2.3.11 shows connection examples of the other microcomputers.



EOL announced

Fig. 2.3.11 Serial I/O connection examples (2)

Downloaded from Elcodis.com electronic components distributor

2. APPLICATION

2.3.3 Setting of serial I/O mode

Whether $\overline{\text{SRDY}}$ signal output, $\overline{\text{CS}}$ signal receive and CLK signal output pin switch (SCLK12) functions can be selected to use or not by the following conditions:

- Serial I/O circuits (serial I/O 1 or serial I/O 2)
- The automatic transfer function is ON or OFF (at the serial I/O 1 only)
- Transfer clock (internal clock or external clock)

Figure 2.3.12 shows a setting of serial I/O mode.

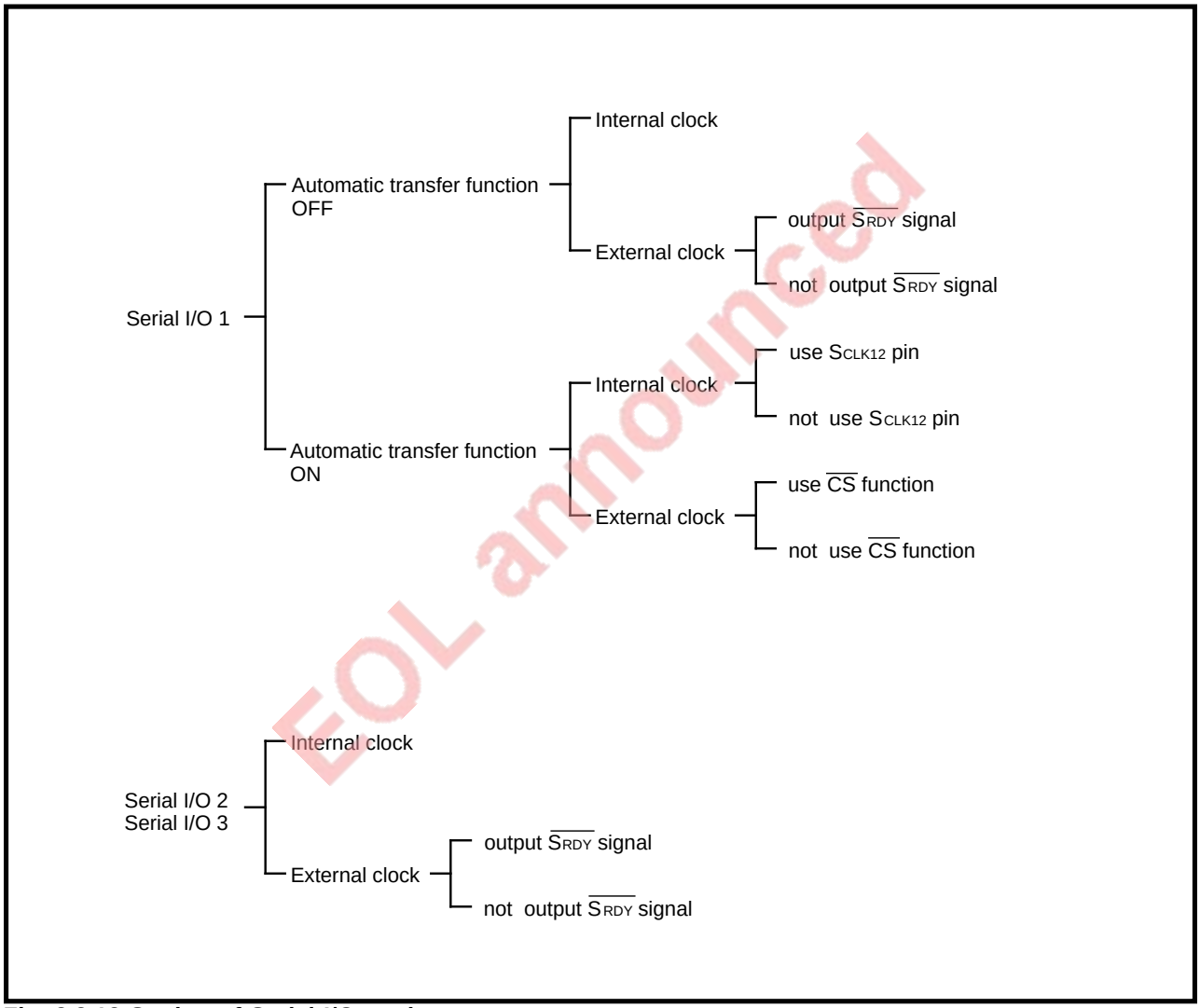


Fig. 2.3.12 Setting of Serial I/O mode

EOL announced

Downloaded from Elcodis.com electronic components distributor

2. APPLICATION

2.3.4 Serial I/O application examples

(1) Output of serial data (control of a peripheral IC)

Outline : The port is connected to the $\overline{CS}$ pin of a peripheral IC and the serial transmission is controlled.

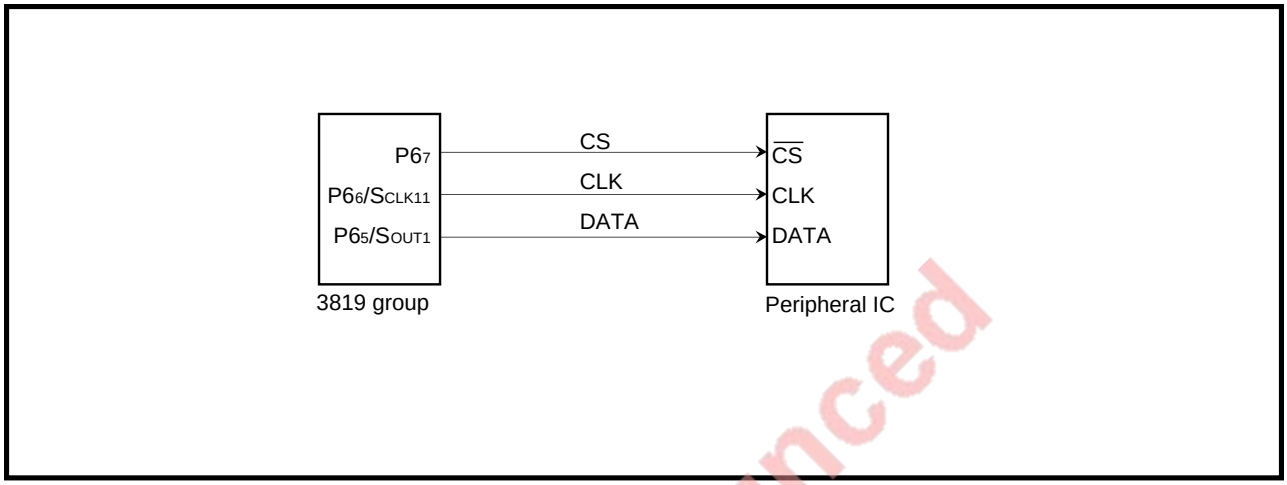


Fig. 2.3.13 Connection diagram [Output of serial data]

Specifications :
- The Serial I/O 1 is used (the automatic transfer function is not used)
- Synchronous clock frequency: 131 kHz (f(XIN) = 4.19 MHz is divided by 32)
- Transmission direction: LSB first
- The Serial I/O 1 interrupt is not used.
- The Port P67 is connected to the $\overline{CS}$ pin ("L" active) of the peripheral IC for a transmission control (the output level of the port P67 is controlled by software).

Figre 2.3.14 shows an output timing chart of serial data.

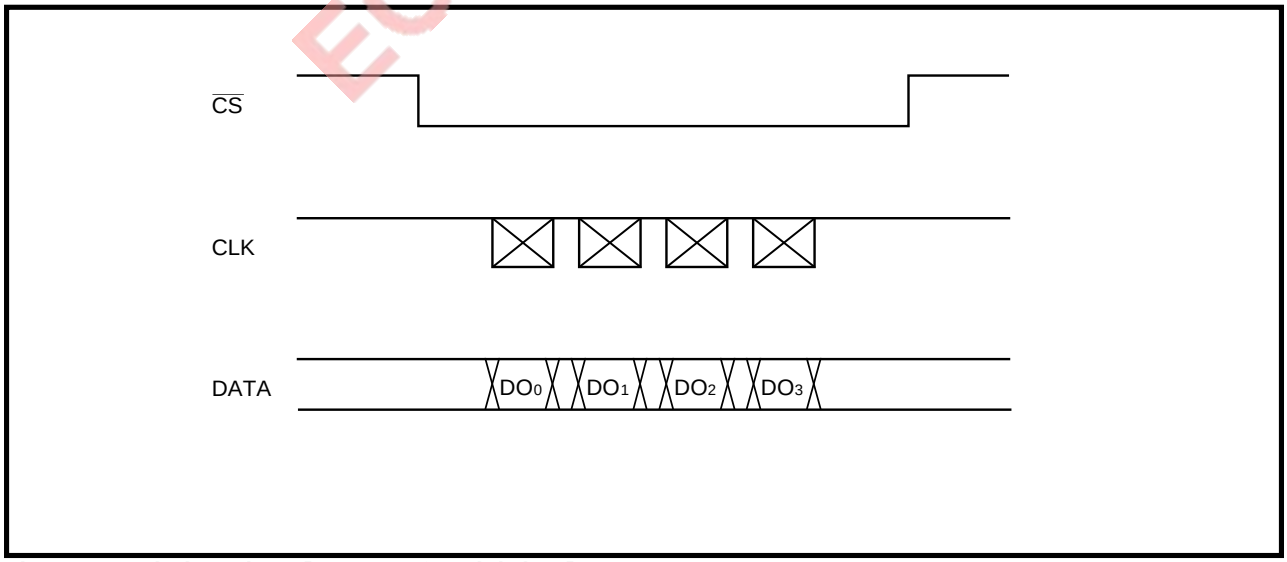


Fig. 2.3.14 Timing chart [Output of serial data]

EOL announced

Downloaded from Elcodis.com electronic components distributor

2. APPLICATION

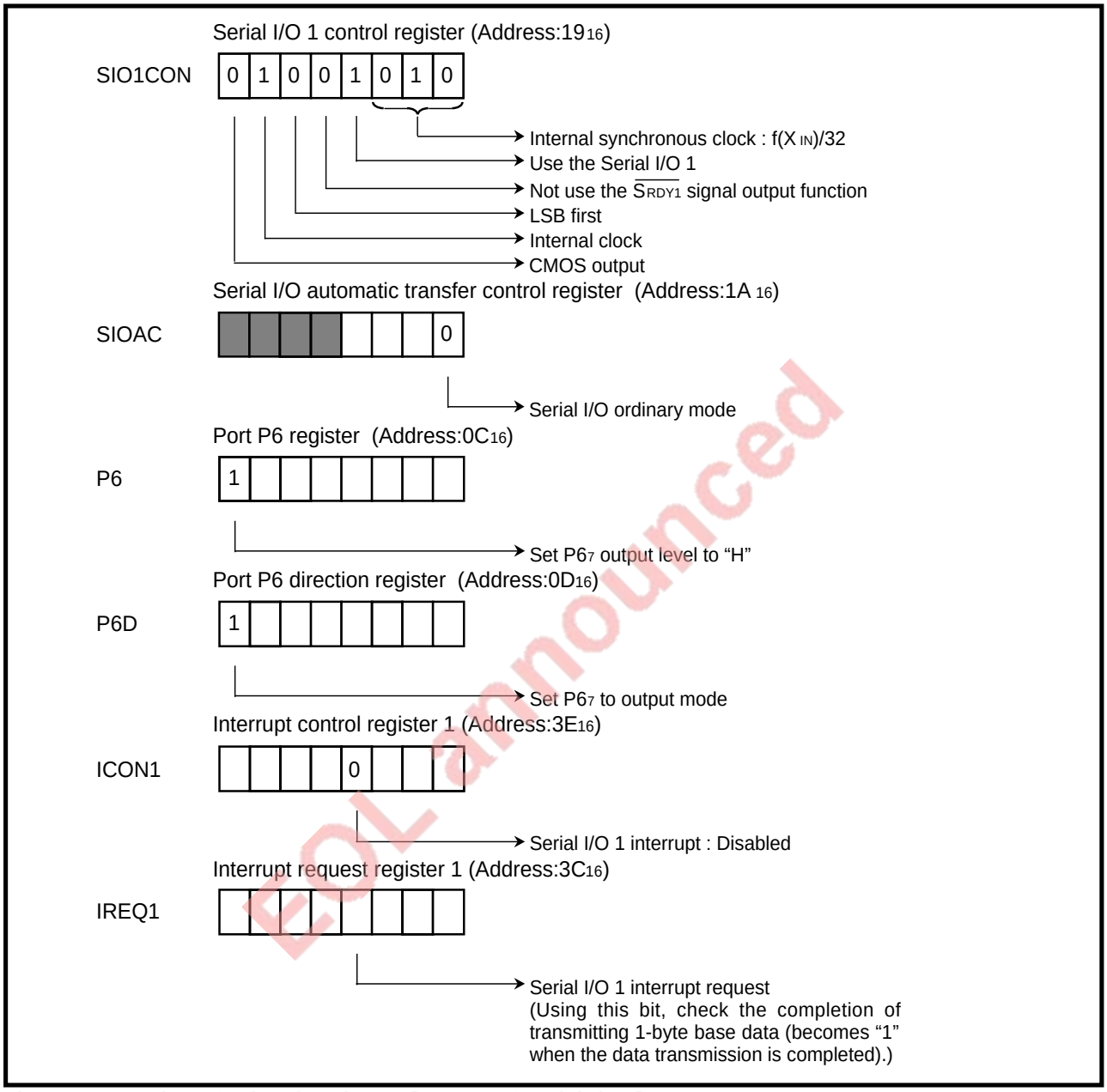


Fig. 2.3.15 Setting of related registers [Output of serial data]

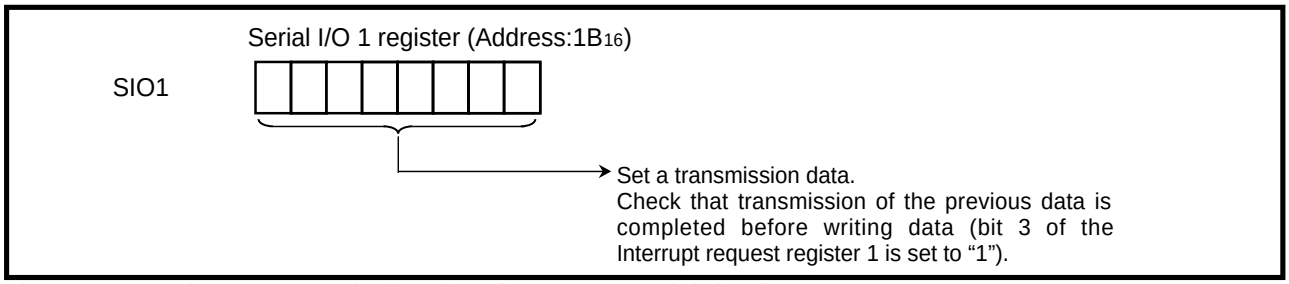


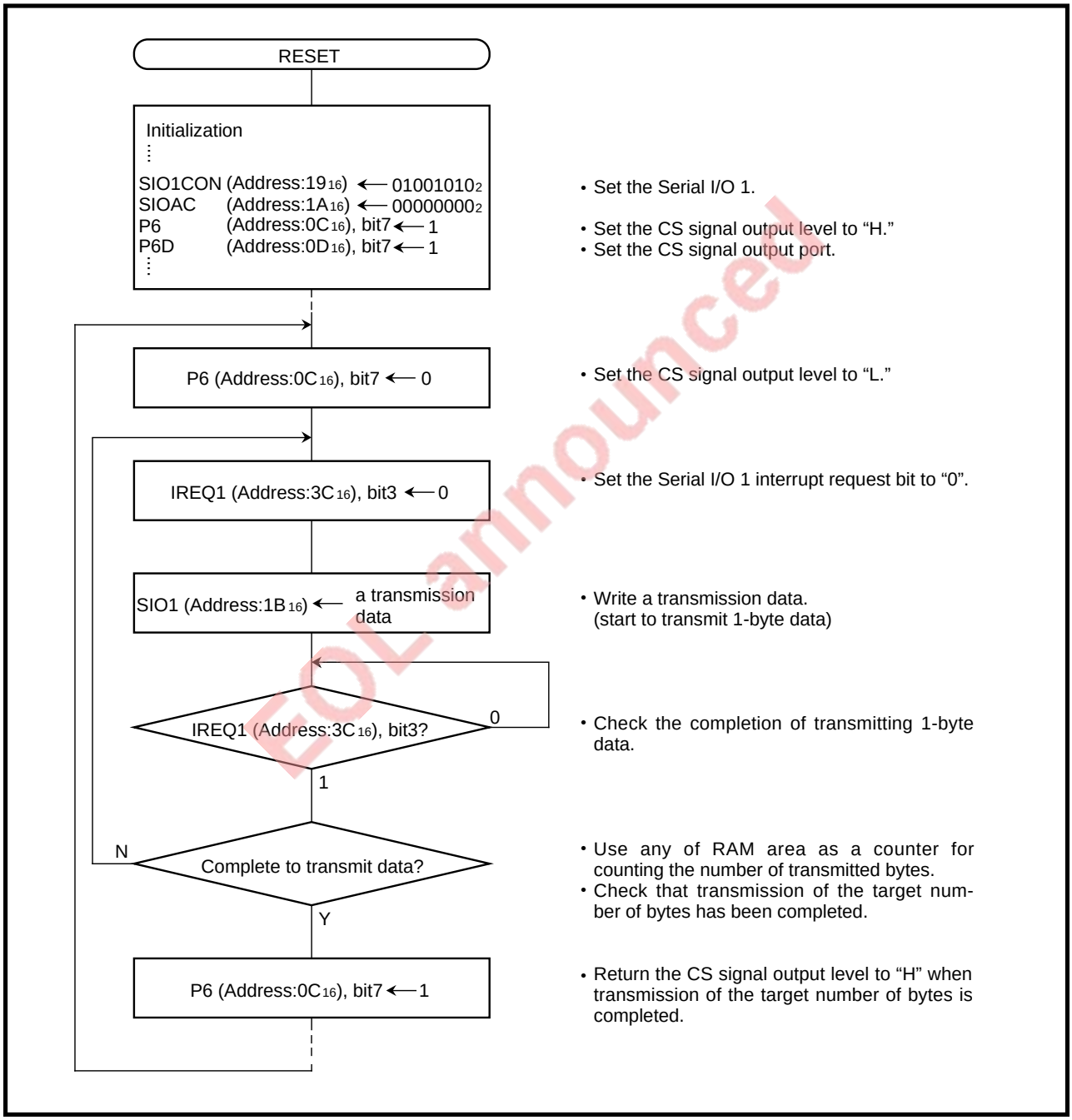
Fig. 2.3.16 Setting of transmission data [Output of serial data]

EOL announced

Downloaded from Elcodis.com electronic components distributor

2. APPLICATION

Control procedure : When the registers are set as shown in Fig. 2.3.15, the Serial I/O 1 can transmit one-byte data simply by writing data to the Serial I/O 1 register.
Thus, after setting the CS signal to “L”, write the transmission data to the Serial I/O 1 register on a one-byte base, and return the CS signal to “H” when the desired number of bytes have been transmitted.



EOL announced

Fig. 2.3.17 Control procedure [Output of serial data]

Downloaded from Elcodis.com electronic components distributor

2. APPLICATION

(2) Data transmission or reception using automatic transfer

Outline : Serial transmission or reception is controlled by using a serial automatic transfer function.

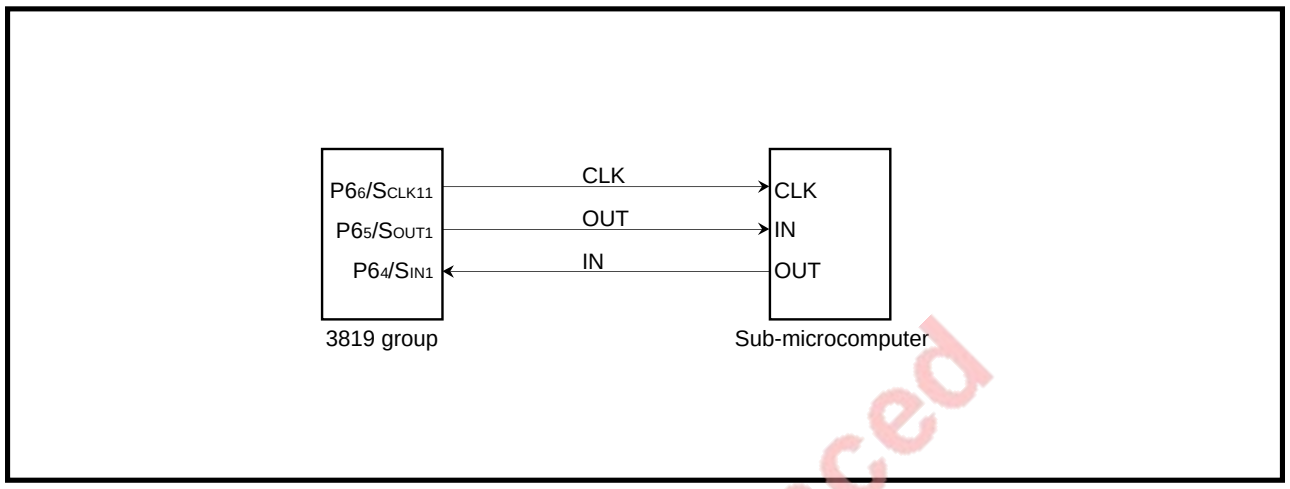


Fig. 2.3.18 Connection diagram [Data transmission or reception using automatic transfer]

Specifications :
- The Serial I/O 1 is used (the automatic transfer function is used).
- Transmission clock frequency: 131 kHz (f(XIN) = 4.19 MHz is divided by 32)
- Transmission direction : LSB first
- Number of bytes for transmission or reception : each 8 bytes/block
- Transmission interval: 244 µs (corresponding to a transmission clock of 32 bits)
- The Serial I/O automatic transfer interrupt is not used.

Figure 2.3.19 shows a transmission or reception timing chart using an automatic transfer.

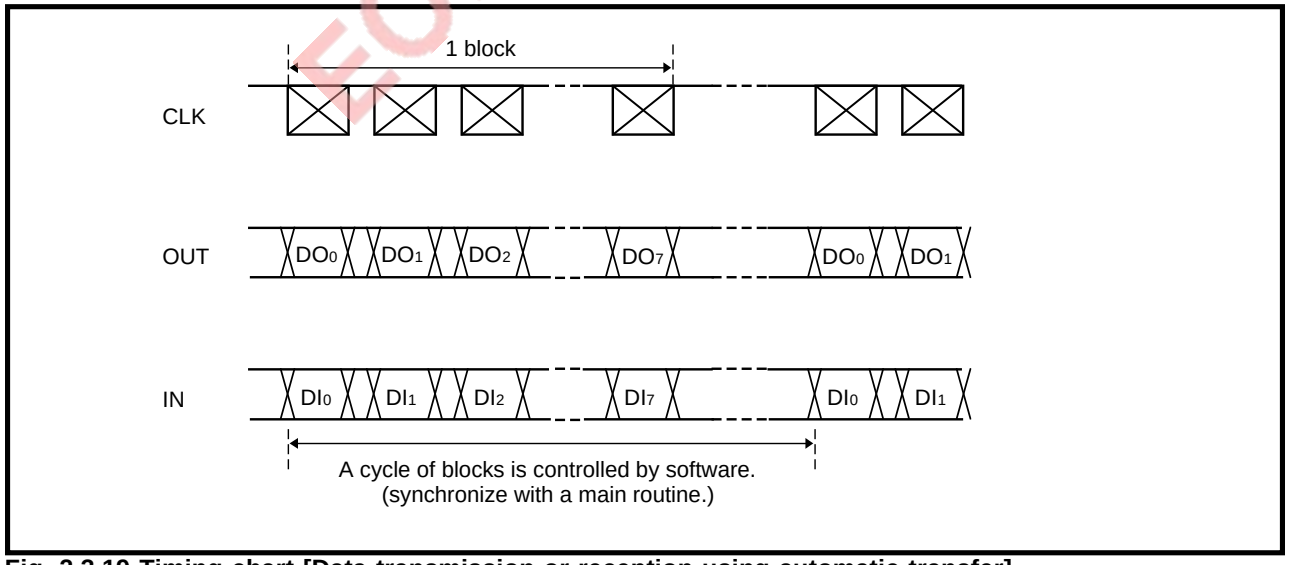


Fig. 2.3.19 Timing chart [Data transmission or reception using automatic transfer]

EOL announced

Downloaded from Elcodis.com electronic components distributor

2. APPLICATION

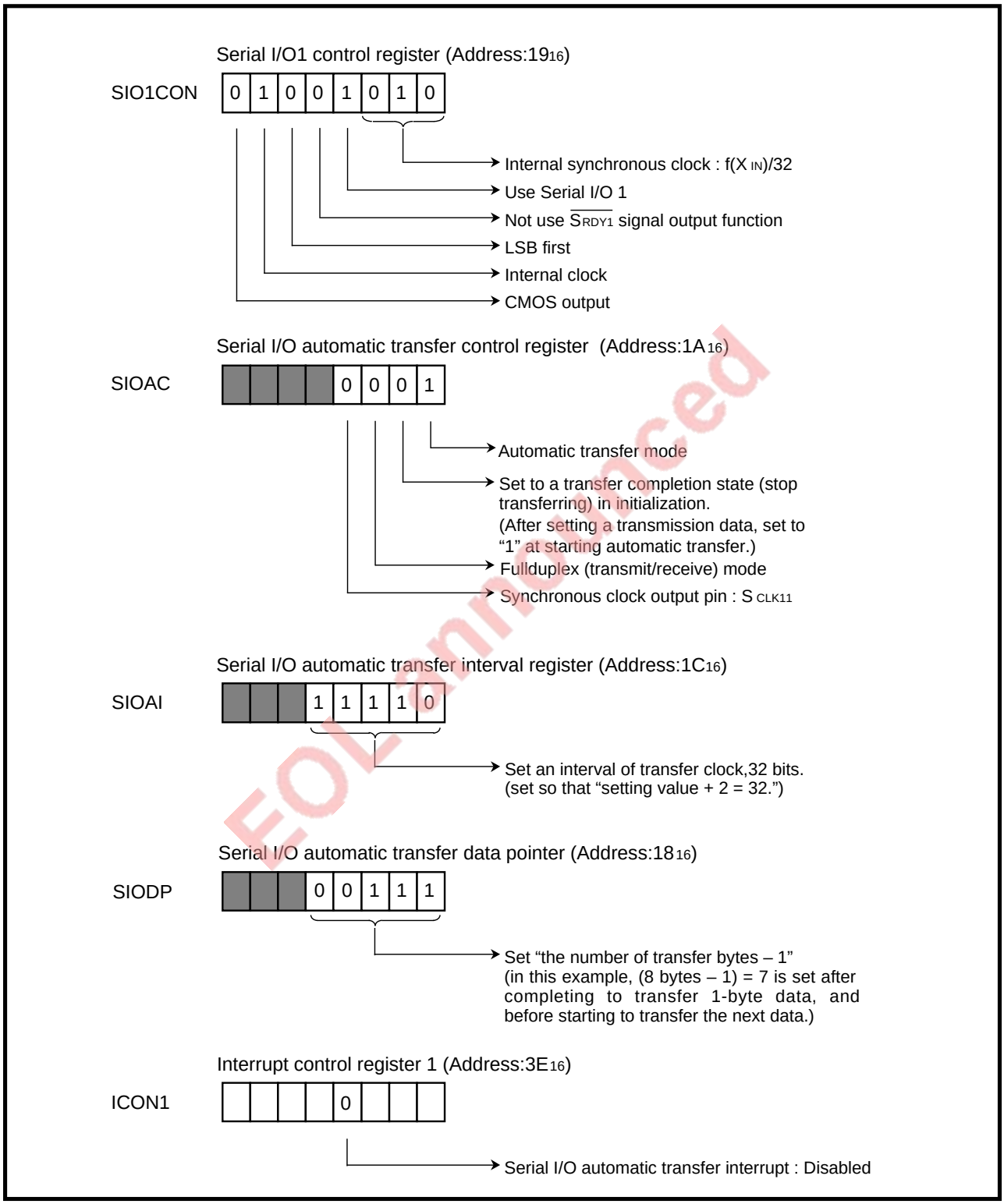
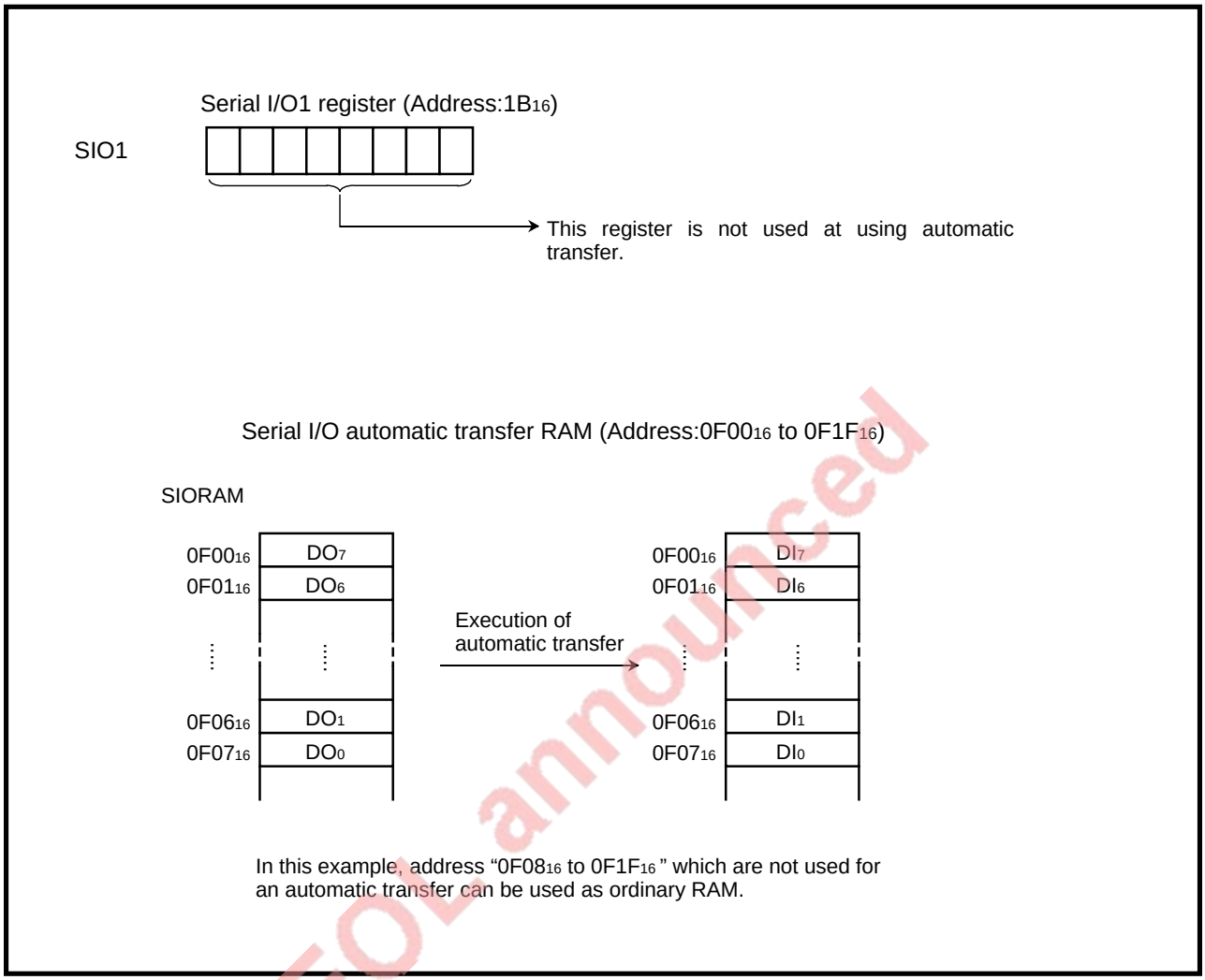


Fig. 2.3.20 Setting of related registers [Data transmission or reception using automatic transfer]

EOL announced

Downloaded from Elcodis.com electronic components distributor

2. APPLICATION



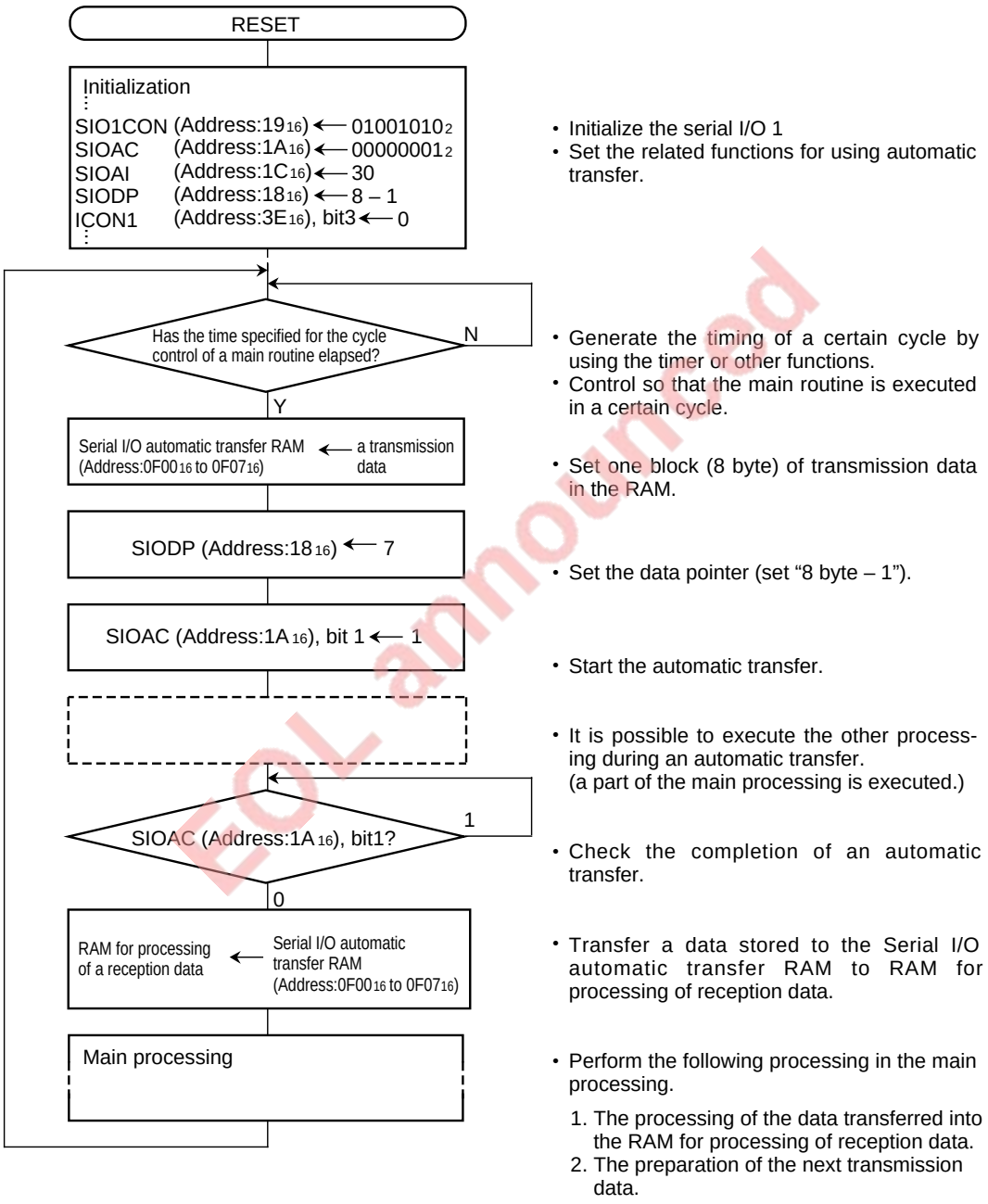
EOL announced

Fig. 2.3.21 Setting of transmission data [Data transmission or reception using automatic transfer]

Downloaded from Elcodis.com electronic components distributor

2. APPLICATION

Control procedure : In this example, a serial communication is performed at the beginning of the main routine which loops in a certain cycle.



EOL announced

Fig. 2.3.22 Control procedure [Data transmission or reception using automatic transfer]

Downloaded from Elcodis.com electronic components distributor

2. APPLICATION

(3) Cyclic transmission or reception of block data (data of a specified number of bytes) between microcomputers [without using an automatic transfer]

Outline : When a clock synchronous serial I/O is used for communication, synchronization of the clock and the data between the transmitter and receiver sides may be lost because of noise included in the synchronizing clock. Thus, it is necessary to be corrected constantly. This "heading adjustment" is carried out by using the interval between blocks in this example.

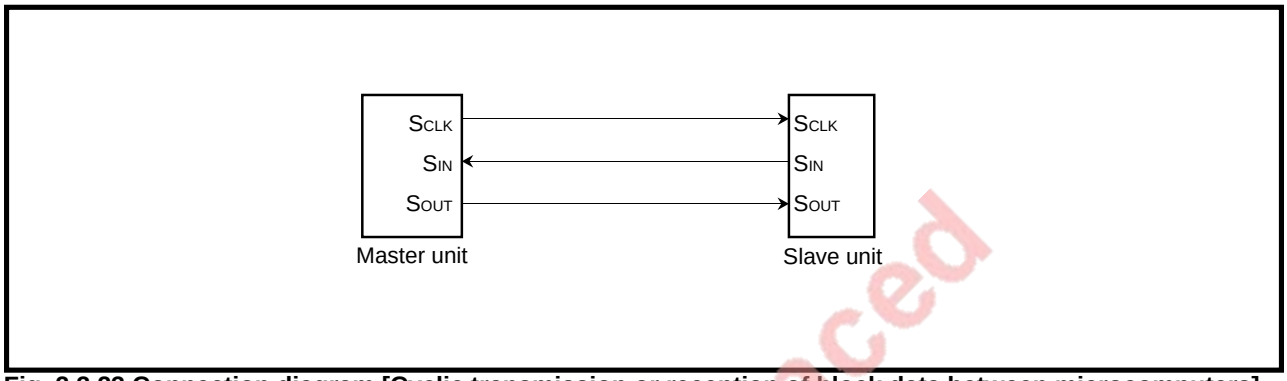


Fig. 2.3.23 Connection diagram [Cyclic transmission or reception of block data between microcomputers]

Specifications :
- Synchronous clock frequency : 131 kHz (f(XIN) = 4.19 MHz is divided by 32)
- Byte cycle : 488 µs
- Number of bytes for transmission or reception : each 8 byte/block
- Block transmission cycle : 16 ms
- Block transmission period : 3.5 ms
- Interval between blocks : 12.5 ms
- Heading adjustive time : 8 ms
- Transmission direction : LSB first

Limitations of the specifications

1. Reading of the reception data and setting of the next transmission data must be completed within the time obtained from "byte cycle – time for transmitting 1-byte data" (in this example, the time taken from generating of the Serial I/O 1 interrupt request to generating of the next synchronizing clock is 431 µs).
2. "Heading adjustive time < interval between blocks" must be satisfied.
3. Although the transmission direction can be switched for the Serial I/O of 3819 group, it cannot be switched for some serial I/Os of 740 family including 38000 series (only LSB first). Be sure to check when deciding specifications.

EOL announced

Downloaded from Elcodis.com electronic components distributor

2. APPLICATION

The communication is performed according to the timing shown below. In the slave unit, when a synchronizing clock is not input within a certain time (heading adjustive time), the next clock input is processed as the beginning (heading) of a block.
When a clock is input again after one block (8 byte) is received, the clock is ignored.
Figure 2.3.25 shows a setting of related registers.

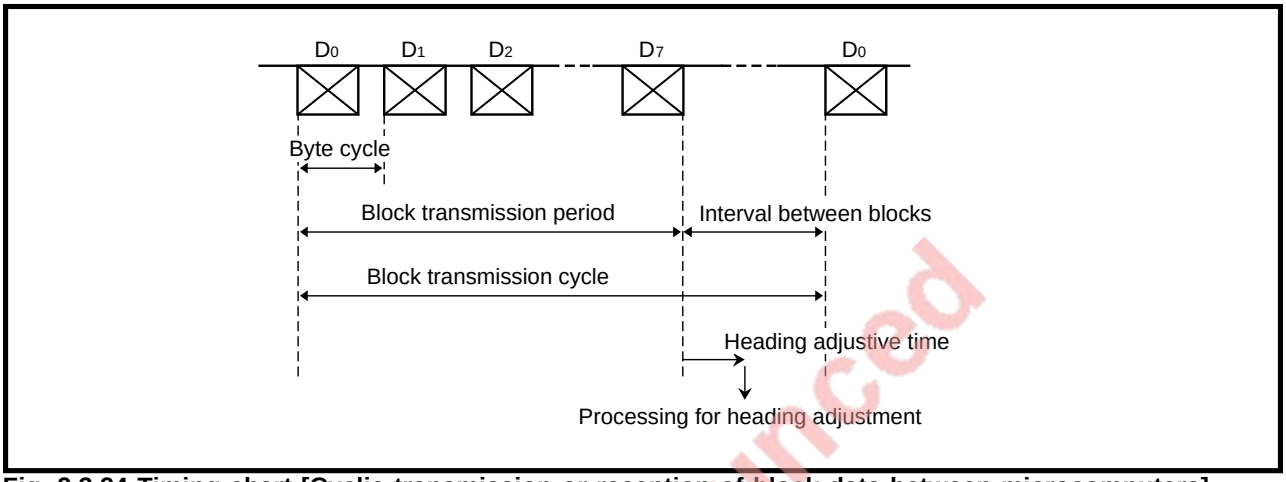


Fig. 2.3.24 Timing chart [Cyclic transmission or reception of block data between microcomputers]

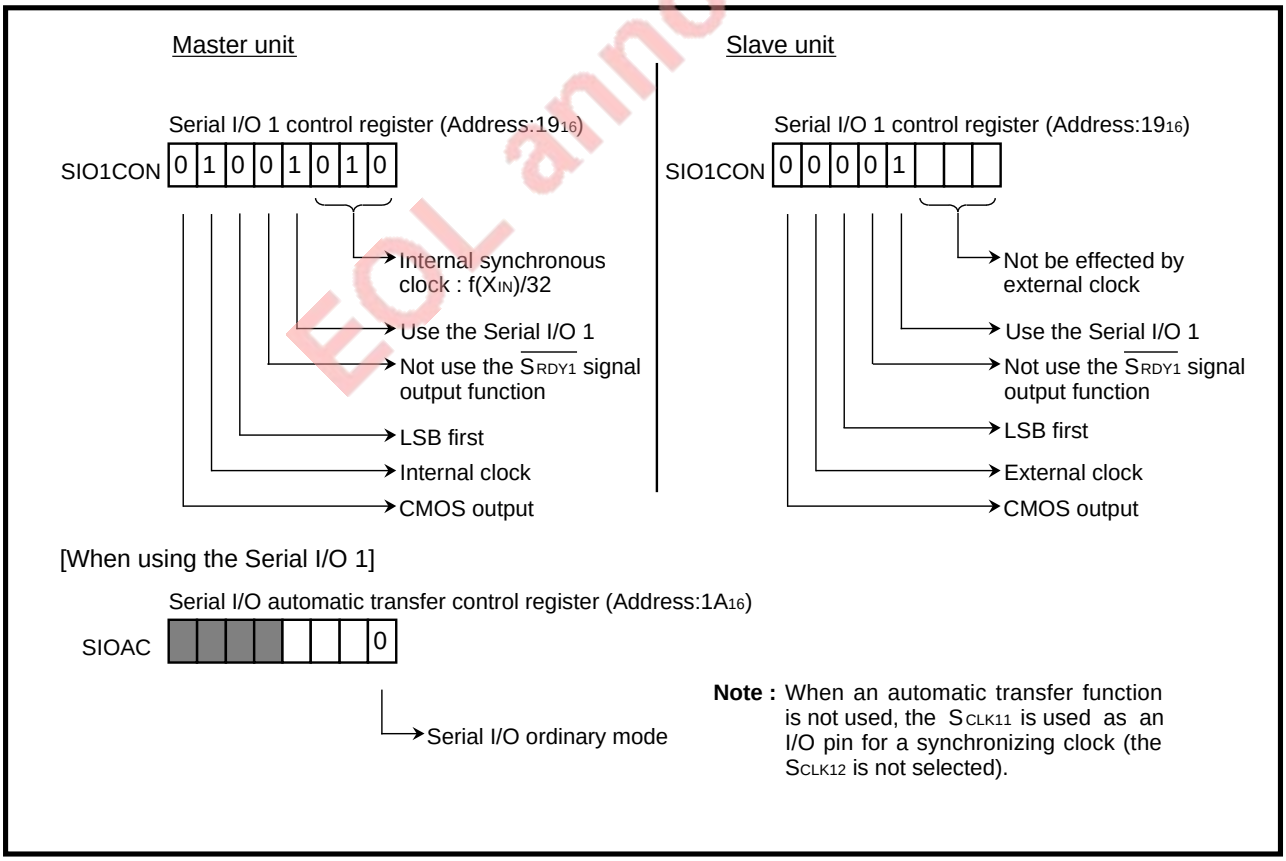


Fig. 2.3.25 Setting of related registers [Cyclic transmission or reception of block data between microcomputers]

EOL announced

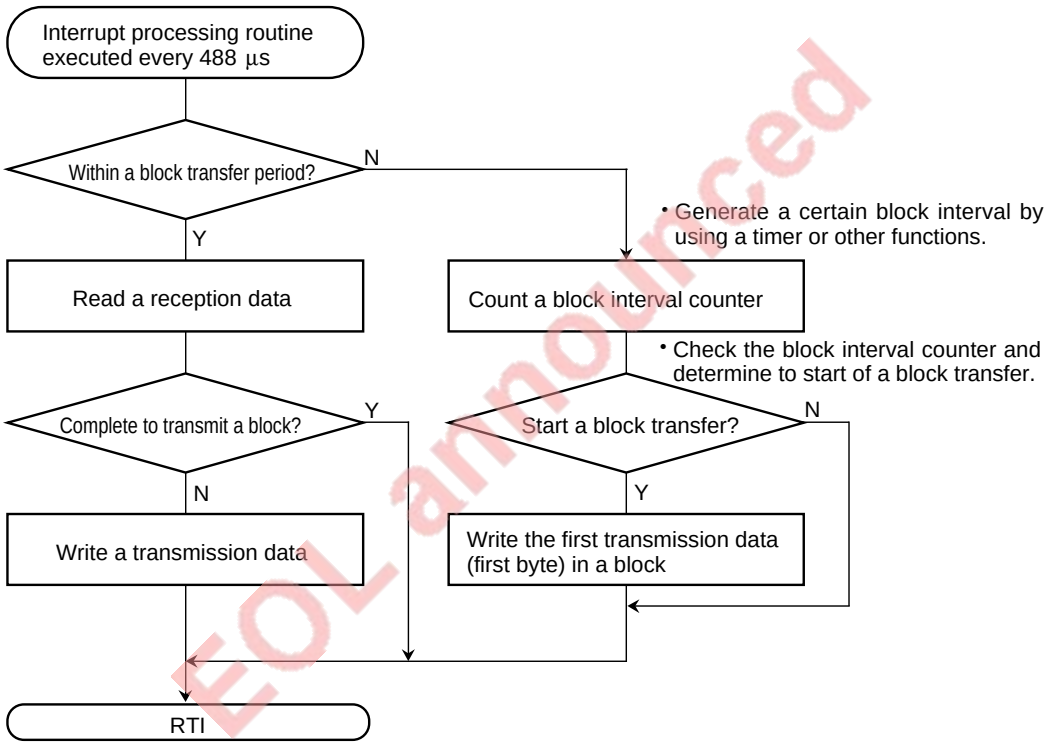
Downloaded from Elcodis.com electronic components distributor

2. APPLICATION

Control procedure :

(1) Control in the master unit

After a setting of the related registers is completed as shown in Figure 2.3.25, in the master unit transmission or reception of one-byte data is started simply by writing transmission data to the Serial I/O 1 register.
To perform the communication in the timing shown in the specifications, therefore, take the timing into account and write transmission data. Read out the reception data when the Serial I/O 1 interrupt request bit is set to "1", or before the next transmission data is written to the Serial I/O 1 register.
A processing example in the master unit using timer interrupts is shown below.



EOL announced

Fig. 2.3.26 Control in the master unit

Downloaded from Elcodis.com electronic components distributor

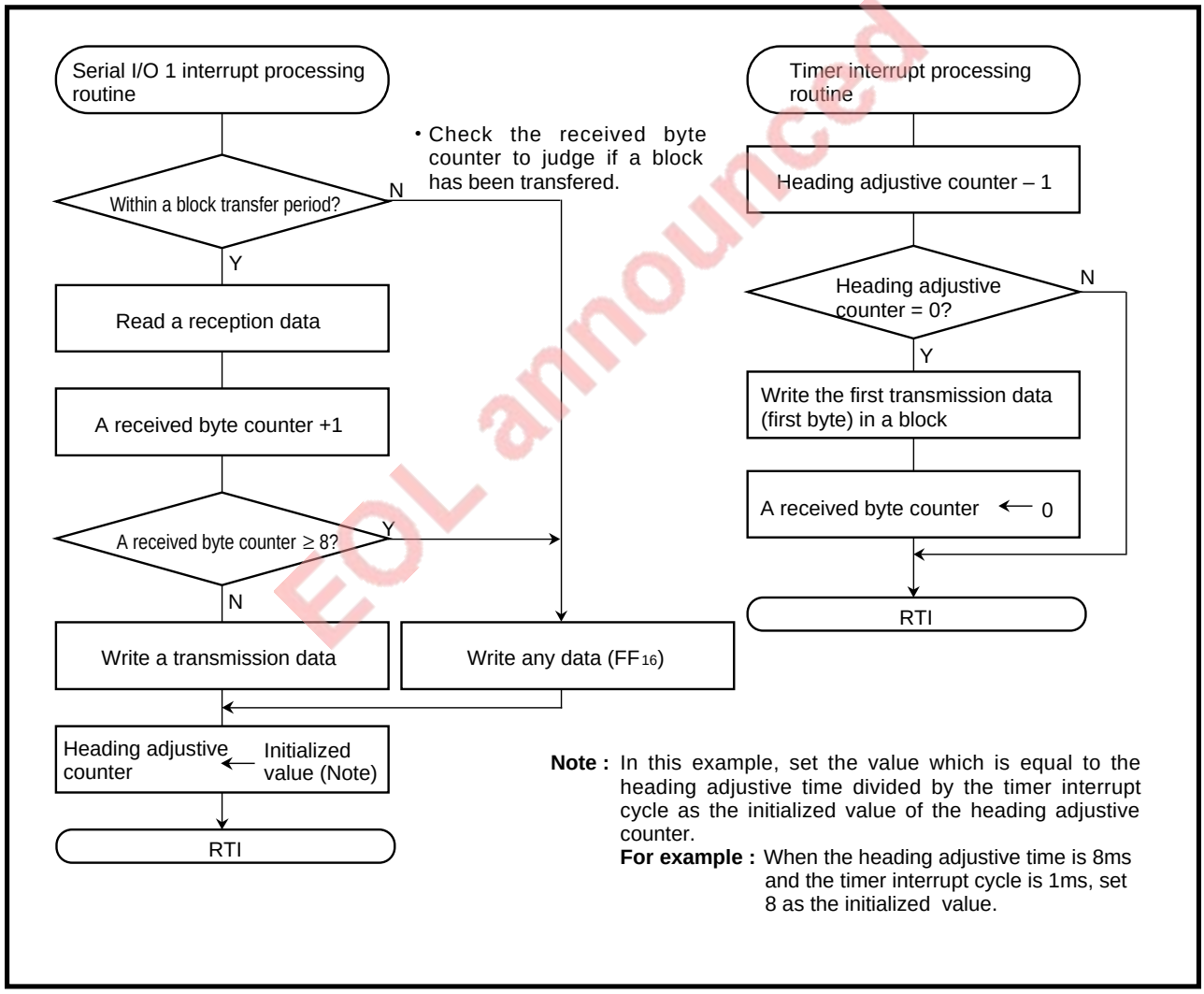
(2) Control in the slave unit

After a setting of the related registers is completed as shown in Figure 2.3.25, the slave unit becomes the state which is received a synchronizing clock at all times, and the Serial I/O 1 interrupt request bit is set to "1" every time an 8-bit synchronous clock is received.

For transmitting or receiving data according to the synchronizing clock input in the timing shown in the specifications, read out the reception data and write the next transmission data to the Serial I/O 1 register in the following conditions.

• When the Serial I/O 1 interrupt occurs.
• When the Serial I/O 1 interrupt request bit is set to "1" as the result of checking.

When the Serial I/O 1 interrupt request bit is not set to "1" within a certain time (heading adjustive time), the first byte of the transmission data in a block is written to the Serial I/O 1 register, then the next reception data is processed as the first byte of the reception data in a block. A processing example in the slave unit using serial I/O interrupts and timer interrupts (for a heading adjustment) is shown below.



EOL announced

Fig. 2.3.27 Control in the slave unit

Downloaded from Elcodis.com electronic components distributor

2.4 A-D conversion

2.4.1 Related registers

AD/DA control register

b7 b6 b5 b4 b3 b2 b1 b0

AD/DA control register (ADCON) [Address:2C16]

B	Name	Function	At reset	R	W
0	Analog input pin selection bits	b3 b2 b1 b0 0 0 0 0 : P70/AN0 0 0 0 1 : P71/AN1 0 0 1 0 : P72/AN2 0 0 1 1 : P73/AN3 0 1 0 0 : P74/AN4 0 1 0 1 : P75/AN5 0 1 1 0 : P76/AN6 0 1 1 1 : P77/AN7 1 0 0 0 : P50/SIN2/AN8 1 0 0 1 : P51/SOUT2/AN9 1 0 1 0 : P52/SCLK2/AN10 1 0 1 1 : P53/SRDY2/AN11 1 1 0 0 : P54/SIN3/AN12 1 1 0 1 : P55/SOUT3/AN13 1 1 1 0 : P56/SCLK3/AN14 1 1 1 1 : P57/SRDY3/AN15	0	○	○
1			0	○	○
2			0	○	○
3			0	○	○
4	A-D conversion completion bit	0 : Conversion in progress 1 : Conversion completed	1	○	○
5	Nothing is allocated for this bit. This is a write disabled bit. When this bit is read out, the value is "0."		0	○	×
6	D-A output enable bit	0 : Disable 1 : Enable	0	○	○
7	Nothing is allocated for this bit. This is a write disabled bit. When this bit is read out, the value is "0."		0	○	×

EOL announced

Fig. 2.4.1 Structure of AD/DA control register

A-D conversion register

b7 b6 b5 b4 b3 b2 b1 b0

A-D conversion register (AD) [Address:2D16]

B	Function	At reset	R	W
0	The read-only register which A-D conversion results are stored.	?	○	×
1		?	○	×
2		?	○	×
3		?	○	×
4		?	○	×
5		?	○	×
6		?	○	×
7		?	○	×

Fig. 2.4.2 Structure of A-D conversion register

Downloaded from Elcodis.com electronic components distributor

2. APPLICATION

Interrupt request register 2

b7 b6 b5 b4 b3 b2 b1 b0

Interrupt request reigster 2 (IREQ2) [Address:3D$_{16}$]

b	Name	Function	At reset	R	W
0	Timer 3 interrupt request bit	0 : No interrupt request 1 : Interrupt request	0	○	*
1	Timer 4 interrupt request bit	0 : No interrupt request 1 : Interrupt request	0	○	*
2	Timer 5 interrupt request bit	0 : No interrupt request 1 : Interrupt request	0	○	*
3	Timer 6 interrupt request bit	0 : No interrupt request 1 : Interrupt request	0	○	*
4	INT_3 interrupt request bit	0 : No interrupt request 1 : Interrupt request	0	○	*
5	• INT_4 interrupt request bit • A-D conversion interrupt request bit	0 : No interrupt request 1 : Interrupt request	0	○	*
6	• FLD blanking interrupt request bit • FLD digit interrupt request bit	0 : No interrupt request 1 : Interrupt request	0	○	*
7	Nothing is allocated for this bit. This is a write disabled bit. When this bit is read out, the value is "0."		0	○	*

* "0" is set by software, but not "1."

Fig. 2.4.3 Structure of Interrupt request register 2

Interrupt control register 2

b7 b6 b5 b4 b3 b2 b1 b0

0

Interrupt control reigster 2 (ICON2) [Address:3F$_{16}$]

b	Name	Function	At reset	R	W
0	Timer 3 interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	○	○
1	Timer 4 interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	○	○
2	Timer 5 interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	○	○
3	Timer 6 interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	○	○
4	INT_3 interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	○	○
5	• INT_4 interrupt enable bit • A-D conversion interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	○	○
6	• FLD blanking interrupt enable bit • FLD digit interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	○	○
7	Fix this bit to "0."		0	○	○

Fig. 2.4.4 Structure of Interrupt control register 2

EOL announced

Downloaded from Elcodis.com electronic components distributor

2. APPLICATION

2.4.2 A-D conversion application example

Conversion of Analog input voltage

Outline : The analog input voltage input from the sensor is converted into digital values.

Figure 2.4.5 shows a connection diagram, and Figure 2.4.6 shows a setting of related registers.

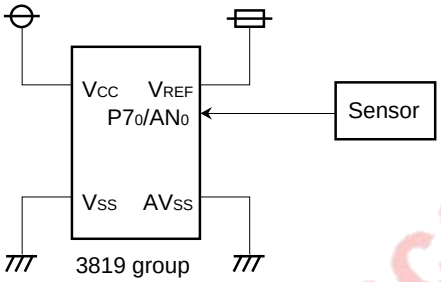
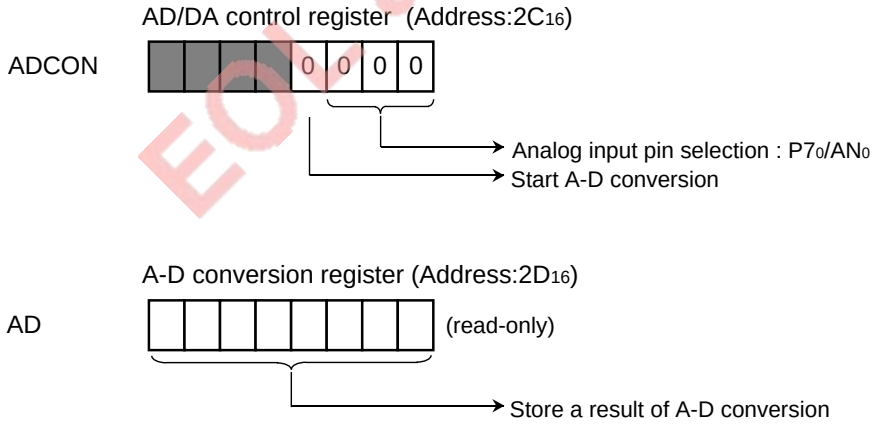


Fig. 2.4.5 Connection diagram [Conversion of Analog input voltage]

Specifications : • The AN_0 pin is used as an analog input pin.
• The analog input voltage input from the sensor is converted into digital values.



Note : Read out a result of A-D conversion after bit 4 of the AD/DA control register (ADCON) is set to "1".

Fig. 2.4.6 Setting of related registers [Conversion of Analog input voltage]

EOL announced

Downloaded from Elcodis.com electronic components distributor

2. APPLICATION

Control procedure : By setting the related registers as shown in Figure 2.4.6, the analog input voltage input from the sensor are converted into digital values.

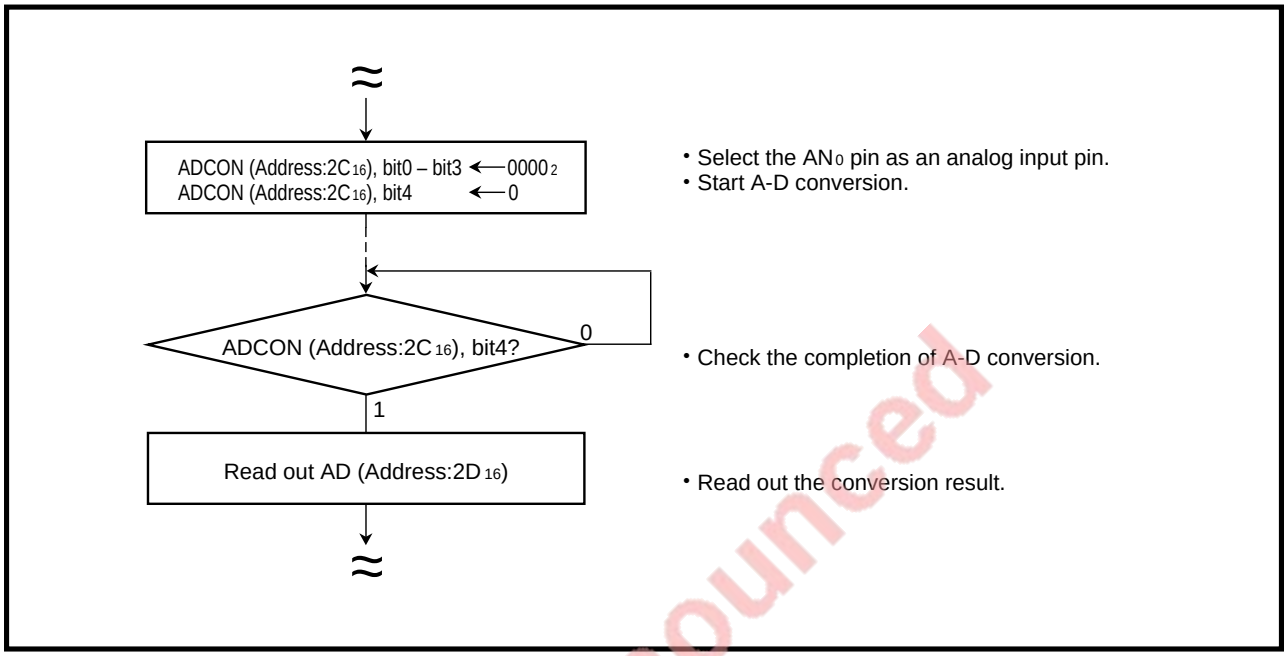


Fig. 2.4.7 Control procedure [Conversion of Analog input voltage]

EOL announced

Downloaded from Elcodis.com electronic components distributor

2.5 FLD controller

2.5.1 Related registers

Port P0 segment/digit switch register

b7 b6 b5 b4 b3 b2 b1 b0

Port P0 segment/digit switch register (P0SDR) [Address:32_{16}]

B	Name	Function	At reset	R	W
0	Port P0 segment/digit switch register	0 : DIG_0 1 : SEG_{32}	0	○	○
1		0 : DIG_1 1 : SEG_{33}	0	○	○
2		0 : DIG_2 1 : SEG_{34}	0	○	○
3		0 : DIG_3 1 : SEG_{35}	0	○	○
4		0 : DIG_4 1 : SEG_{36}	0	○	○
5		0 : DIG_5 1 : SEG_{37}	0	○	○
6		0 : DIG_6 1 : SEG_{38}	0	○	○
7		0 : DIG_7 1 : SEG_{39}	0	○	○

Fig. 2.5.1 Structure of Port P0 segment/digit switch register

Port P2 digit/port switch register

b7 b6 b5 b4 b3 b2 b1 b0

Port P2 digit/port switch register (P2DPR) [Address:33_{16}]

B	Name	Function	At reset	R	W
0	Port P2 digit/port switch register	0 : Port $P2_0$ output-only 1 : DIG_{16}	0	○	○
1		0 : Port $P2_1$ output-only 1 : DIG_{17}	0	○	○
2		0 : Port $P2_2$ output-only 1 : DIG_{18}	0	○	○
3		0 : Port $P2_3$ output-only 1 : DIG_{19}	0	○	○
4	Nothing is allocated for these bits. These are write disabled bits. When these bits are read out, the values are "0."		0	○	×
5			0	○	×
6			0	○	×
7			0	○	×

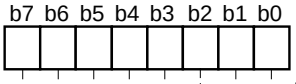
Fig. 2.5.2 Structure of Port P2 digit/port switch register

EOL announced

Downloaded from Elcodis.com electronic components distributor

2. APPLICATION

Port P8 segment/port switch register

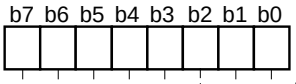


Port P8 segment/port switch register (P8SPR) [Address:34 16]

B	Name	Function	At reset	R	W
0	Port P8 segment/port switch register	0 : Port $P8_0$ for I/O 1 : SEG_8	0	○	○
1		0 : Port $P8_1$ for I/O 1 : SEG_9	0	○	○
2		0 : Port $P8_2$ for I/O 1 : SEG_{10}	0	○	○
3		0 : Port $P8_3$ for I/O 1 : SEG_{11}	0	○	○
4		0 : Port $P8_4$ for I/O 1 : SEG_{12}	0	○	○
5		0 : Port $P8_5$ for I/O 1 : SEG_{13}	0	○	○
6		0 : Port $P8_6$ for I/O 1 : SEG_{14}	0	○	○
7		0 : Port $P8_7$ for I/O 1 : SEG_{15}	0	○	○

Fig. 2.5.3 Structure of Port P8 segment/port switch register

Port PA segment/port switch register



Port PA segment/port switch register (PASPR) [Address:35 16]

B	Name	Function	At reset	R	W
0	Port PA segment/port switch register	0 : Port PA_0 for I/O 1 : SEG_0	0	○	○
1		0 : Port PA_1 for I/O 1 : SEG_1	0	○	○
2		0 : Port PA_2 for I/O 1 : SEG_2	0	○	○
3		0 : Port PA_3 for I/O 1 : SEG_3	0	○	○
4		0 : Port PA_4 for I/O 1 : SEG_4	0	○	○
5		0 : Port PA_5 for I/O 1 : SEG_5	0	○	○
6		0 : Port PA_6 for I/O 1 : SEG_6	0	○	○
7		0 : Port PA_7 for I/O 1 : SEG_7	0	○	○

Fig. 2.5.4 Structure of Port PA segment/port switch register

EOL announced

Downloaded from Elcodis.com electronic components distributor

2. APPLICATION

FLDC mode register 1

b7 b6 b5 b4 b3 b2 b1 b0

FLDC mode register 1 (FLDM1) [Address:36_{16}]

B	Name	Function	At reset	R	W
0	Tscan control bits	b1b0 0 0 : FLD digit interrupt (at rising edge of each digit) 0 1 : 1 × Tdisp 1 0 : 2 × Tdisp 1 1 : 3 × Tdisp } FLD blanking interrupt (at falling edge of the last digit)	0	○	○
1			0	○	○
2	Toff control bit (Setting of digit/segment OFF time)	b5 b4 b3 b2 0 0 0 0 : 1/16 × Tdisp 0 0 0 1 : 2/16 × Tdisp 0 0 1 0 : 3/16 × Tdisp 0 0 1 1 : 4/16 × Tdisp 0 1 0 0 : 5/16 × Tdisp 0 1 0 1 : 6/16 × Tdisp 0 1 1 0 : 7/16 × Tdisp 0 1 1 1 : 8/16 × Tdisp 1 0 0 0 : 9/16 × Tdisp 1 0 0 1 : 10/16 × Tdisp 1 0 1 0 : 11/16 × Tdisp 1 0 1 1 : 12/16 × Tdisp 1 1 0 0 : 13/16 × Tdisp 1 1 0 1 : 14/16 × Tdisp 1 1 1 0 : 15/16 × Tdisp 1 1 1 1 : 16/16 × Tdisp	0	○	○
3			0	○	○
4			0	○	○
5			0	○	○
6	Nothing is allocated for this bit. This is a write disabled bit. When this bit is read out, the value is "0."		0	○	×
7	High-breakdown-voltage drivability selection bit	0 : Strong drivability 1 : Weak drivability	0	○	○

Fig. 2.5.5 Structure of FLDC mode register 1

EOL announced

Downloaded from Elcodis.com electronic components distributor

2. APPLICATION

FLDC mode register 2

b7 b6 b5 b4 b3 b2 b1 b0

FLDC mode register 2 (FLDM2) [Address:37$_{16}$]

B	Name	Function	At reset	R	W
0	Automatic display control bit (P0,P1,P2$_0$–P2$_3$,P3,P8,P9,PA)	0 : Ordinary mode 1 : Automatic display mode	0	○	○
1	Display start bit	0 : Display stopped 1 : Display in progress (display starts by writing "1" to this bit which is set to "0".)	0	○	○
2	Tdisp control bits (digit time setting) (at 8 MHz oscillation frequency)	b5 b4 b3 b2 0 0 0 0 : 128 µs 0 0 0 1 : 256 µs 0 0 1 0 : 384 µs 0 0 1 1 : 512 µs 0 1 0 0 : 640 µs 0 1 0 1 : 768 µs 0 1 1 0 : 896 µs 0 1 1 1 : 1024 µs 1 0 0 0 : 1152 µs 1 0 0 1 : 1280 µs 1 0 1 0 ⋮ } Not available 1 1 1 1	0	○	○
3			0	○	○
4			0	○	○
5			0	○	○
6	P1$_0$ segment/digit switch bit	0 : Digit (DIG$_8$) 1 : Segment (SEG$_{40}$)	0	○	○
7	P1$_1$ segment/digit switch bit	0 : Digit (DIG$_9$) 1 : Segment (SEG$_{41}$)	0	○	○

EOL announced

Fig. 2.5.6 Structure of FLDC mode register 2

Downloaded from Elcodis.com electronic components distributor

2. APPLICATION

FLD data pointer

b7 b6 b5 b4 b3 b2 b1 b0

FLD data pointer (FLDDP) [Address:38$_{16}$]

B	Function	At reset	R	W
0	Indicate the address of data which is transfered to the segment of the FLD automatic display RAM.	?	○	×
1		?	○	×
2		?	○	×
3		?	○	×
4		?	○	×
5		?	○	×
6		?	○	×
7	Nothing is allocated for this bit. This is a write disabled bit. When this bit is read out, the value is "0."	0	○	×

Fig. 2.5.7 Structure of FLD data pointer

FLD data pointer reload register

b7 b6 b5 b4 b3 b2 b1 b0

FLD data pointer reload register (FLDDP) [Address:38$_{16}$]

B	Function	At reset	R	W
0	Indicate the first digit address of the high-order segment.	?	×	○
1		?	×	○
2		?	×	○
3		?	×	○
4		?	×	○
5		?	×	○
6		?	×	○
7	Nothing is allocated for this bit. This is a write disabled bit.	?	×	×

Fig. 2.5.8 Structure of FLD data pointer reload register

E.O.L. announced

Downloaded from Elcodis.com electronic components distributor

2. APPLICATION

Interrupt request register 2

b7 b6 b5 b4 b3 b2 b1 b0

Interrupt request reigster 2 (IREQ2) [Address:3D$_{16}$]

b	Name	Function	At reset	R	W
0	Timer 3 interrupt request bit	0 : No interrupt request 1 : Interrupt request	0	○	*
1	Timer 4 interrupt request bit	0 : No interrupt request 1 : Interrupt request	0	○	*
2	Timer 5 interrupt request bit	0 : No interrupt request 1 : Interrupt request	0	○	*
3	Timer 6 interrupt request bit	0 : No interrupt request 1 : Interrupt request	0	○	*
4	INT$_3$ interrupt request bit	0 : No interrupt request 1 : Interrupt request	0	○	*
5	• INT$_4$ interrupt request bit • A-D conversion interrupt request bit	0 : No interrupt request 1 : Interrupt request	0	○	*
6	• FLD blanking interrupt request bit • FLD digit interrupt request bit	0 : No interrupt request 1 : Interrupt request	0	○	*
7	Nothing is allocated for this bit. This is a write disabled bit. When this bit is read out, the value is "0."		0	○	*

* "0" is set by software, but not "1."

Fig. 2.5.9 Structure of Interrupt request register 2

Interrupt control register 2

b7 b6 b5 b4 b3 b2 b1 b0

0

Interrupt control reigster 2 (ICON2) [Address:3F$_{16}$]

b	Name	Function	At reset	R	W
0	Timer 3 interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	○	○
1	Timer 4 interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	○	○
2	Timer 5 interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	○	○
3	Timer 6 interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	○	○
4	INT$_3$ interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	○	○
5	• INT$_4$ interrupt enable bit • A-D conversion interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	○	○
6	• FLD blanking interrupt enable bit • FLD digit interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	○	○
7	Fix this bit to "0."		0	○	○

Fig. 2.5.10 Structure of Interrupt control register 2

EOL announced

Downloaded from Elcodis.com electronic components distributor

2. APPLICATION

2.5.2 FLD controller application examples

(1) FLD automatic display and Key-scan using segment pin

Outline : The pannel with fluorescent display (FLD) is displayed by using FLD automatic display function. Then the key is read in with using segment pin by software.

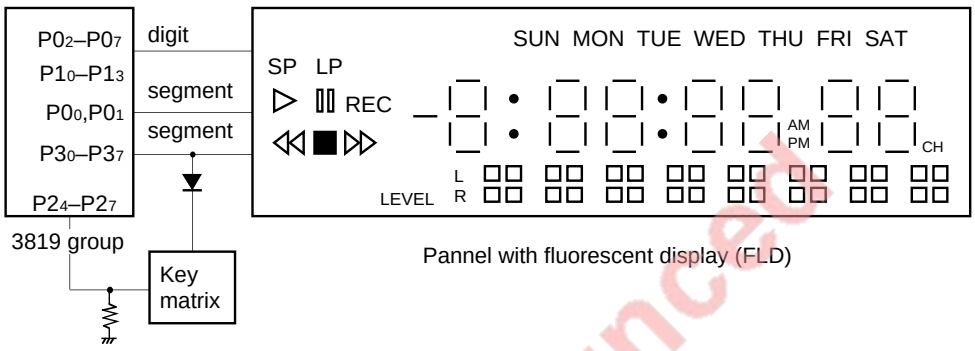


Fig. 2.5.11 Connection diagram [FLD automatic display and Key-scan using segment pin]

Specifications :
- The automatic display function is used.
- 10 digits and 10 segments are used.
- Toff = 15.27 µs, Tdisp = 244.39 µs, Tscan = 733.17 µs (at f(XIN) = 4.19 MHz)
- The FLD blanking interrupt is used.
- The segment pin is used for the Key-scan.

Figure 2.5.12 shows a timing chart of the Key-scan using an FLD automatic display and segments, and Figure 2.5.13 shows an enlarged view of SEG24 to SEG31 during Tscan.

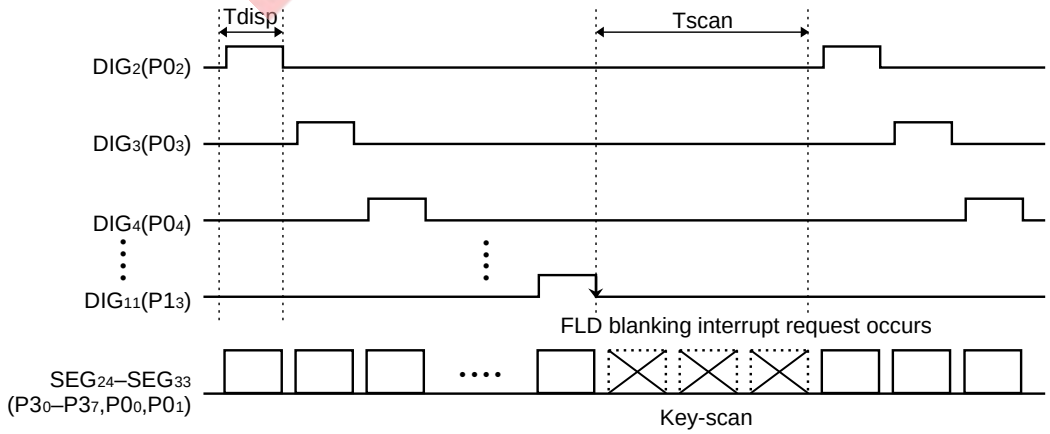


Fig. 2.5.12 Timing chart [FLD automatic display and Key-scan using segment pin]

EOL announced

Downloaded from Elcodis.com electronic components distributor

2. APPLICATION

After switching a segment pin to an output port, the waveform shown below is created by software, and the Key-scan is performed.

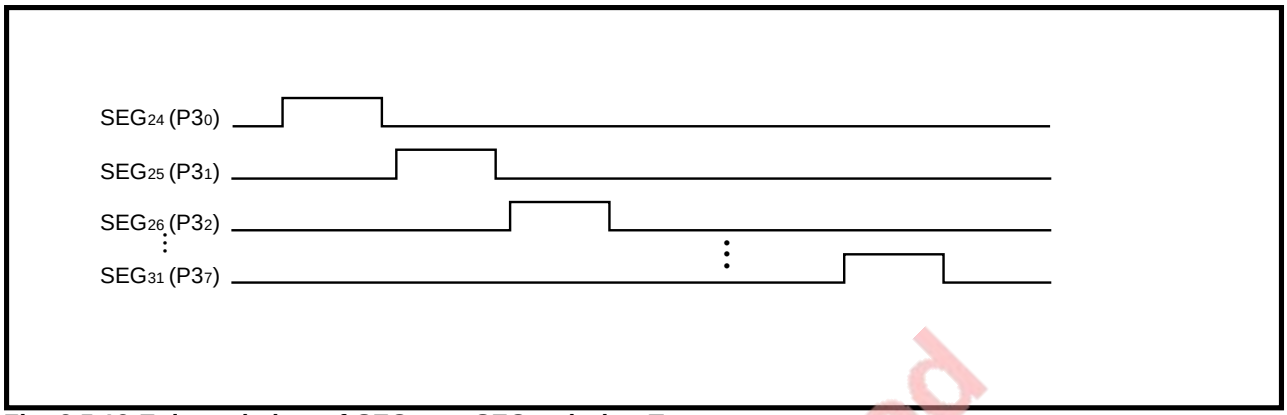


Fig. 2.5.13 Enlarged view of SEG24 to SEG31 during Tscan

Figures 2.5.14 and 2.5.15 show a setting of related registers.

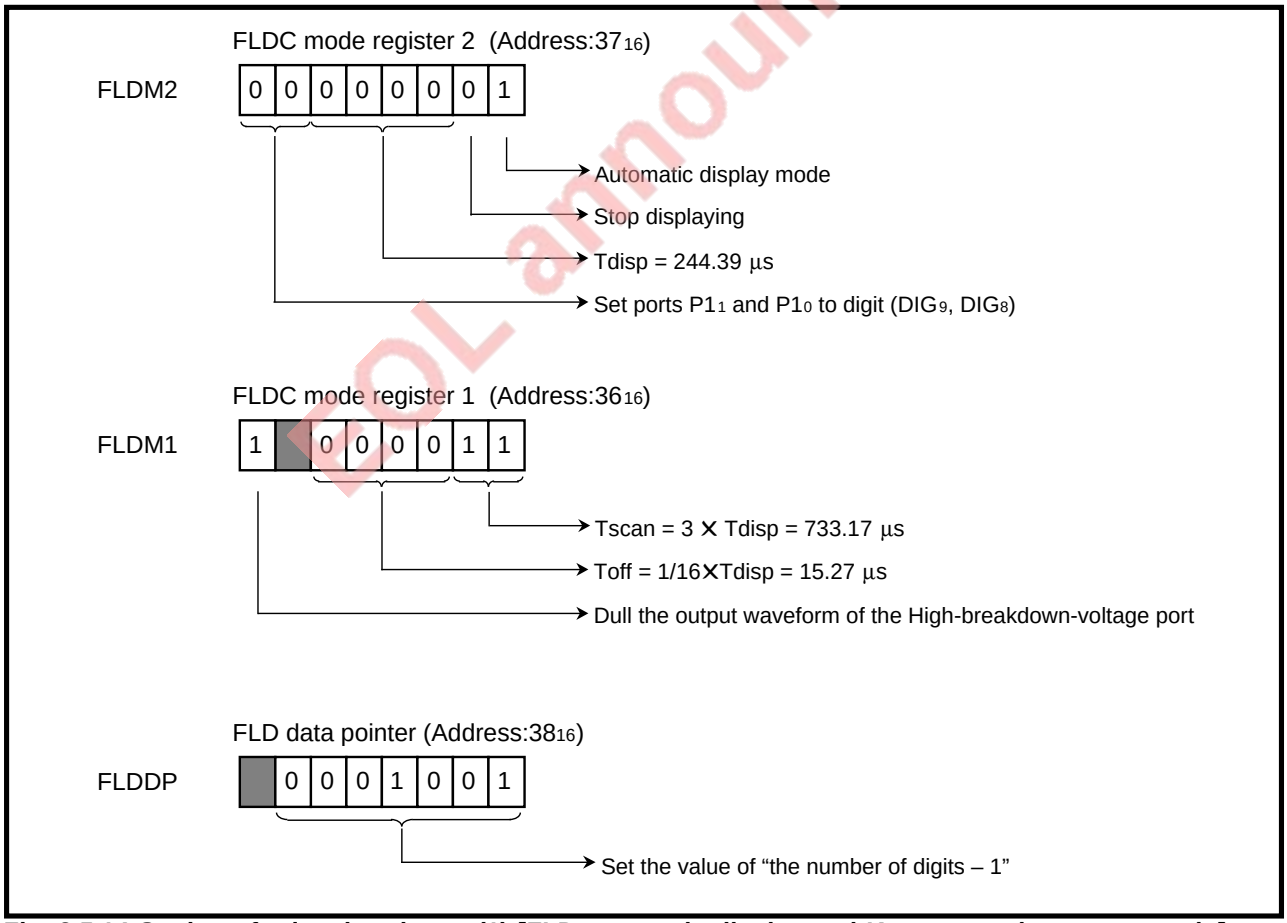


Fig. 2.5.14 Setting of related registers (1) [FLD automatic display and Key-scan using segment pin]

EOL announced

Downloaded from Elcodis.com electronic components distributor

2. APPLICATION

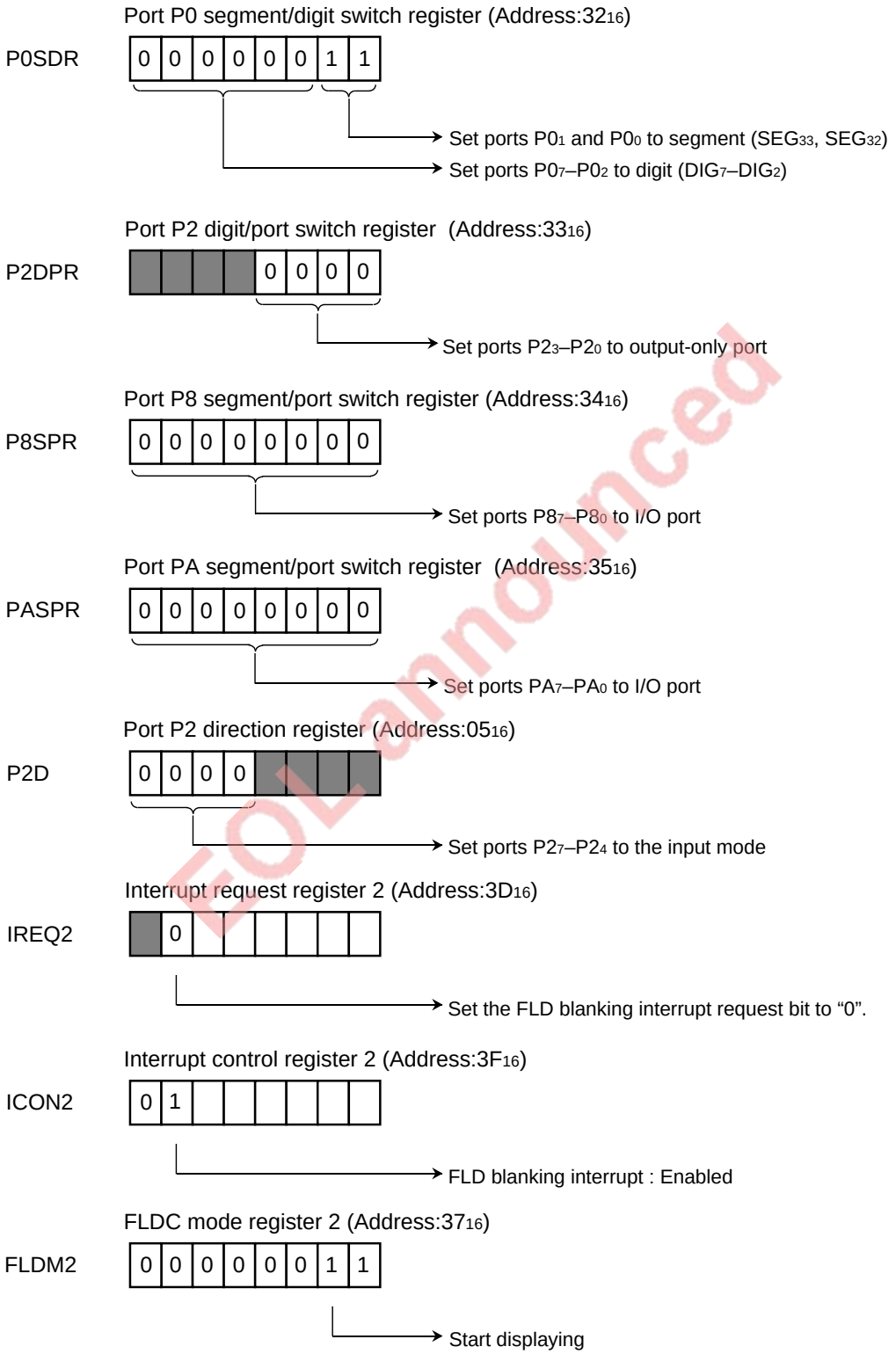


Fig. 2.5.15 Setting of related registers (2) [FLD automatic display and Key-scan using segment pin]

FOL announced

Downloaded from Elcodis.com electronic components distributor

Setting of FLD automatic display RAM :

Table 2.5.1 FLD automatic display RAM map [FLD automatic display and Key-scan using segment pin]

Address	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
$0FB0_{16}$	SEG_{31}	SEG_{30}	SEG_{29}	SEG_{28}	SEG_{27}	SEG_{26}	SEG_{25}	SEG_{24}	→ DIG_{11} ($P1_3$)
$0FB1_{16}$	SEG_{31}	SEG_{30}	SEG_{29}	SEG_{28}	SEG_{27}	SEG_{26}	SEG_{25}	SEG_{24}	→ DIG_{10} ($P1_2$)
$0FB2_{16}$	SEG_{31}	SEG_{30}	SEG_{29}	SEG_{28}	SEG_{27}	SEG_{26}	SEG_{25}	SEG_{24}	→ DIG_9 ($P1_1$)
$0FB3_{16}$	SEG_{31}	SEG_{30}	SEG_{29}	SEG_{28}	SEG_{27}	SEG_{26}	SEG_{25}	SEG_{24}	→ DIG_8 ($P1_0$)
$0FB4_{16}$	SEG_{31}	SEG_{30}	SEG_{29}	SEG_{28}	SEG_{27}	SEG_{26}	SEG_{25}	SEG_{24}	→ DIG_7 ($P0_7$)
$0FB5_{16}$	SEG_{31}	SEG_{30}	SEG_{29}	SEG_{28}	SEG_{27}	SEG_{26}	SEG_{25}	SEG_{24}	→ DIG_6 ($P0_6$)
$0FB6_{16}$	SEG_{31}	SEG_{30}	SEG_{29}	SEG_{28}	SEG_{27}	SEG_{26}	SEG_{25}	SEG_{24}	→ DIG_5 ($P0_5$)
$0FB7_{16}$	SEG_{31}	SEG_{30}	SEG_{29}	SEG_{28}	SEG_{27}	SEG_{26}	SEG_{25}	SEG_{24}	→ DIG_4 ($P0_4$)
$0FB8_{16}$	SEG_{31}	SEG_{30}	SEG_{29}	SEG_{28}	SEG_{27}	SEG_{26}	SEG_{25}	SEG_{24}	→ DIG_3 ($P0_3$)
$0FB9_{16}$	SEG_{31}	SEG_{30}	SEG_{29}	SEG_{28}	SEG_{27}	SEG_{26}	SEG_{25}	SEG_{24}	→ DIG_2 ($P0_2$)
$0FBA_{16}$									
$0FBB_{16}$									
$0FBC_{16}$									
$0FBD_{16}$									
$0FBE_{16}$									
$0FBF_{16}$									
$0FC0_{16}$							SEG_{33}	SEG_{32}	→ DIG_{11} ($P1_3$)
$0FC1_{16}$							SEG_{33}	SEG_{32}	→ DIG_{10} ($P1_2$)
$0FC2_{16}$							SEG_{33}	SEG_{32}	→ DIG_9 ($P1_1$)
$0FC3_{16}$							SEG_{33}	SEG_{32}	→ DIG_8 ($P1_0$)
$0FC4_{16}$							SEG_{33}	SEG_{32}	→ DIG_7 ($P0_7$)
$0FC5_{16}$							SEG_{33}	SEG_{32}	→ DIG_6 ($P0_6$)
$0FC6_{16}$							SEG_{33}	SEG_{32}	→ DIG_5 ($P0_5$)
$0FC7_{16}$							SEG_{33}	SEG_{32}	→ DIG_4 ($P0_4$)
$0FC8_{16}$							SEG_{33}	SEG_{32}	→ DIG_3 ($P0_3$)
$0FC9_{16}$							SEG_{33}	SEG_{32}	→ DIG_2 ($P0_2$)

: Area which is used to set a display value

: Area which is available as ordinary RAM

EOL announced

Downloaded from Elcodis.com electronic components distributor

2. APPLICATION

FLD digit allocation :

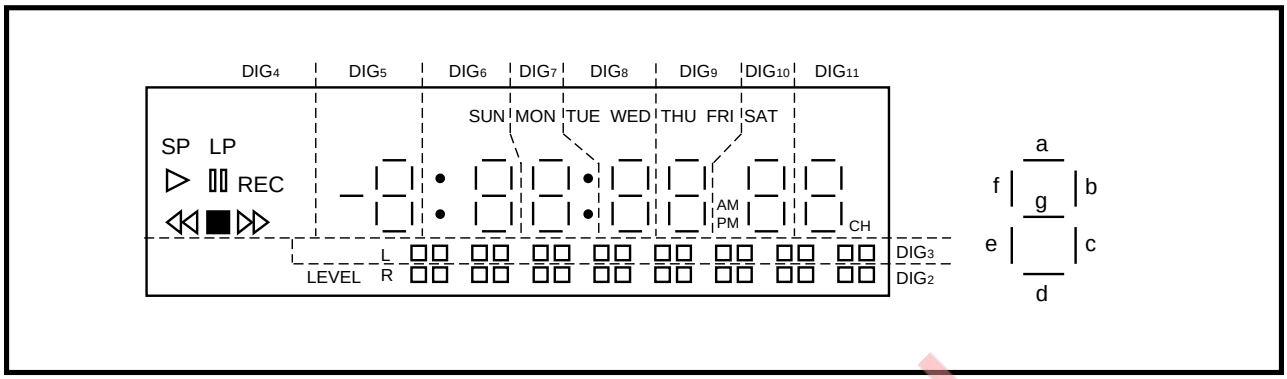


Fig. 2.5.16 Example of FLD digit allocation [FLD automatic display and Key-scan using segment pin]

Table 2.5.2 FLD automatic display RAM map example [FLD automatic display and Key-scan using segment pin]

Address	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
0FB0$_{16}$	CH	g	f	e	d	c	b	a	→ DIG$_{11}$ (P1$_3$)
0FB1$_{16}$	SAT	g	f	e	d	c	b	a	→ DIG$_{10}$ (P1$_2$)
0FB2$_{16}$	FRI	g	f	e	d	c	b	a	→ DIG$_9$ (P1$_1$)
0FB3$_{16}$	WED	g	f	e	d	c	b	a	→ DIG$_8$ (P1$_0$)
0FB4$_{16}$	MON	g	f	e	d	c	b	a	→ DIG$_7$ (P0$_7$)
0FB5$_{16}$	SUN	g	f	e	d	c	b	a	→ DIG$_6$ (P0$_6$)
0FB6$_{16}$	—	g	f	e	d	c	b	a	→ DIG$_5$ (P0$_5$)
0FB7$_{16}$	■	◁◁	▷▷	▯▯	▷	REC	SP	LP	→ DIG$_4$ (P0$_4$)
0FB8$_{16}$	□□	□□	□□	□□	□□	□□	□□	□□	→ DIG$_3$ (P0$_3$)
0FB9$_{16}$	□□	□□	□□	□□	□□	□□	□□	□□	→ DIG$_2$ (P0$_2$)
0FBA$_{16}$									
0FBB$_{16}$									
0FBC$_{16}$									
0FBD$_{16}$									
0FBE$_{16}$									
0FBF$_{16}$									
0FC0$_{16}$									→ DIG$_{11}$ (P1$_3$)
0FC1$_{16}$							PM	AM	→ DIG$_{10}$ (P1$_2$)
0FC2$_{16}$								THU	→ DIG$_9$ (P1$_1$)
0FC3$_{16}$								TUE	→ DIG$_8$ (P1$_0$)
0FC4$_{16}$								⋮	→ DIG$_7$ (P0$_7$)
0FC5$_{16}$								⋮	→ DIG$_6$ (P0$_6$)
0FC6$_{16}$									→ DIG$_5$ (P0$_5$)
0FC7$_{16}$									→ DIG$_4$ (P0$_4$)
0FC8$_{16}$							L		→ DIG$_3$ (P0$_3$)
0FC9$_{16}$							R	LEVEL	→ DIG$_2$ (P0$_2$)

: Unused

EOL announced

Downloaded from Elcodis.com electronic components distributor

2. APPLICATION

Control procedure :
Figure 2.5.17 shows a control procedure.

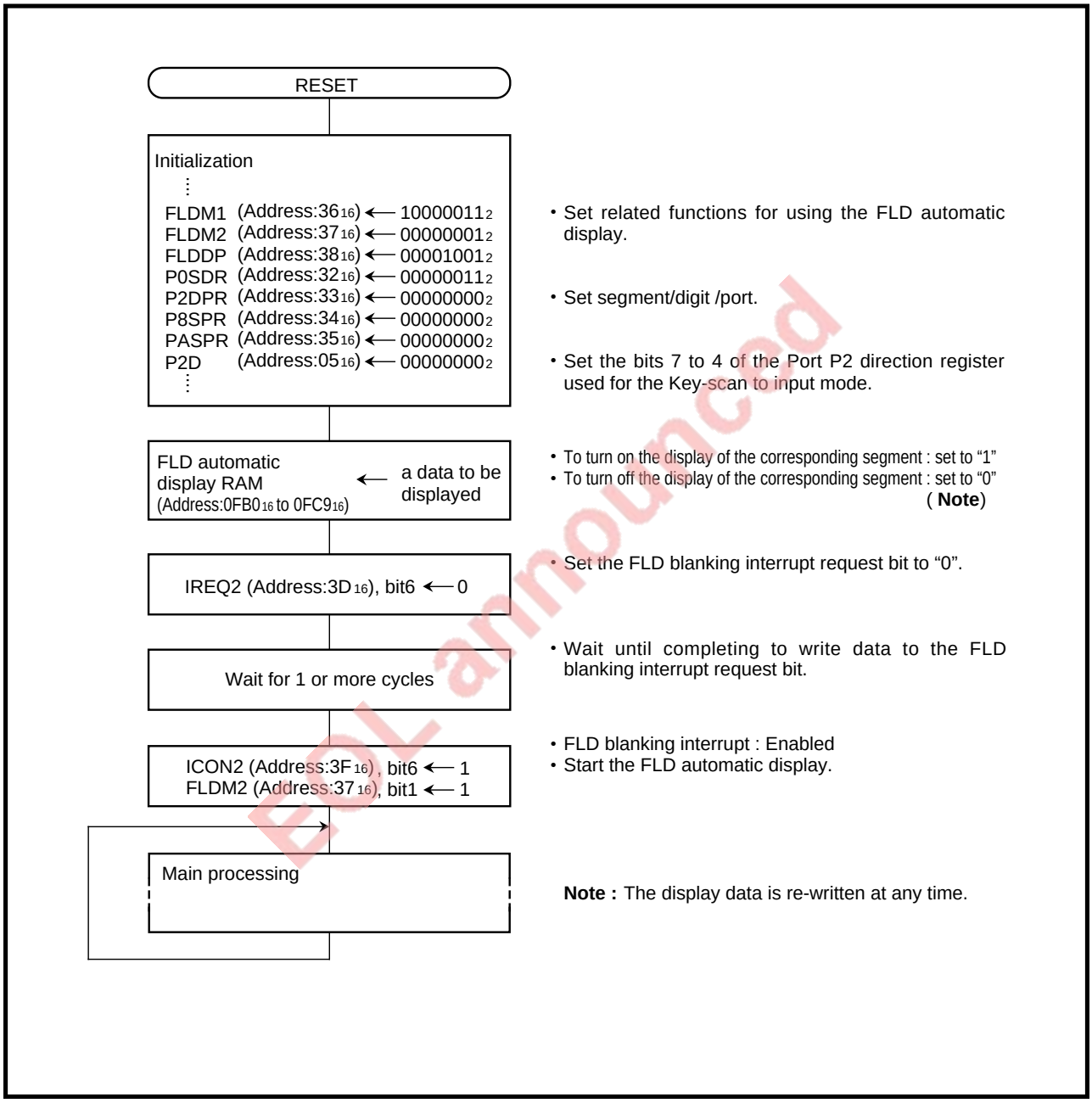


Fig. 2.5.17 Control procedure [FLD automatic display and Key-scan using segment pin]

EOL announced

Downloaded from Elcodis.com electronic components distributor

2. APPLICATION

Segment key-scan (FLD blanking interrupt) :

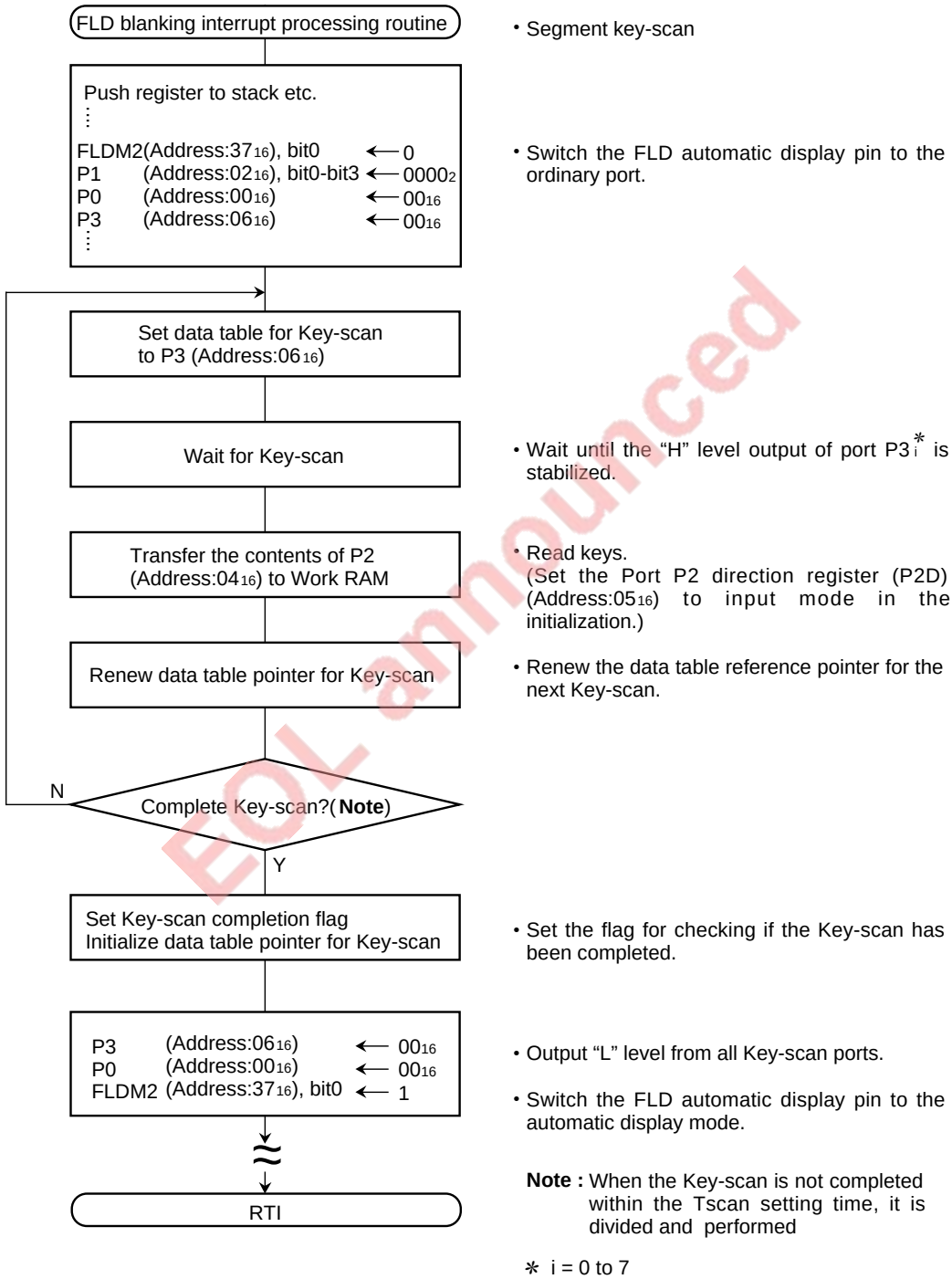


Fig. 2.5.18 Control procedure of Segment key-scan

EOL announced

Downloaded from Elcodis.com electronic components distributor

2. APPLICATION

(2) FLD automatic display and Key-scan using digit pin

Outline : The pannel with fluorescent display (FLD) is displayed by using FLD automatic display function. Then the key is read in with using digit output waveforms.

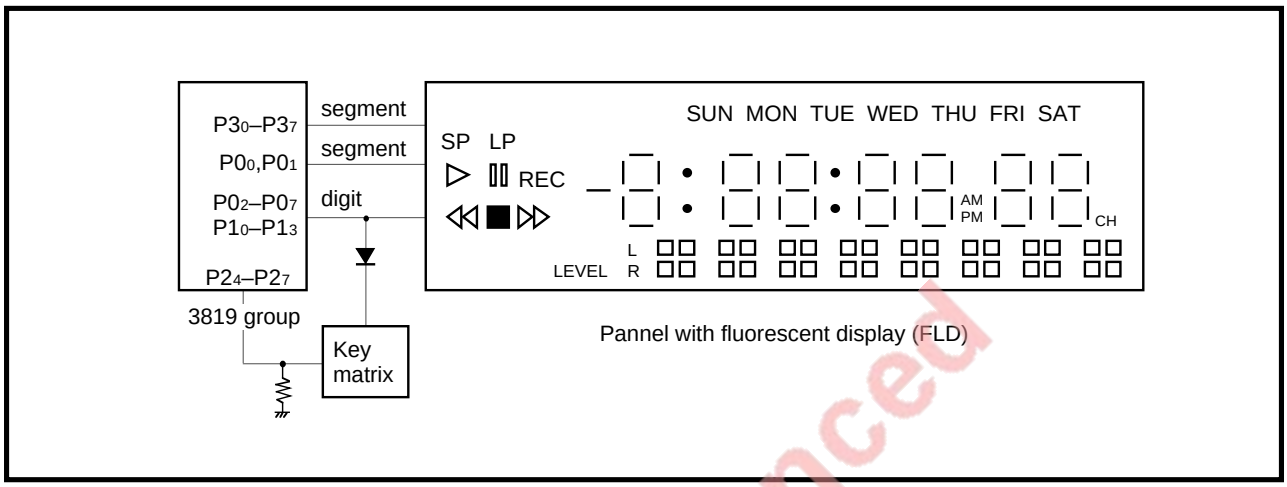


Fig. 2.5.19 Connection diagram [FLD automatic display and Key-scan using digit pin]

Specifications :
- The automatic display function is used.
- 10 digits and 10 segments are used.
- Toff = 15.27 µs, Tdisp = 244.39 µs, Tscan = 0 µs (at f(XIN) = 4.19 MHz)
- The FLD digit interrupt is used.
- The digit pin is used for the Key-scan.

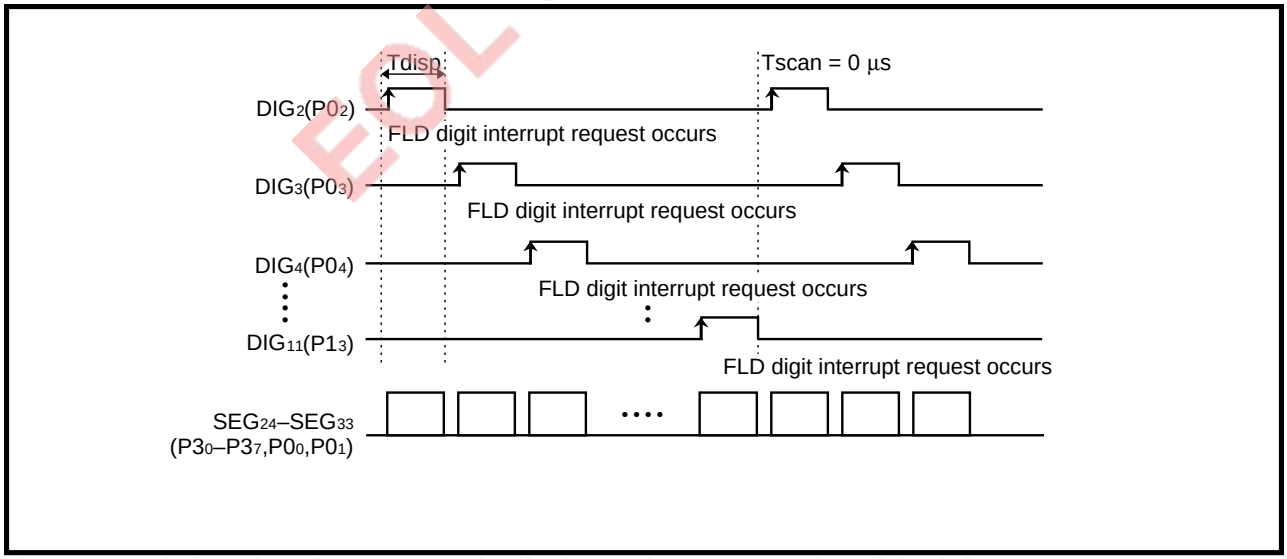
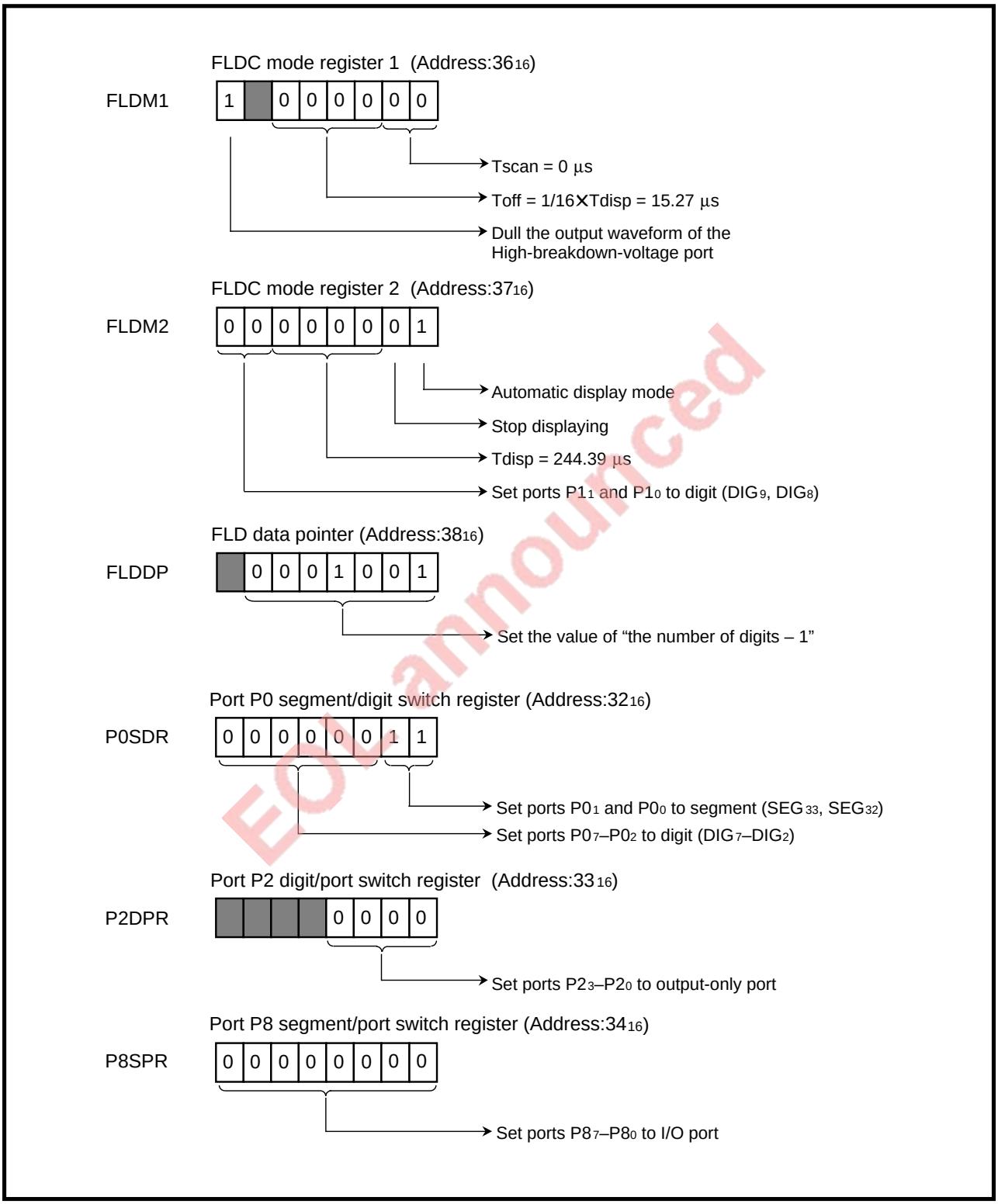


Fig. 2.5.20 Timing chart [FLD automatic display and Key-scan using digit pin]

EOL announced

Downloaded from Elcodis.com electronic components distributor

2. APPLICATION

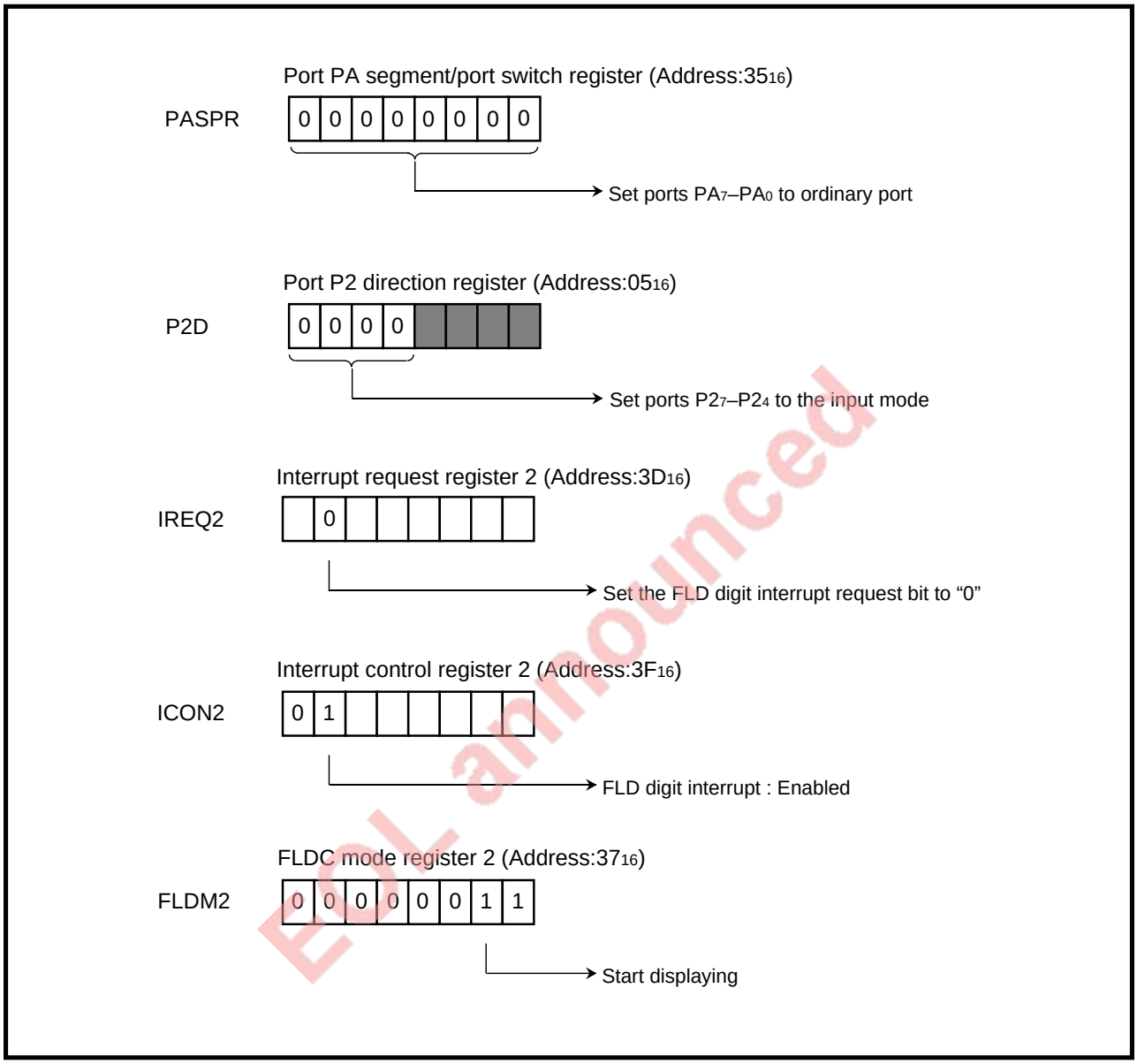


EOL announced

Fig. 2.5.21 Setting of related registers (1) [FLD automatic display and Key-scan using digit pin]

Downloaded from Elcodis.com electronic components distributor

2. APPLICATION



EOL announced

Fig. 2.5.22 Setting of related registers (2) [FLD automatic display and Key-scan using digit pin]

Downloaded from Elcodis.com electronic components distributor

2. APPLICATION

Setting of FLD automatic display RAM :

Table 2.5.3 FLD automatic display RAM map [FLD automatic display and Key-scan using digit pin]

Address	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
$0FB0_{16}$	SEG_{31}	SEG_{30}	SEG_{29}	SEG_{28}	SEG_{27}	SEG_{26}	SEG_{25}	SEG_{24}	→ DIG_{11} ($P1_3$)
$0FB1_{16}$	SEG_{31}	SEG_{30}	SEG_{29}	SEG_{28}	SEG_{27}	SEG_{26}	SEG_{25}	SEG_{24}	→ DIG_{10} ($P1_2$)
$0FB2_{16}$	SEG_{31}	SEG_{30}	SEG_{29}	SEG_{28}	SEG_{27}	SEG_{26}	SEG_{25}	SEG_{24}	→ DIG_9 ($P1_1$)
$0FB3_{16}$	SEG_{31}	SEG_{30}	SEG_{29}	SEG_{28}	SEG_{27}	SEG_{26}	SEG_{25}	SEG_{24}	→ DIG_8 ($P1_0$)
$0FB4_{16}$	SEG_{31}	SEG_{30}	SEG_{29}	SEG_{28}	SEG_{27}	SEG_{26}	SEG_{25}	SEG_{24}	→ DIG_7 ($P0_7$)
$0FB5_{16}$	SEG_{31}	SEG_{30}	SEG_{29}	SEG_{28}	SEG_{27}	SEG_{26}	SEG_{25}	SEG_{24}	→ DIG_6 ($P0_6$)
$0FB6_{16}$	SEG_{31}	SEG_{30}	SEG_{29}	SEG_{28}	SEG_{27}	SEG_{26}	SEG_{25}	SEG_{24}	→ DIG_5 ($P0_5$)
$0FB7_{16}$	SEG_{31}	SEG_{30}	SEG_{29}	SEG_{28}	SEG_{27}	SEG_{26}	SEG_{25}	SEG_{24}	→ DIG_4 ($P0_4$)
$0FB8_{16}$	SEG_{31}	SEG_{30}	SEG_{29}	SEG_{28}	SEG_{27}	SEG_{26}	SEG_{25}	SEG_{24}	→ DIG_3 ($P0_3$)
$0FB9_{16}$	SEG_{31}	SEG_{30}	SEG_{29}	SEG_{28}	SEG_{27}	SEG_{26}	SEG_{25}	SEG_{24}	→ DIG_2 ($P0_2$)
$0FBA_{16}$									
$0FBB_{16}$									
$0FBC_{16}$									
$0FBD_{16}$									
$0FBE_{16}$									
$0FBF_{16}$									
$0FC0_{16}$							SEG_{33}	SEG_{32}	→ DIG_{11} ($P1_3$)
$0FC1_{16}$							SEG_{33}	SEG_{32}	→ DIG_{10} ($P1_2$)
$0FC2_{16}$							SEG_{33}	SEG_{32}	→ DIG_9 ($P1_1$)
$0FC3_{16}$							SEG_{33}	SEG_{32}	→ DIG_8 ($P1_0$)
$0FC4_{16}$							SEG_{33}	SEG_{32}	→ DIG_7 ($P0_7$)
$0FC5_{16}$							SEG_{33}	SEG_{32}	→ DIG_6 ($P0_6$)
$0FC6_{16}$							SEG_{33}	SEG_{32}	→ DIG_5 ($P0_5$)
$0FC7_{16}$							SEG_{33}	SEG_{32}	→ DIG_4 ($P0_4$)
$0FC8_{16}$							SEG_{33}	SEG_{32}	→ DIG_3 ($P0_3$)
$0FC9_{16}$							SEG_{33}	SEG_{32}	→ DIG_2 ($P0_2$)

: Area which is used to set a display value

: Area which is available as ordinary RAM

EOL announced

Downloaded from Elcodis.com electronic components distributor

2. APPLICATION

FLD digit allocation :

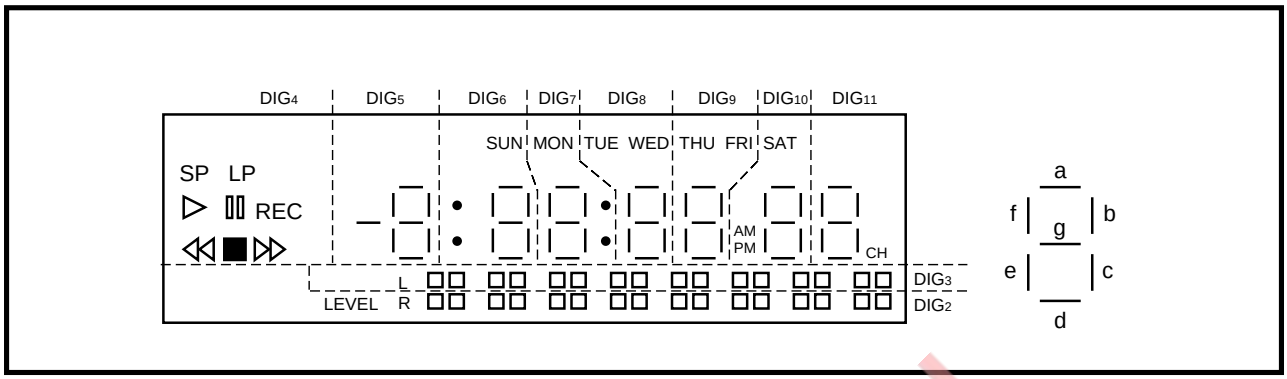


Fig. 2.5.23 Example of FLD digit allocation [FLD automatic display and Key-scan using digit pin]

Table 2.5.4 FLD automatic display RAM map example [FLD automatic display and Key-scan using digit pin]

Address	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
0FB0$_{16}$	CH	g	f	e	d	c	b	a	→ DIG$_{11}$ (P1$_3$)
0FB1$_{16}$	SAT	g	f	e	d	c	b	a	→ DIG$_{10}$ (P1$_2$)
0FB2$_{16}$	FRI	g	f	e	d	c	b	a	→ DIG$_9$ (P1$_1$)
0FB3$_{16}$	WED	g	f	e	d	c	b	a	→ DIG$_8$ (P1$_0$)
0FB4$_{16}$	MON	g	f	e	d	c	b	a	→ DIG$_7$ (P0$_7$)
0FB5$_{16}$	SUN	g	f	e	d	c	b	a	→ DIG$_6$ (P0$_6$)
0FB6$_{16}$	—	g	f	e	d	c	b	a	→ DIG$_5$ (P0$_5$)
0FB7$_{16}$	■	◁◁	▷▷	▯▯	▷	REC	SP	LP	→ DIG$_4$ (P0$_4$)
0FB8$_{16}$	□□	□□	□□	□□	□□	□□	□□	□□	→ DIG$_3$ (P0$_3$)
0FB9$_{16}$	□□	□□	□□	□□	□□	□□	□□	□□	→ DIG$_2$ (P0$_2$)
0FBA$_{16}$									
0FBB$_{16}$									
0FBC$_{16}$									
0FBD$_{16}$									
0FBE$_{16}$									
0FBF$_{16}$									
0FC0$_{16}$									→ DIG$_{11}$ (P1$_3$)
0FC1$_{16}$							PM	AM	→ DIG$_{10}$ (P1$_2$)
0FC2$_{16}$								THU	→ DIG$_9$ (P1$_1$)
0FC3$_{16}$								TUE	→ DIG$_8$ (P1$_0$)
0FC4$_{16}$								:	→ DIG$_7$ (P0$_7$)
0FC5$_{16}$								:	→ DIG$_6$ (P0$_6$)
0FC6$_{16}$									→ DIG$_5$ (P0$_5$)
0FC7$_{16}$									→ DIG$_4$ (P0$_4$)
0FC8$_{16}$							L		→ DIG$_3$ (P0$_3$)
0FC9$_{16}$							R	LEVEL	→ DIG$_2$ (P0$_2$)

: Unused

EOL announced

Downloaded from Elcodis.com electronic components distributor

2. APPLICATION

Control procedure :
Figure 2.5.24 shows a control procedure.

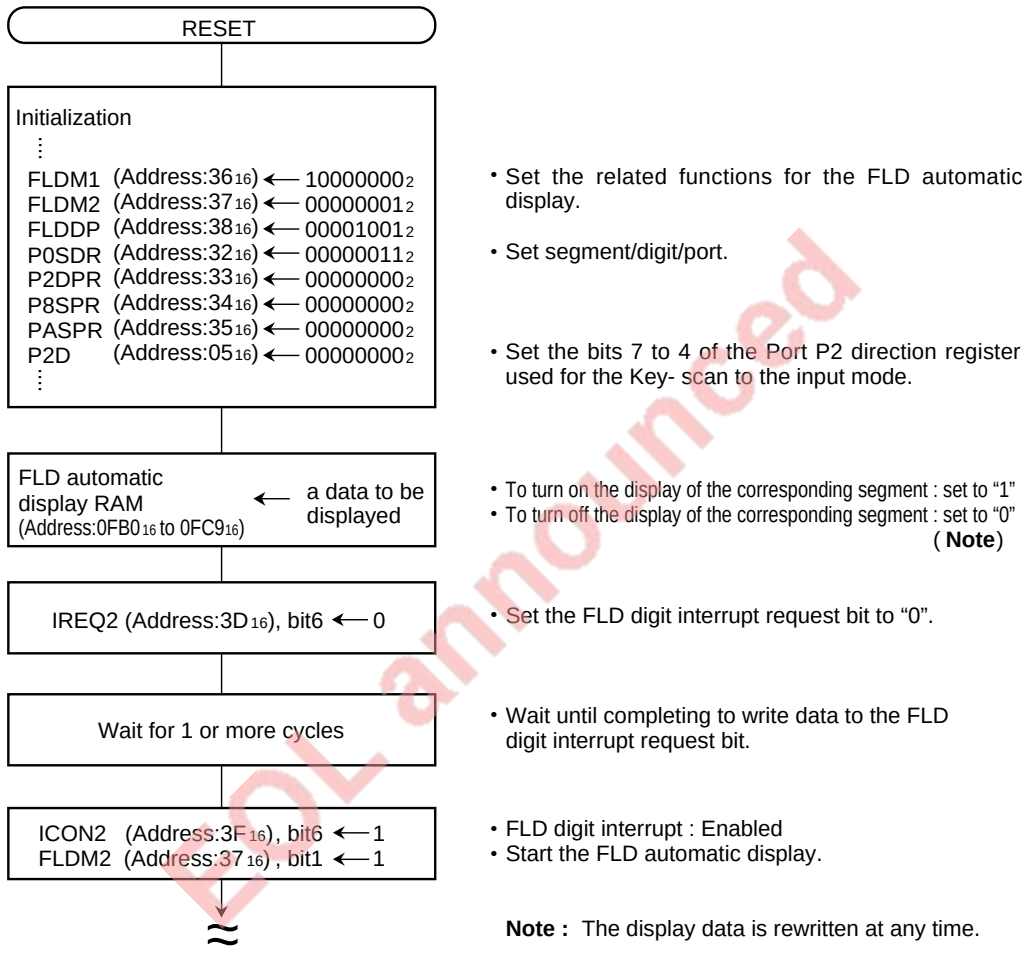
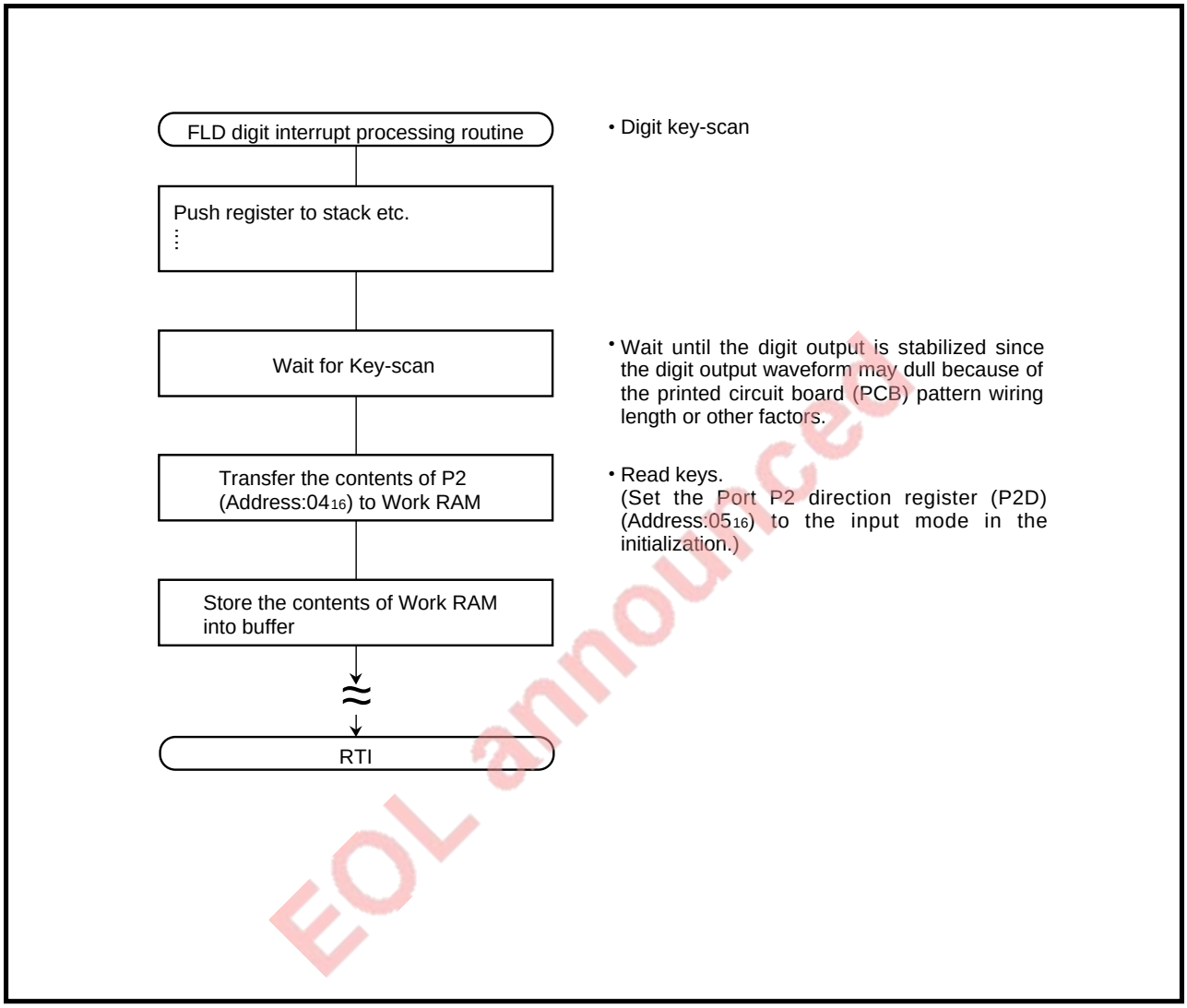


Fig. 2.5.24 Control procedure [FLD automatic display and Key-scan using digit pin]

EOL announced

Downloaded from Elcodis.com electronic components distributor

Digit key-scan (FLD digit interrupt) :



EOL announced

Fig. 2.5.25 Control procedure of Digit key-scan

Downloaded from Elcodis.com electronic components distributor

(3) FLD display by software (example of without using FLD controller)

Outline : The FLD display and the key read-in are performed by using timer interrupts.

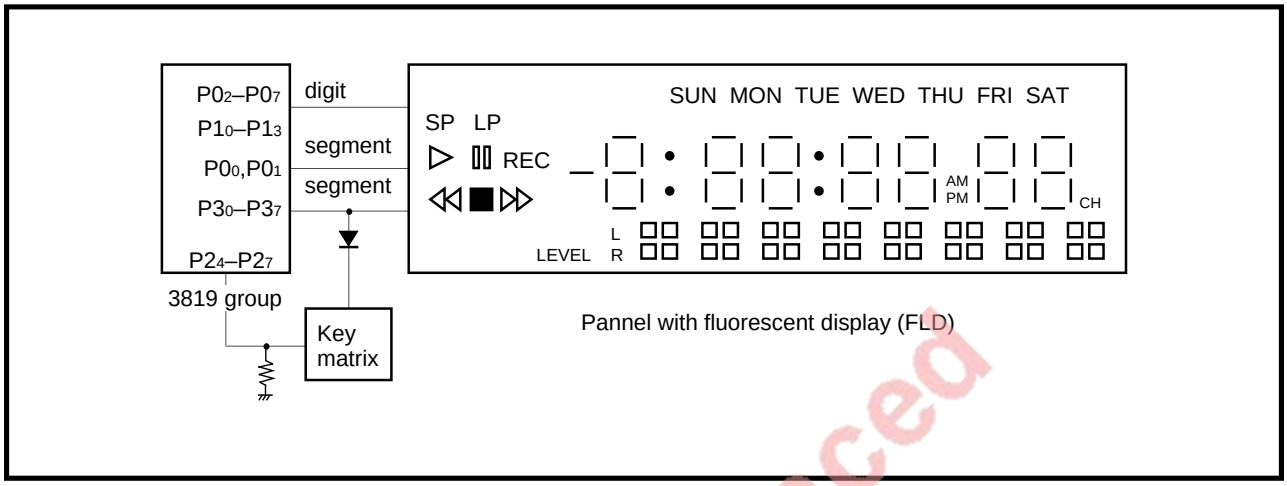


Fig. 2.5.26 Connection diagram [FLD display by software]

Specifications :
- The display is controlled by software.
- 10 digits and 10 segments are used.
- The Timer 1 interrupts are used.
- The segment pin is used for Key-scan.

Fig. 2.5.27 shows a timing chart of FLD display by software, and Fig. 2.5.28 shows an enlarged view of Key-scan of ports P30 to P37.

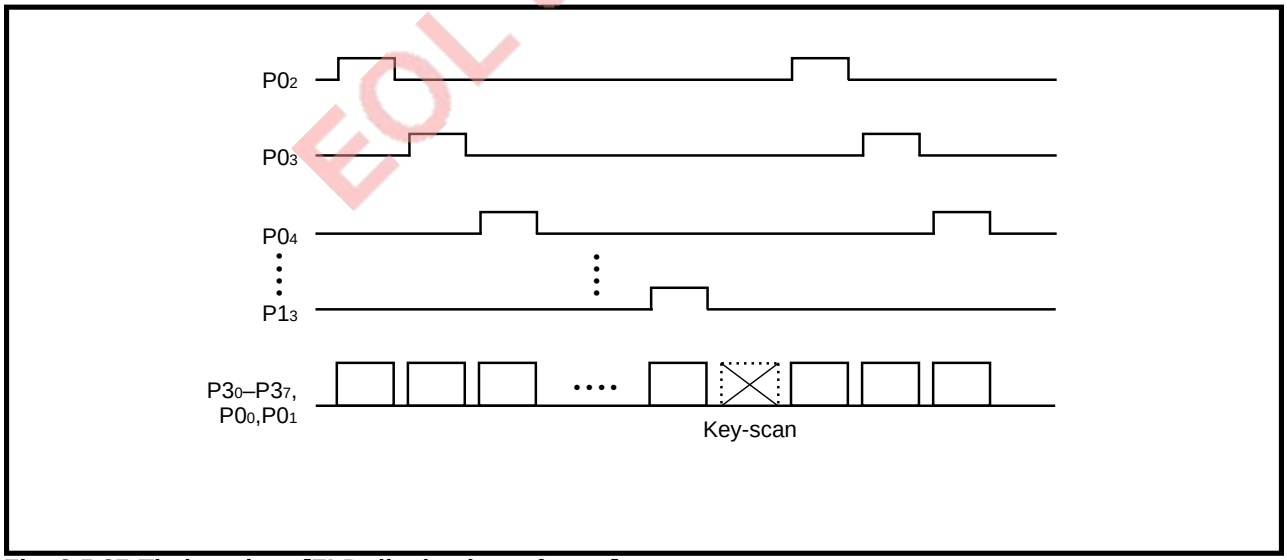


Fig. 2.5.27 Timing chart [FLD display by software]

EOL announced

Downloaded from Elcodis.com electronic components distributor

2. APPLICATION

The waveform shown below is created by software, and the Key-scan is performed.

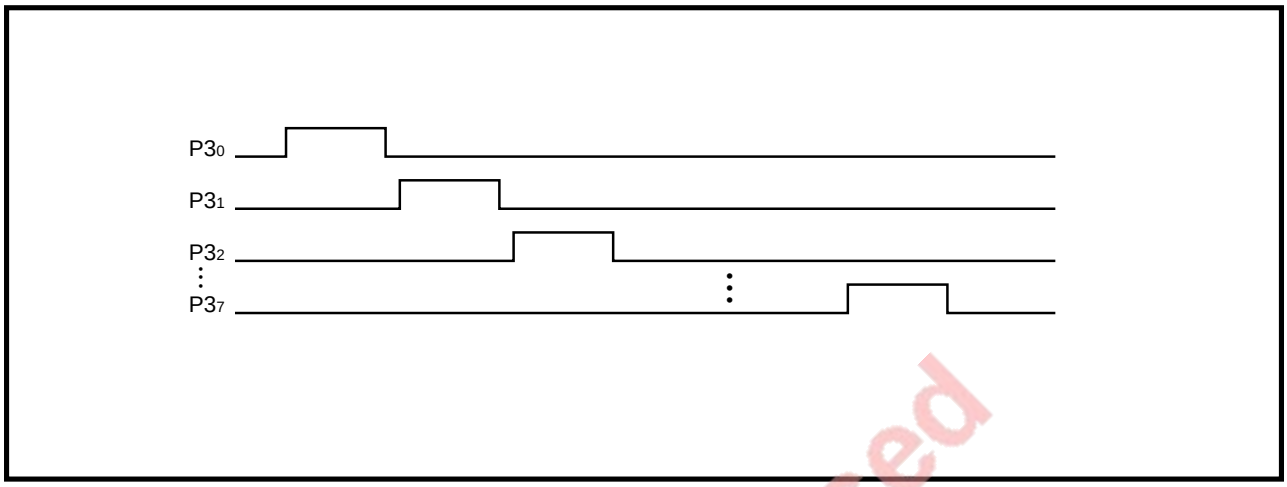


Fig. 2.5.28 Enlarged view of Key-scan of ports P30 to P37

Figure 2.5.29 shows a setting of related registers.

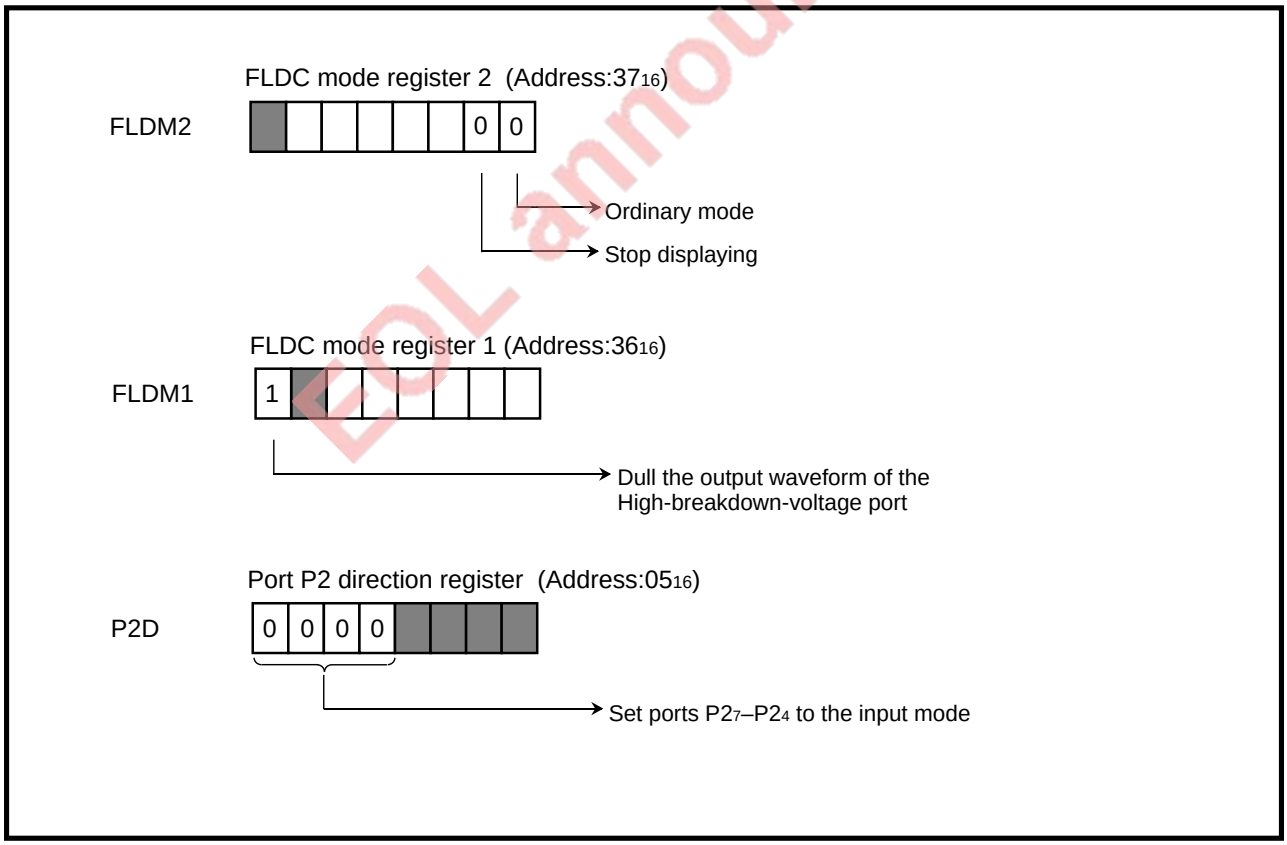


Fig. 2.5.29 Setting of related registers [FLD display by software]

EOL announced

Downloaded from Elcodis.com electronic components distributor

2. APPLICATION

FLD digit allocation :

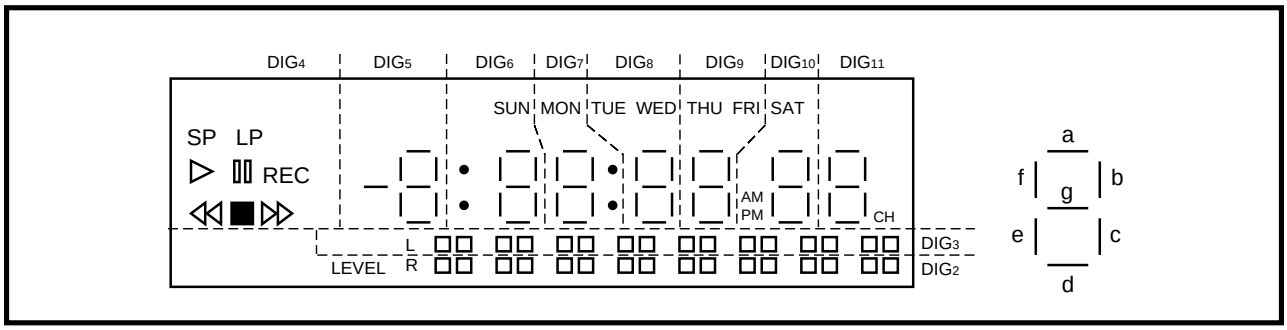


Fig. 2.5.30 Example of FLD digit allocation [FLD display by software]

Table 2.5.5 FLD automatic display RAM map example [FLD display by software]
(Automatic display is not performed because of not using FLD controller)

Address	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
0FB0$_{16}$	CH	g	f	e	d	c	b	a	→ DIG$_{11}$ (P1$_3$)
0FB1$_{16}$	SAT	g	f	e	d	c	b	a	→ DIG$_{10}$ (P1$_2$)
0FB2$_{16}$	FRI	g	f	e	d	c	b	a	→ DIG$_9$ (P1$_1$)
0FB3$_{16}$	WED	g	f	e	d	c	b	a	→ DIG$_8$ (P1$_0$)
0FB4$_{16}$	MON	g	f	e	d	c	b	a	→ DIG$_7$ (P0$_7$)
0FB5$_{16}$	SUN	g	f	e	d	c	b	a	→ DIG$_6$ (P0$_6$)
0FB6$_{16}$	—	g	f	e	d	c	b	a	→ DIG$_5$ (P0$_5$)
0FB7$_{16}$	■	◁◁	▷▷	▯▯	▷	REC	SP	LP	→ DIG$_4$ (P0$_4$)
0FB8$_{16}$	□□	□□	□□	□□	□□	□□	□□	□□	→ DIG$_3$ (P0$_3$)
0FB9$_{16}$	□□	□□	□□	□□	□□	□□	□□	□□	→ DIG$_2$ (P0$_2$)
0FBA$_{16}$									
0FBB$_{16}$									
0FBC$_{16}$									
0FBD$_{16}$									
0FBE$_{16}$									
0FBF$_{16}$									
0FC0$_{16}$									→ DIG$_{11}$ (P1$_3$)
0FC1$_{16}$							PM	AM	→ DIG$_{10}$ (P1$_2$)
0FC2$_{16}$								THU	→ DIG$_9$ (P1$_1$)
0FC3$_{16}$								TUE	→ DIG$_8$ (P1$_0$)
0FC4$_{16}$								⋮	→ DIG$_7$ (P0$_7$)
0FC5$_{16}$								⋮	→ DIG$_6$ (P0$_6$)
0FC6$_{16}$									→ DIG$_5$ (P0$_5$)
0FC7$_{16}$									→ DIG$_4$ (P0$_4$)
0FC8$_{16}$							L		→ DIG$_3$ (P0$_3$)
0FC9$_{16}$							R	LEVEL	→ DIG$_2$ (P0$_2$)

: Unused

EOL announced

Downloaded from Elcodis.com electronic components distributor

2. APPLICATION

Control procedure :

Figure 2.5.31 shows a control procedure.

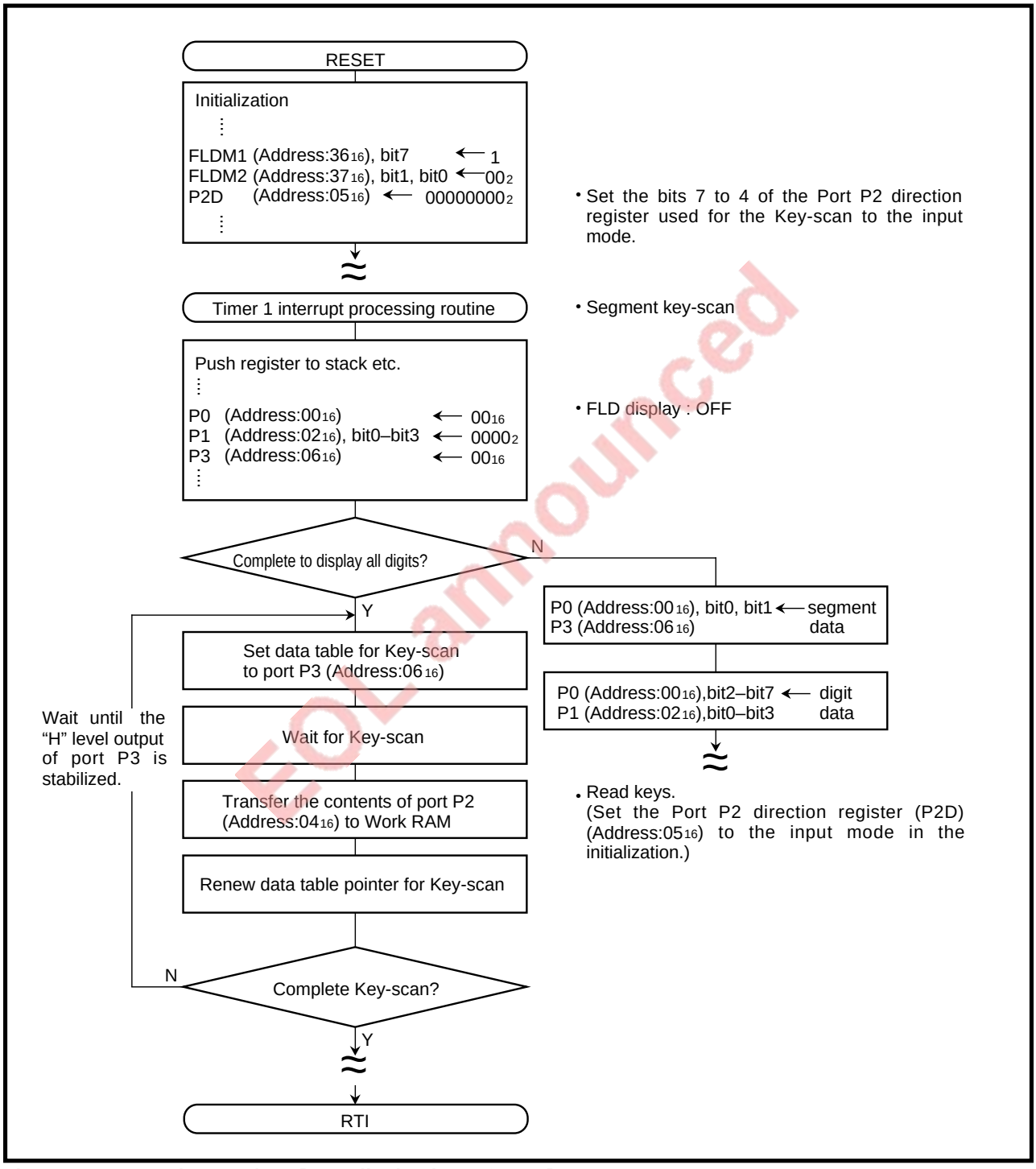


Fig. 2.5.31 Control procedure [FLD display by software]

EOL announced

Downloaded from Elcodis.com electronic components distributor

(4) 5 × 7 dot display

Outline : The 5 × 7 dot display is performed by using the FLD automatic display function.

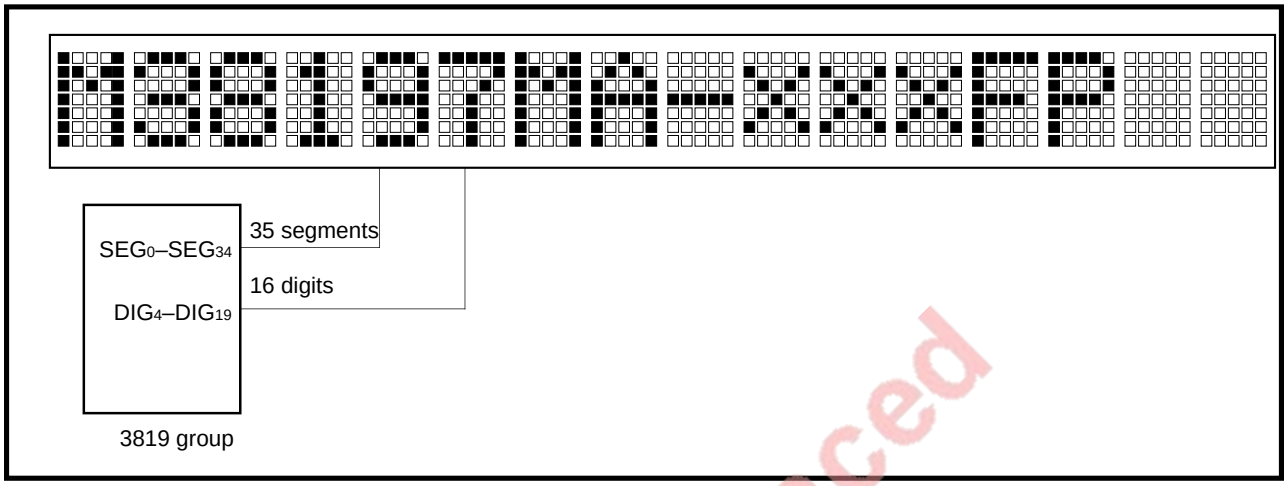


Fig. 2.5.32 Connection diagram [5 × 7 dot display]

Specifications :
- The automatic display function is used.
- 16 digits and 35 segments are used.
- Toff = 288 µs, Tdisp = 512 µs, Tscan = 512 µs (at f(XIN) = 8 MHz)

Figure 2.5.33 shows a timing chart of FLD automatic display.

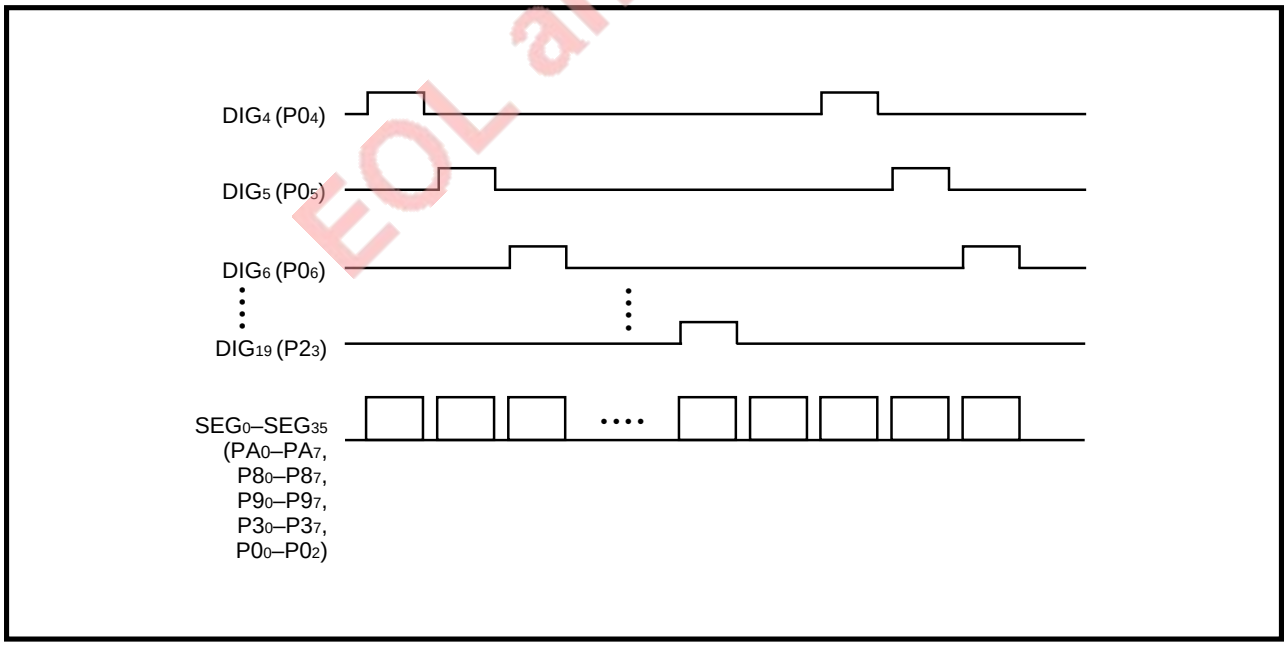


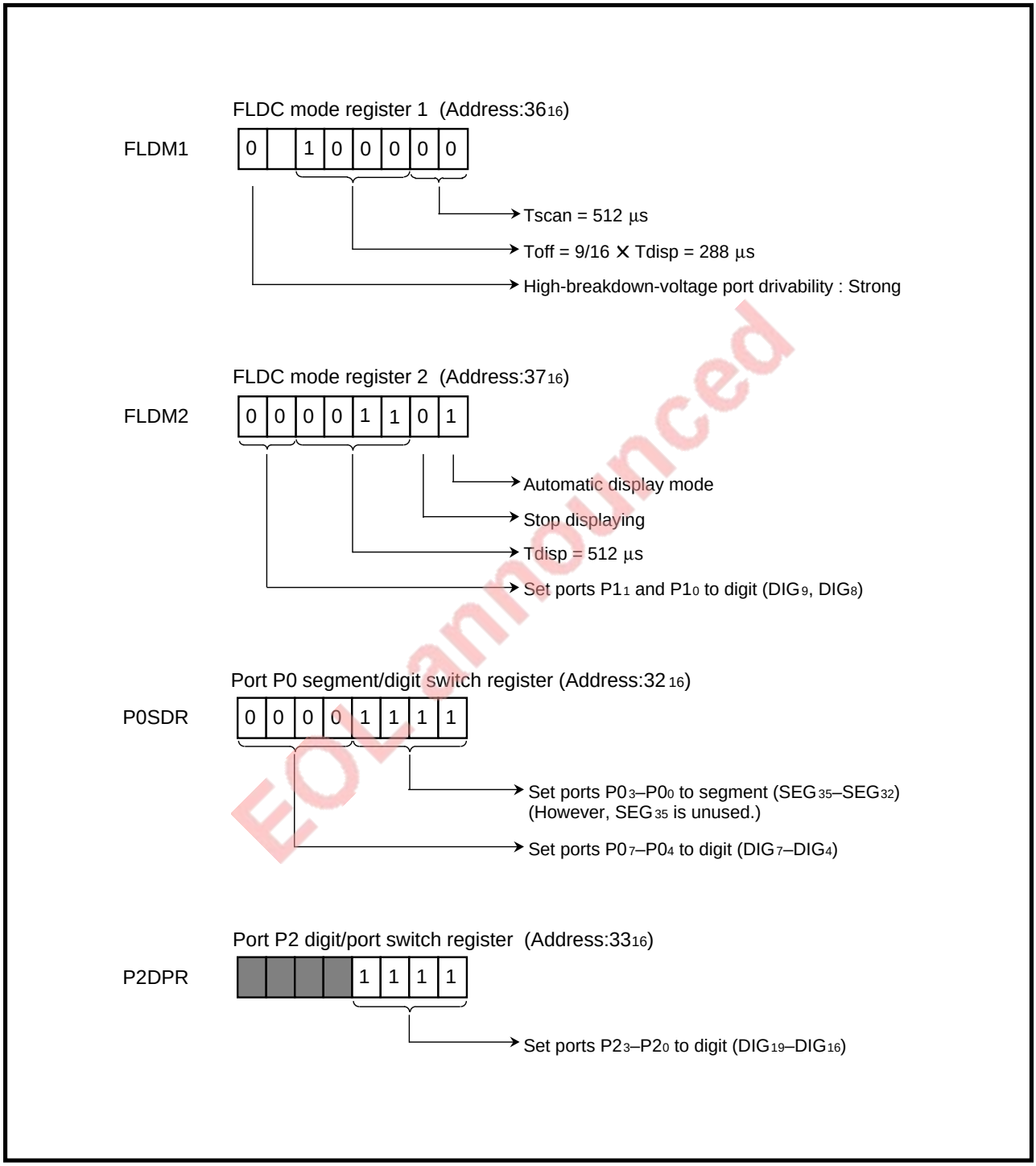
Fig. 2.5.33 Timing chart [5 × 7 dot display]

EOL announced

Downloaded from Elcodis.com electronic components distributor

2. APPLICATION

Figures 2.5.34 and 2.5.35 show a setting of related registers.

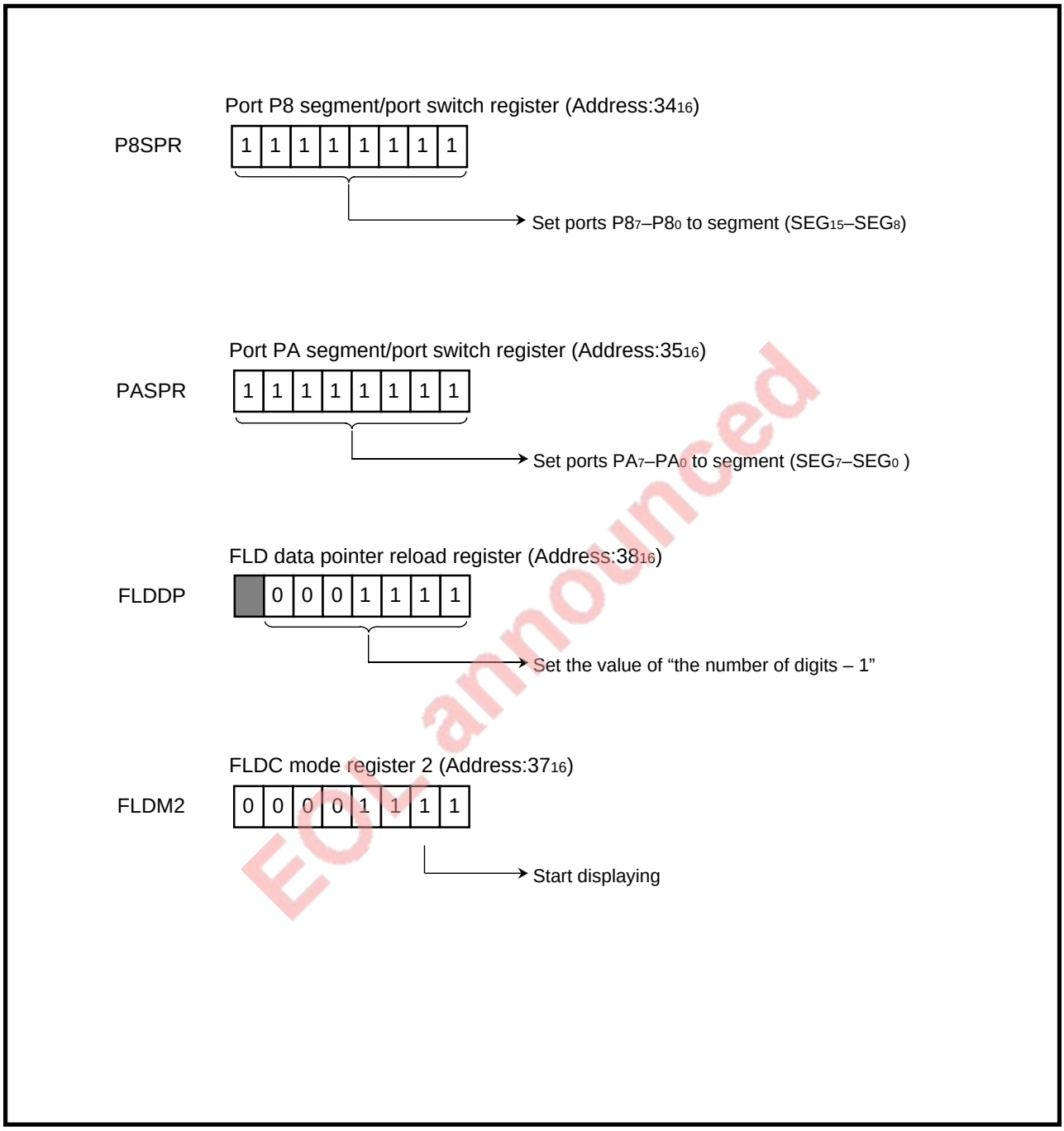


EOL announced

Fig. 2.5.34 Setting of related registers (1) [5 × 7 dot display]

Downloaded from Elcodis.com electronic components distributor

2. APPLICATION



EOL announced

Fig. 2.5.35 Setting of related registers (2) [5 × 7 dot display]

Downloaded from Elcodis.com electronic components distributor

2. APPLICATION

Setting of FLD automatic display RAM :

Table 2.5.6 FLD automatic display RAM map [5 × 7 dot display]

Address	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
$0F80_{16}$	SEG7	SEG6	SEG5	SEG4	SEG3	SEG2	SEG1	SEG0	→ DIG19 (P23)
$0F81_{16}$									→ DIG18 (P22)
$0F82_{16}$									→ DIG17 (P21)
$0F83_{16}$									→ DIG16 (P20)
$0F84_{16}$									→ DIG15 (P17)
$0F85_{16}$									→ DIG14 (P16)
$0F86_{16}$									→ DIG13 (P15)
$0F87_{16}$									→ DIG12 (P14)
$0F88_{16}$									→ DIG11 (P13)
$0F89_{16}$									→ DIG10 (P12)
$0F8A_{16}$									→ DIG9 (P11)
$0F8B_{16}$									→ DIG8 (P10)
$0F8C_{16}$									→ DIG7 (P07)
$0F8D_{16}$									→ DIG6 (P06)
$0F8E_{16}$									→ DIG5 (P05)
$0F8F_{16}$									→ DIG4 (P04)
$0F90_{16}$	SEG15	SEG14	SEG13	SEG12	SEG11	SEG10	SEG9	SEG8	→ DIG19 (P23)
$0F91_{16}$									→ DIG18 (P22)
$0F92_{16}$									→ DIG17 (P21)
$0F93_{16}$									→ DIG16 (P20)
$0F94_{16}$									→ DIG15 (P17)
$0F95_{16}$									→ DIG14 (P16)
$0F96_{16}$									→ DIG13 (P15)
$0F97_{16}$									→ DIG12 (P14)
$0F98_{16}$									→ DIG11 (P13)
$0F99_{16}$									→ DIG10 (P12)
$0F9A_{16}$									→ DIG9 (P11)
$0F9B_{16}$									→ DIG8 (P10)
$0F9C_{16}$									→ DIG7 (P07)
$0F9D_{16}$									→ DIG6 (P06)
$0F9E_{16}$									→ DIG5 (P05)
$0F9F_{16}$									→ DIG4 (P04)
$0FA0_{16}$	SEG23	SEG22	SEG21	SEG20	SEG19	SEG18	SEG17	SEG16	→ DIG19 (P23)
$0FA1_{16}$									→ DIG18 (P22)
$0FA2_{16}$									→ DIG17 (P21)
$0FA3_{16}$									→ DIG16 (P20)
$0FA4_{16}$									→ DIG15 (P17)
$0FA5_{16}$									→ DIG14 (P16)
$0FA6_{16}$									→ DIG13 (P15)
$0FA7_{16}$									→ DIG12 (P14)
$0FA8_{16}$									→ DIG11 (P13)
$0FA9_{16}$									→ DIG10 (P12)
$0FAA_{16}$									→ DIG9 (P11)
$0FAB_{16}$									→ DIG8 (P10)
$0FAC_{16}$									→ DIG7 (P07)
$0FAD_{16}$									→ DIG6 (P06)
$0FAE_{16}$									→ DIG5 (P05)
$0FAF_{16}$									→ DIG4 (P04)
$0FB0_{16}$	SEG31	SEG30	SEG29	SEG28	SEG27	SEG26	SEG25	SEG24	→ DIG19 (P23)
$0FB1_{16}$									→ DIG18 (P22)
$0FB2_{16}$									→ DIG17 (P21)
$0FB3_{16}$									→ DIG16 (P20)
$0FB4_{16}$									→ DIG15 (P17)
$0FB5_{16}$									→ DIG14 (P16)
$0FB6_{16}$									→ DIG13 (P15)
$0FB7_{16}$									→ DIG12 (P14)
$0FB8_{16}$									→ DIG11 (P13)
$0FB9_{16}$									→ DIG10 (P12)
$0FBA_{16}$									→ DIG9 (P11)
$0FBB_{16}$									→ DIG8 (P10)
$0FBC_{16}$									→ DIG7 (P07)
$0FBD_{16}$									→ DIG6 (P06)
$0FBE_{16}$									→ DIG5 (P05)
$0FBF_{16}$									→ DIG4 (P04)
$0FC0_{16}$						SEG34	SEG33	SEG32	→ DIG19 (P23)
$0FC1_{16}$									→ DIG18 (P22)
$0FC2_{16}$									→ DIG17 (P21)
$0FC3_{16}$									→ DIG16 (P20)
$0FC4_{16}$									→ DIG15 (P17)
$0FC5_{16}$									→ DIG14 (P16)
$0FC6_{16}$									→ DIG13 (P15)
$0FC7_{16}$									→ DIG12 (P14)
$0FC8_{16}$									→ DIG11 (P13)
$0FC9_{16}$									→ DIG10 (P12)
$0FCA_{16}$									→ DIG9 (P11)
$0FCB_{16}$									→ DIG8 (P10)
$0FCC_{16}$									→ DIG7 (P07)
$0FCD_{16}$									→ DIG6 (P06)
$0FCE_{16}$									→ DIG5 (P05)
$0FCF_{16}$									→ DIG4 (P04)

: Area which is used to set a display value

: Area which is available as ordinary RAM

EOL announced

Downloaded from Elcodis.com electronic components distributor

2. APPLICATION

FLD digit allocation :

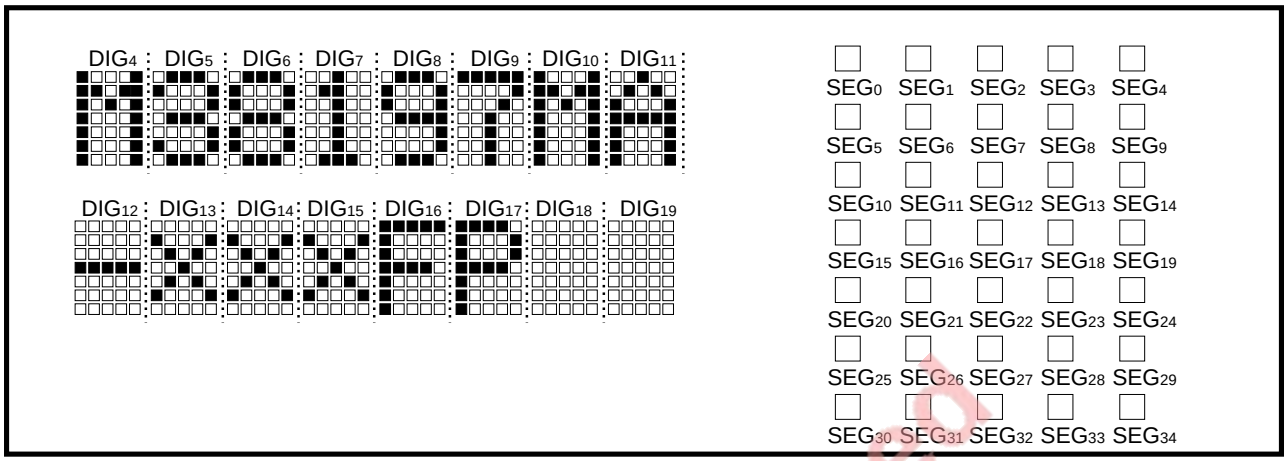
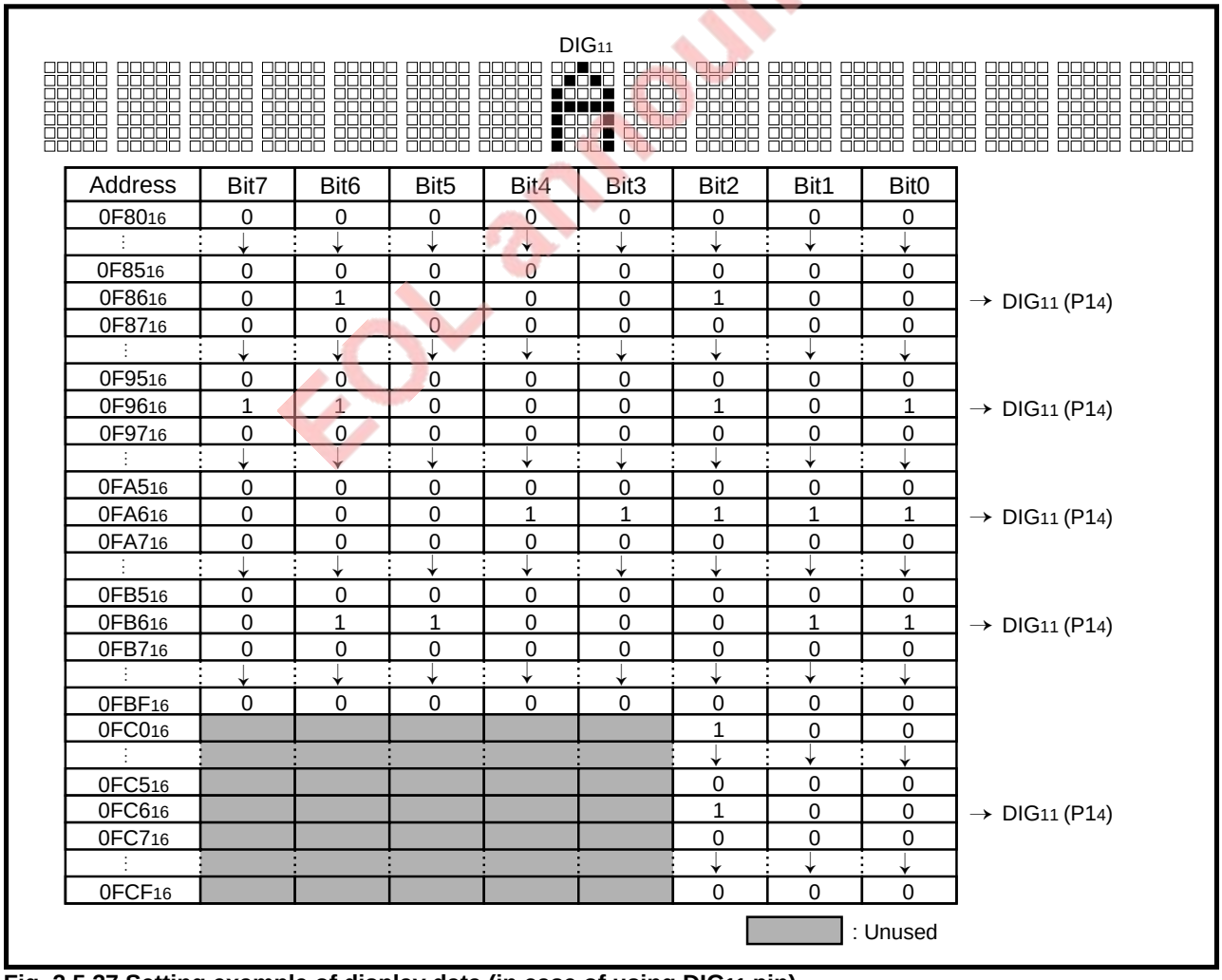


Fig. 2.5.36 Example of FLD digit allocation and segment arrangment

Setting example of display data (in case of using DIG11) :



Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	
0F80$_{16}$	0	0	0	0	0	0	0	0	
⋮	↓	↓	↓	↓	↓	↓	↓	↓	
0F85$_{16}$	0	0	0	0	0	0	0	0	
0F86$_{16}$	0	1	0	0	0	1	0	0	→ DIG11 (P14)
0F87$_{16}$	0	0	0	0	0	0	0	0	
⋮	↓	↓	↓	↓	↓	↓	↓	↓	
0F95$_{16}$	0	0	0	0	0	0	0	0	
0F96$_{16}$	1	1	0	0	0	1	0	1	→ DIG11 (P14)
0F97$_{16}$	0	0	0	0	0	0	0	0	
⋮	↓	↓	↓	↓	↓	↓	↓	↓	
0FA5$_{16}$	0	0	0	0	0	0	0	0	
0FA6$_{16}$	0	0	0	1	1	1	1	1	→ DIG11 (P14)
0FA7$_{16}$	0	0	0	0	0	0	0	0	
⋮	↓	↓	↓	↓	↓	↓	↓	↓	
0FB5$_{16}$	0	0	0	0	0	0	0	0	
0FB6$_{16}$	0	1	1	0	0	0	1	1	→ DIG11 (P14)
0FB7$_{16}$	0	0	0	0	0	0	0	0	
⋮	↓	↓	↓	↓	↓	↓	↓	↓	
0FBF$_{16}$	0	0	0	0	0	0	0	0	
0FC0$_{16}$						1	0	0	
⋮						↓	↓	↓	
0FC5$_{16}$						0	0	0	
0FC6$_{16}$						1	0	0	→ DIG11 (P14)
0FC7$_{16}$						0	0	0	
⋮						↓	↓	↓	
0FCF$_{16}$						0	0	0	

: Unused

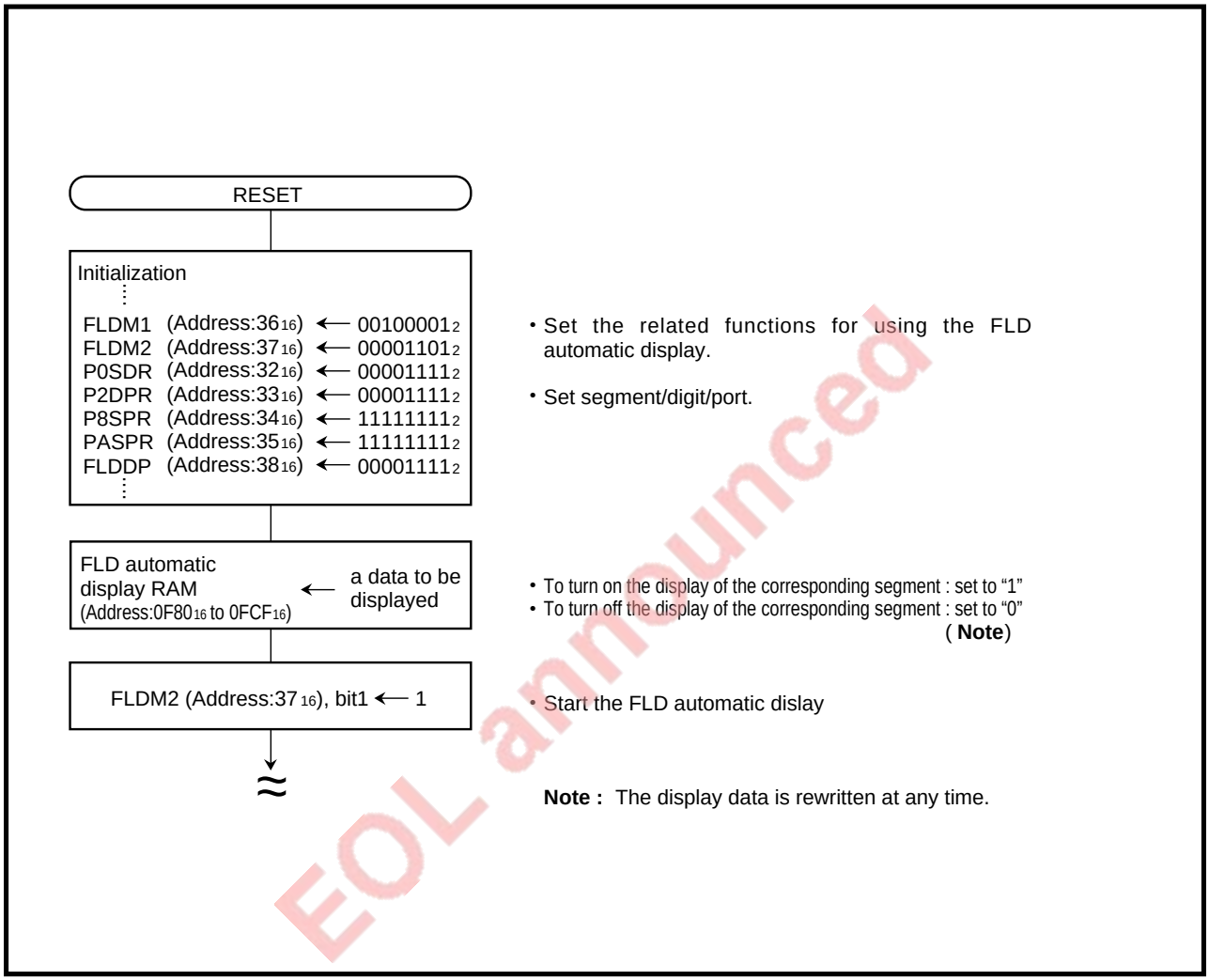
EOL announced

Fig. 2.5.37 Setting example of display data (in case of using DIG11 pin)

Downloaded from Elcodis.com electronic components distributor

2. APPLICATION

Control procedure :
Figure 2.5.38 shows a control procedure.



EOL announced

Fig. 2.5.38 Control procedure [5 × 7 dot display]

Downloaded from Elcodis.com electronic components distributor

2.6 Interrupt interval determination function

2.6.1 Related registers

Interrupt interval determination register

b7 b6 b5 b4 b3 b2 b1 b0

Interrupt interval determination register (IID) [Address:30$_{16}$]

B	Function	At reset	R	W
0	This register stores the values obtaind by counting the following interval with a counter sampling clock. • Falling edge interval • Rising edge interval • Both-sided edge interval (selected by the interrupt edge selection register) This register is read-only.	?	○	×
1		?	○	×
2		?	○	×
3		?	○	×
4		?	○	×
5		?	○	×
6		?	○	×
7		?	○	×

Note : When the noise filter sampling clock selection bits (bits 2 and 3) of the Interrupt interval determination control register (IIDCON) (Address: 31 $_{16}$) is set to "00" (when no noise filter is used), the both-sided edge detection function is not available.

Fig. 2.6.1 Structure of Interrupt interval determination register

Interrupt interval determination control register

b7 b6 b5 b4 b3 b2 b1 b0

Interrupt interval determination control register (IIDCON) [Address:31$_{16}$]

B	Name	Function	At reset	R	W
0	Interrupt interval determination circuit operating selection bit	0 : Stopped 1 : Operating	0	○	○
1	Counter sampling clock selection bit	0 : f(X$_{IN}$)/256 1 : f(X$_{IN}$)/512	0	○	○
2	Noise filter sampling clock selection bits (INT$_2$)	00 : Filter stop 01 : f(X$_{IN}$)/64 10 : f(X$_{IN}$)/128 11 : f(X$_{IN}$)/256	0	○	○
3			0	○	○
4	One-sided/both-sided edge detection selection bit	0 : One-sided edge detection 1 : Both-sided edge detection (Note)	0	○	○
5	Nothing is allocated for these bits. These are write disabled bits. When these bits are read out, the values are "0."		0	○	×
6			0	○	×
7			0	○	×

Note : When the noise filter sampling clock selection bits (bits 2 and 3) of the Interrupt interval determination control register (IIDCON) (Address: 31 $_{16}$) is set to "00" (when no noise filter is used), the both-sided edge detection function is not available.

Fig. 2.6.2 Structure of Interrupt interval determination control register

EOL announced

Downloaded from Elcodis.com electronic components distributor

Interrupt edge selection register

b7 b6 b5 b4 b3 b2 b1 b0

Interrupt edge selecton reigster (INTEDGE) [Address:3A16]

b	Name	Function	At reset	R	W
0	INT_0 interrupt edge selection bit	0 : Falling edge active 1 : Rising edge active	0	○	○
1	INT_1/ZCR interrupt edge selection bit	0 : Falling edge active 1 : Rising edge active	0	○	○
2	INT_2 interrupt edge selection bit	0 : Falling edge active 1 : Rising edge active	0	○	○
3	INT_3 interrupt edge selection bit	0 : Falling edge active 1 : Rising edge active	0	○	○
4	INT_4 interrupt edge selection bit	0 : Falling edge active 1 : Rising edge active	0	○	○
5	INT_4/A-D conversion interrupt switch bit	0 : INT_4 interrupt 1 : A-D conversion interrupt	0	○	○
6	$CNTR_0$ pin active edge switch bit	0 : Falling edge active 1 : Rising edge active	0	○	○
7	$CNTR_1$ pin active edge switch bit	0 : Falling edge active 1 : Rising edge active	0	○	○

Fig. 2.6.3 Structure of Interrupt edge selection register

Interrupt request register 1

b7 b6 b5 b4 b3 b2 b1 b0

Interrupt request reigster 1 (IREQ1) [Address:3C16]

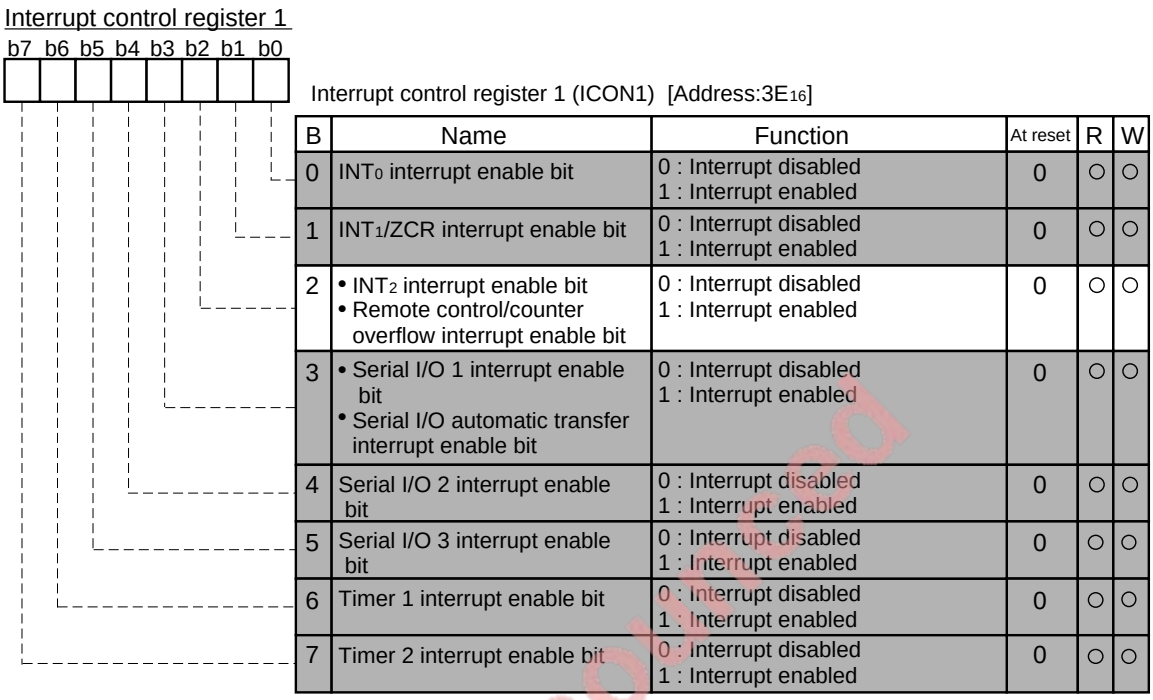
B	Name	Function	At reset	R	W
0	INT_0 interrupt request bit	0 : No interrupt request 1 : Interrupt request	0	○	*
1	INT_1/ZCR interrupt request bit	0 : No interrupt request 1 : Interrupt request	0	○	*
2	• INT_2 interrupt request bit • Remote control/counter overflow interrupt request bit	0 : No interrupt request 1 : Interrupt request	0	○	*
3	• Serial I/O 1 interrupt request bit • Serial I/O automatic transfer interrupt request bit	0 : No interrupt request 1 : Interrupt request	0	○	*
4	Serial I/O 2 interrupt request bit	0 : No interrupt request 1 : Interrupt request	0	○	*
5	Serial I/O 3 interrupt request bit	0 : No interrupt request 1 : Interrupt request	0	○	*
6	Timer 1 interrupt request bit	0 : No interrupt request 1 : Interrupt request	0	○	*
7	Timer 2 interrupt request bit	0 : No interrupt request 1 : Interrupt request	0	○	*

* "0" is set by software, but not "1."

Fig. 2.6.4 Structure of Interrupt request register 1

EOL announced

Downloaded from Elcodis.com electronic components distributor



Interrupt control register 1 (ICON1) [Address:3E$_{16}$]

B	Name	Function	At reset	R	W
0	INT_0 interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	○	○
1	INT_1/ZCR interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	○	○
2	• INT_2 interrupt enable bit • Remote control/counter overflow interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	○	○
3	• Serial I/O 1 interrupt enable bit • Serial I/O automatic transfer interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	○	○
4	Serial I/O 2 interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	○	○
5	Serial I/O 3 interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	○	○
6	Timer 1 interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	○	○
7	Timer 2 interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	○	○

Fig. 2.6.5 Structure of Interrupt control register 1

EOL announced

Downloaded from Elcodis.com electronic components distributor

2.6.2 Interrupt interval determination function

Reception of remote-control signal

Outline : Remote-control signal is read in by both of the interrupt interval determination function using a noise filter and a timer interrupt.

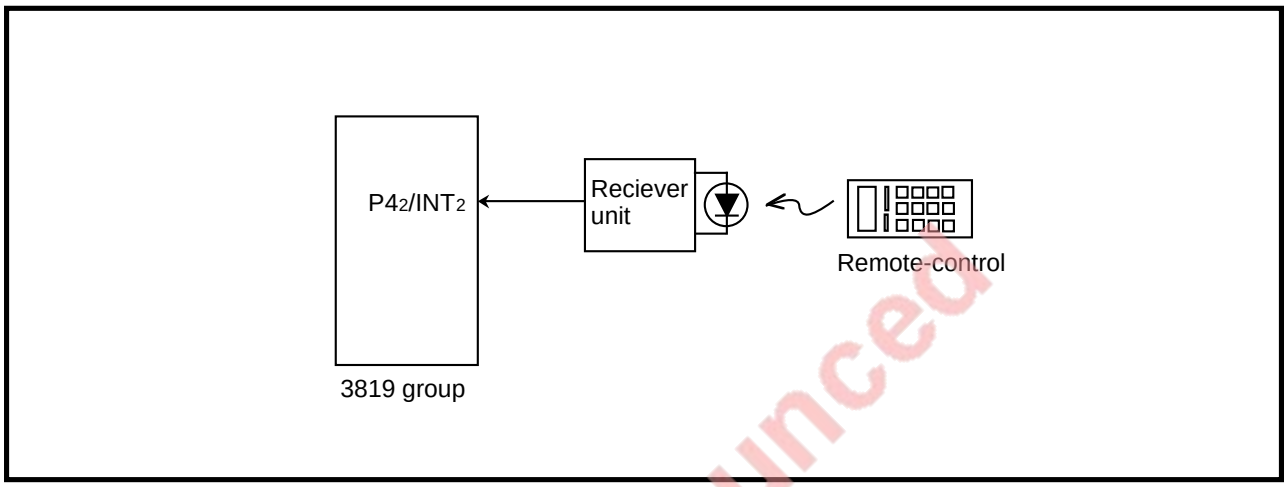


Fig. 2.6.6 Connection diagram [Reception of remote-control signal]

Specifications :
- Operation at f(XIN) = 8 MHz in the high-speed mode.
- The one-sided edge interval is measured.
- The noise filter is used.
- The remote control interrupt request is checked within the timer 2 interrupt (488 µs cycle) processing routine.

Figure 2.6.7 shows a function block diagram, and Figure 2.6.8 shows a timing chart of data determination.

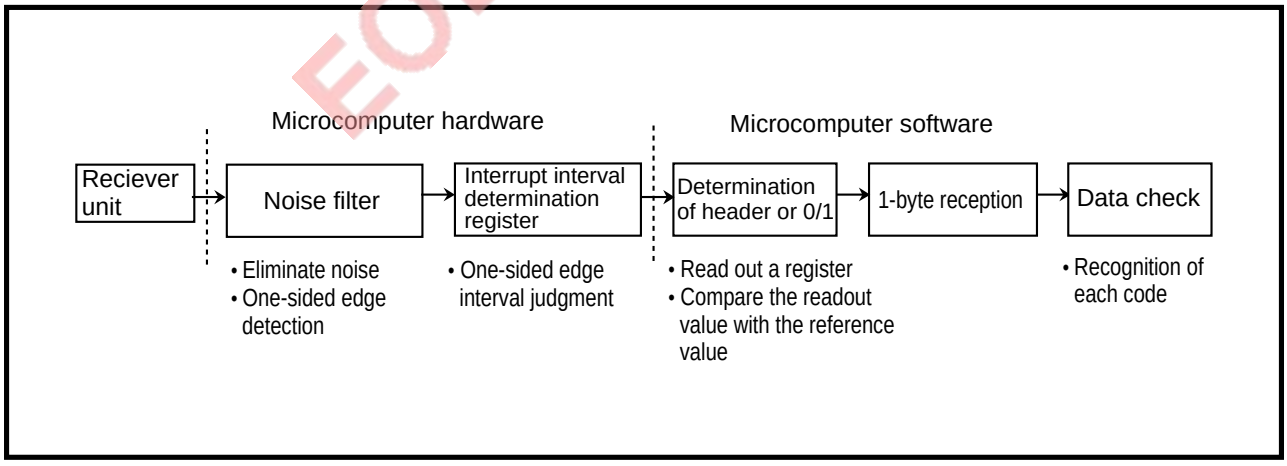


Fig. 2.6.7 Function block diagram [Reception of remote-control signal]

EOL announced

Downloaded from Elcodis.com electronic components distributor

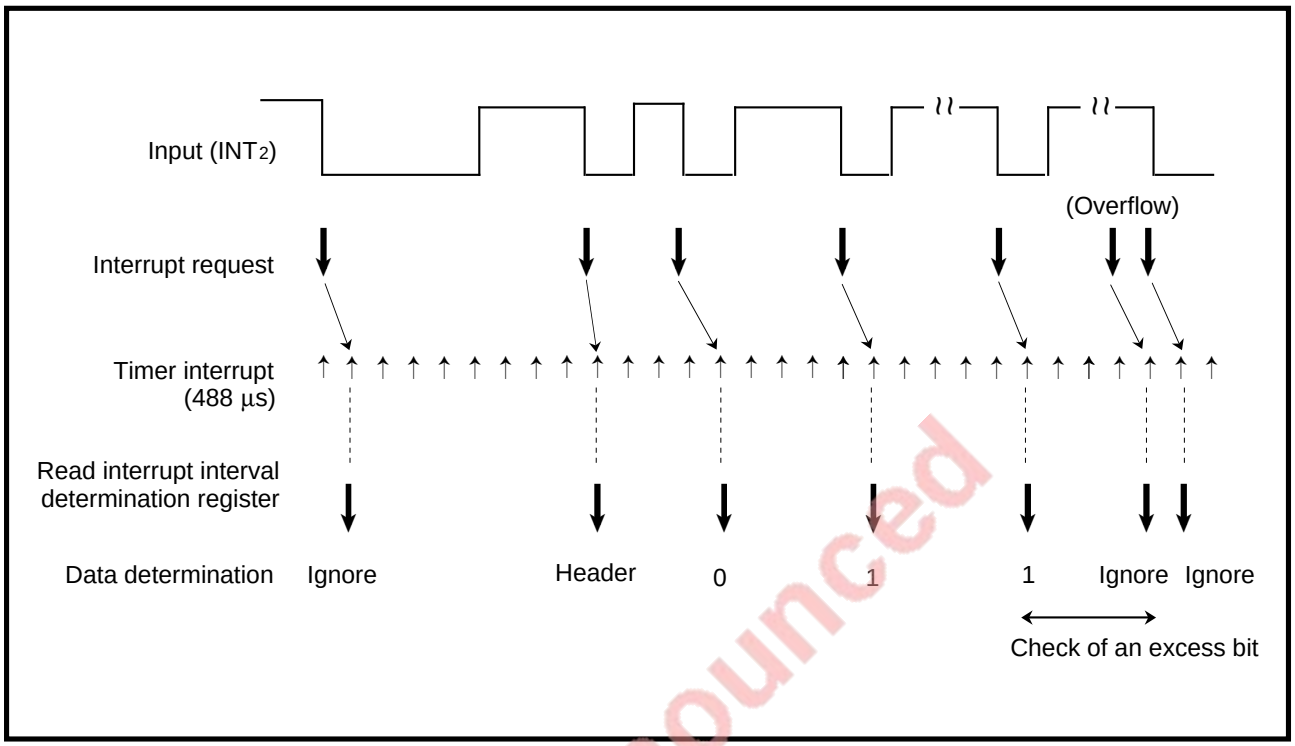
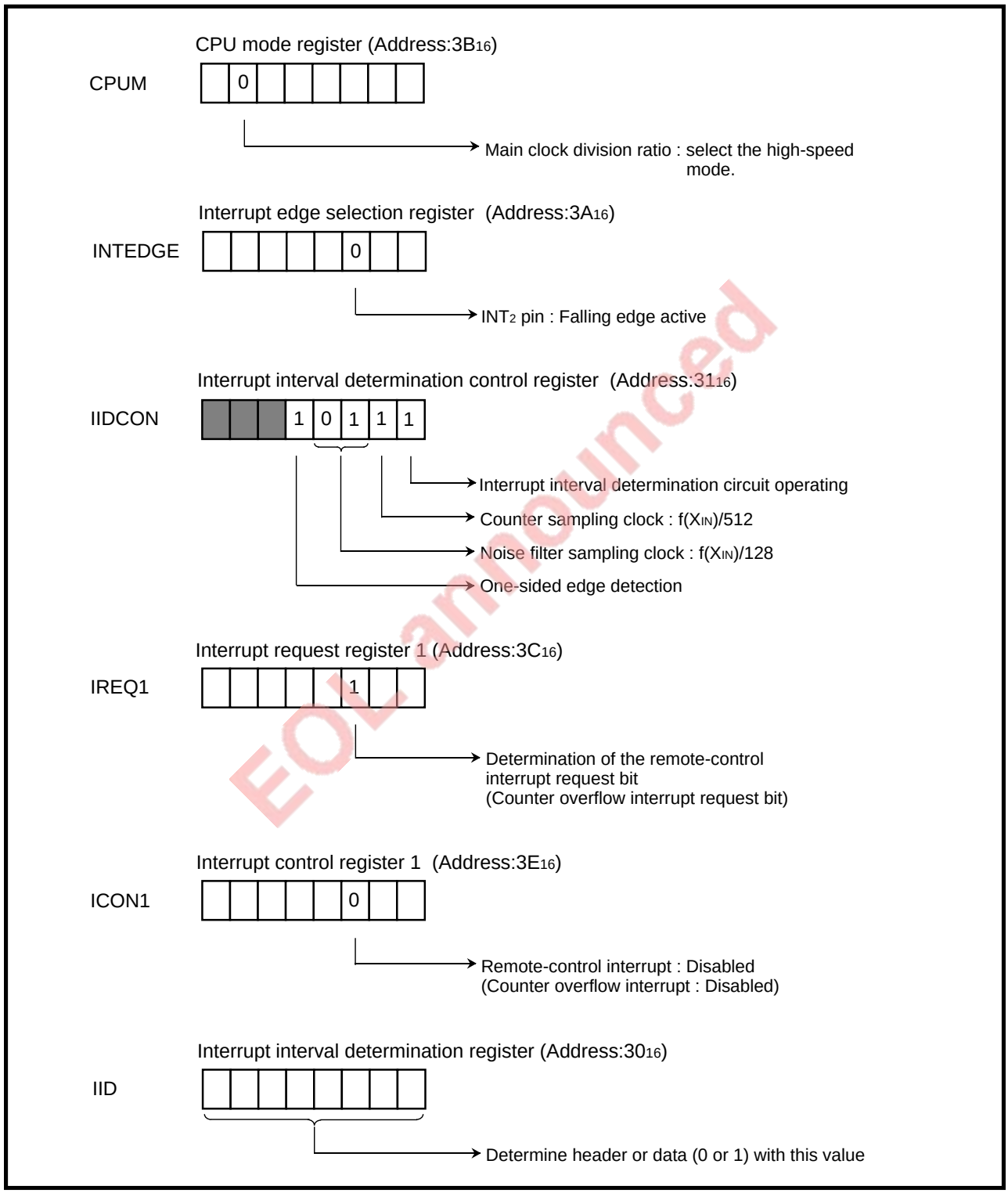


Fig. 2.6.8 Timing chart of data determination

EOL announced

Downloaded from Elcodis.com electronic components distributor

Figure 2.6.9 shows a setting of related registers.



EOL announced

Fig. 2.6.9 Setting of related registers [Reception of remote-control signal]

Downloaded from Elcodis.com electronic components distributor

Control procedure : When the registers are set as shown in Figure 2.6.9, remote-control signals are receivable. Figure 2.6.10 shows a control procedure and Figure 2.6.11 shows reception of remote-control signal (Timer 2 interrupt).

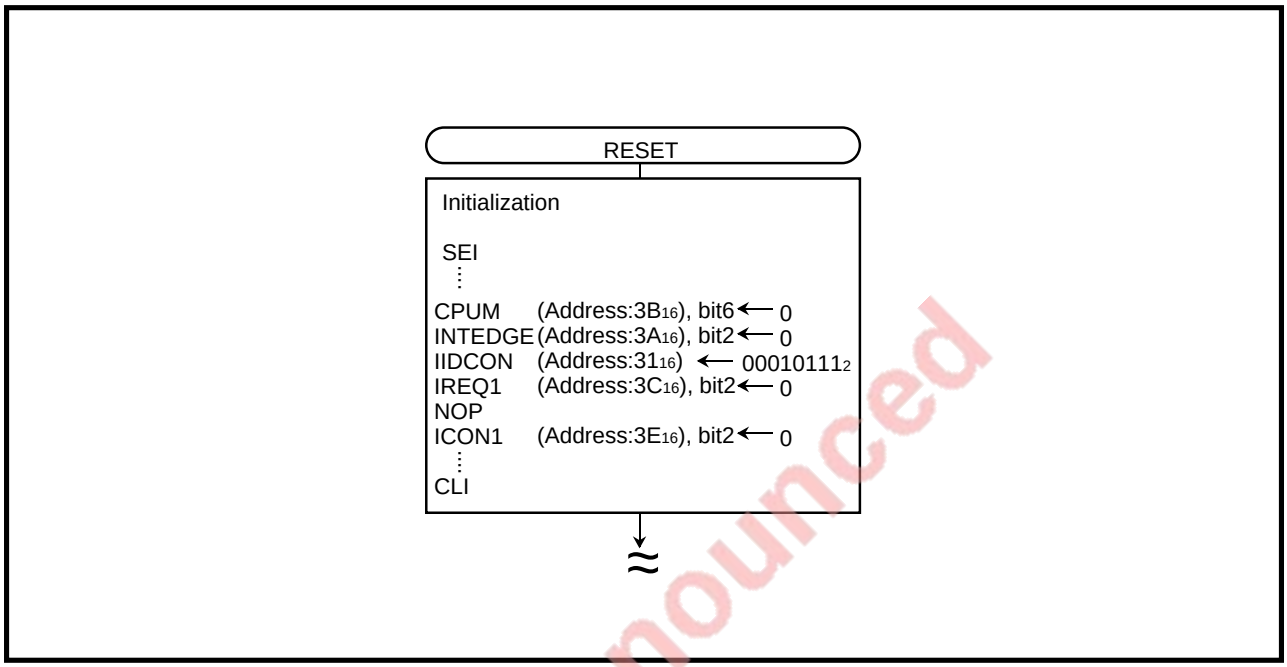


Fig. 2.6.10 Control procedure (1) [Reception of remote-control signal]

EOL announced

Downloaded from Elcodis.com electronic components distributor

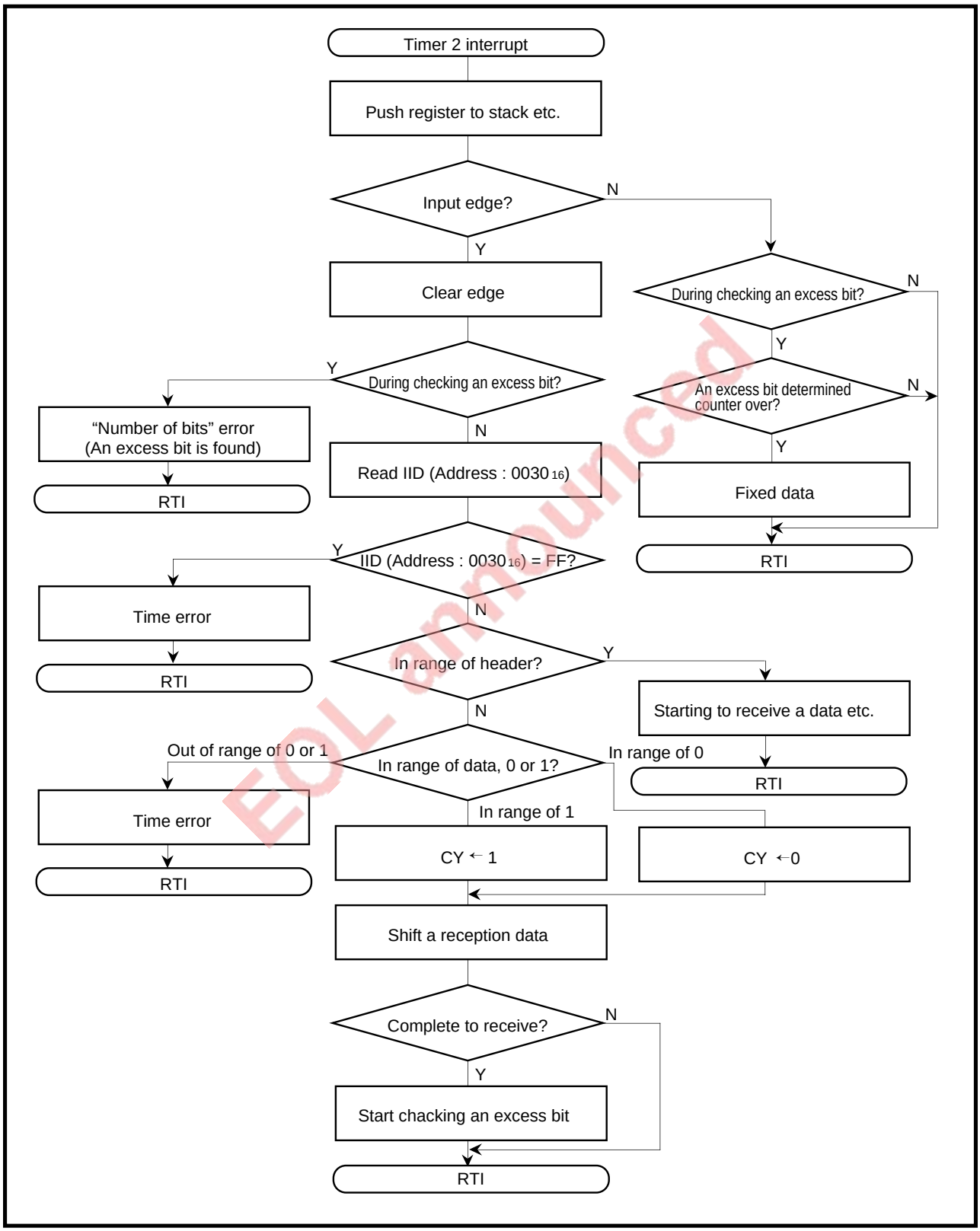


Fig. 2.6.11 Control procedure (2) [Reception of remote-control signal] (Timer 2 interrupt)

EOL announced

Downloaded from Elcodis.com electronic components distributor

2.7 Zero cross detection circuit

2.7.1 Related registers

Zero cross detection control register

b7 b6 b5 b4 b3 b2 b1 b0

Zero cross detection control register (ZCRCON) [Address:39$_{16}$]

B	Name	Function	At reset	R	W
0	Zero cross detection ON/OFF selection bit	0 : Without passing through zero cross detection comparator 1 : Passing through zero cross detection comparator	0	○	○
1	Nothing is allocated for this bit. It is a write disabled bit. When this bit is read out, the value is "0."		0	○	×
2	Noise filter sampling clock selection bits (INT$_1$)	b3 b2 00 : Note use noise filter 01 : f(X$_{IN}$)/64 or f(X$_{CIN}$)/64 10 : f(X$_{IN}$)/128 or f(X$_{CIN}$)/128 11 : f(X$_{IN}$)/256 or f(X$_{CIN}$)/256	0	○	○
3			0	○	○
4	One-sided/both-sided edge detection selection bit	0 : One-sided edge detection 1 : Both-sided edges detection (**Note**)	0	○	○
5	Nothing is allocated for these bits. These are write disabled bits. When these bits are read out, the values are "0."		0	○	×
6				○	×
7	Zero cross detection circuit input bit (read-only)	0 : Less than 0 V 1 : 0 V or more	0	○	×

Note : When the noise filter sampling clock selection bits (bits 2 and 3) of the Zero cross detection control register (ZCRCON) (Address: 39 $_{16}$) is set to “00” (when no noise filter is used), the both-sided edge detection function is not available.

Fig. 2.7.1 Structure of Zero cross detection control register

Interrupt edge selection register

b7 b6 b5 b4 b3 b2 b1 b0

Interrupt edge selecton reigster (INTEDGE) [Address:3A$_{16}$]

b	Name	Function	At reset	R	W
0	INT$_0$ interrupt edge selection bit	0 : Falling edge active 1 : Rising edge active	0	○	○
1	INT$_1$/ZCR interrupt edge selection bit	0 : Falling edge active 1 : Rising edge active	0	○	○
2	INT$_2$ interrupt edge selection bit	0 : Falling edge active 1 : Rising edge active	0	○	○
3	INT$_3$ interrupt edge selection bit	0 : Falling edge active 1 : Rising edge active	0	○	○
4	INT$_4$ interrupt edge selection bit	0 : Falling edge active 1 : Rising edge active	0	○	○
5	INT$_4$/A-D conversion interrupt switch bit	0 : INT$_4$ interrupt 1 : A-D conversion interrupt	0	○	○
6	CNTR$_0$ pin active edge switch bit	0 : Falling edge active 1 : Rising edge active	0	○	○
7	CNTR$_1$ pin active edge switch bit	0 : Falling edge active 1 : Rising edge active	0	○	○

Fig. 2.7.2 Structure of Interrupt edge selection register

EOL announced

Downloaded from Elcodis.com electronic components distributor

Interrupt request register 1

b7 b6 b5 b4 b3 b2 b1 b0

Interrupt request reigster 1 (IREQ1) [Address:3C16]

B	Name	Function	At reset	R	W
0	INT0 interrupt request bit	0 : No interrupt request 1 : Interrupt request	0	○	*
1	INT1/ZCR interrupt request bit	0 : No interrupt request 1 : Interrupt request	0	○	*
2	• INT2 interrupt request bit • Remote control/counter overflow interrupt request bit	0 : No interrupt request 1 : Interrupt request	0	○	*
3	• Serial I/O 1 interrupt request bit • Serial I/O automatic transfer interrupt request bit	0 : No interrupt request 1 : Interrupt request	0	○	*
4	Serial I/O 2 interrupt request bit	0 : No interrupt request 1 : Interrupt request	0	○	*
5	Serial I/O 3 interrupt request bit	0 : No interrupt request 1 : Interrupt request	0	○	*
6	Timer 1 interrupt request bit	0 : No interrupt request 1 : Interrupt request	0	○	*
7	Timer 2 interrupt request bit	0 : No interrupt request 1 : Interrupt request	0	○	*

* "0" is set by software, but not "1."

Fig. 2.7.3 Structure of Interrupt request register 1

Interrupt control register 1

b7 b6 b5 b4 b3 b2 b1 b0

Interrupt control register 1 (ICON1) [Address:3E16]

B	Name	Function	At reset	R	W
0	INT0 interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	○	○
1	INT1/ZCR interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	○	○
2	• INT2 interrupt enable bit • Remote control/counter overflow interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	○	○
3	• Serial I/O 1 interrupt enable bit • Serial I/O automatic transfer interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	○	○
4	Serial I/O 2 interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	○	○
5	Serial I/O 3 interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	○	○
6	Timer 1 interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	○	○
7	Timer 2 interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	○	○

Fig. 2.7.4 Structure of Interrupt control register 1

EOL announced

Downloaded from Elcodis.com electronic components distributor

2.7.2 Connection example of Zero cross detection circuit

Figure 2.7.5 shows a connection example of the Zero cross detection circuit.
R_1 is a current limiting resistor. Determine its value according to the current standard of the clamp diode. In this case, the AC input is not the effective value of 100 V but is the peak value of 140 V.
R_2 is a noise elimination resistor. Connect a resistor of about 1 kΩ near the port.

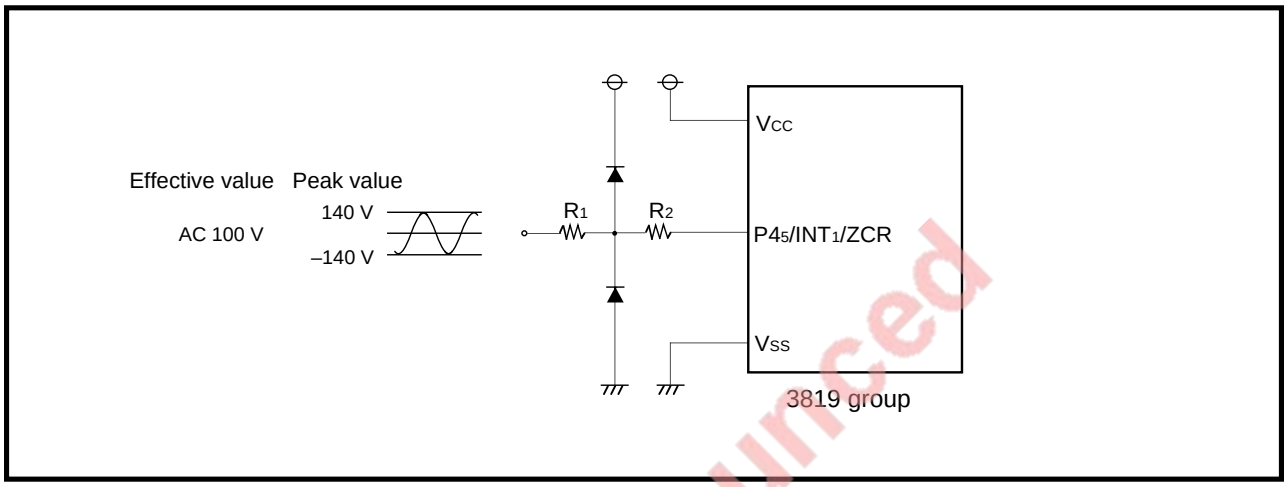


Fig. 2.7.5 Connection example of Zero cross detection circuit

EOL announced

Downloaded from Elcodis.com electronic components distributor

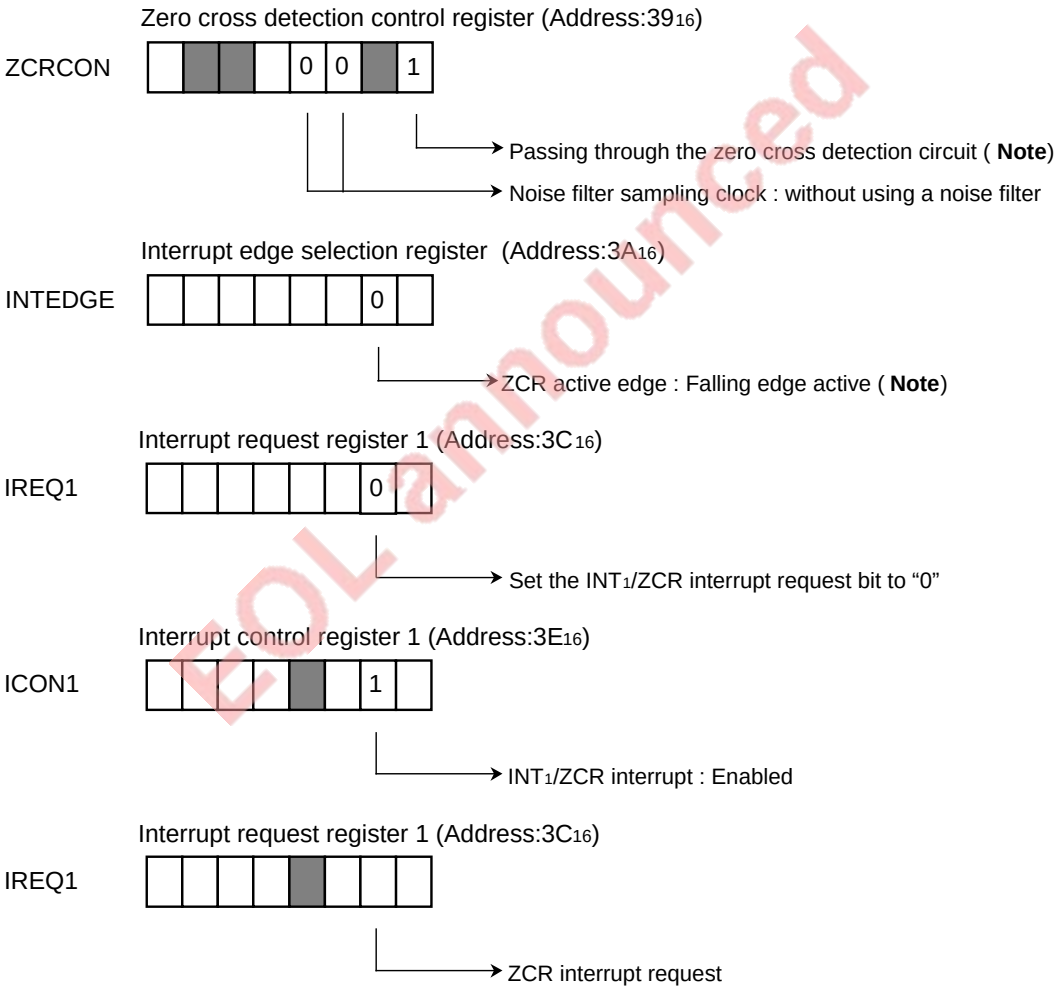
2.7.3 Zero cross detection circuit application example 1

Clock count using ZCR interrupt (without using a noise filter)

Outline : The clock is counted up every second by using the ZCR interrupts.

Specifications :
- The noise filter is not used.
- The commercial frequency (50 Hz or 60 Hz) is input.
- The clock is counted up by using the ZCR interrupts.

Figure 2. 7. 6 shows a setting of related registers.



Note : When changing the values of bit 0 of the zero cross detection control register and bit 1 of the interrupt edge selection register, make sure the following contents.
1. During changeing, set bit 1 of the interrupt control register 1 to "0".
2. After changeing, set bit 1 of the interrupt request register 1 to "0".

Fig. 2.7.6 Setting of related registers [Clock count using ZCR interrupt (without using a noise filter)]

EOL announced

Downloaded from Elcodis.com electronic components distributor

Control procedure : ① Set the related registers according to Figure 2.7.6.
② At the falling edge of the commercial frequency (50 Hz or 60 Hz), the ZCR interrupt occurs.
③ The clock is counted up every second in the ZCR interrupt processing routine.

Figure 2.7.7 shows a control procedure.

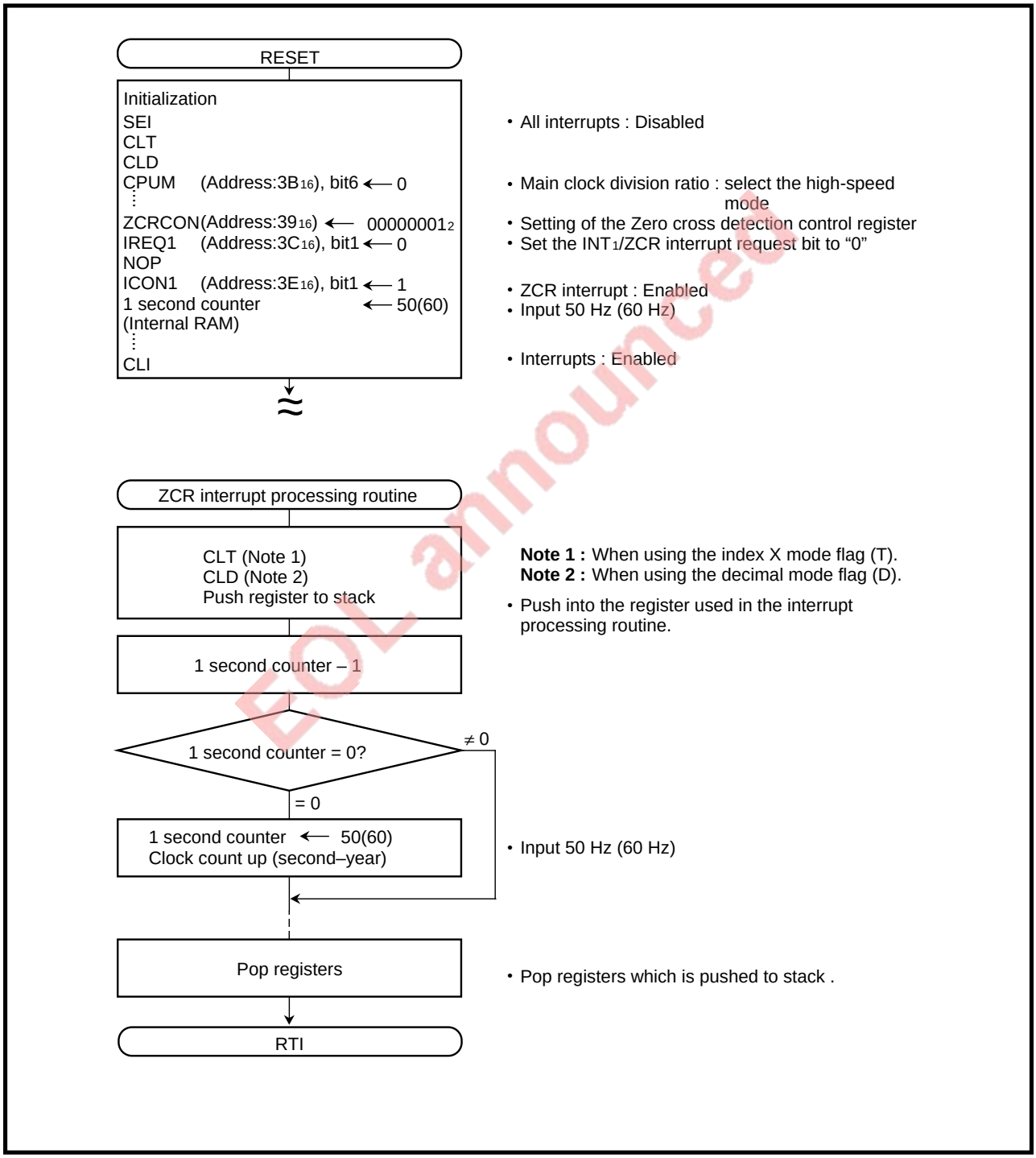


Fig. 2.7.7 Control procedure [Clock count using ZCR interrupt (without using a noise filter)]

EOL announced

Downloaded from Elcodis.com electronic components distributor

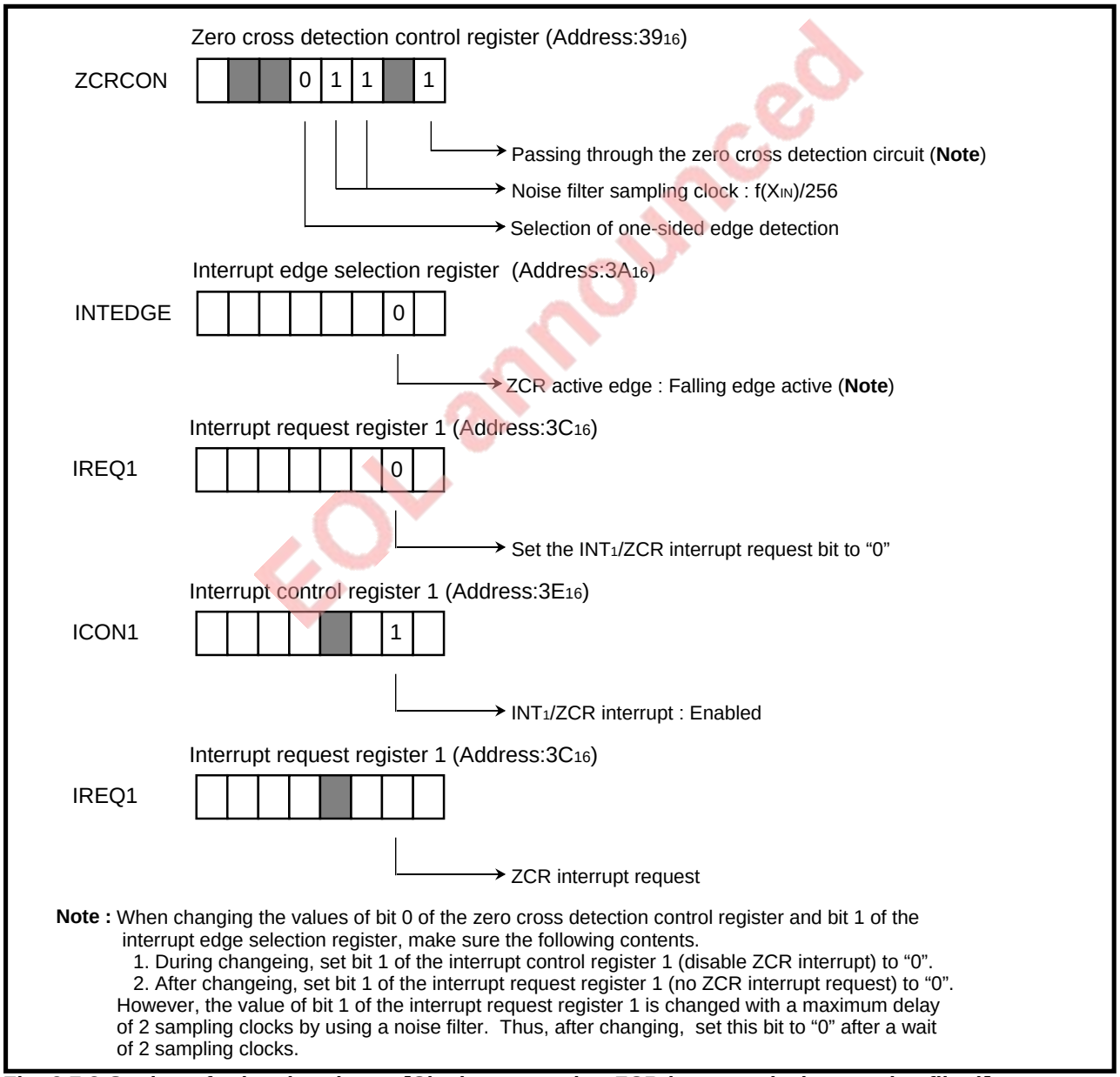
2.7.4 Zero cross detection circuit application example 2

Clock count using ZCR interrupt (using a noise filter)

Outline : The clock is counted up every second by using the ZCR interrupts.

Specifications :
- f(XIN)=4 MHz
- The noise filter (sampling clock : f(XIN)/256) is used. (Pulse less than 64 μs is eliminated as a noise.)
- The commercial frequency (50 Hz or 60 Hz) is input.
- The clock is counted up by using the ZCR interrupts.

Figure 2.7.8 shows a setting of related registers.



Note : When changing the values of bit 0 of the zero cross detection control register and bit 1 of the interrupt edge selection register, make sure the following contents.
1. During changeing, set bit 1 of the interrupt control register 1 (disable ZCR interrupt) to "0".
2. After changeing, set bit 1 of the interrupt request register 1 (no ZCR interrupt request) to "0".

However, the value of bit 1 of the interrupt request register 1 is changed with a maximum delay of 2 sampling clocks by using a noise filter. Thus, after changing, set this bit to "0" after a wait of 2 sampling clocks.

Fig. 2.7.8 Setting of related registers [Clock count using ZCR interrupt (using a noise filter)]

EOL announced

Downloaded from Elcodis.com electronic components distributor

Control procedure : ① Set the related registers according to Figure 2.7.8.
② At the falling edge of the commercial frequency (50 Hz or 60 Hz), the ZCR interrupt occurs.
③ The clock is counted up every second in the ZCR interrupt processing routine.

Figure 2.7.9 shows a control procedure.

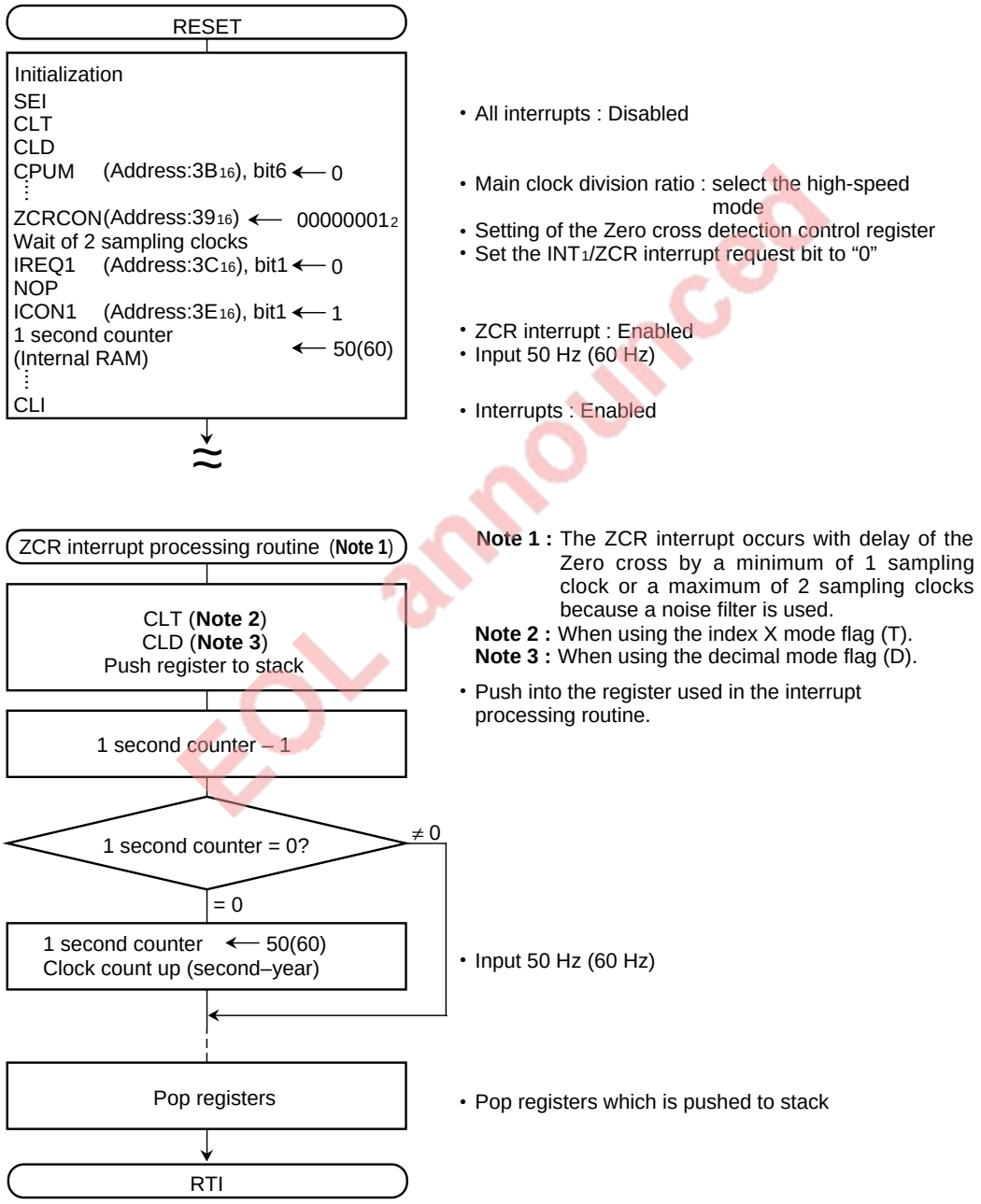


Fig. 2.7.9 Control procedure [Clock count using ZCR interrupt (using a noise filter)]

EOL announced

Downloaded from Elcodis.com electronic components distributor

2. APPLICATION

2.8 Reset

2.8.1 Connection example of reset IC

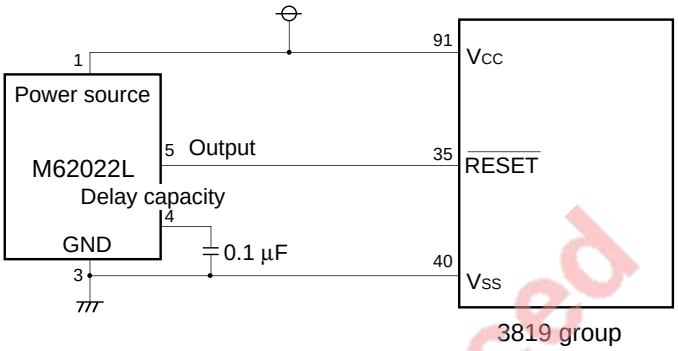


Fig. 2.8.1 Example of Poweron reset circuit

Figure 2.8.2 shows the system example which switch to the RAM backup mode by detecting a drop of the system power source voltage with the INT interrupt.

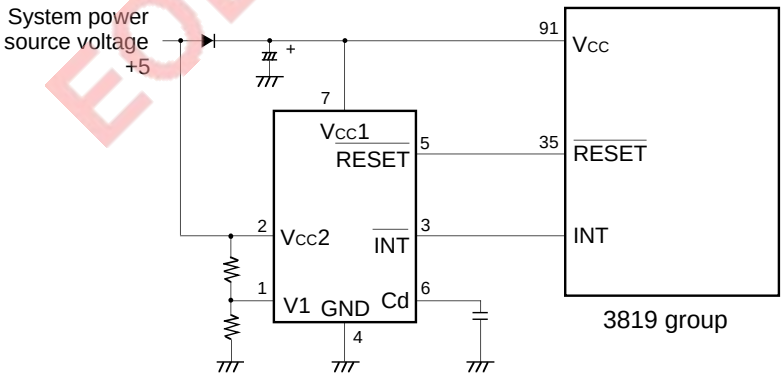


Fig. 2.8.2 RAM back-up system

EOL announced

Downloaded from Elcodis.com electronic components distributor

2.9 Clock generating circuit

2.9.1 Related registers

Timer i

b7	b6	b5	b4	b3	b2	b1	b0

Timer i (Ti) (i = 1, 3)
[Address:20_{16}, 22_{16}]

B	Function	At reset	R	W
0	● The counter value of the Timer i is set. ● The value set in this register is written to both the Timer i and the Timer i latch at the same time. ● When the Timer i is read out, the value (count value) of the Timer i is read out.	1	○	○
1		1	○	○
2		1	○	○
3		1	○	○
4		1	○	○
5		1	○	○
6		1	○	○
7		1	○	○

Fig. 2.9.1 Structure of Timer i (i = 1, 3)

Timer 2

b7	b6	b5	b4	b3	b2	b1	b0

Timer 2 (T2) [Address:21_{16}]

B	Function	At reset	R	W
0	● The counter value of the Timer 2 is set. ● The value set in this register is written to both the Timer 2 and the Timer 2 latch at the same time. ● When the Timer 2 is read out, the value (count value) of the Timer 2 is read out.	1	○	○
1		0	○	○
2		0	○	○
3		0	○	○
4		0	○	○
5		0	○	○
6		0	○	○
7		0	○	○

Fig. 2.9.2 Structure of Timer 2

End announced

Downloaded from Elcodis.com electronic components distributor

Timer 12 mode register

b7 b6 b5 b4 b3 b2 b1 b0

Timer 12 mode register (T12M) [Address:28$_{16}$]

B	Name	Function	At reset	R	W
0	Timer 1 count stop bit	0 : Operating 1 : Stopped	0	○	○
1	Timer 2 count stop bit	0 : Operating 1 : Stopped	0	○	○
2	Timer 1 count source selection bit	0 : f(X_{IN})/16 or f(X_{CIN})/16 1 : f(X_{CIN})	0	○	○
3	Nothing is allocated for this bit. This is a write disabled bit. When this bit is read out, the value is "0."		0	○	×
4	Timer 2 count source selection bits	b5 b4 00 : Timer 1 underflow 01 : f(X_{CIN}) 10 : External count input CNTR$_0$ 11 : Not available	0	○	○
5			0	○	○
6	Timer 1 output selection bit ($P4_6$)	0 : I/O port 1 : Timer 1 output	0	○	○
7	Nothing is allocated for this bit. This is a write disabled bit. When this bit is read out, the value is "0."		0	○	×

Fig. 2.9.3 Structure of Timer 12 mode register

Timer 34 mode register

b7 b6 b5 b4 b3 b2 b1 b0

Timer 34 mode register (T34M) [Address:29$_{16}$]

B	Name	Function	At reset	R	W
0	Timer 3 count stop bit	0 : Operating 1 : Stopped	0	○	○
1	Timer 4 count stop bit	0 : Operating 1 : Stopped	0	○	○
2	Timer 3 count source selection bit	0 : f(X_{IN})/16 or f(X_{CIN})/16 1 : Timer 2 underflow	0	○	○
3	Nothing is allocated for this bit. This is a write disabled bit. When this bit is read out, the value is "0."		0	○	×
4	Timer 4 count source selection bits	b5 b4 00 : f(X_{IN})/16 or f(X_{CIN})/16 01 : Timer 3 underflow 10 : External count input CNTR$_1$ 11 : Not available	0	○	○
5			0	○	○
6	Timer 3 output selection bit ($P4_7$)	0 : I/O port 1 : Timer 3 output	0	○	○
7	Nothing is allocated for this bit. This is a write disabled bit. When this bit is read out, the value is "0."		0	○	×

Fig. 2.9.4 Structure of Timer 34 mode register

EOL announced

Downloaded from Elcodis.com electronic components distributor

CPU mode register

b7 b6 b5 b4 b3 b2 b1 b0

CPU mode register (CPUM) [Address:3B16]

B	Name	Function	At reset	R	W
0	Processor mode bits	b1b0 0 0 : Single-chip mode 0 1 : 1 0 : Not available 1 1 :	0	○	○
1			0	○	○
2	Stack page selection bit	0 : 0 page 1 : 1 page	0	○	○
3	XCOUT drivability selection bit	0 : Low 1 : High	1	○	○
4	Port Xc switch bit	0 : I/O port function 1 : XCIN–XCOUT oscillating function	0	○	○
5	Main clock (XIN-XOUT) stop bit	0 : Operating 1 : Stopped	0	○	○
6	Main clock division ratio selection bit	0 : f(XIN)/2 (high-speed mode) 1 : f(XIN)/8 (middle-speed mode)	1	○	○
7	Internal system clock selection bit	0 : XIN-XOUT selected (middle/high-speed mode) 1 : XCIN-XCOUT selected (low-speed mode)	0	○	○

Fig. 2.9.5 Structure of CPU mode register

Interrupt request register 1

b7 b6 b5 b4 b3 b2 b1 b0

Interrupt request reigster 1 (IREQ1) [Address:3C16]

B	Name	Function	At reset	R	W
0	INT0 interrupt request bit	0 : No interrupt request 1 : Interrupt request	0	○	*
1	INT1/ZCR interrupt request bit	0 : No interrupt request 1 : Interrupt request	0	○	*
2	• INT2 interrupt request bit • Remote control/counter overflow interrupt request bit	0 : No interrupt request 1 : Interrupt request	0	○	*
3	• Serial I/O 1 interrupt request bit • Serial I/O automatic transfer interrupt request bit	0 : No interrupt request 1 : Interrupt request	0	○	*
4	Serial I/O 2 interrupt request bit	0 : No interrupt request 1 : Interrupt request	0	○	*
5	Serial I/O 3 interrupt request bit	0 : No interrupt request 1 : Interrupt request	0	○	*
6	Timer 1 interrupt request bit	0 : No interrupt request 1 : Interrupt request	0	○	*
7	Timer 2 interrupt request bit	0 : No interrupt request 1 : Interrupt request	0	○	*

* "0" is set by software, but not "1."

Fig. 2.9.6 Structure of Interrupt request register 1

EOL announced

Downloaded from Elcodis.com electronic components distributor

Interrupt request register 2

b7 b6 b5 b4 b3 b2 b1 b0

Interrupt request reigster 2 (IREQ2) [Address:3D16]

b	Name	Function	At reset	R	W
0	Timer 3 interrupt request bit	0 : No interrupt request 1 : Interrupt request	0	○	*
1	Timer 4 interrupt request bit	0 : No interrupt request 1 : Interrupt request	0	○	*
2	Timer 5 interrupt request bit	0 : No interrupt request 1 : Interrupt request	0	○	*
3	Timer 6 interrupt request bit	0 : No interrupt request 1 : Interrupt request	0	○	*
4	INT_3 interrupt request bit	0 : No interrupt request 1 : Interrupt request	0	○	*
5	• INT_4 interrupt request bit • A-D conversion interrupt request bit	0 : No interrupt request 1 : Interrupt request	0	○	*
6	• FLD blanking interrupt request bit • FLD digit interrupt request bit	0 : No interrupt request 1 : Interrupt request	0	○	*
7	Nothing is allocated for this bit. This is a write disabled bit. When this bit is read out, the value is "0."		0	○	*

* "0" is set by software, but not "1."

Fig. 2.9.7 Structure of Interrupt request register 2

Interrupt control register 1

b7 b6 b5 b4 b3 b2 b1 b0

Interrupt control register 1 (ICON1) [Address:3E16]

B	Name	Function	At reset	R	W
0	INT_0 interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	○	○
1	INT_1/ZCR interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	○	○
2	• INT_2 interrupt enable bit • Remote control/counter overflow interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	○	○
3	• Serial I/O 1 interrupt enable bit • Serial I/O automatic transfer interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	○	○
4	Serial I/O 2 interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	○	○
5	Serial I/O 3 interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	○	○
6	Timer 1 interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	○	○
7	Timer 2 interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	○	○

Fig. 2.9.8 Structure of Interrupt control register 1

EOL announced

Downloaded from Elcodis.com electronic components distributor

Interrupt control register 2

b7	b6	b5	b4	b3	b2	b1	b0
0							

Interrupt control reigster 2 (ICON2) [Address:$3F_{16}$]

b	Name	Function	At reset	R	W
0	Timer 3 interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	○	○
1	Timer 4 interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	○	○
2	Timer 5 interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	○	○
3	Timer 6 interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	○	○
4	INT_3 interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	○	○
5	• INT_4 interrupt enable bit • A-D conversion interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	○	○
6	• FLD blanking interrupt enable bit • FLD digit interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	○	○
7	Fix this bit to "0."		0	○	○

Fig. 2.9.9 Structure of Interrupt control register 2

EOL announced

Downloaded from Elcodis.com electronic components distributor

2.9.2 Clock generating circuit application examples

(1) Status transition upon a power failure

Outline : The clock is counted up every second by using the timer interrupt during a power failure.

Specifications :

- Keep a power consumption as low as possible while maintaining a clock function.
- f(X_{IN}) = 4.19 MHz, f(X_{CIN}) = 32.768 kHz
- Port processing

Input port : Fix to "H" or "L" level in the external unit.

Output port : Fix to an output level which does not cause a current flow to the external unit.

[Example]
When a circuit turns on LED at "L" output level, fix the output level to "H."

I/O port : Input port — Fix to "H" or "L" level in the external unit .
Output port — Output the data which does not consume current.

V_{REF} : Supplying to the Reference voltage input pin is stopped by the external circuit.

$P4_5$/ZCR (using as the input port) : Fix to "H" level in the external unit .

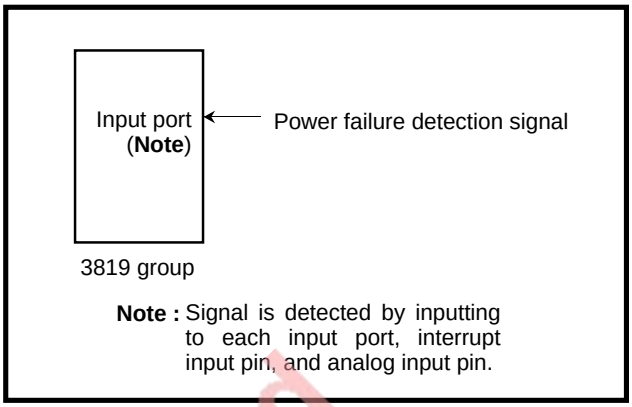


Fig. 2.9.10 Connection diagram [Status transition upon a power failure]

Figure 2.9.11 shows a status transition diagram upon a power failure, Figure 2.9.12 shows a setting of related registers, and Figure 2.9.13 shows a control procedure.

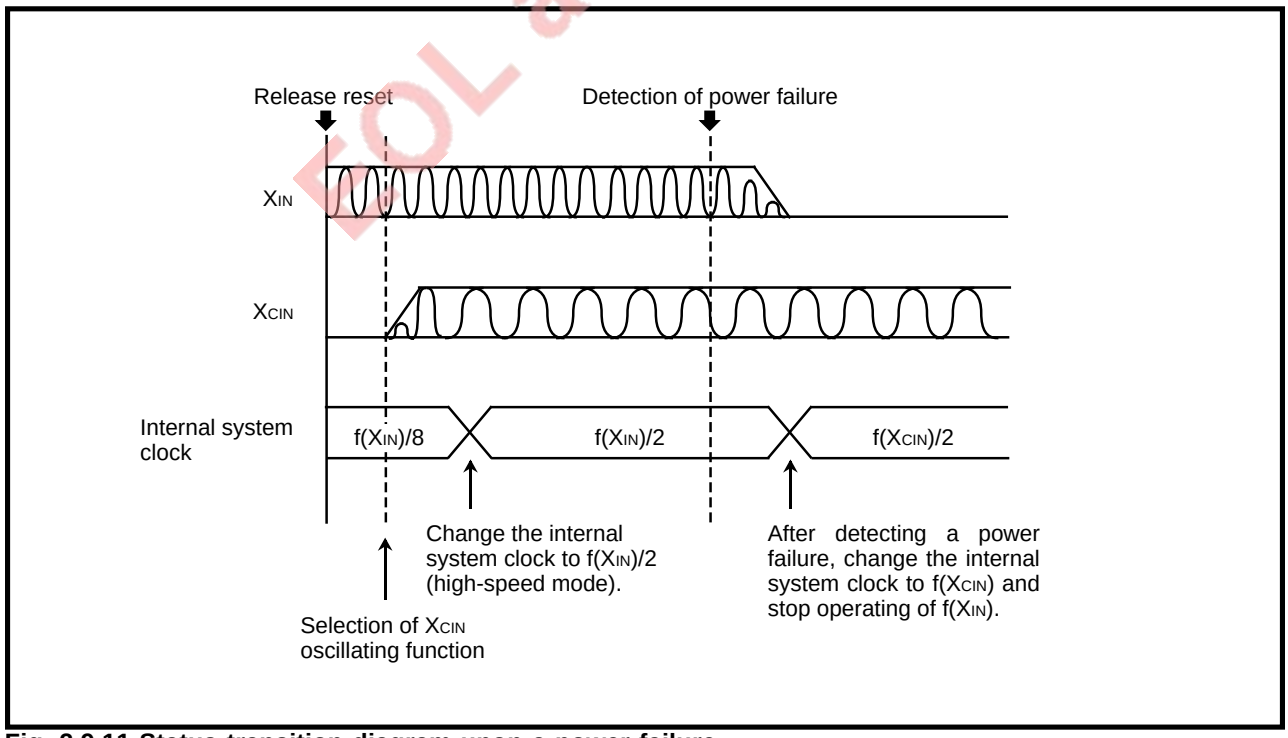
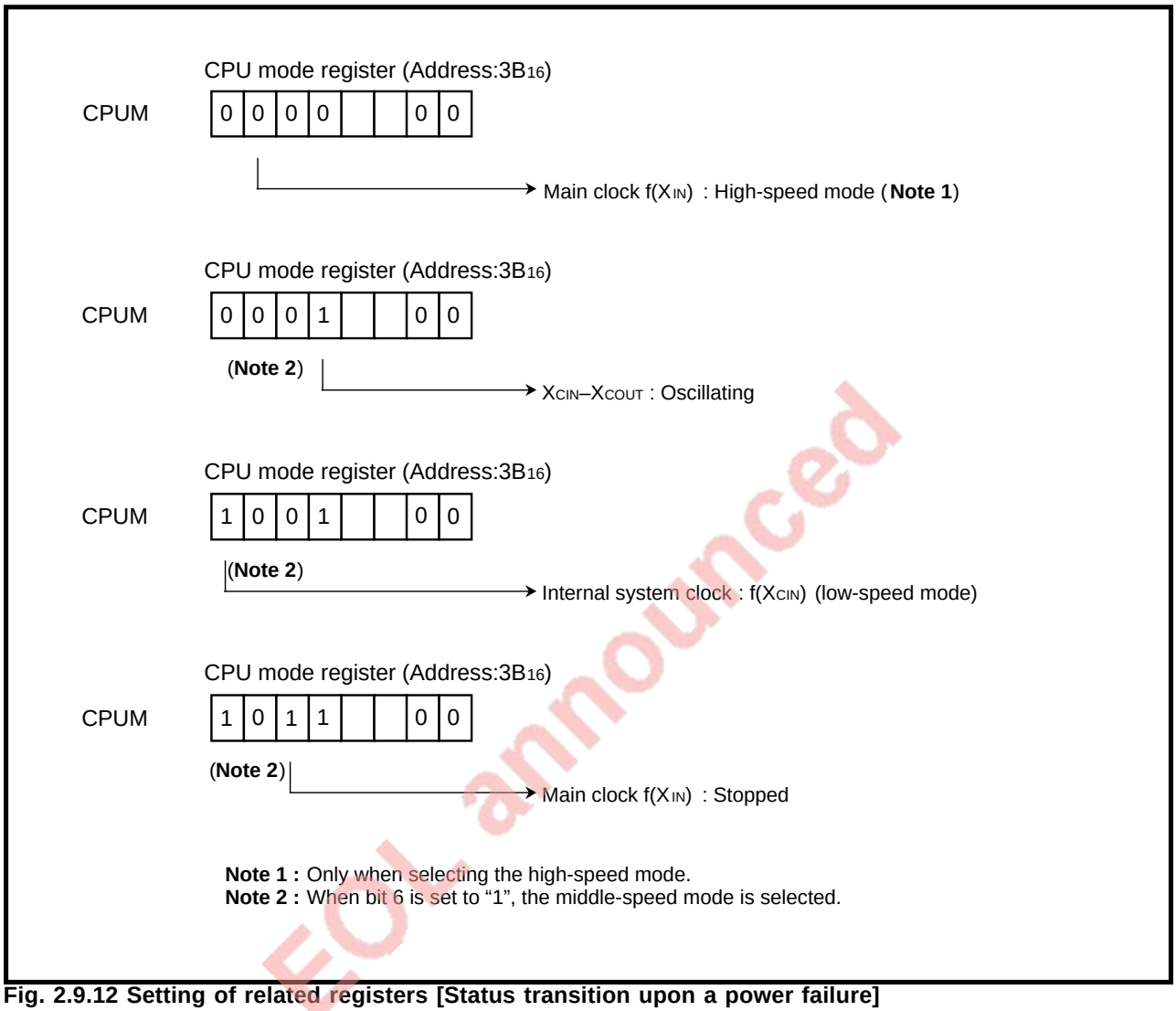


Fig. 2.9.11 Status transition diagram upon a power failure

EOL announced

Downloaded from Elcodis.com electronic components distributor

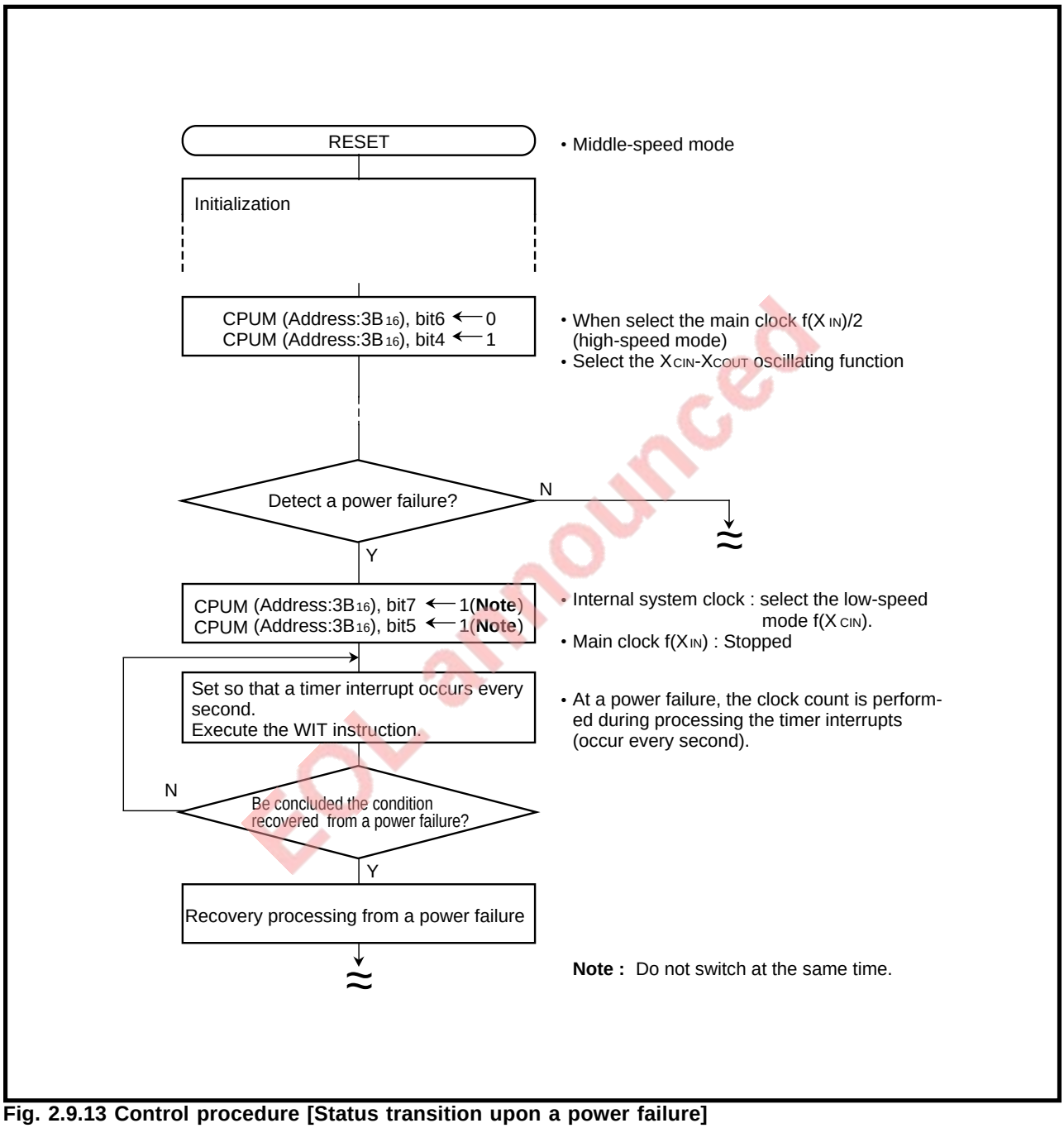


EOL announced

Fig. 2.9.12 Setting of related registers [Status transition upon a power failure]

Downloaded from Elcodis.com electronic components distributor

Control procedure : Set the related registers in the order shown below to prepare for a power failure.



EOL announced

Fig. 2.9.13 Control procedure [Status transition upon a power failure]

Downloaded from Elcodis.com electronic components distributor

(2) Counting without clock error during a power failure

Outline : It keeps counting without clock errors during a power failure.

Specifications :

- Keep a power consumption as low as possible while maintaining a clock function.
- Keep counting a clock correctly.
- f(XIN) = 4.19 MHz, f(XCIN) = 32.768 kHz
- The Timer 1 interrupt is used in a normal power state. The Timer 3 interrupt is used during a power failure.
- Port processing

Input port : Fix to "H" or "L" level in the external unit.

Output port : Fix to an output level which does not cause a current flow to the external unit.

[Example]

When a circuit turns on LED at "L" output level, fix the output level to "H".

I/O port : Input port — Fix to "H" or "L" level in the external unit.
Output port — Output the data which does not consume current.

VREF : Supplying to the Reference voltage input pin is stopped by the external circuit.

P45/ZCR (using as the input port) : Fix to "H" level in the external unit.

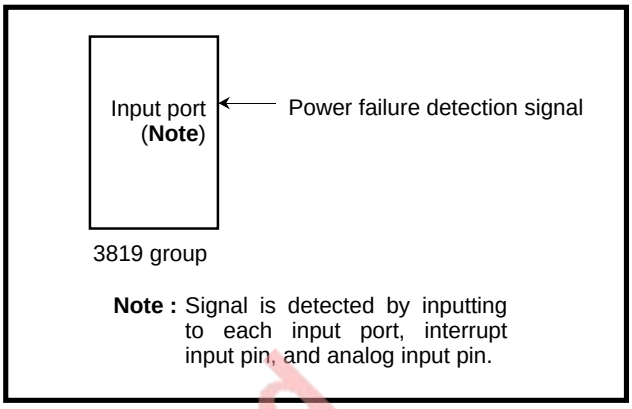


Fig. 2.9.14 Connection diagram [Counting without clock errors during a power failure]

Figure 2.9.15 shows a timing chart of counting without clock errors during a power failure, Figure 2.9.16 shows a structure of a clock counter, and Figures 2.9.17 and 2.9.18 show a setting of related registers.

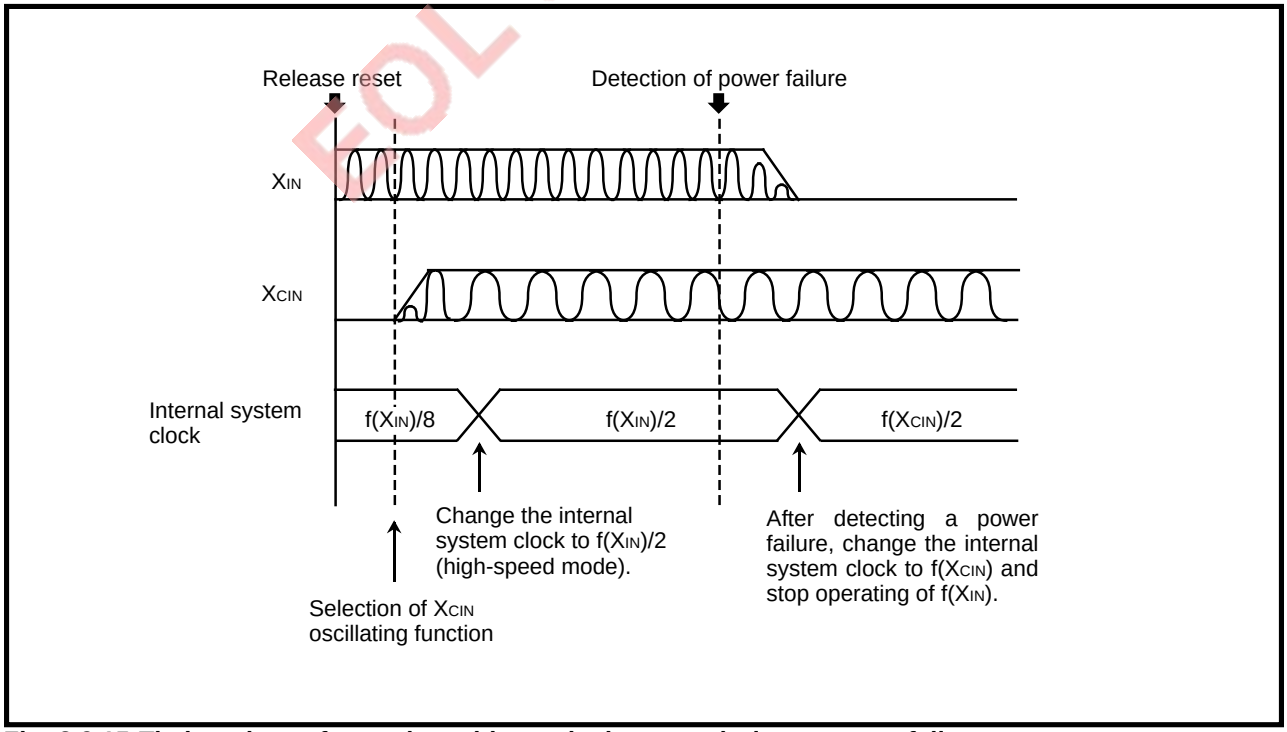


Fig. 2.9.15 Timing chart of counting without clock errors during a power failure

Downloaded from Elcodis.com electronic components distributor

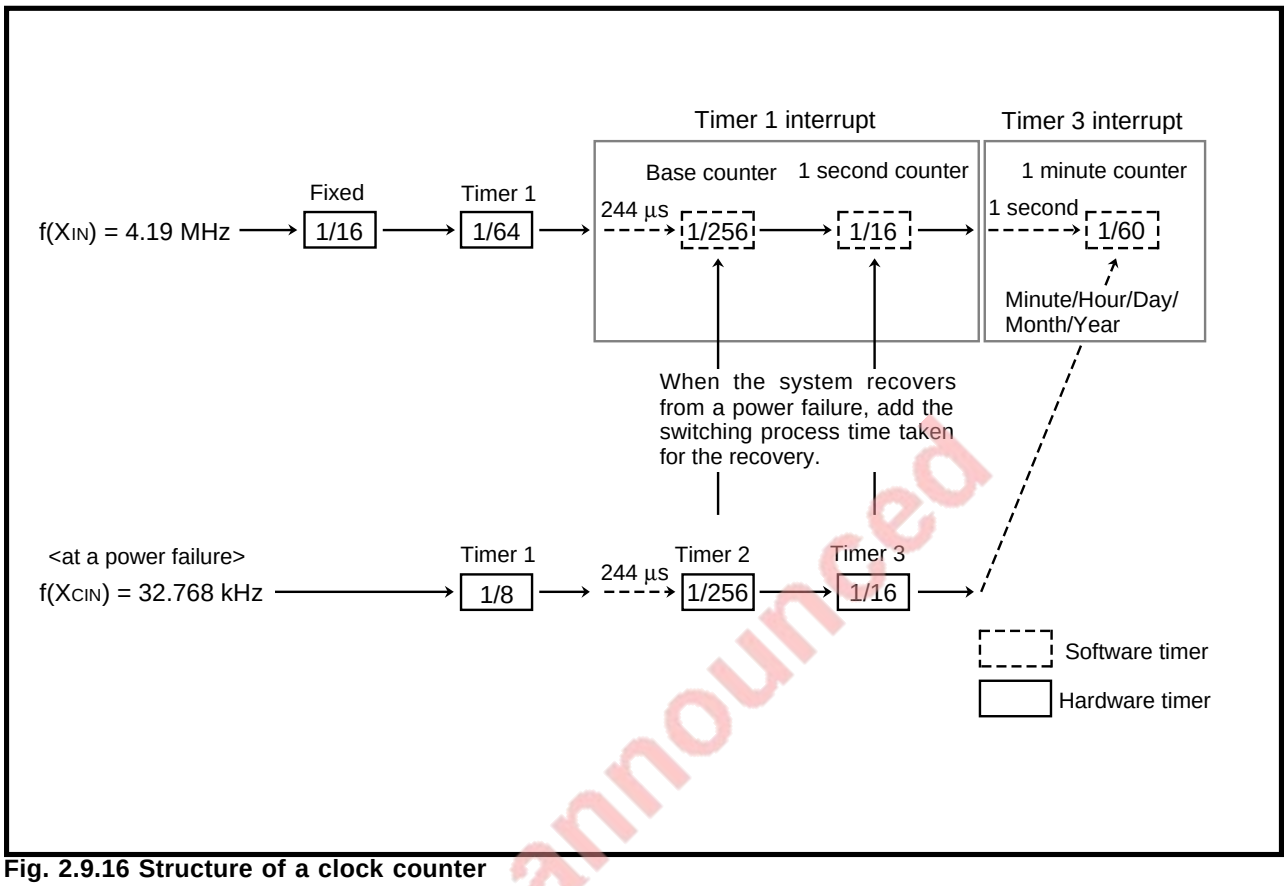


Fig. 2.9.16 Structure of a clock counter

EOL announced

Downloaded from Elcodis.com electronic components distributor

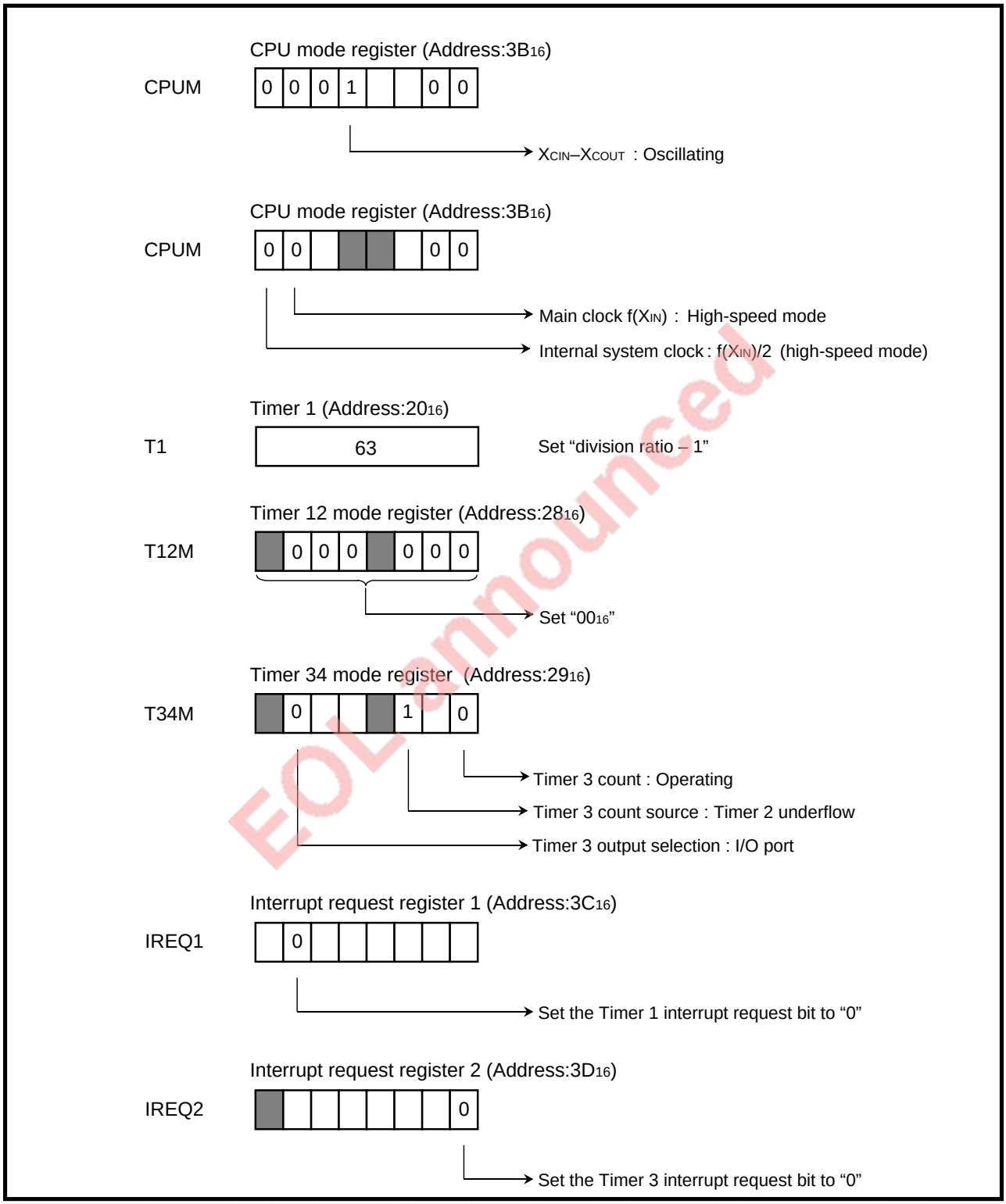
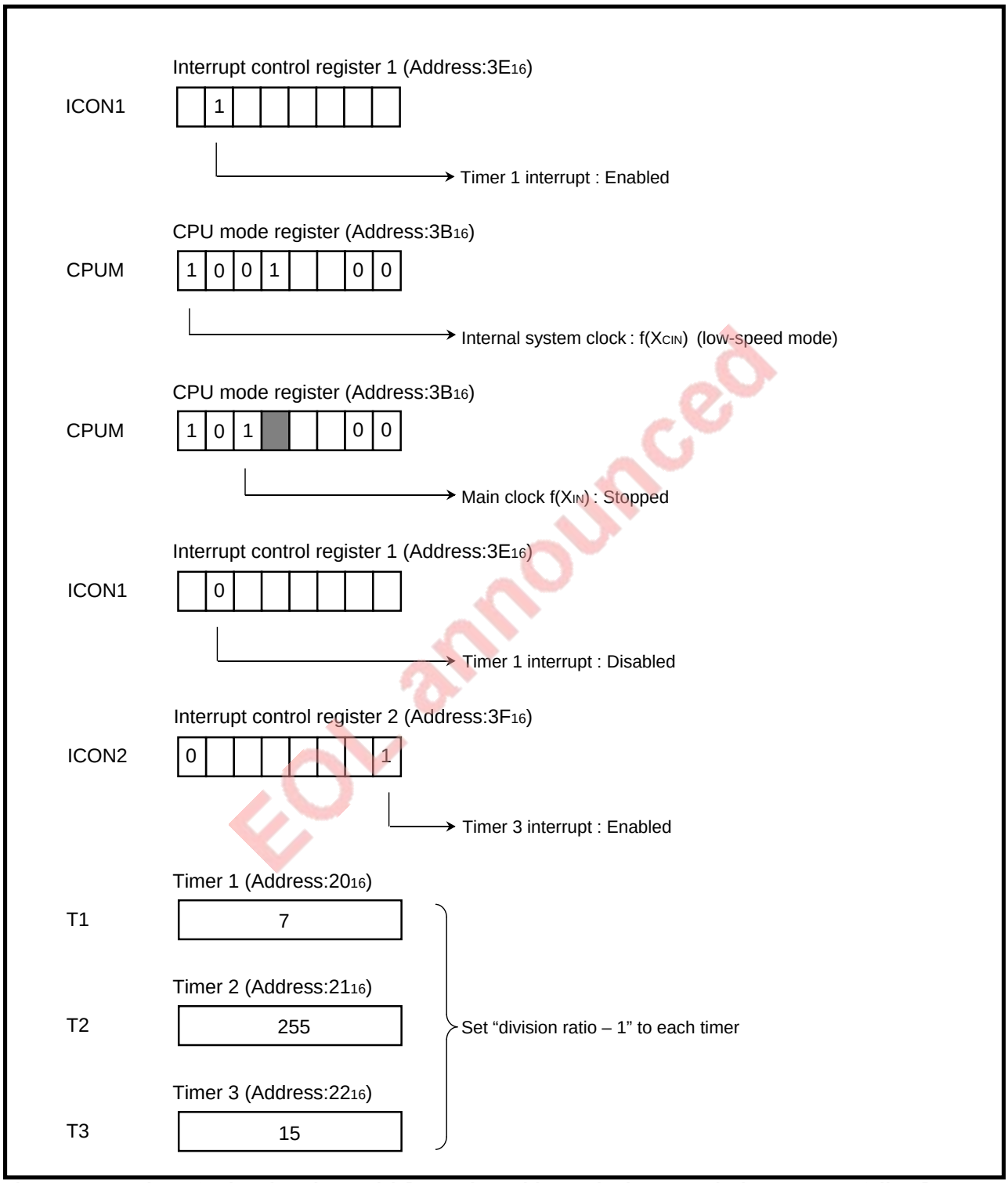


Fig. 2.9.17 Setting of related registers (1) [Counting without clock errors during a power failure]

EOL announced

Downloaded from Elcodis.com electronic components distributor



EOL announced

Fig. 2.9.18 Setting of related registers (2) [Counting without clock errors during a power failure]

Downloaded from Elcodis.com electronic components distributor

Control procedure : Set the related registers in the order shown below to prepare for a power failure.

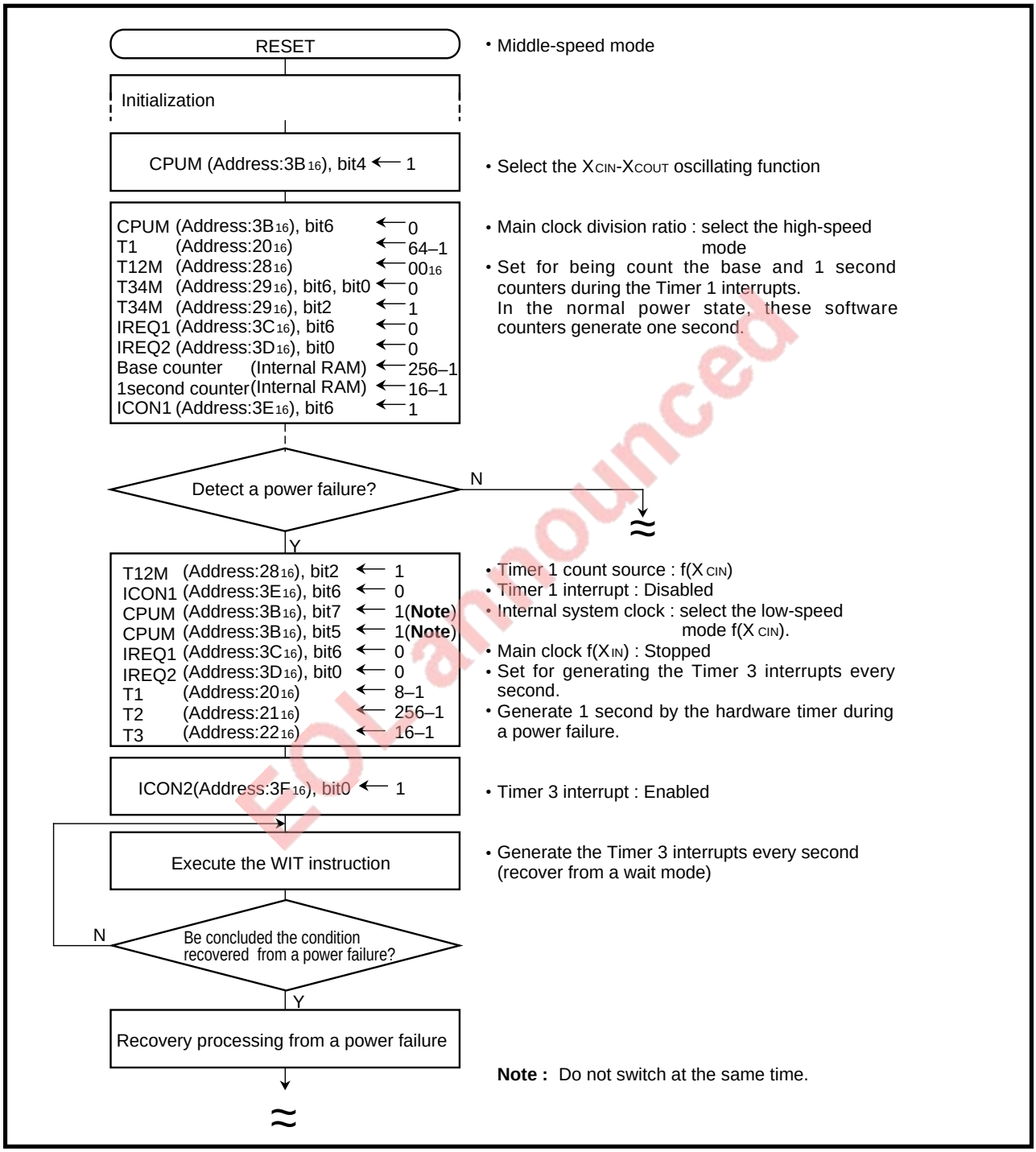


Fig. 2.9.19 Control procedure (1) [Counting without clock errors during a power failure]

EOL announced

Downloaded from Elcodis.com electronic components distributor

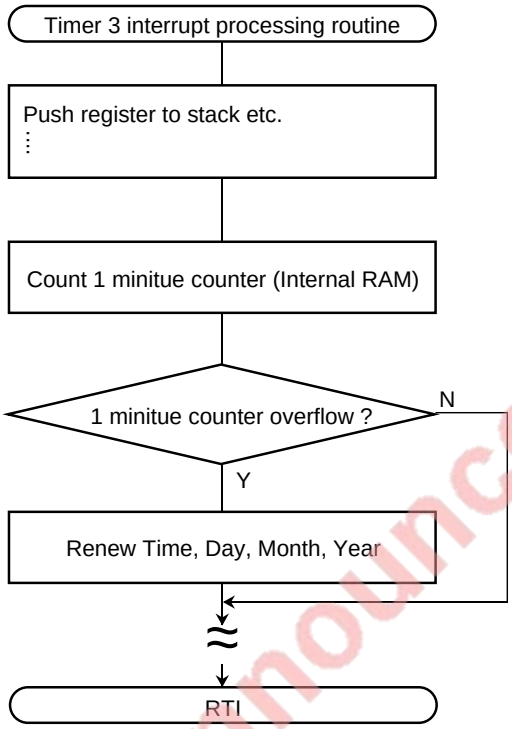


Fig. 2.9.20 Control procedure (2) [Counting without clock errors during a power failure]

EOL announced

Downloaded from Elcodis.com electronic components distributor

CHAPTER 3

APPENDIX

EOL announced

Downloaded from Elcodis.com electronic components distributor

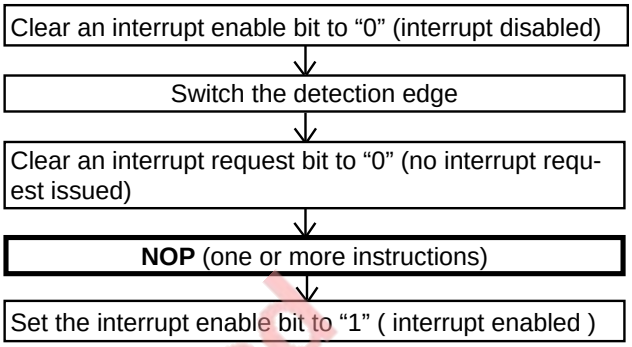
3. APPENDIX

3.1 Notes on use

3.1.1 Notes on Interrupts

<Note 1>
For the products able to switch the external interrupt detection edge, switch it as the following sequence.

Reason
The interrupt circuit recognizes the switching of the detection edge as the change of external input signals. This may cause an unnecessary interrupt.



<Note 2>
Fix the bit 7 of the interrupt control register 2 to “0”.

Figure 3.1.1 shows the structure of the interrupt control register 2.

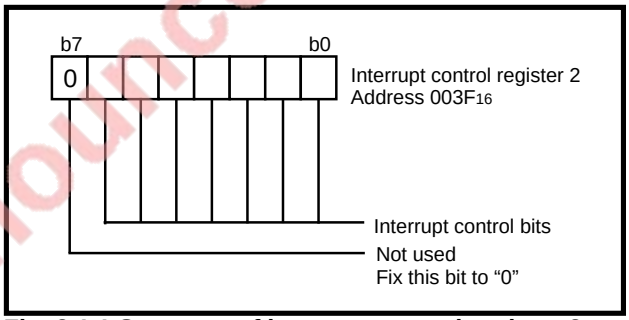


Fig. 3.1.1 Structure of interrupt control register 2

EOL announced

3.1.2 Notes on the FLD controller and the serial I/O automatic transfer function

When using the FLD controller function and the serial I/O automatic transfer function, set the system clock to the high-speed mode or the middle-speed mode.

3.1.3 Notes on the A-D converter

<Note 1>
Make the signal source impedance for analog input low, or equip an analog input pin with an external capacitor of 0.01 μF to 1 μF. Further, be sure to verify the operation of application products on the user side.

Reason
An analog input pin includes the capacitor for analog voltage comparison. Accordingly, when signals from signal source with high impedance are input to an analog input pin, charge and discharge noise generates. This may cause the A-D comparison precision to be worse.

<Note 2>
Pins AVCC and AVSS are A-D converter power source pins. Connect them as following :
●AVCC : Connect to the VCC line which is the analog system
●AVSS : Connect to the VSS line which is the analog system

Downloaded from Elcodis.com electronic components distributor

<Note 3>
The comparator uses internal capacitors whose charge will be lost if the clock frequency is too low. Thus, make sure the following during an A-D conversion.
● f(XIN) is 500 kHz or more .
● Do not execute the STP instruction and WIT instruction.

3.1.4 Notes on the $\overline{\text{RESET}}$ pin

<Note>
n case where the RESET signal rise time is long, connect a ceramic capacitor or others across the $\overline{\text{RESET}}$ pin and the VSS pin. And use a 1000 pF or more capacitor for high frequency use. When connecting the capacitor, note the following :
●Make the length of the wiring which is connected to a capacitor.
●Be sure to check the operation of application products on the user side.

Reason
If the several nanosecond or several ten nanosecond impulse noise enters the $\overline{\text{RESET}}$ pin, it may cause a microcomputer failure.

3.1.5 Notes on input and output pins

<Note 1>
In stand-by state* for low-power dissipation, do not make input levels of an input and an I/O port "undefined," especially for the I/O ports of the P-channel and the N-channel open-drain.
Pull-up (connect the port to VCC) or pull-down (connect the port to VSS) these ports through a resistor.
When determining a resistance value, note the following points:
●External circuit
●Variation of output levels during the ordinary operation

When using built-in pull-up or pull-down resistor as an option, note on varied current values.
●When setting as an input port : Fix its input level
●When setting as an output port : Prevent current from flowing out to external

Reason
Even when setting as an output port with its direction register, in the following state :
●P-channel.....when the content of the data register (port latch) is "0"
●N-channel.....when the content of the data register (port latch) is "1"
the transistor becomes the OFF state, which causes the ports to be the high-impedance state. Note that the level becomes "undefined" depending on external circuits.
Accordingly, the potential which is input to the input buffer in a microcomputer is unstable in the state that input levels of an input and an I/O port are "undefined." This may cause power source current.

* stand-by state : the stop mode by executing the **STP** instruction
the wait mode by executing the **WIT** instruction

Eol announced

Downloaded from Elcodis.com electronic components distributor

<Note 2>
When the data register (port latch) of an I/O port is modified with the bit managing instruction*, the value of the unspecified bit may be changed.

Reason
The bit managing instructions are read-modify-write form instructions for reading and writing data by a byte unit. Accordingly, when these instructions are executed on a bit of the data register of an I/O port, the following is executed to all bits of the data register.
●As for a bit which is set to an input port : The pin state is read in the CPU, and is written to this bit after bit managing.
●As for a bit which is set to an output port : The bit value is read in the CPU, and is written to this bit after bit managing.

Note the following :
●Even when a port which is set as an output port is changed for an input port, its data register holds the output data.
●As for a bit of which is set to an input port , its value may be changed even when not specified with a bit managing instruction in case where the pin state differs from its data register contents

* bit managing instructions : **SEB** and **CLB** instruction

<Note 3>
When not using the A-D converter, connect the A-D converter power source AVSS pin as follows :
●AVSS : Connect to the VSS pin

Reason
If the AVSS pin is opened, the microcomputer may have a failure because of noise or others.

3.1.6 Notes on clock synchronous serial I/O

<Note>
When an external clock is used as the synchronous clock for data transmission, set the transmit enable bit to “1” at “H” of the SCLK input level. Also, write data to the transmit buffer register at “H” of the SCLK input level.

EOL announced

Downloaded from Elcodis.com electronic components distributor

3. APPENDIX

3.1.7 Notes on built-in PROM

(1) Programming adapter

To write into or read from data the internal PROM, use the dedicated programming adapter and general-purpose PROM programmer as shown in Table 3.1.1.

Table 3.1.1 Programming adapter

Microcomputer	Programming adapter
M38197EAFS	PCA4738L-100A
M38197EAFP (one-time blank)	PCA4738F-100A

(2) Write and read

In PROM mode, operation is the same as that of the M5M27C101, but programming conditions of PROM programmer are not set automatically because there are no built-in device ID codes.
Accurately set the following conditions for data write/read. Do not apply 21 V to the Vpp pin (is also used as port $P4_0$), or the product may be permanently damaged.

- Programming voltage : 12.5 V
- Setting of programming adapter switch : refer to "**Table 3.1.2**"
- Setting of PROM programmer address : refer to "**Table 3.1.3**"

Table 3.1.2 Setting of programming adapter switch

Programming adapter	SW 1	SW 2	SW 3
PCA4738L-100A	P-channel	OFF (CMOS)	OFF
PCA4738F-100A			

Table 3.1.3 Setting of PROM programmer address

Microcomputer	PROM programmer start address (Note)	PROM programmer completion address (Note)
M38197EAFS	Address : 6080_{16}	Address : $FFFD_{16}$
M38197EAFP		

Note : Because addresses 6000_{16} to $607F_{16}$ and $FFFE_{16}$ to $FFFF_{16}$ are the reserved ROM area, do not use these addresses.

(3) Erasing

Contents of the windowed EPROM (38197 EAFS) are erased by an ultraviolet light source with the wavelength 2537-Ångstrom . At least 15 W•sec/cm^2 are required to erase EPROM contents.

EOL announced

Downloaded from Elcodis.com electronic components distributor

3.2 Countermeasures against noise

Countermeasures against noise are described below. The following countermeasures are effective against noise in theory, however, it is necessary not only to take measures as follows but to evaluate before actual use.

3.2.1 Shortest wiring length

The wiring on a printed circuit board can be as an antenna which feeds noise into the microcomputer.
The shorter the total wiring length (by mm unit), the less the possibility of noise insertion into a microcomputer.

(1) Wiring for the $\overline{\text{RESET}}$ pin

Make the length of wiring which is connected to the $\overline{\text{RESET}}$ pin as short as possible. Especially, connect a capacitor across the $\overline{\text{RESET}}$ pin and the Vss pin with the shortest possible wiring (within 20mm).

Reason

The reset works to initialize a microcomputer.
The width of a pulse input into the $\overline{\text{RESET}}$ pin is determined by the timing necessary conditions. If noise having a shorter pulse width than the standard is input to the $\overline{\text{RESET}}$ pin, the reset is released before the internal state of the microcomputer is completely initialized. This may cause a program runaway.

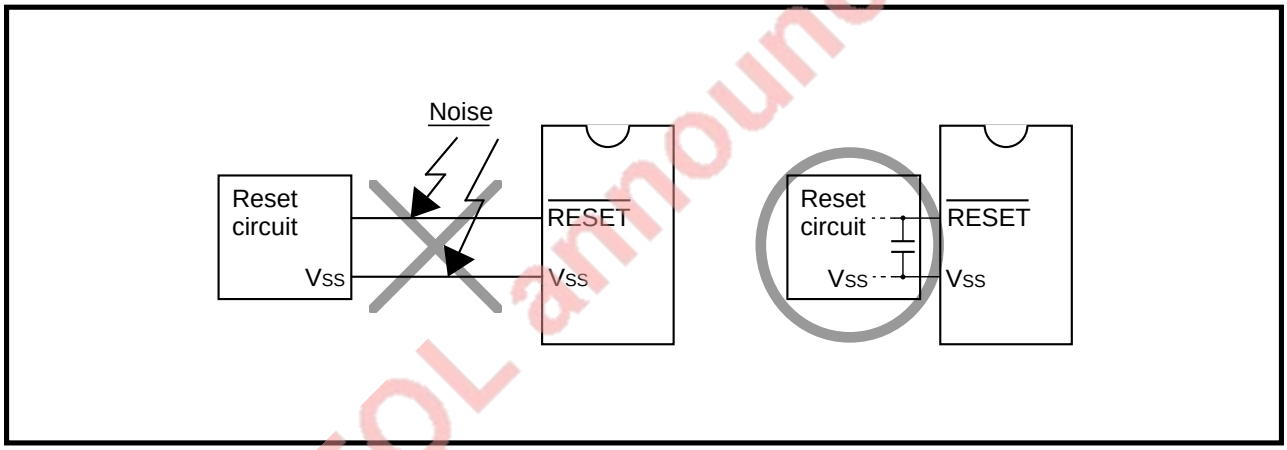


Fig. 3.2.1 Wiring for the $\overline{\text{RESET}}$ pin

(2) Wiring for clock input/output pins

- Make the length of wiring which is connected to clock I/O pins as short as possible.
- Make the length of wiring (within 20mm) across the grounding lead of a capacitor which is connected to an oscillator and the Vss pin of a microcomputer as short as possible.
- Separate the Vss pattern only for oscillation from other Vss patterns.

Reason

A microcomputer's operation synchronizes with a clock generated by the oscillator (circuit). If noise enters clock I/O pins, clock waveforms may be deformed. This may cause a program failure or program runaway.
Also, if a potential difference is caused by the noise between the Vss level of a microcomputer and the Vss level of an oscillator, the correct clock will not be input in the microcomputer.

EOL announced

Downloaded from Elcodis.com electronic components distributor

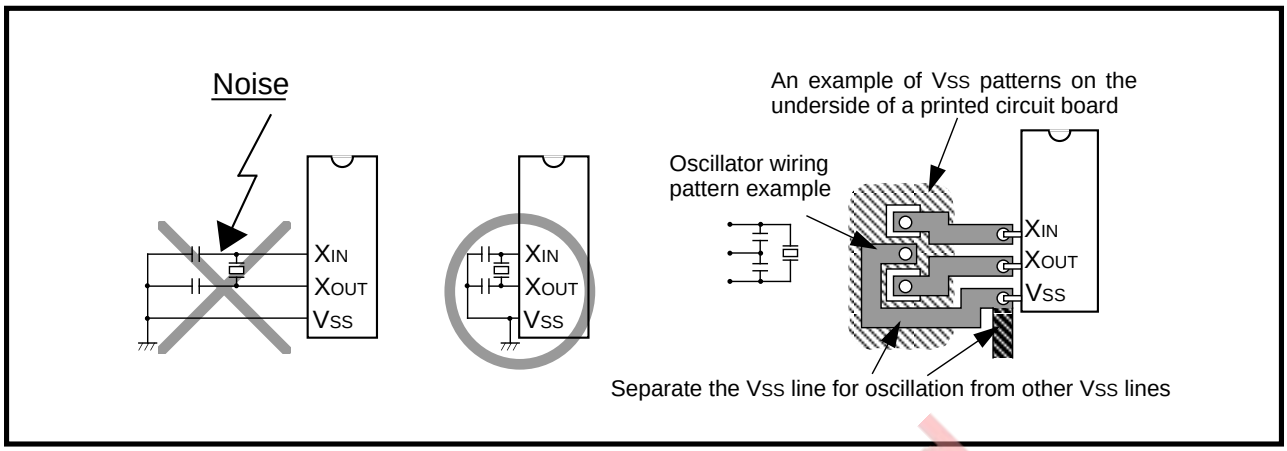


Fig. 3.2.2 Wiring for clock I/O pins

(3) Wiring for the VPP pin of the One Time PROM version and the eprom version

- Make the length of wiring which is connected to the VPP pin as short as possible.
- Connect an approximately 5 kΩ resistor to the VPP pin in serial.

Reason

The VPP pin of the One Time PROM and the EPROM version is the power source input pin for the built-in PROM. When programming in the built-in PROM, the impedance of the VPP pin is low to allow the electric current for wiring flow into the PROM. Because of this, noise can enter easily. If noise enters the VPP pin, abnormal in struction codes or data are read from the built-in PROM, which may cause a program runaway.

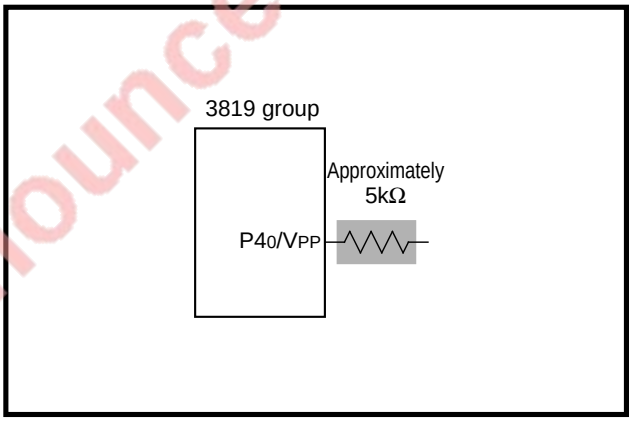


Fig. 3.2.3 Wiring for the VPP pin of the One Time PROM and the EPROM version

EOL announced

3.2.2 Connection of a bypass capacitor across the Vss line and the Vcc line

Connect an approximately 0.1 µF bypass capacitor across the VSS line and the VCC line as follows:

- Connect a bypass capacitor across the VSS pin and the VCC pin at equal length .
- Connect a bypass capacitor across the VSS pin and the VCC pin with the shortest possible wiring.
- Use lines with a larger diameter than other signal lines for VSS line and VCC line.

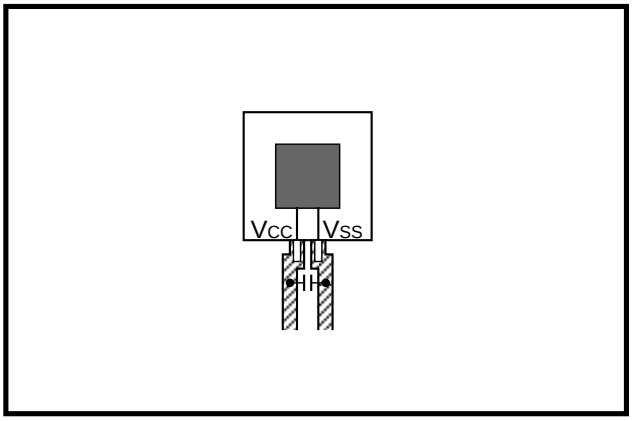


Fig. 3.2.4 Bypass capacitor across the VSS line and the VCC line

Downloaded from Elcodis.com electronic components distributor

3.2.3 Wiring to analog input pins

- Connect an approximately 100 Ω to 1 kΩ resistor to an analog signal line which is connected to an analog input pin in series. Besides, connect the resistor to the microcomputer as close as possible.
- Connect an approximately 1000 pF capacitor across the Vss pin and the analog input pin. Besides, connect the capacitor to the Vss pin as close as possible.

Reason

Signals which is input in an analog input pin (such as an A-D converter input pin) are usually output signals from sensor. The sensor which detects a change of event is installed far from the printed circuit board with a microcomputer, the wiring to an analog input pin is longer necessarily. This long wiring functions as an antenna which feeds noise into the microcomputer, which causes noise to an analog input pin.

If a capacitor between an analog input pin and the Vss pin is grounded at a position far away from the Vss pin, noise on the GND line may enter a microcomputer through the capacitor.

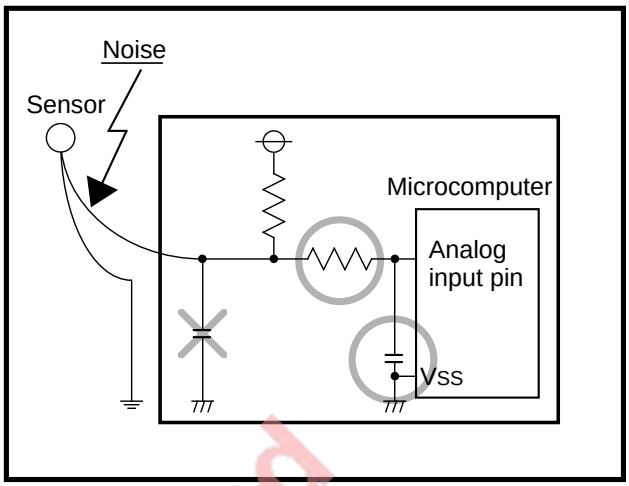


Fig.3.2.5 Analog signal line and a resistor and a capacitor

3.2.4. Oscillator concerns

Take care to prevent an oscillator that generates clocks for a microcomputer operation from being affected by other signals.

(1) Keeping an oscillator away from large current signal lines

Install a microcomputer (and especially an oscillator) as far as possible from signal lines where a current larger than the tolerance of current value flows.

Reason

In the system using a microcomputer, there are signal lines for controlling motors, LEDs, and thermal heads or others. When a large current flows through those signal lines, strong noise occurs because of mutual inductance.

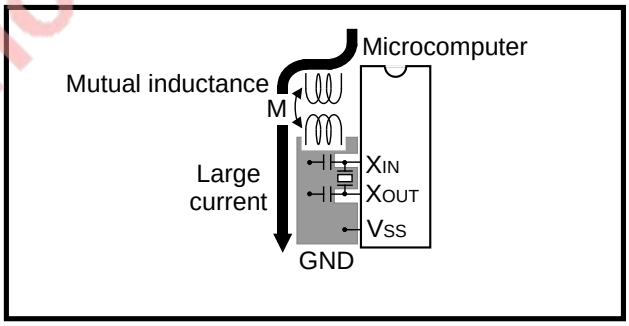


Fig.3.2.6 Wiring for a large current signal line

(2) Keeping an oscillator away from signal lines where potential levels change frequently

Install an oscillator away from signal lines where potential levels change frequently. Also, do not cross such signal lines over the clock lines or the signal lines which are sensitive to noise.

Reason

Signal lines where potential levels change frequently (such as the CNTR pin line) may affect other lines at signal rising or falling edge. If such lines cross over a clock line, clock waveforms may be deformed, which causes a microcomputer failure or a program runaway.

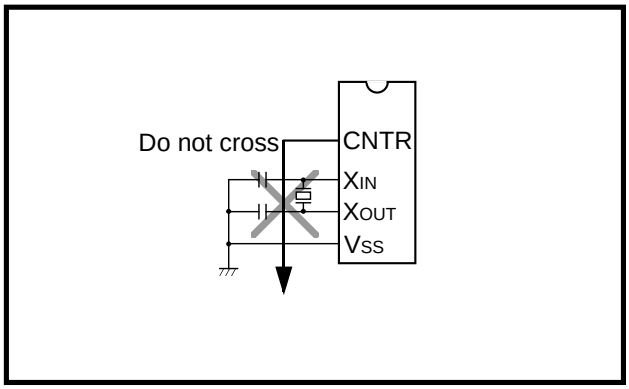


Fig.3.2.7 Wiring to a signal line where potential levels change frequently

Eol announced

Downloaded from Elcodis.com electronic components distributor

3.2.5 Setup for I/O ports

Setup I/O ports using hardware and software as follows:

<Hardware>

- Connect a resistor of 100 Ω or more to an I/O port in series.

<Software>

- As for an input port, read data several times by a program for checking whether input levels are equal or not.
- As for an output port, since the output data may reverse because of noise, rewrite data to its data register at fixed periods.
- Rewirte data to direction registers and pull-up control registers (only the product having it) at fixed periods.

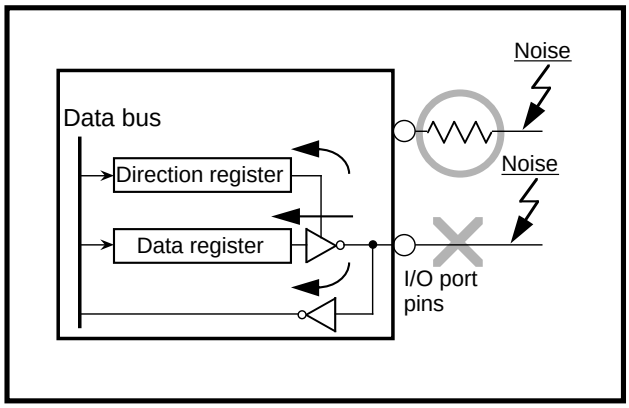


Fig. 3.2.8 Setup for I/O ports

When a direction register is set to input port again at fixed periods, a several-nanosecond short pulse may be output from this port. If this is undesirable, connect a capacitor to this port to remove the noise pulse.

3.2.6 Providing of watchdog timer function by software

If a microcomputer runs away because of noise or others, it can be detected by a software watchdog timer and the microcomputer can be reset to normal operation. This is equal to or more effective than program runaway detection by a hardware watchdog timer. The following shows an example of a watchdog timer provided by software.

In the following example, to reset a microcomputer to normal operation, the main routine detects errors of the interrupt processing routine and the interrupt processing routine detects errors of the main routine.

This example assumes that interrupt processing is repeated multiple times in a single main routine processing.

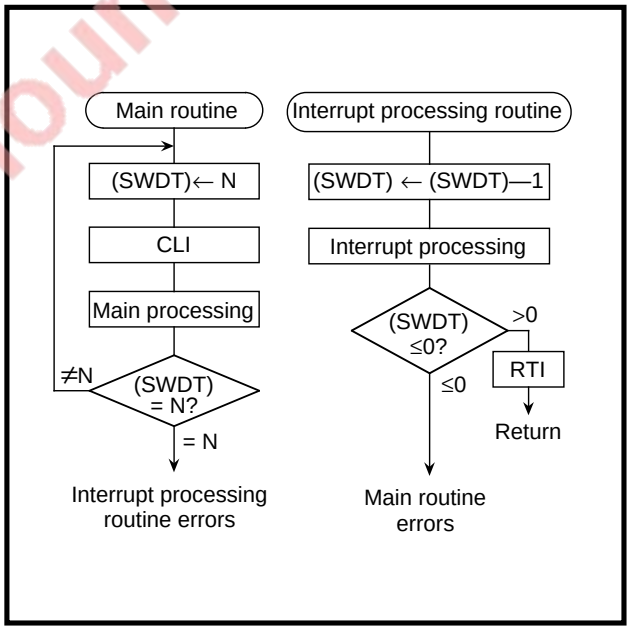


Fig. 3.2.9 Watchdog timer by software

EDL announced

<The main routine>

- Assigns a single byte of RAM to a software watchdog timer (SWDT) and writes the initial value N in the SWDT once at each execution of the main routine.
  The initial value N should satisfy the following condition:
  N+1 ≥ (Counts of interrupt processing executed in each main routine)

As the main routine execution cycle may change because of an interrupt processing or others, the initial value N should have a margin.

- Watches the operation of the interrupt processing routine by comparing the SWDT contents with counts of interrupt processing count after the initial value N has been set.
- Detects that the interrupt processing routine has failed and determines to branch to the program initialization routine for recovery processing in the following cases:
  ① If the SWDT contents do not change after interrupt processing
  ② If the changed SWDT contents are abnormal
  (In Figure 3.2.9, the main routine determines that the interrupt processing routine has failed only if the SWDT contents do not change).

Downloaded from Elcodis.com electronic components distributor

<The interrupt processing routine>
●Decrements the SWDT contents by 1 at each interrupt processing.
●Determins that the main routine operates normally when the SWDT contents are reset to the initial value N at almost fixed cycles (at the fixed interrupt processing count).
●Detects that the main routine has failed and determines to branch to the program initialization routine for recovery processing in the following case:
① If the SWDT contents are not initialized to the initial value N but continued to decrement and if they exceed the limit (and reach 0 or less).

EOL announced

Downloaded from Elcodis.com electronic components distributor

3.3 Control registers

Port Pi direction register

b7 b6 b5 b4 b3 b2 b1 b0

Port Pi direction register (PiD) (i = 4, 5, 6, 7, 8, A, B)
[Address:09 16, 0B16, 0D16, 0F16, 1116, 1516, 1716]

B	Name	Function	At reset	R	W
0	Port Pi direction register	0 : Port Pi_0 input mode 1 : Port Pi_0 output mode (**Note**)	0	×	○
1		0 : Port Pi_1 input mode 1 : Port Pi_1 output mode	0	×	○
2		0 : Port Pi_2 input mode 1 : Port Pi_2 output mode	0	×	○
3		0 : Port Pi_3 input mode 1 : Port Pi_3 output mode	0	×	○
4		0 : Port Pi_4 input mode 1 : Port Pi_4 output mode	0	×	○
5		0 : Port Pi_5 input mode 1 : Port Pi_5 output mode (**Note**)	0	×	○
6		0 : Port Pi_6 input mode 1 : Port Pi_6 output mode	0	×	○
7		0 : Port Pi_7 input mode 1 : Port Pi_7 output mode	0	×	○

Note : Port P4 direction register [Address:09 16]
Ports $P4_0$ and $P4_5$ are input ports. Accordingly, these bits do not have a direction register function.

Fig. 3.3.1 Structure of Port Pi direction register (i = 4, 5, 6, 7, 8, A, B)

Port P2 direction register

b7 b6 b5 b4 b3 b2 b1 b0

Port P2 direction register (P2D) [Address:0516]

B	Name	Function	At reset	R	W
0	Because $P2_0$ to $P2_3$ are output ports, these bits do not have a direction register function and nothing is allocated.		1	×	×
1			1	×	×
2			1	×	×
3			1	×	×
4	Port P2 direction register	0 : Port $P2_4$ input mode 1 : Port $P2_4$ output mode	0	×	○
5		0 : Port $P2_5$ input mode 1 : Port $P2_5$ output mode	0	×	○
6		0 : Port $P2_6$ input mode 1 : Port $P2_6$ output mode	0	×	○
7		0 : Port $P2_7$ input mode 1 : Port $P2_7$ output mode	0	×	○

Fig. 3.3.2 Structure of Port P2 direction register

EOL announced

Downloaded from Elcodis.com electronic components distributor

3. APPENDIX

Serial I/O automatic transfer data pointer

b7 b6 b5 b4 b3 b2 b1 b0

Serial I/O automatic transfer data pointer (SIODP) [Address:18$_{16}$]

B	Function	At reset	R	W
0	Indicate an address of Serial I/O automatic transfer RAM.	?	○	○
1		?	○	○
2		?	○	○
3		?	○	○
4		?	○	○
5	Nothing is allocated for these bits. These are write disabled bits. When these bits are read out, the values are "0."	0	○	×
6		0	○	×
7		0	○	×

Fig. 3.3.3 Structure of Serial I/O automatic transfer data pointer

Serial I/O 1 control register

b7 b6 b5 b4 b3 b2 b1 b0

Serial I/O 1 control register (SIO1CON) [Address:19$_{16}$]

B	Name	Function	At reset	R	W
0	Internal synchronous clock selection bits	b2 b1b0 000 : f(X$_{IN}$)/8 or f(X$_{CIN}$)/8 001 : f(X$_{IN}$)/16 or f(X$_{CIN}$)/16 010 : f(X$_{IN}$)/32 or f(X$_{CIN}$)/32 011 : f(X$_{IN}$)/64 or f(X$_{CIN}$)/64 110 : f(X$_{IN}$)/128 or f(X$_{CIN}$)/128 111 : f(X$_{IN}$)/256 or f(X$_{CIN}$)/256	0	○	○
1			0	○	○
2			0	○	○
3	Serial I/O 1 port selection bit (P6$_5$,P6$_6$,P6$_7$*)	0 : I/O port 1 : S$_{OUT1}$, S$_{CLK11}$, S$_{CLK12}$* signal pins	0	○	○
4	S$_{RDY1}$ output selection bit (P6$_7$)	0 : I/O port 1 : $\overline{S_{RDY1}}$/$\overline{CS}$* signal pin (**Note**)	0	○	○
5	Transfer direction selection bit	0 : LSB first 1 : MSB first	0	○	○
6	Synchronous clock selection bit	0 : External clock 1 : Internal clock	0	○	○
7	P6$_5$/S$_{OUT1}$ P-channel output disable bit	0 : CMOS output (in output mode) 1 : N-channel open-drain output (in output mode)	0	○	○

* Valid only in the Serial I/O automatic transfer mode

Note : When an external clock is selected in the serial I/O 1 automatic transfer mode, the $\overline{S_{RDY1}}$ signal pin is used as the $\overline{CS}$ signal input pin.

Fig. 3.3.4 Structure of Serial I/O 1 control register

EOL announced

Downloaded from Elcodis.com electronic components distributor

3. APPENDIX

Serial I/O automatic transfer control register

b7 b6 b5 b4 b3 b2 b1 b0

Serial I/O automatic transfer control register (SIOAC) [Address:1A16]

B	Name	Function	At reset	R	W
0	Automatic transfer control bit	0 : Serial I/O ordinary mode (serial I/O 1 interrupt) 1 : Automatic transfer mode (serial I/O automatic transfer interrupt)	0	○	○
1	Automatic transfer start bit	0 : Transfer completion 1 : Transferring (starts by writing "1")	0	○	○
2	Transfer mode switch bit	0 : Fullduplex (transmit / receive) mode 1 : Transmit-only mode	0	○	○
3	Synchronous clock output pin selection bit	0 : S_{CLK11} 1 : S_{CLK12}	0	○	○
4	Nothing is allocated for these bits. These are write disabled bits. When these bits are read out, the values are "0."		0	○	×
5			0	○	×
6			0	○	×
7			0	○	×

Fig. 3.3.5 Structure of Serial I/O automatic transfer control register

Serial I/O automatic transfer interval register

b7 b6 b5 b4 b3 b2 b1 b0

Serial I/O automatic transfer interval register (SIOAI) [Address:1C16]

B	Function	At reset	R	W
0	Ti = (n + 2) × Tc Ti = a length of transfer interval n = a setting value Tc = a length of a bit of transfer clock	0	○	○
1		0	○	○
2		0	○	○
3		0	○	○
4		0	○	○
5	Nothing is allocated for these bits. These are write disabled bits. When these bits are read out, the values are "0."	0	○	×
6		0	○	×
7		0	○	×

Fig. 3.3.6 Structure of Serial I/O automatic transfer interval register

EOL announced

Downloaded from Elcodis.com electronic components distributor

3. APPENDIX

Serial I/O 2 control register

b7	b6	b5	b4	b3	b2	b1	b0

Serial I/O 2 control register (SIO2CON) [Address:1D16]

B	Name	Function	At reset	R	W
0	Internal synchronous clock selection bits	b2 b1b0 000 : f(XIN)/8 or f(XCIN)/8 001 : f(XIN)/16 or f(XCIN)/16 010 : f(XIN)/32 or f(XCIN)/32 011 : f(XIN)/64 or f(XCIN)/64 110 : f(XIN)/128 or f(XCIN)/128 111 : f(XIN)/256 or f(XCIN)/256	0	○	○
1			0	○	○
2			0	○	○
3	Serial I/O 2 port selection bit (P51,P52)	0 : I/O port 1 : SOUT2, SCLK2 signal pins	0	○	○
4	SRDY2 output selection bit (P53)	0 : I/O port 1 : SRDY2 signal pin	0	○	○
5	Transfer direction selection bit	0 : LSB first 1 : MSB first	0	○	○
6	Synchronous clock selection bit	0 : External clock 1 : Internal clock	0	○	○
7	P51/SOUT2 P-channel output disable bit	0 : CMOS output (in output mode) 1 : N-channel open-drain output (in output mode)	0	○	○

Fig. 3.3.7 Structure of Serial I/O 2 control register

Serial I/O 3 control register

b7	b6	b5	b4	b3	b2	b1	b0

Serial I/O 3 control register (SIO3CON) [Address:1E16]

B	Name	Function	At reset	R	W
0	Internal synchronous clock selection bits	b2 b1b0 000 : f(XIN)/8 or f(XCIN)/8 001 : f(XIN)/16 or f(XCIN)/16 010 : f(XIN)/32 or f(XCIN)/32 011 : f(XIN)/64 or f(XCIN)/64 110 : f(XIN)/128 or f(XCIN)/128 111 : f(XIN)/256 or f(XCIN)/256	0	○	○
1			0	○	○
2			0	○	○
3	Serial I/O 3 port selection bit (P55,P56)	0 : I/O port 1 : SOUT3, SCLK3 signal pins	0	○	○
4	SRDY3 output selection bit (P57)	0 : I/O port 1 : SRDY3 signal pin	0	○	○
5	Transfer direction selection bit	0 : LSB first 1 : MSB first	0	○	○
6	Synchronous clock selection bit	0 : External clock 1 : Internal clock	0	○	○
7	P55/SOUT3 P-channel output disable bit	0 : CMOS output (in output mode) 1 : N-channel open-drain output (in output mode)	0	○	○

Fig. 3.3.8 Structure of Serial I/O 3 control register

EOL announced

Downloaded from Elcodis.com electronic components distributor

3. APPENDIX

Timer 12 mode register

b7 b6 b5 b4 b3 b2 b1 b0

Timer 12 mode register (T12M) [Address:28 16]

B	Name	Function	At reset	R	W
0	Timer 1 count stop bit	0 : Operating 1 : Stopped	0	○	○
1	Timer 2 count stop bit	0 : Operating 1 : Stopped	0	○	○
2	Timer 1 count source selection bit	0 : f(XIN)/16 or f(XCIN)/16 1 : f(XCIN)	0	○	○
3	Nothing is allocated for this bit. It is a write disabled bit. When this bit is read out, the value is "0. "		0	○	×
4	Timer 2 count source selection bits	b5 b4 00 : Timer 1 underflow 01 : f(XCIN) 10 : External count input CNTR 0 11 : Not available	0	○	○
5			0	○	○
6	Timer 1 output selection bit (P46)	0 : I/O port 1 : Timer 1 output	0	○	○
7	Nothing is allocated for this bit. It is a write disabled bit. When this bit is read out, the value is "0. "		0	○	×

Fig. 3.3.9 Structure of Timer 12 mode register

Timer 34 mode register

b7 b6 b5 b4 b3 b2 b1 b0

Timer 34 mode register (T34M) [Address:29 16]

B	Name	Function	At reset	R	W
0	Timer 3 count stop bit	0 : Operating 1 : Stopped	0	○	○
1	Timer 4 count stop bit	0 : Operating 1 : Stopped	0	○	○
2	Timer 3 count source selection bit	0 : f(XIN)/16 or f(XCIN)/16 1 : Timer 2 underflow	0	○	○
3	Nothing is allocated for this bit. It is a write disabled bit. When this bit is read out, the value is "0. "		0	○	×
4	Timer 4 count source selection bits	b5 b4 00 : f(XIN)/16 or f(XCIN)/16 01 : Timer 3 underflow 10 : External count input CNTR 1 11 : Not available	0	○	○
5			0	○	○
6	Timer 3 output selection bit (P47)	0 : I/O port 1 : Timer 3 output	0	○	○
7	Nothing is allocated for this bit. It is a write disabled bit. When this bit is read out, the value is "0. "		0	○	×

Fig. 3.3.10 Structure of Timer 34 mode register

EOL announced

Downloaded from Elcodis.com electronic components distributor

3. APPENDIX

Timer 56 mode register

b7	b6	b5	b4	b3	b2	b1	b0
0							

Timer 56 mode register (T56M) [Address:2A16]

B	Name	Function	At reset	R	W
0	Timer 5 count stop bit	0 : Operating 1 : Stopped	0	○	○
1	Timer 6 count stop bit	0 : Operating 1 : Stopped	0	○	○
2	Timer 5 count source selection bit	0 : f(XIN)/16 or f(XCIN)/16 1 : Timer 4 underflow	0	○	○
3	Timer 6 operation mode selection bit	0 : Timer mode 1 : PWM mode	0	○	○
4	Timer 6 count source selection bits	b5 b4 00 : f(XIN)/16 or f(XCIN)/16 01 : Timer 5 underflow 10 : Timer 4 underflow 11 : Not available	0	○	○
5			0	○	○
6	Timer 6 (PWM) output selection bit (P61)	0 : I/O port 1 : Timer 6 output	0	○	○
7	Fix this bit to "0."		0	○	○

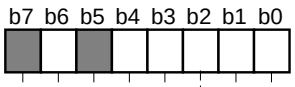
Fig. 3.3.11 Structure of Timer 56 mode register

EOL announced

Downloaded from Elcodis.com electronic components distributor

3. APPENDIX

AD/DA control register



AD/DA control register (ADCON) [Address:2C16]

B	Name	Function	At reset	R	W
0	Analog input pin selection bits	b3 b2 b1 b0 0 0 0 0 : P70/AN0 0 0 0 1 : P71/AN1 0 0 1 0 : P72/AN2 0 0 1 1 : P73/AN3 0 1 0 0 : P74/AN4 0 1 0 1 : P75/AN5 0 1 1 0 : P76/AN6 0 1 1 1 : P77/AN7 1 0 0 0 : P50/SIN2/AN8 1 0 0 1 : P51/SOUT2/AN9 1 0 1 0 : P52/SCLK2/AN10 1 0 1 1 : P53/SRDY2/AN11 1 1 0 0 : P54/SIN3/AN12 1 1 0 1 : P55/SOUT3/AN13 1 1 1 0 : P56/SCLK3/AN14 1 1 1 1 : P57/SRDY3/AN15	0	○	○
1			0	○	○
2			0	○	○
3			0	○	○
4	A-D conversion completion bit	0 : Conversion in progress 1 : Conversion completed	1	○	○
5	Nothing is allocated for this bit. This is a write disabled bit. When this bit is read out, the value is "0."		0	○	×
6	D-A output enable bit	0 : Disable 1 : Enable	0	○	○
7	Nothing is allocated for this bit. This is a write disabled bit. When this bit is read out, the value is "0."		0	○	×

Fig. 3.3.12 Structure of AD/DA control register

EOL announced

Downloaded from Elcodis.com electronic components distributor

Interrupt interval determination register

b7 b6 b5 b4 b3 b2 b1 b0

Interrupt interval determination register (IID) [Address:30$_{16}$]

B	Function	At reset	R	W
0	This register stores the values obtaind by counting the following interval with a counter sampling clock. • Falling edge interval • Rising edge interval • Both-sided edge interval (selected by the interrupt edge selection register) This register is read-only.	?	○	×
1		?	○	×
2		?	○	×
3		?	○	×
4		?	○	×
5		?	○	×
6		?	○	×
7		?	○	×

Note : When the noise filter sampling clock selection bits (bits 2 and 3) of the Interrupt interval determination control register (IIDCON) (Address: 31 $_{16}$) is set to "00" (when no noise filter is used), the both-sided edge detection function is not available.

Fig. 3.3.13 Structure of Interrupt interval determination register

Interrupt interval determination control register

b7 b6 b5 b4 b3 b2 b1 b0

Interrupt interval determination control register (IIDCON) [Address:31$_{16}$]

B	Name	Function	At reset	R	W
0	Interrupt interval determination circuit operating selection bit	0 : Stopped 1 : Operating	0	○	○
1	Counter sampling clock selection bit	0 : f(X$_{IN}$)/256 1 : f(X$_{IN}$)/512	0	○	○
2	Noise filter sampling clock selection bits (INT$_2$)	00 : Filter stop 01 : f(X$_{IN}$)/64 10 : f(X$_{IN}$)/128 11 : f(X$_{IN}$)/256	0	○	○
3			0	○	○
4	One-sided/both-sided edge detection selection bit	0 : One-sided edge detection 1 : Both-sided edge detection (Note)	0	○	○
5	Nothing is allocated for these bits. These are write disabled bits. When these bits are read out, the values are "0."		0	○	×
6			0	○	×
7			0	○	×

Note : When the noise filter sampling clock selection bits (bits 2 and 3) of the Interrupt interval determination control register (IIDCON) (Address: 31 $_{16}$) is set to "00" (when no noise filter is used), the both-sided edge detection function is not available.

Fig. 3.3.14 Structure of Interrupt interval determination control register

Now announced

Downloaded from Elcodis.com electronic components distributor

3. APPENDIX

Port P0 segment/digit switch register

b7 b6 b5 b4 b3 b2 b1 b0

Port P0 segment/digit switch register (P0SDR) [Address:32$_{16}$]

B	Name	Function	At reset	R	W
0	Port P0 segment/digit switch register	0 : DIG$_0$ 1 : SEG$_{32}$	0	○	○
1		0 : DIG$_1$ 1 : SEG$_{33}$	0	○	○
2		0 : DIG$_2$ 1 : SEG$_{34}$	0	○	○
3		0 : DIG$_3$ 1 : SEG$_{35}$	0	○	○
4		0 : DIG$_4$ 1 : SEG$_{36}$	0	○	○
5		0 : DIG$_5$ 1 : SEG$_{37}$	0	○	○
6		0 : DIG$_6$ 1 : SEG$_{38}$	0	○	○
7		0 : DIG$_7$ 1 : SEG$_{39}$	0	○	○

Fig. 3.3.15 Structure of Port P0 segment/digit switch register

Port P2 digit/port switch register

b7 b6 b5 b4 b3 b2 b1 b0

Port P2 digit/port switch register (P2DPR) [Address:33$_{16}$]

B	Name	Function	At reset	R	W
0	Port P2 digit/port switch register	0 : Port P2$_0$ output-only 1 : DIG$_{16}$	0	○	○
1		0 : Port P2$_1$ output-only 1 : DIG$_{17}$	0	○	○
2		0 : Port P2$_2$ output-only 1 : DIG$_{18}$	0	○	○
3		0 : Port P2$_3$ output-only 1 : DIG$_{19}$	0	○	○
4	Nothing is allocated for these bits. These are write disabled bits. When these bits are read out, the values are "0."		0	○	×
5			0	○	×
6			0	○	×
7			0	○	×

Fig. 3.3.16 Structure of Port P2 digit/port switch register

EOL announced

Downloaded from Elcodis.com electronic components distributor

3. APPENDIX

Port P8 segment/port switch register

b7 b6 b5 b4 b3 b2 b1 b0

Port P8 segment/port switch register (P8SPR) [Address:34 16]

B	Name	Function	At reset	R	W
0	Port P8 segment/port switch register	0 : Port $P8_0$ for I/O 1 : SEG_8	0	○	○
1		0 : Port $P8_1$ for I/O 1 : SEG_9	0	○	○
2		0 : Port $P8_2$ for I/O 1 : SEG_{10}	0	○	○
3		0 : Port $P8_3$ for I/O 1 : SEG_{11}	0	○	○
4		0 : Port $P8_4$ for I/O 1 : SEG_{12}	0	○	○
5		0 : Port $P8_5$ for I/O 1 : SEG_{13}	0	○	○
6		0 : Port $P8_6$ for I/O 1 : SEG_{14}	0	○	○
7		0 : Port $P8_7$ for I/O 1 : SEG_{15}	0	○	○

Fig. 3.3.17 Structure of Port P8 segment/port switch register

Port PA segment/port switch register

b7 b6 b5 b4 b3 b2 b1 b0

Port PA segment/port switch register (PASPR) [Address:35 16]

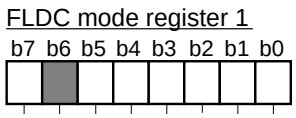
B	Name	Function	At reset	R	W
0	Port PA segment/port switch register	0 : Port PA_0 for I/O 1 : SEG_0	0	○	○
1		0 : Port PA_1 for I/O 1 : SEG_1	0	○	○
2		0 : Port PA_2 for I/O 1 : SEG_2	0	○	○
3		0 : Port PA_3 for I/O 1 : SEG_3	0	○	○
4		0 : Port PA_4 for I/O 1 : SEG_4	0	○	○
5		0 : Port PA_5 for I/O 1 : SEG_5	0	○	○
6		0 : Port PA_6 for I/O 1 : SEG_6	0	○	○
7		0 : Port PA_7 for I/O 1 : SEG_7	0	○	○

Fig. 3.3.18 Structure of Port PA segment/port switch register

EOL announced

Downloaded from Elcodis.com electronic components distributor

3. APPENDIX



FLDC mode register 1 (FLDM1) [Address:36_{16}]

B	Name	Function	At reset	R	W
0	Tscan control bits	b1b0 0 0 : FLD digit interrupt (at rising edge of each digit) 0 1 : 1 × Tdisp 1 0 : 2 × Tdisp 1 1 : 3 × Tdisp } FLD blanking interrupt (at falling edge of the last digit)	0	○	○
1			0	○	○
2	Toff control bit (Setting of digit/segment OFF time)	b5 b4 b3 b2 0 0 0 0 : 1/16 × Tdisp 0 0 0 1 : 2/16 × Tdisp 0 0 1 0 : 3/16 × Tdisp 0 0 1 1 : 4/16 × Tdisp 0 1 0 0 : 5/16 × Tdisp 0 1 0 1 : 6/16 × Tdisp 0 1 1 0 : 7/16 × Tdisp 0 1 1 1 : 8/16 × Tdisp 1 0 0 0 : 9/16 × Tdisp 1 0 0 1 : 10/16 × Tdisp 1 0 1 0 : 11/16 × Tdisp 1 0 1 1 : 12/16 × Tdisp 1 1 0 0 : 13/16 × Tdisp 1 1 0 1 : 14/16 × Tdisp 1 1 1 0 : 15/16 × Tdisp 1 1 1 1 : 16/16 × Tdisp	0	○	○
3			0	○	○
4			0	○	○
5			0	○	○
6	Nothing is allocated for this bit. This is a write disabled bit. When this bit is read out, the value is "0."		0	○	×
7	High-breakdown-voltage drivability selection bit	0 : Strong drivability 1 : Weak drivability	0	○	○

Fig. 3.3.19 Structure of FLDC mode register 1

EOL Technology

Downloaded from Elcodis.com electronic components distributor

FLDC mode register 2

b7 b6 b5 b4 b3 b2 b1 b0

FLDC mode register 2 (FLDM2) [Address:37$_{16}$]

B	Name	Function	At reset	R	W
0	Automatic display control bit (P0,P1,P2$_0$–P2$_3$,P3,P8,P9,PA)	0 : Ordinary mode 1 : Automatic display mode	0	○	○
1	Display start bit	0 : Display stopped 1 : Display in progress (display starts by writing "1" to this bit which is set to "0".)	0	○	○
2	Tdisp control bits (digit time setting) (at 8 MHz oscillation frequency)	b5 b4 b3 b2 0 0 0 0 : 128 µs 0 0 0 1 : 256 µs 0 0 1 0 : 384 µs 0 0 1 1 : 512 µs 0 1 0 0 : 640 µs 0 1 0 1 : 768 µs 0 1 1 0 : 896 µs 0 1 1 1 : 1024 µs 1 0 0 0 : 1152 µs 1 0 0 1 : 1280 µs 1 0 1 0 ⋮ 1 1 1 1 } Not available	0	○	○
3			0	○	○
4			0	○	○
5			0	○	○
6	P1$_0$ segment/digit switch bit	0 : Digit (DIG$_8$) 1 : Segment (SEG$_{40}$)	0	○	○
7	P1$_1$ segment/digit switch bit	0 : Digit (DIG$_9$) 1 : Segment (SEG$_{41}$)	0	○	○

EOL announced

Fig. 3.3.20 Structure of FLDC mode register 2

Downloaded from Elcodis.com electronic components distributor

3. APPENDIX

FLD data pointer

b7 b6 b5 b4 b3 b2 b1 b0

FLD data pointer (FLDDP) [Address:38$_{16}$]

B	Function	At reset	R	W
0	Indicate the address of data which is transfered to the segment of the FLD automatic display RAM.	?	○	×
1		?	○	×
2		?	○	×
3		?	○	×
4		?	○	×
5		?	○	×
6		?	○	×
7	Nothing is allocated for this bit. This is a write disabled bit. When this bit is read out, the value is "0."	0	○	×

Fig. 3.3.21 Structure of FLD data pointer

FLD data pointer reload register

b7 b6 b5 b4 b3 b2 b1 b0

FLD data pointer reload register (FLDDP) [Address:38$_{16}$]

B	Function	At reset	R	W
0	Indicate the first digit address of the high-order segment.	?	×	○
1		?	×	○
2		?	×	○
3		?	×	○
4		?	×	○
5		?	×	○
6		?	×	○
7	Nothing is allocated for this bit. This is a write disabled bit.	?	×	×

Fig. 3.3.22 Structure of FLD data pointer reload register

EOL announced

Downloaded from Elcodis.com electronic components distributor

3. APPENDIX

Zero cross detection control register

b7 b6 b5 b4 b3 b2 b1 b0

Zero cross detection control register (ZCRCON) [Address:39$_{16}$]

B	Name	Function	At reset	R	W
0	Zero cross detection ON/OFF selection bit	0 : Without passing through zero cross detection comparator 1 : Passing through zero cross detection comparator	0	○	○
1	Nothing is allocated for this bit. It is a write disabled bit. When this bit is read out, the value is "0."		0	○	×
2	Noise filter sampling clock selection bits (INT$_1$)	b3 b2 00 : Note use noise filter 01 : f(X$_{IN}$)/64 or f(X$_{CIN}$)/64 10 : f(X$_{IN}$)/128 or f(X$_{CIN}$)/128 11 : f(X$_{IN}$)/256 or f(X$_{CIN}$)/256	0	○	○
3			0	○	○
4	One-sided/both-sided edge detection selection bit	0 : One-sided edge detection 1 : Both-sided edges detection (**Note**)	0	○	○
5	Nothing is allocated for these bits. These are write disabled bits. When these bits are read out, the values are "0."		0	○	×
6				○	×
7	Zero cross detection circuit input bit (read-only)	0 : Less than 0 V 1 : 0 V or more	0	○	×

Note : When the noise filter sampling clock selection bits (bits 2 and 3) of the Zero cross detection control register (ZCRCON) (Address: 39 $_{16}$) is set to “00” (when no noise filter is used), the both-sided edge detection function is not available.

Fig. 3.3.23 Structure of Zero cross detection control register

Interrupt edge selection register

b7 b6 b5 b4 b3 b2 b1 b0

Interrupt edge selecton reigster (INTEDGE) [Address:3A$_{16}$]

b	Name	Function	At reset	R	W
0	INT$_0$ interrupt edge selection bit	0 : Falling edge active 1 : Rising edge active	0	○	○
1	INT$_1$/ZCR interrupt edge selection bit	0 : Falling edge active 1 : Rising edge active	0	○	○
2	INT$_2$ interrupt edge selection bit	0 : Falling edge active 1 : Rising edge active	0	○	○
3	INT$_3$ interrupt edge selection bit	0 : Falling edge active 1 : Rising edge active	0	○	○
4	INT$_4$ interrupt edge selection bit	0 : Falling edge active 1 : Rising edge active	0	○	○
5	INT$_4$/A-D conversion interrupt switch bit	0 : INT$_4$ interrupt 1 : A-D conversion interrupt	0	○	○
6	CNTR$_0$ pin active edge switch bit	0 : Falling edge active 1 : Rising edge active	0	○	○
7	CNTR$_1$ pin active edge switch bit	0 : Falling edge active 1 : Rising edge active	0	○	○

Fig. 3.3.24 Structure of Interrupt edge selection register

EOL announced

Downloaded from Elcodis.com electronic components distributor

3. APPENDIX

CPU mode register

b7 b6 b5 b4 b3 b2 b1 b0

CPU mode register (CPUM) [Address:3B16]

B	Name	Function	At reset	R	W
0	Processor mode bits	b1b0 0 0 : Single-chip mode 0 1 : 1 0 : } Not available 1 1 :	0	○	○
1			0	○	○
2	Stack page selection bit	0 : 0 page 1 : 1 page	0	○	○
3	XCOUT drivability selection bit	0 : Low 1 : High	1	○	○
4	Port Xc switch bit	0 : I/O port function 1 : XCIN–XCOUT oscillating function	0	○	○
5	Main clock (XIN-XOUT) stop bit	0 : Operating 1 : Stopped	0	○	○
6	Main clock division ratio selection bit	0 : f(XIN)/2 (high-speed mode) 1 : f(XIN)/8 (middle-speed mode)	1	○	○
7	Internal system clock selection bit	0 : XIN-XOUT selected (middle/high-speed mode) 1 : XCIN-XCOUT selected (low-speed mode)	0	○	○

Fig. 3.3.25 Structure of CPU mode register

Interrupt request register 1

b7 b6 b5 b4 b3 b2 b1 b0

Interrupt request reigster 1 (IREQ1) [Address:3C16]

B	Name	Function	At reset	R	W
0	INT0 interrupt request bit	0 : No interrupt request 1 : Interrupt request	0	○	*
1	INT1/ZCR interrupt request bit	0 : No interrupt request 1 : Interrupt request	0	○	*
2	• INT2 interrupt request bit • Remote control/counter overflow interrupt request bit	0 : No interrupt request 1 : Interrupt request	0	○	*
3	• Serial I/O 1 interrupt request bit • Serial I/O automatic transfer interrupt request bit	0 : No interrupt request 1 : Interrupt request	0	○	*
4	Serial I/O 2 interrupt request bit	0 : No interrupt request 1 : Interrupt request	0	○	*
5	Serial I/O 3 interrupt request bit	0 : No interrupt request 1 : Interrupt request	0	○	*
6	Timer 1 interrupt request bit	0 : No interrupt request 1 : Interrupt request	0	○	*
7	Timer 2 interrupt request bit	0 : No interrupt request 1 : Interrupt request	0	○	*

* "0" is set by software, but not "1."

Fig. 3.3.26 Structure of Interrupt request register 1

EOL announced

Downloaded from Elcodis.com electronic components distributor

3. APPENDIX

Interrupt request register 2

b7 b6 b5 b4 b3 b2 b1 b0

Interrupt request reigster 2 (IREQ2) [Address:3D16]

b	Name	Function	At reset	R	W
0	Timer 3 interrupt request bit	0 : No interrupt request 1 : Interrupt request	0	○	*
1	Timer 4 interrupt request bit	0 : No interrupt request 1 : Interrupt request	0	○	*
2	Timer 5 interrupt request bit	0 : No interrupt request 1 : Interrupt request	0	○	*
3	Timer 6 interrupt request bit	0 : No interrupt request 1 : Interrupt request	0	○	*
4	INT_3 interrupt request bit	0 : No interrupt request 1 : Interrupt request	0	○	*
5	• INT_4 interrupt request bit • A-D conversion interrupt request bit	0 : No interrupt request 1 : Interrupt request	0	○	*
6	• FLD blanking interrupt request bit • FLD digit interrupt request bit	0 : No interrupt request 1 : Interrupt request	0	○	*
7	Nothing is allocated for this bit. This is a write disabled bit. When this bit is read out, the value is "0."		0	○	*

* "0" is set by software, but not "1."

Fig. 3.3.27 Structure of Interrupt request register 2

Interrupt control register 1

b7 b6 b5 b4 b3 b2 b1 b0

Interrupt control register 1 (ICON1) [Address:3E16]

B	Name	Function	At reset	R	W
0	INT_0 interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	○	○
1	INT_1/ZCR interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	○	○
2	• INT_2 interrupt enable bit • Remote control/counter overflow interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	○	○
3	• Serial I/O 1 interrupt enable bit • Serial I/O automatic transfer interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	○	○
4	Serial I/O 2 interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	○	○
5	Serial I/O 3 interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	○	○
6	Timer 1 interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	○	○
7	Timer 2 interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	○	○

Fig. 3.3.28 Structure of Interrupt control register 1

EOL announced

Downloaded from Elcodis.com electronic components distributor

3. APPENDIX

Interrupt control register 2

b7	b6	b5	b4	b3	b2	b1	b0
0							

Interrupt control reigster 2 (ICON2) [Address:3F16]

b	Name	Function	At reset	R	W
0	Timer 3 interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	○	○
1	Timer 4 interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	○	○
2	Timer 5 interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	○	○
3	Timer 6 interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	○	○
4	INT_3 interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	○	○
5	• INT_4 interrupt enable bit • A-D conversion interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	○	○
6	• FLD blanking interrupt enable bit • FLD digit interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	○	○
7	Fix this bit to "0."		0	○	○

Fig. 3.3.29 Structure of Interrupt control register 2

EOL announced

Downloaded from Elcodis.com electronic components distributor

3.4 Mask ROM ordering method

GZZ–SH07–32B <33B0 >

Mask ROM number	

740 FAMILY MASK ROM CONFIRMATION FORM
SINGLE-CHIP MICROCOMPUTER M38197MA-XXXFP
MITSUBISHI ELECTRIC

Receipt	Date :	
	Section head signature	Supervisor signature

Note : Please fill in all items marked ✻.

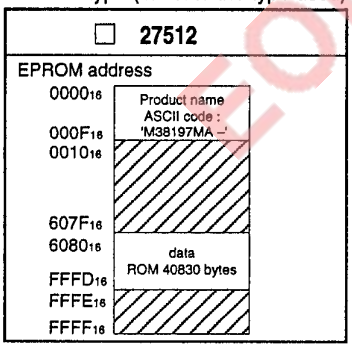
✻	Customer	Company name	TEL ( )	Issuance signature	Submitted by	Supervisor
		Date issued	Date :			

✻ 1. Confirmation
Specify the name of the product being ordered and the type of EPROMs submitted.
Three EPROMs are required for each pattern.
If at least two of the three sets of EPROMs submitted contain identical data, we will produce masks based on this data. We shall assume the responsibility for errors only if the mask ROM data on the products we produce differs from this data. Thus, extreme care must be taken to verify the data in the submitted EPROMs.

Checksum code for entire EPROM | | | | | (hexadecimal notation)

EPROM type (indicate the type used)

☐ 27512



In the address space of the microcomputer, the internal ROM area is from address 6080₁₆ to FFFD₁₆. The reset vector is stored in addresses FFFC₁₆ and FFFD₁₆.

(1) Set the data in the unused area (the shaded area of the diagram) to "FF₁₆".
(2) The ASCII codes of the product name "M38197 MA–" must be entered in addresses 0000₁₆ to 0008₁₆. And set the data "FF₁₆" in addresses 0009₁₆ to 000F₁₆.
The ASCII codes and addresses are listed to the right in hexadecimal notation.

Address		Address	
0000₁₆	'M' = 4D ₁₆	0008₁₆	'–' = 2D ₁₆
0001₁₆	'3' = 33 ₁₆	0009₁₆	FF ₁₆
0002₁₆	'8' = 38 ₁₆	000A₁₆	FF ₁₆
0003₁₆	'1' = 31 ₁₆	000B₁₆	FF ₁₆
0004₁₆	'9' = 39 ₁₆	000C₁₆	FF ₁₆
0005₁₆	'7' = 37 ₁₆	000D₁₆	FF ₁₆
0006₁₆	'M' = 4D ₁₆	000E₁₆	FF ₁₆
0007₁₆	'A' = 41 ₁₆	000F₁₆	FF ₁₆

EOL announced

Downloaded from Elcodis.com electronic components distributor

GZZ–SH07–32B <33B0 >

Mask ROM number	

740 FAMILY MASK ROM CONFIRMATION FORM
SINGLE-CHIP MICROCOMPUTER M38197MA-XXXFP
MITSUBISHI ELECTRIC

We recommend the use of the following pseudo-command to set the start address of the assembler source program.

EPROM type	27512
The pseudo-command	*=△$0000 .BYTE△'M38197MA–'

Note : If the name of the product written to the EPROMs does not match the name of the mask confirmation form, the ROM will not be processed.

❋ 2. Mark specification
Mark specification must be submitted using the correct form for the package being ordered. Fill out the appropriate mark specification form (100P6S for M38197MA-XXXFP) and attach it to the mask ROM confirmation form.

❋ 3. Usage conditions
Please answer the following questions about usage for use in our product inspection :
(1) How will you use the XIN-XOUT oscillator?

☐ Ceramic resonator ☐ Quartz crystal
☐ External clock input ☐ Other ( )

At what frequency? f(XIN) = ☐ MHz

(2) In which operation mode will you use your microcomputer ?

☐ Single-chip mode ☐ Memory expansion mode
☐ Microprocessor mode

❋ 4. Comments

EOL announced

Downloaded from Elcodis.com electronic components distributor

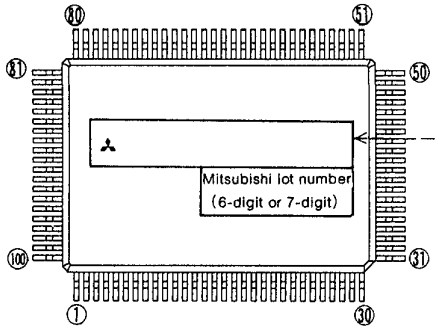
3.5 Mark specification form

100P6S (100-PIN QFP) MARK SPECIFICATION FORM

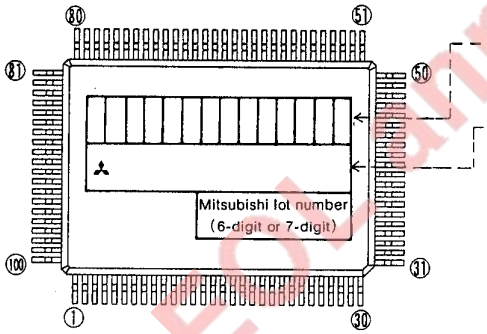
Mitsubishi IC catalog name

Please choose one of the marking types below (A, B, C), and enter the Mitsubishi IC catalog name and the special mark (if needed).

A. Standard Mitsubishi Mark



B. Customer's Parts Number + Mitsubishi Catalog Name



Note1 : The mark field should be written right aligned.
2. : The fonts and size of characters are standard Mitsubishi type.

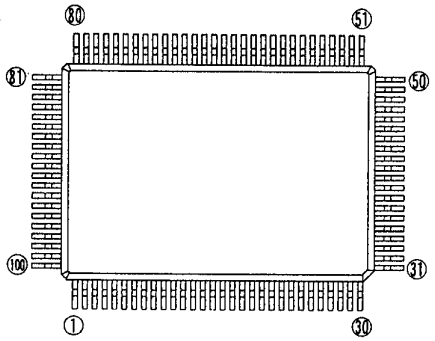
Note : The fonts and size of characters are standard Mitsubishi type.

Note3 : Customer's parts number can be up to 14 characters :
Only 0~9, A~Z, +, −, /, (,), &, ©, . (period), and , (comma) are usable.

4 : If the Mitsubishi logo is not required, check the box below.

Mitsubishi logo is not required ☐

C. Special Mark Required



Note1 : If the special mark is to be printed, indicate the desired layout of the mark in the left figure. The layout will be duplicated as close as possible. Mitsubishi lot number (6-digit or 7-digit) and mask ROM number (3-digit) are always marked.

2 : If the customer's trade mark logo must be used in the special mark, check the box below. Please submit a clean original of the logo. For the new special character fonts a clean font original (ideally logo drawing) must be submitted.

Special logo required ☐

The standard Mitsubishi font is used for all characters except for a logo.

Announced

Downloaded from Elcodis.com electronic components distributor

3. APPENDIX

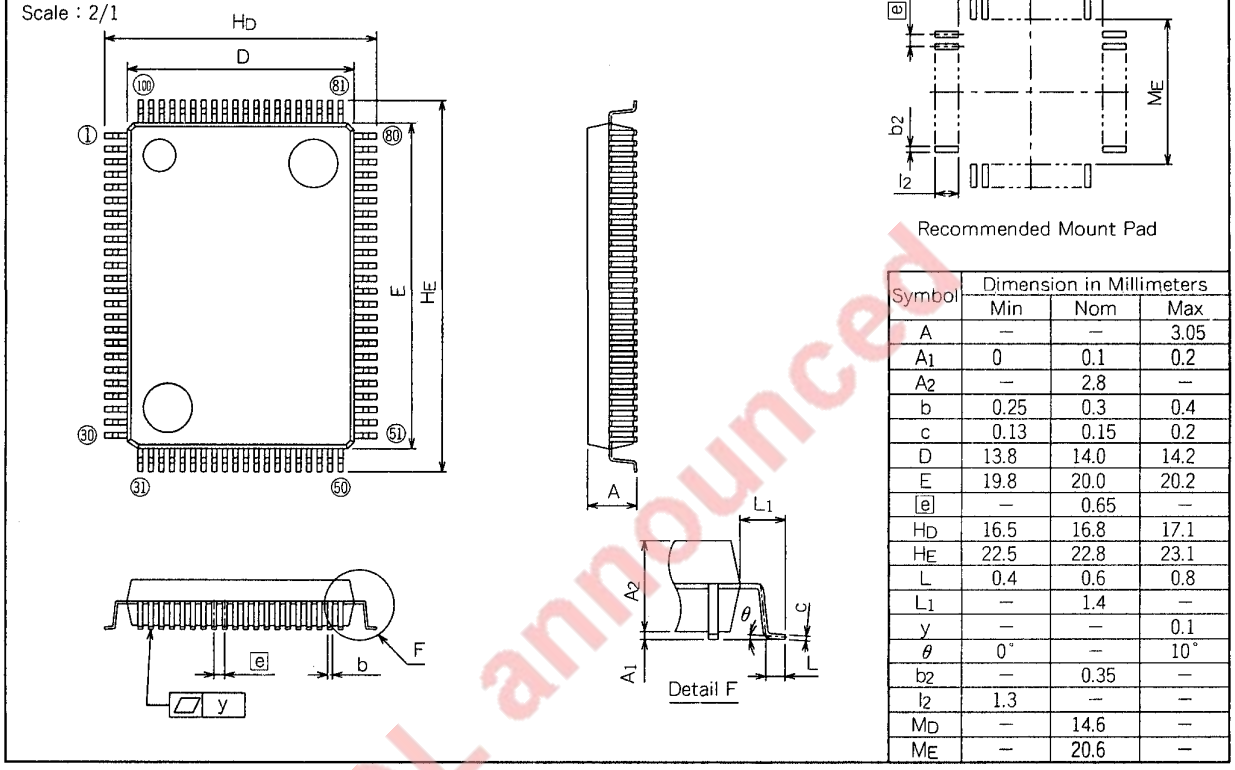
3.6 Package outline

100P6S−A

Plastic 100pin 14×20mm body QFP

EIAJ Package Code	JEDEC Code	Weight(g)
*QFP100-P-1420	—	1.58

Scale : 2/1



Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	—	—	3.05
A_1	0	0.1	0.2
A_2	—	2.8	—
b	0.25	0.3	0.4
c	0.13	0.15	0.2
D	13.8	14.0	14.2
E	19.8	20.0	20.2
e	—	0.65	—
H_D	16.5	16.8	17.1
H_E	22.5	22.8	23.1
L	0.4	0.6	0.8
L_1	—	1.4	—
y	—	—	0.1
θ	0°	—	10°
b_2	—	0.35	—
l_2	1.3	—	—
M_D	—	14.6	—
M_E	—	20.6	—

EOL announced

Downloaded from Elcodis.com electronic components distributor

3.7 Memory map

0000₁₆	Port P0 (P0)
0001₁₆	
0002₁₆	Port P1 (P1)
0003₁₆	
0004₁₆	Port P2 (P2)
0005₁₆	Port P2 direction register (P2D)
0006₁₆	Port P3 (P3)
0007₁₆	
0008₁₆	Port P4 (P4)
0009₁₆	Port P4 direction register (P4D)
000A₁₆	Port P5 (P5)
000B₁₆	Port P5 direction register (P5D)
000C₁₆	Port P6 (P6)
000D₁₆	Port P6 direction register (P6D)
000E₁₆	Port P7 (P7)
000F₁₆	Port P7 direction register (P7D)
0010₁₆	Port P8 (P8)
0011₁₆	Port P8 direction register (P8D)
0012₁₆	Port P9 (P9)
0013₁₆	
0014₁₆	Port PA (PA)
0015₁₆	Port PA direction register (PAD)
0016₁₆	Port PB (PB)
0017₁₆	Port PB direction register (PBD)
0018₁₆	Serial I/O automatic transfer data pointer (SIODP)
0019₁₆	Serial I/O1 control register (SIO1CON)
001A₁₆	Serial I/O automatic transfer control register (SIOAC)
001B₁₆	Serial I/O1 register (SIO1)
001C₁₆	Serial I/O automatic transfer interval register (SIOAI)
001D₁₆	Serial I/O2 control register (SIO2CON)
001E₁₆	Serial I/O3 control register (SIO3CON)
001F₁₆	Serial I/O2 register (SIO2)

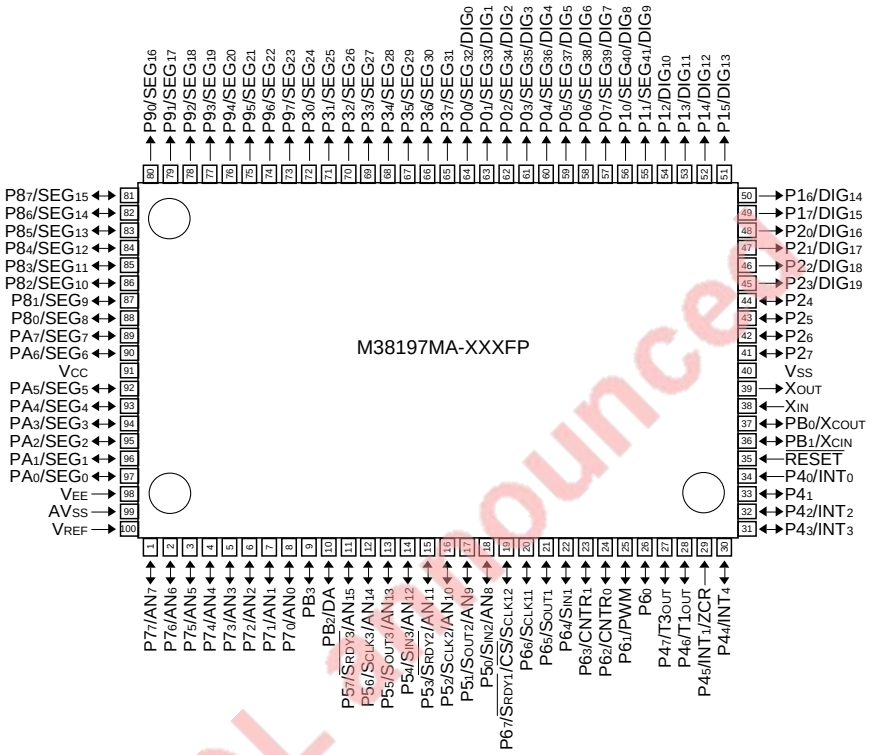
0020₁₆	Timer 1 (T1)
0021₁₆	Timer 2 (T2)
0022₁₆	Timer 3 (T3)
0023₁₆	Timer 4 (T4)
0024₁₆	Timer 5 (T5)
0025₁₆	Timer 6 (T6)
0026₁₆	Serial I/O3 register (SIO3)
0027₁₆	Timer 6 PWM register (T6PWM)
0028₁₆	Timer 12 mode register (T12M)
0029₁₆	Timer 34 mode register (T34M)
002A₁₆	Timer 56 mode register (T56M)
002B₁₆	D-A conversion register (DA)
002C₁₆	AD-DA control register (ADCON)
002D₁₆	A-D conversion register (AD)
002E₁₆	
002F₁₆	
0030₁₆	Interrupt interval determination register (IID)
0031₁₆	Interrupt interval determination control register (IIDCON)
0032₁₆	Port P0 segment/digit switch register (P0SDR)
0033₁₆	Port P2 digit/port switch register (P2DPR)
0034₁₆	Port P8 segment/port switch register (P8SPR)
0035₁₆	Port PA segment/port switch register (PASPR)
0036₁₆	FLDC mode register 1 (FLDM1)
0037₁₆	FLDC mode register 2 (FLDM2)
0038₁₆	FLD data pointer (FLDDP)
0039₁₆	Zero cross detection control register (ZCRCON)
003A₁₆	Interrupt edge selection register (INTEDGE)
003B₁₆	CPU mode register (CPUM)
003C₁₆	Interrupt request register 1 (IREQ1)
003D₁₆	Interrupt request register 2 (IREQ2)
003E₁₆	Interrupt control register 1 (ICON1)
003F₁₆	Interrupt control register 2 (ICON2)

EOL announced

Downloaded from Elcodis.com electronic components distributor

3. APPENDIX

3.8 Pin configuration



Package type : 100P6S-A
100-pin plastic-molded QFP

EOL announced

Downloaded from Elcodis.com electronic components distributor

EOL announced

MITSUBISHI SEMICONDUCTORS
USER'S MANUAL
3819 Group

Mar. First Edition 1995

Editioned by
Committee of editing of Mitsubishi Semiconductor USER'S MANUAL

Published by
Mitsubishi Electric Corp., Semiconductor Marketing Division

This book, or parts thereof, may not be reproduced in any form without permission of Mitsubishi Electric Corporation.
©1998 MITSUBISHI ELECTRIC CORPORATION

Downloaded from Elcodis.com electronic components distributor

User's Manual
3819 Group

EOL announced

Renesas Technology Corp.
Nippon Bldg.,6-2,Otemachi 2-chome,Chiyoda-ku,Tokyo,100-0004 Japan

H-ED346-A KI-9503 Printed in Japan (ROD)
© 1995 MITSUBISHI ELECTRIC CORPORATION.
New publication, effective Mar. 1995.
Specifications subject to change without notice.

Downloaded from Elcodis.com electronic components distributor

REVISION DESCRIPTION LIST	3819 Group User's Manual

Rev. No.	Revision Description	Rev. date
1.0	First Edition	980216

EOL announced

Downloaded from Elcodis.com electronic components distributor