20-OUTPUT LVTTL CLOCK DRIVERS SC3306/08

FEATURES

- **20 clock outputs:**
  - Ten or twenty outputs (SC3308) at primary frequency, up to 80 MHz
  - Ten outputs at 1/2 primary frequency (SC3306)
- **All outputs are leading edge synchronized to within ≤0.5 ns**
- **Proprietary output drivers with:**
  - Complementary 24 mA peak outputs, source and sink
  - 65–75Ω source series termination
  - Dynamic drive adjustment to match load conditions
  - Edge rates less than 1.5 ns
- **Output levels comply with JEDEC LVTTL standard**
- **+5V Vcc supply**
- **52 PQFP package**
- **Minimizes the ground-bounce, overshoot, and ringing problems often encountered when using CMOS and Bipolar drivers**

APPLICATIONS

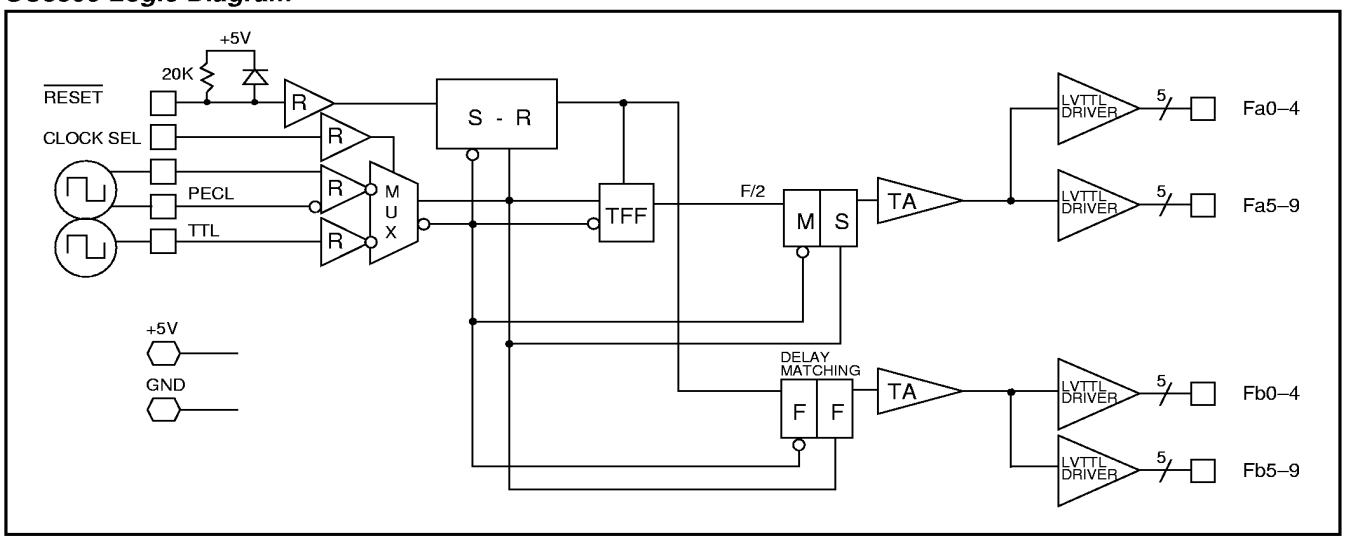
- **Compatible with Intel's Pentium™ and Pentium Pro™ processors, and PowerPC™ 603/604 processors**
- **PCI Bus clock distribution**
- **Workstation and server systems with high clock fanout**
- **Datacom and Telecom networks**

GENERAL DESCRIPTION

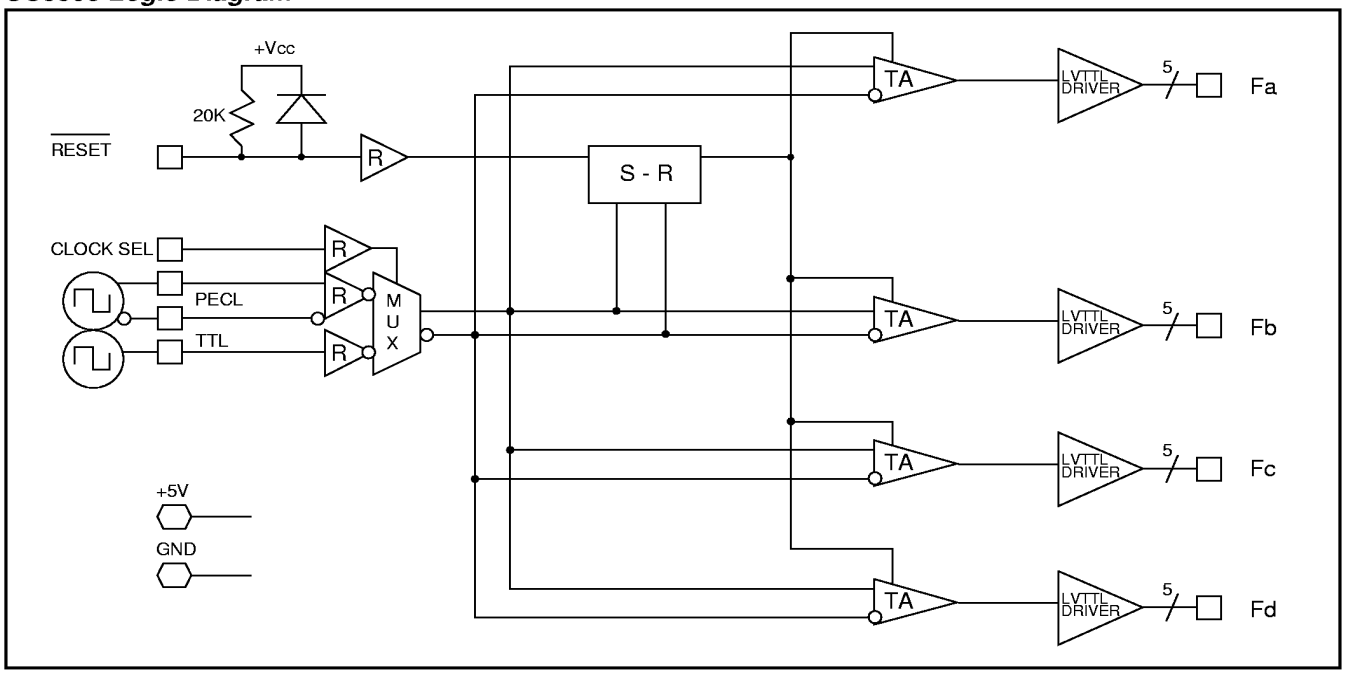
The SC3306 and SC3308 are precision low skew clock drivers with 20 outputs. These employ a clock input from a single-ended TTL or an ECL differential source operating between +5V and ground (PECL). This reference frequency input is received and distributed to divide-by-two or master-slave flip-flops. The resultant output is distributed to the clock output drivers. All outputs conform with JEDEC LVTTL levels.

Applied Micro Circuits Corporation (AMCC) uses proprietary complementary (source and sink) 24 mA peak output drivers. In addition to their drive capability, these circuits provide "source (series) termination" at the TTL outputs that minimize over/undershoot without requiring on-board termination networks. They are designed for a maximum output slew rate of ≈1.5V/ns to minimize simultaneous output-switching noise and distortion.

SC3306 Logic Diagram



SC3308 Logic Diagram



SC3306/08 Product Selection Guide

	Output Frequency with Respect to Input Frequency				
P/N	Total Outputs	Number of Outputs ÷ 1	Number of Outputs ÷ 2	Special Features	Package
SC3306	20	10	10		52 PQFP
SC3308	20	20	N/A		52 PQFP

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Absolute Maximum Ratings

Storage Temperature ..... -55° to +150°C
V_{CC} Potential to Ground ..... -0.5V to +7.0V
Input Voltage ..... -0.5V to +V_{CC}
Static Discharge Voltage ..... >1750V
Maximum Junction Temperature ..... +140°C
Latch-up Current ..... >200 mA
Operating Ambient Temperature ..... 0° to +70°C

Capacitance (package and die total)

Input Pins ..... 5.0 pF
TTL Output Pins ..... 5.0 pF

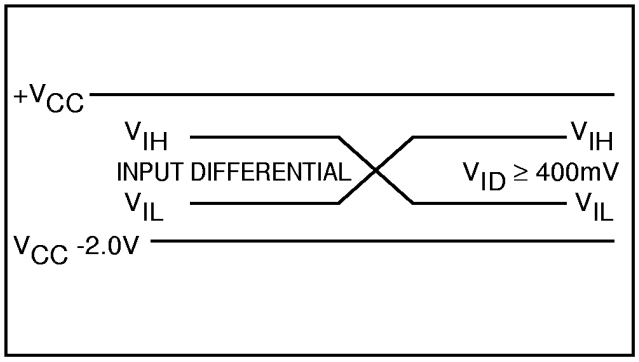
Electrical Characteristics

V_{CC} = +5.0V ± 5%, T_a = 0°C to + 70°C (reference "AC Test/Evaluation Circuit")

Symbol	Parameter	Conditions	Min	Max	Unit
V_{IH}	Input HIGH Voltage (PECL)	Differential Source–PECL	V_{IL} +0.4	V_{CC}	V
	Input HIGH Voltage (TTL)	All TTL Inputs	2.0	V_{CC}	V
V_{IL}	Input LOW Voltage (PECL)	Differential Source–PECL	V_{CC} -2.0	V_{IH} -0.4	V
	Input LOW Voltage (TTL)	All TTL Inputs	-0.5	0.8	V
I_{IH}	Input HIGH Current (PECL)	V_{IN} = V_{CC} (max)		200	uA
	CLKSEL	V_{IN} = V_{CC} (max)		350	uA
	RESET	V_{IN} = 2.4V		-200	uA
	TTL	V_{IN} = 2.4V		15	uA
I_{IL}	Input LOW Current (PECL)	V_{IN} = V_{CC} -2.0V		15	uA
	CLKSEL	V_{IN} = 0.4V		25	uA
	RESET	V_{IN} = 0.5V		-325	uA
	TTL	V_{IN} = 0.4V		15	uA
V_{OH}	Output HIGH Voltage	F_{OUT} = 80MHz, C_L = 10pF	2.3	3.65	V
V_{OL}	Output LOW Voltage	F_{OUT} = 80MHz, C_L = 10pF		0.4V	V
I_{OHS}[1]	Output HIGH Short Ckt Current	Output High, V_{OUT} = 0V Typ	-45		mA
I_{OLS}[1]	Output LOW Short Ckt Current	Output Low, V_{OUT} = V_{CC} Typ	55		mA
PWR	Static Core Power Dissipation	SC3306, 70°C, Typ Pwr=370mW SC3308, 70˚C, Typ Pwr=370mW		600 600	mW mW

1. Maximum test duration, one second.
2. The driver feature source series termination of approximately 40 Ohms to assist in matching 65–75 Ohm P.C. board environments.

PECL Differential Input Voltage Range



DC Characteristics

The outputs have been designed specifically for clock distribution. In the development of this product, AMCC has made several trade-offs between the historic "high-drive, totem-pole outputs" and AMCC's dynamically adjusting source series terminated outputs. As a result of this, the outputs will dynamically source and sink a symmetrical 24 mA of current. In a DC state, it exhibits the following specifications:

	Conditions	Min	Max
V_{OH}	I_{OH} = -2mA	2.1V	
V_{OL}	I_{OL} = 2mA		0.6V

AC Specifications—Using "AC Test/Evaluation Circuit"

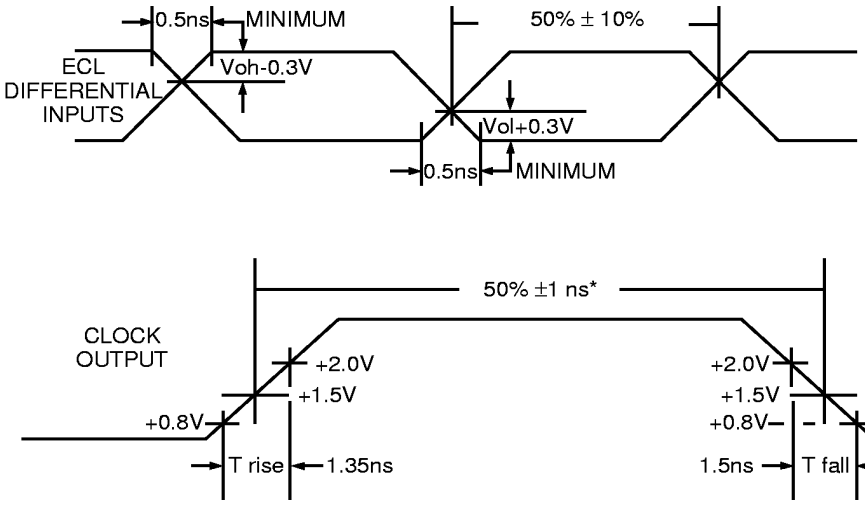
V_{CC} = +5.0V ± 5%, Ta = 0°C to +70°C, C_{LOAD} = 10pF

Parameter	SC3306	SC3308	Units
Maximum Skew Across All Outputs Options: Standard –1	 1.0 0.5	 1.0 0.5	ns
Maximum Skew within an Output Group	0.25	0.25	ns
Maximum Output Duty Cycle Asymmetry at 1.5V	±1.0	—	ns
Maximum TTL Input Frequency	80	80	MHz
Maximum PECL Differential Input Frequency	80	80	MHz
Maximum Rising/Falling Edge Rate	1.35/1.5	1.35/1.5	ns

Notes:

1. Skew is referenced to the rising and falling edges of all outputs.
2. Output symmetry follows input symmetry for the 1X outputs.
3. Asymmetry is defined as the deviation from a 50% duty cycle measured at 1.5V. Asymmetry will be affected by voltage, temperature, and load (including the length of the PC trace).
4. Typical skew derating factor for different loads is 50ps/pF at 1.5V threshold. For example, a 5pF load difference equals a 250 ps skew difference.
5. Edge rates are measured from 0.8V to 2.0V. Load consists of a 6" board trace (70 Ohm) with a 10 pF capacitive load. See "AC Test/Evaluation Circuit." Synchronous outputs may be paralleled for higher loads. The maximum rising edge rate is specified at 5.0V and must be derated at 1.4ns/V for V_{CC} <5.0V.
6. Parameters guaranteed by design and characterization or tested.

Threshold Crossing Characteristics



NOTE: Trise and Tfall are "real load" dependent. The values indicated are for 6" of board trace (70 Ohm) with a 10 pF capacitive load. See the Clock Driver Application Note.

*Applies only to divide-by-two outputs.

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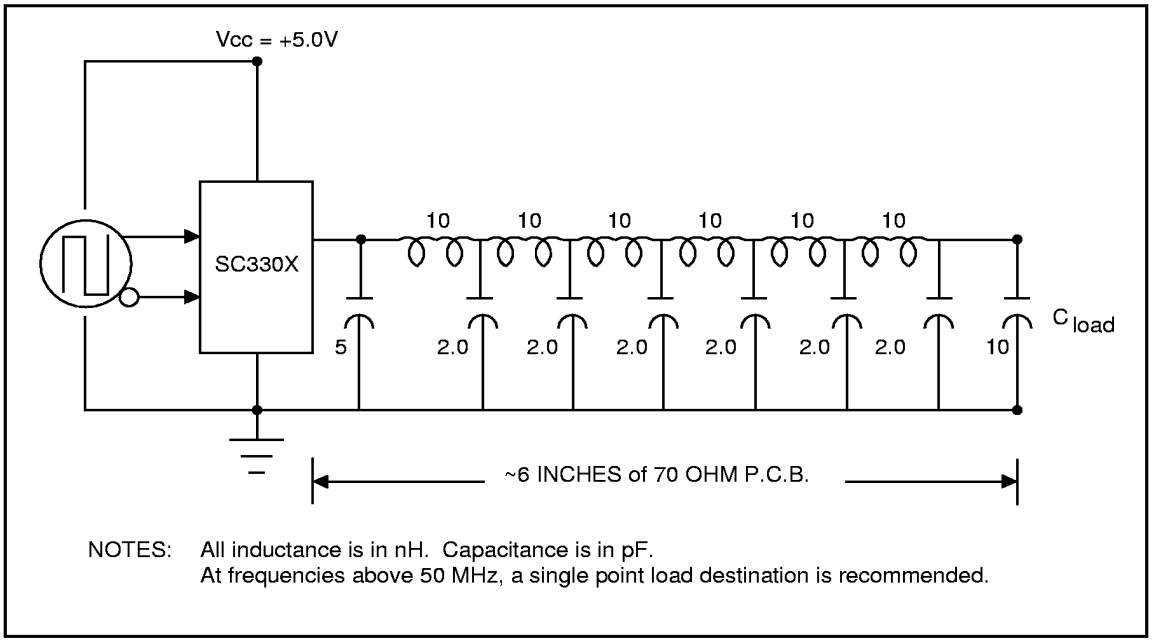
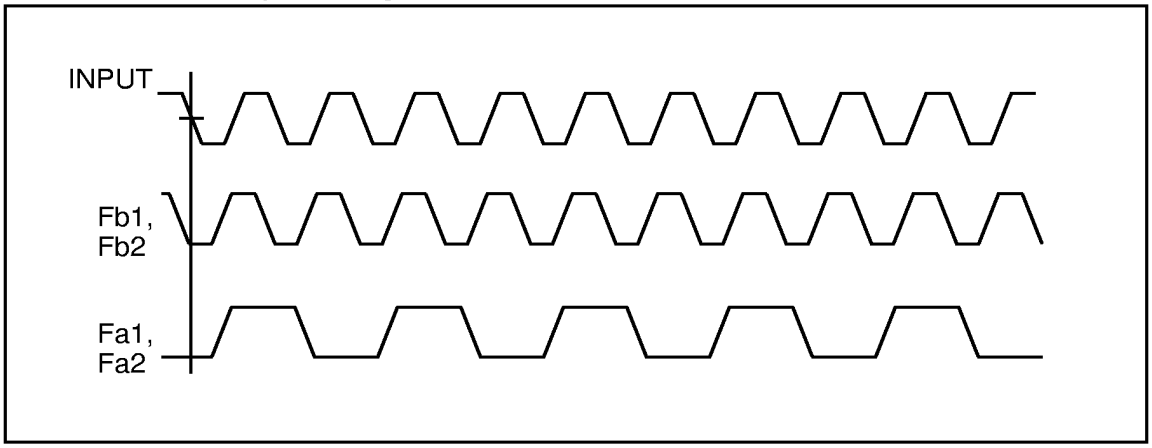
AC Test/Evaluation Circuit

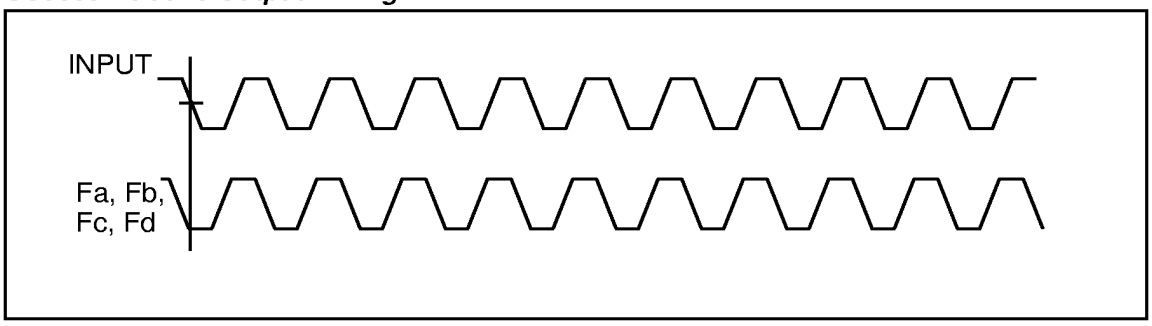


NOTES: All inductance is in nH. Capacitance is in pF.
At frequencies above 50 MHz, a single point load destination is recommended.

SC3306 Relative Output Timing



SC3308 Relative Output Timing



DESCRIPTION OF OPERATION
(Refer to Logic Diagram)

AMCC has developed the clock drivers using an advanced BiCMOS process. This design has been optimized for minimum skew across all twenty outputs.

For highest performance this approach requires a clock source input from a crystal-controlled oscillator (XCO) located adjacent to the clock driver. This oscillator can provide either differential ECL inputs (referenced to +5V, PECL) or TTL (CMOS) input levels to the clock driver. The input selection is accomplished via the "Clock Sel" input where a "HIGH" level activates the differential ECL input and a "LOW" activates the TTL input. This input clock will be fanned out to a toggle flip-flop or output flip-flops for synchronization, refer to Logic Diagrams. Using this methodology, the output duty cycle for the 1/2x outputs becomes largely a function of output driver slew rate into the AC load, and the duty cycle of the 1x outputs is a functions of the input clock waveshape and the output driver slew rate into the AC load.

The RESET input is provided to hold off or clear the outputs as may be required by the user's system. This pin may be logically driven from a TTL output. Optionally, if a capacitor (4.7uF = ~100 ms) is connected between this pin and ground, the device will respond with a "power up reset"—a delay in the clock outputs becoming active. At the onset of RESET (low) the outputs will go low following four falling-edge clock inputs. At the expiration of RESET (high) outputs will resume, after four falling-edge clock inputs, from a high (leading edge) count origin (see Figure 5, Reset To Output Timing, in the Clock Driver Application Note).

The output drivers are rise and fall slew rate controlled to ~1.5V/ns to minimize noise and distortion resulting from simultaneous switching of the 20 outputs. These outputs also feature series termination to significantly reduce the overshoot and undershoot of non-terminated transmission lines. This will satisfy printed circuit line impedances of 65–75 Ohms terminated into 15 pF (two IC input package receiver pins). When applications require large load capacitance (>25pF with 50 Ohm P.C. board impedance) and/or large peak voltage amplitudes, two adjacent drivers may be paralleled, thereby halving the series resistance and doubling the peak current (see the Clock Driver Application Note for Spice models).

Power and ground are interdigitated with the outputs. Of the 52 package pins, 22 are used for low impedance on-chip power distribution. Due to the simultaneously switching outputs, low impedance $+V_{CC}$ and ground planes within the P.C. board are recommended, as well as substantial decoupling capacitance (see the Clock Driver Application Note for recommendations).

The IC package and die layouts are tightly coupled to assure precise matching of all of the outputs. Collectively, the resistance, inductance, and capacitance of the package and wire bonding is managed to ensure that the clock driver will exhibit skews less than the specified maximum. A plastic 52-lead quad flat pack with .039" lead pitch is employed with an outer lead square footprint of approximately 0.7" per side.

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Power Management

The overall goal of managing the power dissipated by the clock driver is to limit its junction (die) temperature to 140°C. A major component of the power dissipated internally by the clock driver is determined by the load that each output drives and the frequency that each output is running. The "Output Power Dissipation" table summarizes these dependencies (see "AC Test/ Evaluation Circuit", for complete load definition).

The output power must be added to the core power (600 mW) of the clock driver to determine the total power being dissipated by the clock driver. This total power is then multiplied by the clock driver's thermal resistance, with the result being added to the ambient temperature to determine the junction temperature of the clock driver. For greatest reliability, this junction temperature should not exceed 140°C. The thermal resistance for the clock driver is detailed in the 52-pin PQFP Thermal Dissipation vs. Airflow graph in the Package appendix at the end of this section.

For example: An application utilizes a clock driver with 8 Fb outputs driving 10 pF loads at 66 MHz, 3 Fa outputs driving 5 pF loads at 33 MHz and 2 Fa outputs driving 15 pF loads at 33 Mhz. Total chip power is calculated as follows:

Core Power	= 600 mW
8 Fb, 10 pF, 66 MHz = (8 x 33 mW)	= 264 mW
2 Fb, no load, 66 MHz = (2 x 11 mW)	= 22 mW
3 Fa1, 5 pF, 33 MHz = (3 x 13 mW)	= 39 mW
2 Fa1, no load, 33 MHz = (2 x 8 mW)	= 16 mW
2 Fa2, 15 pF, 33 MHz = (2 x 17 mW)	= 34 mW
3 Fa2, no load, 33 MHz = (3 x 8 mW)	= 24 mW
Total Power	= 999 mW

The design specifies a 70˚C still air ambient. Referring to the 52-pin PQFP Thermal Dissipation vs. Airflow graph in the Package appendix, the Θ_{ja} for still air is 46.2˚C/watt. The clock driver's junction temperature would then be:

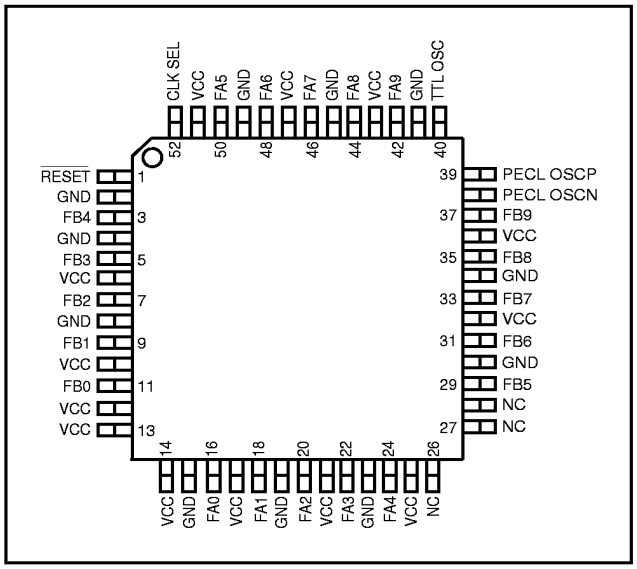
70˚C + (.999 watts x 46.2˚C/watt) = 116˚C

Note this is below the 140˚C maximum junction temperature.

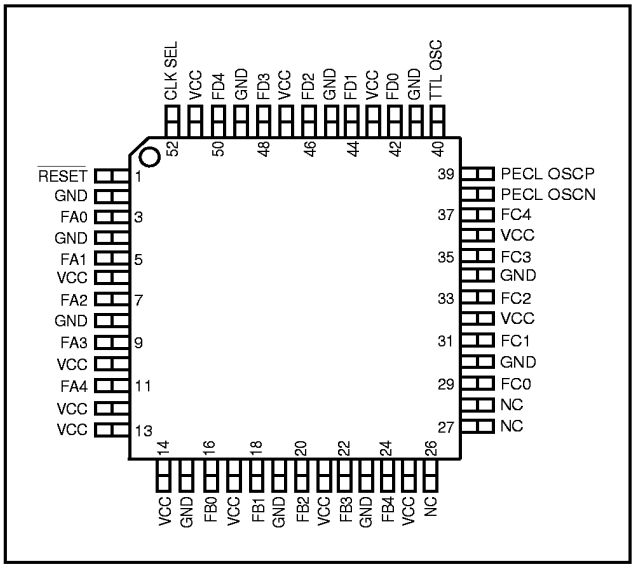
Output Power Dissipation

FREQUENCY	C_{LOAD}=5pF	C_{LOAD}=10pF	C_{LOAD}=15pF	C_{LOAD}=25pF	NO LOAD
80 MHz	29 mW	36 mW	43 mW	62 mW	13 mW
66 MHz	27 mW	33 mW	39 mW	53 mW	11 mW
50 MHz	20 mW	23 mW	27 mW	42 mW	10 mW
40 MHz	18 mW	21 mW	25 mW	36 mW	9 mW
33 MHz	13 mW	15 mW	17 mW	32 mW	8 mW
25 MHz	11 mW	13 mW	14 mW	22 mW	8 mW
20 MHz	10 mW	11 mW	13 mW	17 mW	7 mW

SC3306 Pinout



SC3308 Pinout



Ordering Information

AMCC clock driver products are available in several output skew and shipping configurations. The order number is formed by a combination of:

- **Device Number**
- **Package Type**
- **Skew Option (if applicable)**
- **Optional Shipping Configuration**

SC330X **Q** **– 1** **/TD**

Optional Shipping Configuration
Blank = 84-unit matrix tray
/D = dry pack
/TD = tape, reel and dry pack

Skew Option
Blank = 1.0 ns output-output skew
– 1 = 500 ps output-output skew

Package Option
Q = 52-pin Plastic Quad Flat Pack (PQFP)

Device Number

Example: SC330XQ–1/D
52-pin PQFP package, 500 ps output-output skew, shipped dry packed in the standard matrix tray.

Part Number	Standard	–1
SC3306	✔	✔
SC3308	✔	✔

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