

# 4.8 V NPN Common Emitter Output Power Transistor for GSM Class IV Phones

## Technical Data

### AT-36408

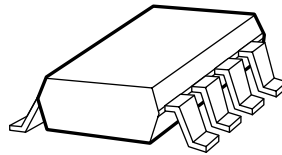
#### Features

- 4.8 Volt Pulsed Operation (pulse width = 577  $\mu$ sec, duty cycle = 12.5%)
- +35.0 dBm  $P_{out}$  @ 900 MHz, Typ.
- 65% Collector Efficiency @ 900 MHz, Typ.
- 9 dB Power Gain @ 900 MHz, Typ.
- Internal Input Pre-Matching Facilitates Cascading

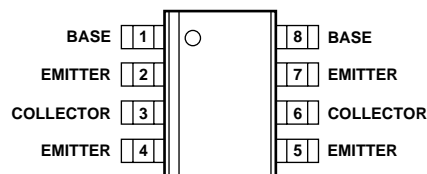
#### Applications

- Output Power Device for GSM Class IV Handsets

#### SOIC-8 Surface Mount Plastic Package Outline P8



#### Pin Configuration



#### Description

Hewlett Packard's AT-36408 combines internal input pre-matching with low cost, NPN power silicon bipolar junction transistors in a SOIC-8 surface mount plastic package. This device is designed for use as the output device for GSM Class IV handsets. At 4.8 volts, the device features +35 dBm pulsed output power, superior power added efficiency, and excellent gain, making the AT-36408 an excellent choice for battery powered systems.

The AT-36408 is fabricated with Hewlett Packard's 10 GHz  $F_t$  Self-Aligned-Transistor (SAT) process. The die are nitride passivated for surface protection. Excellent device uniformity, performance and reliability are produced by the use of ion-implantation, self-alignment techniques, and gold metalization in the fabrication of these devices.

## AT-36408 Absolute Maximum Ratings

Symbol	Parameter	Units	Absolute Maximum <sup>[1]</sup>
V <sub>EBO</sub>	Emitter-Base Voltage	V	1.4
V <sub>CBO</sub>	Collector-Base Voltage	V	16.0
V <sub>CEO</sub>	Collector-Emitter Voltage	V	9.5
I <sub>C</sub>	Collector Current <sup>[2]</sup>	A	1.7
P <sub>T</sub>	Peak Power Dissipation <sup>[2, 3]</sup>	W	8.6
T <sub>j</sub>	Junction Temperature	°C	150
T <sub>STG</sub>	Storage Temperature	°C	-65 to 150

Thermal Resistance<sup>[4]</sup>:

$$\theta_{jc} = 60^{\circ}\text{C/W}$$

### Notes:

1. Permanent damage may occur if any of these limits are exceeded.
2. Pulsed operation, pulse width = 577  $\mu\text{sec}$ , duty cycle = 12.5%.
3. Derate at 133.3 mW/°C for T<sub>C</sub> > 85 °C. T<sub>C</sub> is defined to be the temperature of the collector pins 3 and 6, where the lead contacts the circuit board.
4. Using the liquid crystal technique, V<sub>CE</sub> = 4.5 V, I<sub>C</sub> = 100 mA, T<sub>j</sub> = 150°C, 1-2  $\mu\text{m}$  "hot-spot" resolution.

## Electrical Specifications, T<sub>C</sub> = 25°C

Symbol	Parameters and Test Conditions	Units	Min.	Typ.	Max.
	Freq. = 900 MHz, V <sub>CE</sub> = 4.8 V, I <sub>CQ</sub> = 50 mA, pulsed operation, pulse width = 577 $\mu\text{sec}$ , duty cycle = 12.5%, Test Circuit A, unless otherwise specified				
P <sub>out</sub>	Output Power <sup>[1]</sup> P <sub>in</sub> = +26 dBm	dBm	+34.0	+35.0	
$\eta_C$	Collector Efficiency <sup>[1]</sup> P <sub>in</sub> = +26 dBm	%	55	65	
H2	2nd Harmonic <sup>[1]</sup> F <sub>0</sub> = 900 MHz	dBc		-50	
H3	3rd Harmonic <sup>[1]</sup> F <sub>0</sub> = 900 MHz	dBc		-40	
	Mismatch Tolerance, No Damage <sup>[1]</sup> P <sub>out</sub> = +35 dBm any phase, 2 sec duration				7:1
BV <sub>EBO</sub>	Emitter-Base Breakdown Voltage I <sub>E</sub> = 0.8 mA, open collector	V	1.4		
BV <sub>CBO</sub>	Collector-Base Breakdown Voltage I <sub>C</sub> = 4.0 mA, open emitter	V	16.0		
BV <sub>CEO</sub>	Collector-Emitter Breakdown Voltage I <sub>C</sub> = 20.0 mA, open base	V	9.5		
h <sub>FE</sub>	Forward Current Transfer Ratio V <sub>CE</sub> = 3 V, I <sub>C</sub> = 180 mA	—	80	150	330
I <sub>CEO</sub>	Collector Leakage Current V <sub>CEO</sub> = 5 V	$\mu\text{A}$			50

### Note:

1. With external matching on input and output, tested in a 50 ohm environment. Refer to Test Circuit A (GSM).

## AT-36408 Typical Performance, $T_C = 25^\circ\text{C}$

Frequency = 900 MHz,  $V_{CE} = 4.8\text{ V}$ ,  $I_{CQ} = 50\text{ mA}$ , pulsed operation, pulse width = 577  $\mu\text{sec}$ , duty cycle = 12.5%, Test Circuit A (GSM), unless otherwise specified.

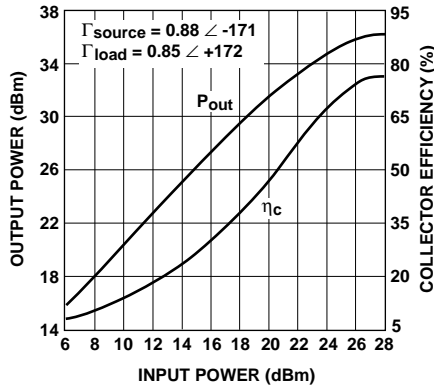


Figure 1. Output Power and Collector Efficiency vs. Input Power.

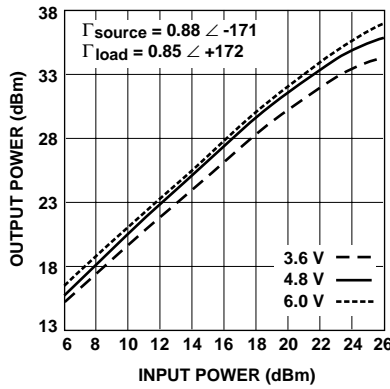


Figure 2. Output Power vs. Input Power Over Bias Voltage.

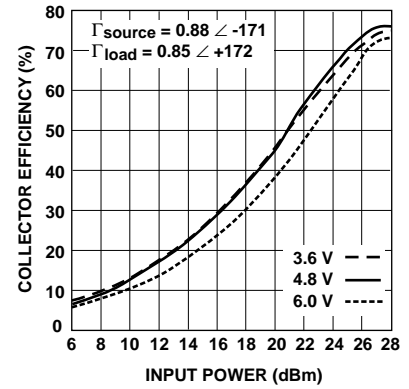


Figure 3. Collector Efficiency vs. Input Power Over Bias Voltage.

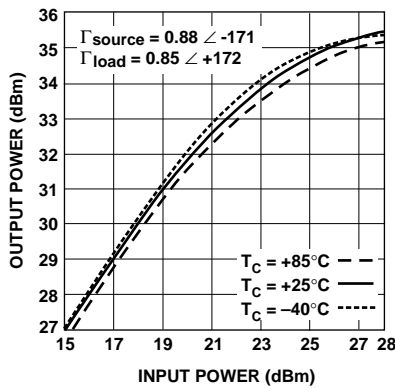


Figure 4. Output Power vs. Input Power Over Temperature.

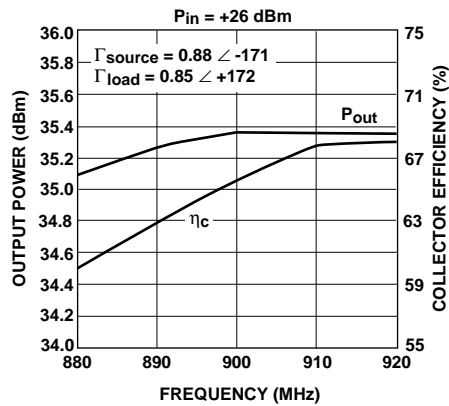


Figure 5. Output Power and Collector Efficiency vs. Frequency.

Note: Tuned at 900 MHz, then swept over frequency.

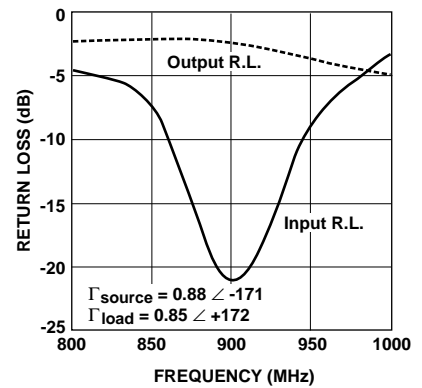


Figure 6. Input and Output Return Loss vs. Frequency.

## AT-36408 Typical Large Signal Impedances

$V_{CE} = 4.8\text{ V}$ ,  $I_{CQ} = 50\text{ mA}$ , Pulsed Operation,  $P_{out} = +35.0\text{ dBm}$

Freq. MHz	$\Gamma_{source}$		$\Gamma_{load}$	
	Mag.	Ang.	Mag.	Ang.
880	0.882	-170.0	0.847	172.7
890	0.885	-170.5	0.849	172.2
900	0.887	-171.1	0.851	171.6
910	0.890	-171.4	0.853	171.1
915	0.891	-169.0	0.854	168.4
920	0.893	-168.4	0.855	168.2

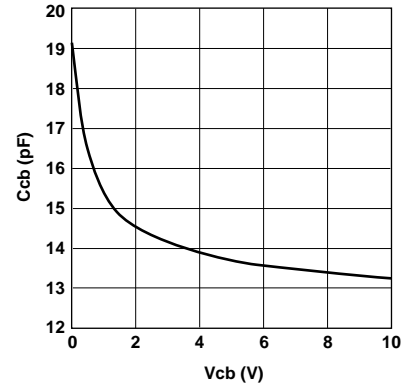
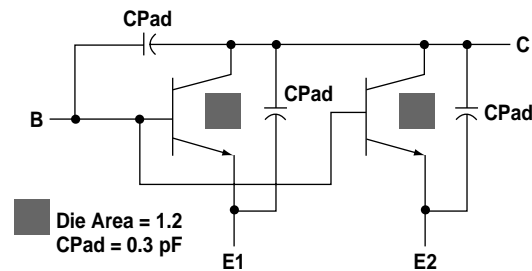


Figure 7. Collector-Base Capacitance vs. Collector-Base Voltage (DC Test).

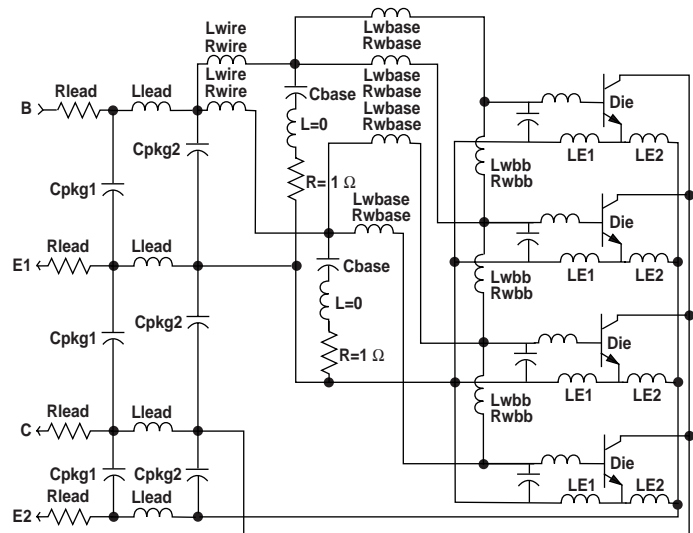
## SPICE Model Parameters

### Die Model



Label	Value	Label	Value
BF	280	TR	1E-9
IKF	299.9	EG	1.11
ISE	9.9E-11	IS	3.598E-15
NE	2.399	XTI	3
VAF	33.16	CJC	0.8E-12
NF	0.9935	VJC	0.4831
TF	1.6E-11	MJC	0.2508
XTF	0.006656	XCJC	0.001
VTF	0.02785	FC	0.999
ITF	0.001	CJE	6.16E-12
PTF	23	VJE	1.186
XTB	0	MJE	0.5965
BR	54.61	RB	0.752
IKR	81	IRB	0
ISC	8.7E-13	RBM	0.01
NC	1.587	RE	1.27
VAR	1.511	RC	0.107
NR	0.9886		

### Packaged Model



Label	Value	Label	Value
Rlead	0.63 $\Omega$	LE2	0.00064 nH
Llead	1.45 nH	Cbase	46.0 pF
Rwire	1.3 $\Omega$	Rwbase	0.2 $\Omega$
Lwire	0.52 nH	Lwbase	1.19 nH
Cpkg1	0.4 pF	Rwbb	0.1 $\Omega$
Cpkg2	1.2 pF	Lwbb	0.1 nH
LE1	0.3 nH		

## AT-36408 Typical Scattering Parameters, Common Emitter, $Z_0 = 50 \Omega$

$V_{CE} = 3.6 \text{ V}$ ,  $I_c = 200 \text{ mA}$ ,  $T_c = 25^\circ\text{C}$

Freq. GHz	$S_{11}$		dB	$S_{21}$		dB	$S_{12}$		$S_{22}$	
	Mag.	Ang.		Mag.	Ang.		Mag.	Ang.	Mag.	Ang.
0.05	0.96	-175	22.3	13.08	93	-38.4	0.012	11	0.74	-169
0.10	0.96	-178	16.4	6.61	88	-37.7	0.013	13	0.74	-174
0.25	0.96	177	8.8	2.76	80	-36.5	0.015	24	0.75	-177
0.50	0.94	173	4.2	1.63	66	-34.4	0.019	33	0.73	-177
0.75	0.90	169	3.4	1.49	46	-32.0	0.025	27	0.71	-172
0.90	0.84	168	4.2	1.63	24	-32.0	0.025	10	0.72	-165
1.00	0.79	170	4.6	1.70	0	-34.0	0.020	-14	0.81	-160
1.25	0.92	175	-1.2	0.87	-68	-37.1	0.014	126	1.01	-172
1.50	0.97	169	-9.6	0.33	-98	-30.2	0.031	97	0.96	-177

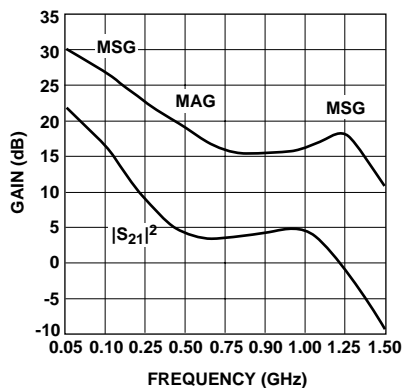
$V_{CE} = 4.8 \text{ V}$ ,  $I_c = 200 \text{ mA}$ ,  $T_c = 25^\circ\text{C}$

0.05	0.96	-174	22.6	13.42	93	-37.7	0.013	11	0.74	-169
0.10	0.96	-178	16.6	6.79	88	-37.7	0.013	13	0.73	-174
0.25	0.96	178	9.0	2.83	80	-36.5	0.015	23	0.74	-177
0.50	0.94	173	4.4	1.66	66	-34.4	0.019	32	0.72	-176
0.75	0.90	169	3.6	1.51	46	-32.4	0.024	26	0.70	-172
0.90	0.84	168	4.3	1.64	24	-32.0	0.025	9	0.72	-164
1.00	0.80	170	4.6	1.71	0	-34.0	0.020	-14	0.81	-160
1.25	0.92	175	-1.0	0.89	-67	-37.1	0.014	126	1.01	-171
1.50	0.97	169	-9.4	0.34	-97	-30.2	0.031	97	0.96	-177

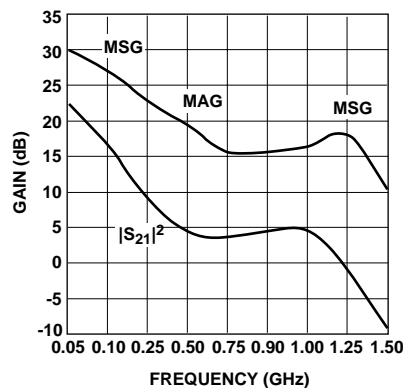
$V_{CE} = 6.0 \text{ V}$ ,  $I_c = 200 \text{ mA}$ ,  $T_c = 25^\circ\text{C}$

0.05	0.96	-174	22.7	13.60	93	-37.7	0.013	12	0.73	-169
0.10	0.96	-178	16.7	6.88	88	-37.1	0.014	14	0.72	-174
0.25	0.96	178	9.2	2.87	79	-35.9	0.016	23	0.73	-177
0.50	0.94	173	4.5	1.68	65	-34.0	0.020	30	0.71	-176
0.75	0.90	169	3.7	1.52	45	-32.0	0.025	24	0.69	-171
0.90	0.85	168	4.3	1.64	23	-32.0	0.025	8	0.72	-164
1.00	0.80	170	4.6	1.70	0	-34.0	0.020	-14	0.81	-159
1.25	0.92	175	-1.0	0.90	-67	-37.7	0.013	125	1.01	-171
1.50	0.97	169	-9.2	0.35	-97	-30.2	0.031	96	0.95	-177

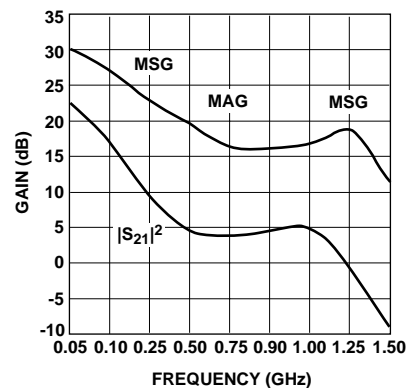
### Typical Performance



**Figure 8. Insertion Power Gain, Maximum Available Gain, and Maximum Stable Gain vs. Frequency.  $V_{CE} = 3.6 \text{ V}$ ,  $I_c = 200 \text{ mA}$ .**

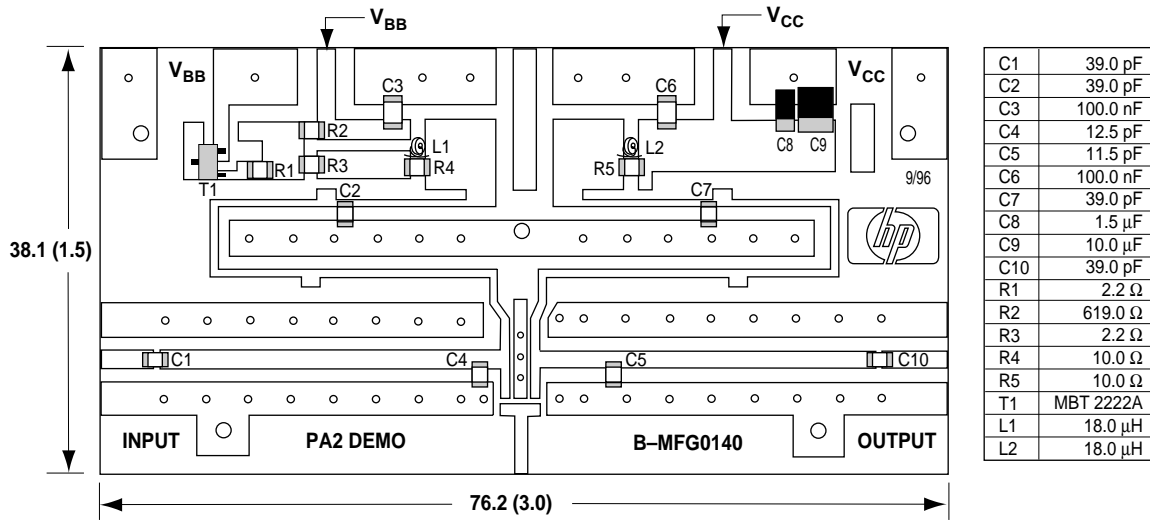


**Figure 9. Insertion Power Gain, Maximum Available Gain, and Maximum Stable Gain vs. Frequency.  $V_{CE} = 4.8 \text{ V}$ ,  $I_c = 200 \text{ mA}$ .**



**Figure 10. Insertion Power Gain, Maximum Available Gain, and Maximum Stable Gain vs. Frequency.  $V_{CE} = 6.0 \text{ V}$ ,  $I_c = 200 \text{ mA}$ .**

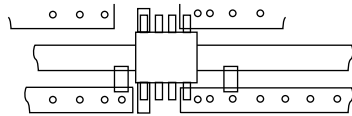
### Test Circuit A: Test Circuit Board Layout @ 900 MHz (GSM)



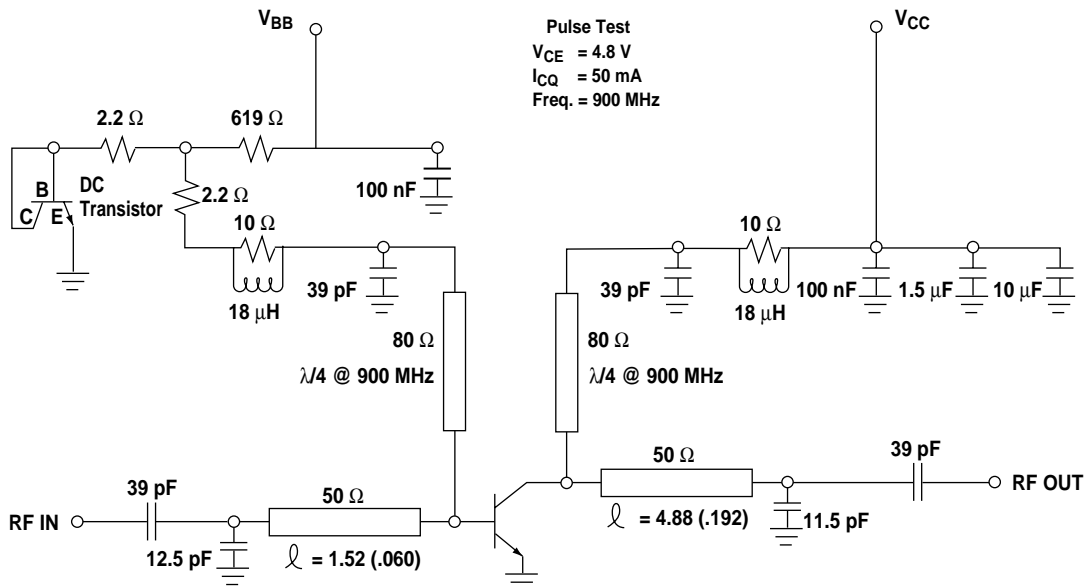
**Pulse Test**  
 $V_{CE} = 4.8\text{ V}$   
 $I_{CQ} = 50\text{ mA}$   
 Freq. = 900 MHz

**Test Circuit:**  
 FR-4 Microstrip, glass epoxy board  
 Dielectric Constant = 4.5  
 Thickness = 0.79 (.031)

**NOTE:**  
 Dimensions are shown in millimeters (inches).



### Test Circuit A: Test Circuit Schematic Diagram @ 900 MHz (GSM)

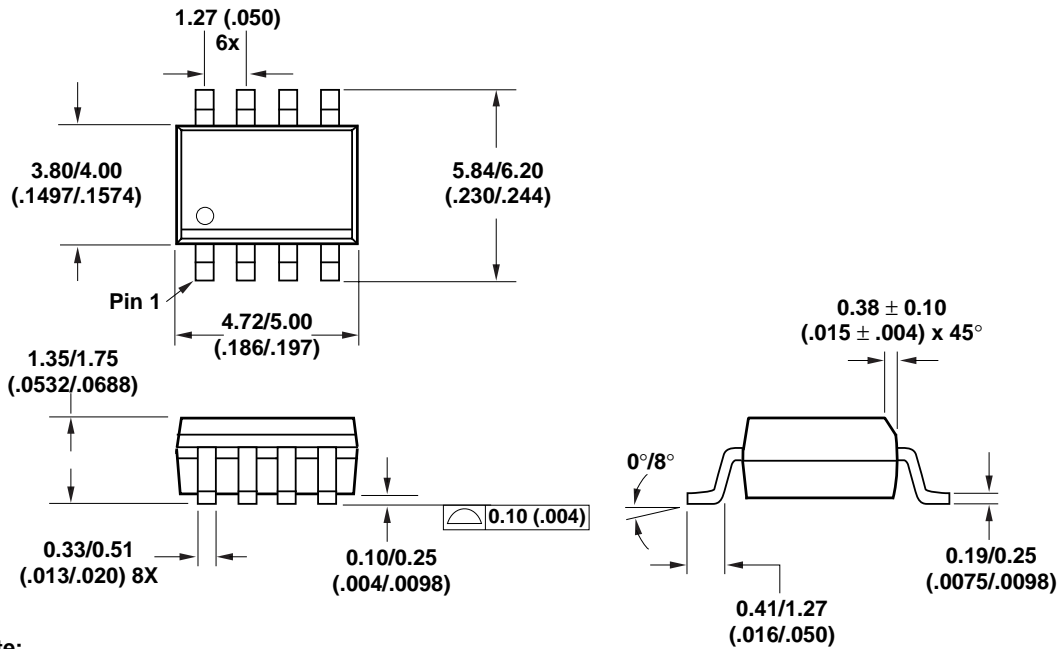


## Part Number Ordering Information

Part Number	No. of Devices	Container
AT-36408-TR1	1000	7" Reel
AT-36408-BLK	25	Carrier Tape

## Package Dimensions

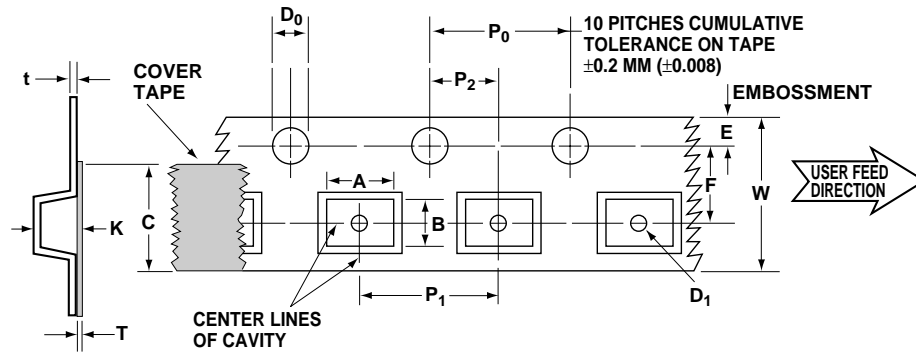
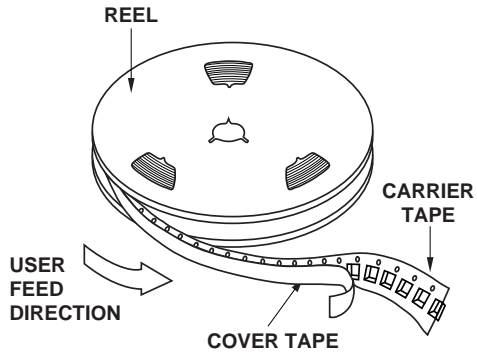
### SOIC-8 Surface Mount Plastic Package



#### Note:

1. Dimensions are shown in millimeters (inches).

## Tape Dimensions and Product Orientation For Package SOIC-8



	DESCRIPTION	SYMBOL	SIZE (mm)	SIZE (INCHES)
CAVITY	LENGTH	A	$6.45 \pm 0.10$	$0.254 \pm 0.004$
	WIDTH	B	$5.13 \pm 0.10$	$0.202 \pm 0.004$
	DEPTH	K	$2.11 \pm 0.10$	$0.083 \pm 0.004$
	PITCH	$P_1$	$8.00 \pm 0.10$	$0.315 \pm 0.004$
	BOTTOM HOLE DIAMETER	$D_1$	1.50 min.	0.059 min.
PERFORATION	DIAMETER	$D_0$	$1.50 + 0.10/-0$	$0.059 + 0.004/-0$
	PITCH	$P_0$	$4.00 \pm 0.10$	$0.157 \pm 0.004$
	POSITION	E	$1.75 \pm 0.10$	$0.069 \pm 0.004$
CARRIER TAPE	WIDTH	W	$8.00 \pm 0.30$	$0.315 \pm 0.012$
	THICKNESS	t	$0.255 \pm 0.013$	$0.0100 \pm 0.0005$
COVER TAPE	WIDTH	C	$9.19 \pm 0.10$	$0.362 \pm 0.004$
	TAPE THICKNESS	T	$0.051 \pm 0.010$	$0.0020 \pm 0.0004$
DISTANCE BETWEEN CENTERLINE	CAVITY TO PERFORATION (WIDTH DIRECTION)	F	$5.51 \pm 0.05$	$0.217 \pm 0.002$
	CAVITY TO PERFORATION (LENGTH DIRECTION)	$P_2$	$2.00 \pm 0.05$	$0.079 \pm 0.002$