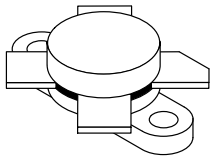
The RF MOSFET Line

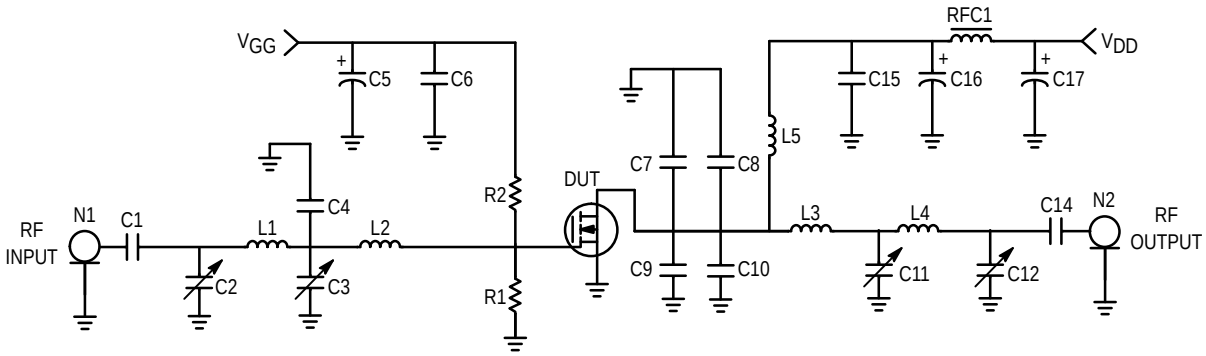
RF Power Field-Effect Transistor

N–Channel Enhancement–Mode

MRF255
PHOTOMASTER



CASE 211–11, STYLE 2

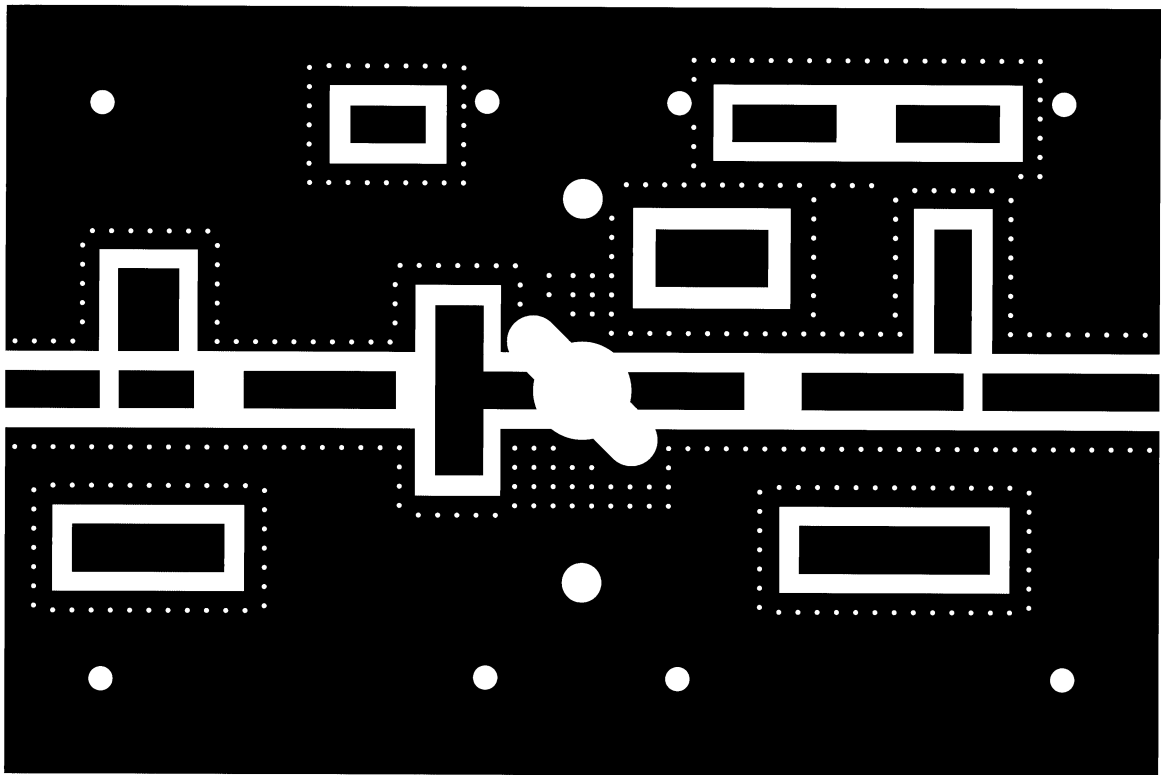


C1 — 470 pF, Chip Capacitor
C2, C3, C11, C12 — 20–200 pF, Trimmer, ARCO #464
C4 — 100 pF, Chip Capacitor
C5, C17 — 100 µF, 15 V, Electrolytic
C6 — 0.001 µF, Disc Ceramic
C7, C8, C9, C10 — 330 pF, Chip Capacitor
C14 — 1200 pF, ATC Chip Capacitor
C15 — 910 pF, 500 V, Dipped Mica
C16 — 47 µF, 16 V, Electrolytic

L1 — 8 Turns, #20 AWG, 0.126″ ID
L2 — 5 Turns, #18 AWG, 0.142″ ID
L3 — 3 Turns, #20 AWG, 0.102″ ID
L4 — 7 Turns, #24 AWG, 0.070″ ID
L5 — 6.5 Turns, #18 AWG, 0.230″ ID, 0.5″ Long
N1, N2 — Type N Flange Mount
RFC1 — Ferroxcube VK–200–19/4B
R1 — 39 kΩ, 1/4 W Carbon
R2 — 150 Ω, 1/4 W Carbon
Board — G–10 .060″

Figure 1. 54 MHz Linear RF Test Circuit Electrical Schematic

Handling and Packaging — MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.



(SCALE: 1:1)

Figure 2. Photomaster for 54 MHz Narrowband Test Fixture

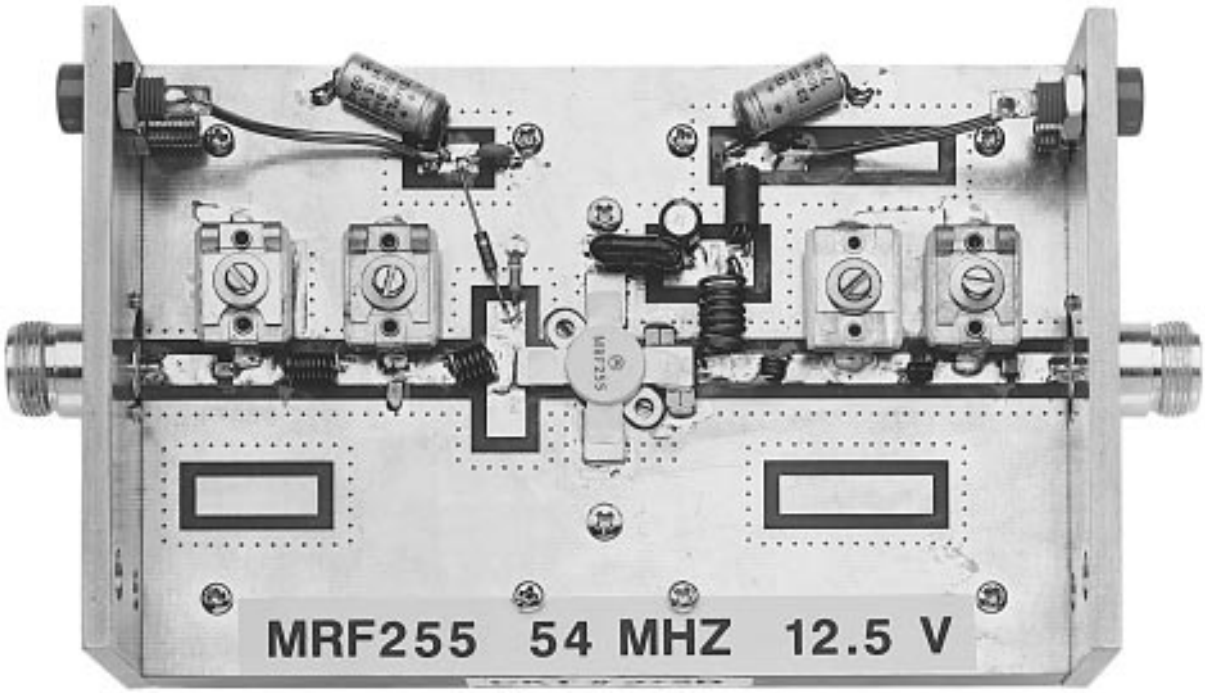
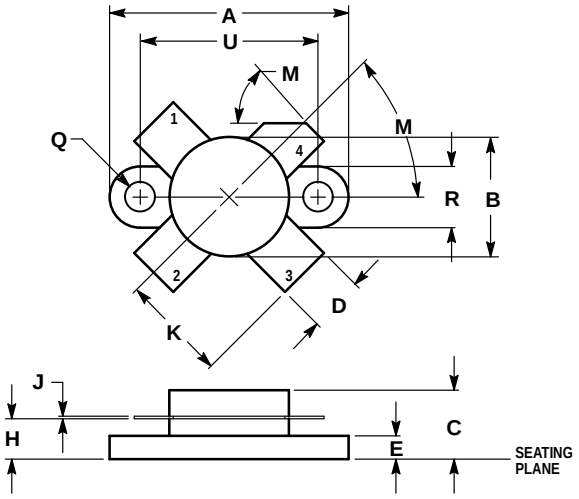


Figure 3. Test Fixture Photograph — MRF255

PACKAGE DIMENSIONS



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.960	0.990	24.39	25.14
B	0.465	0.510	11.82	12.95
C	0.229	0.275	5.82	6.98
D	0.216	0.235	5.49	5.96
E	0.084	0.110	2.14	2.79
H	0.144	0.178	3.66	4.52
J	0.003	0.007	0.08	0.17
K	0.435	—	11.05	—
M	45 °NOM		45 °NOM	
Q	0.115	0.130	2.93	3.30
R	0.246	0.255	6.25	6.47
U	0.720	0.730	18.29	18.54

STYLE 2:
PIN 1. SOURCE
2. GATE
3. SOURCE
4. DRAIN

CASE 211–11
ISSUE N

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