

The RF MOSFET Line  
**RF Power Field Effect Transistors**  
N-Channel Enhancement-Mode Lateral MOSFETs

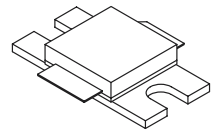
Designed for GSM and EDGE base station applications with frequencies from 1.8 to 2.0 GHz. Suitable for FM, TDMA, CDMA and multicarrier amplifier applications. Specified for GSM 1930 – 1990 MHz.

- Typical GSM Performance:  
Power Gain – 14 dB (Typ) @ 30 Watts  
Efficiency – 50% (Typ) @ 30 Watts
- Internally Matched, Controlled Q, for Ease of Use
- High Gain, High Efficiency and High Linearity
- Integrated ESD Protection
- Designed for Maximum Gain and Insertion Phase Flatness
- Capable of Handling 5:1 VSWR, @ 26 Vdc, 30 W CW Output Power
- Excellent Thermal Stability
- Available in Tape and Reel. R3 Suffix = 250 Units per 32 mm, 13 inch Reel.

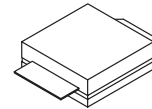
**MRF18030BR3**  
**MRF18030BSR3**

**GSM/GSM EDGE 1.93 – 1.99 GHz,  
30 W, 26 V  
LATERAL N-CHANNEL  
RF POWER MOSFETs**

**CASE 465E-03, STYLE 1  
NI-400  
MRF18030BR3**



**CASE 465F-03, STYLE 1  
NI-400S  
MRF18030BSR3**



**MAXIMUM RATINGS**

Rating	Symbol	Value	Unit
Drain-Source Voltage	$V_{DSS}$	65	Vdc
Gate-Source Voltage	$V_{GS}$	+15, -0.5	Vdc
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	83.3 0.48	Watts $\text{W}/^\circ\text{C}$
Storage Temperature Range	$T_{stg}$	-65 to +200	$^\circ\text{C}$
Operating Junction Temperature	$T_J$	200	$^\circ\text{C}$

**ESD PROTECTION CHARACTERISTICS**

Test Conditions	Class
Human Body Model	2 (Minimum)
Machine Model	M3 (Minimum)

**THERMAL CHARACTERISTICS**

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	2.1	$^\circ\text{C}/\text{W}$

NOTE – **CAUTION** – MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

**ELECTRICAL CHARACTERISTICS** ( $T_C = 25^\circ\text{C}$ , 50 ohm system unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
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**OFF CHARACTERISTICS**

Drain–Source Breakdown Voltage ( $V_{GS} = 0 \text{ Vdc}$ , $I_D = 20 \mu\text{Adc}$ )	$V_{(BR)DSS}$	65	—	—	Vdc
Zero Gate Voltage Drain Current ( $V_{DS} = 26 \text{ Vdc}$ , $V_{GS} = 0 \text{ Vdc}$ )	$I_{DSS}$	—	—	1	$\mu\text{Adc}$
Gate–Source Leakage Current ( $V_{GS} = 5 \text{ Vdc}$ , $V_{DS} = 0 \text{ Vdc}$ )	$I_{GSS}$	—	—	1	$\mu\text{Adc}$

**ON CHARACTERISTICS**

Gate Threshold Voltage ( $V_{DS} = 10 \text{ Vdc}$ , $I_D = 100 \mu\text{Adc}$ )	$V_{GS(th)}$	2	3	4	Vdc
Gate Quiescent Voltage ( $V_{DS} = 26 \text{ Vdc}$ , $I_D = 250 \text{ mAdc}$ )	$V_{GS(Q)}$	2	3.9	4.5	Vdc
Drain–Source On–Voltage ( $V_{GS} = 10 \text{ Vdc}$ , $I_D = 1 \text{ Adc}$ )	$V_{DS(on)}$	—	0.29	0.4	Vdc
Forward Transconductance ( $V_{DS} = 10 \text{ Vdc}$ , $I_D = 1 \text{ Adc}$ )	$g_{fs}$	—	2	—	S

**DYNAMIC CHARACTERISTICS**

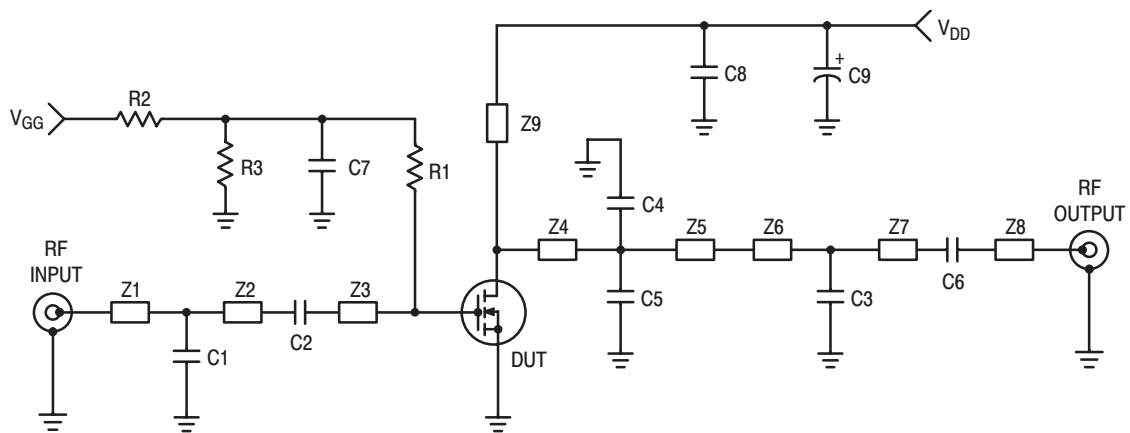
Reverse Transfer Capacitance (1) ( $V_{DS} = 26 \text{ Vdc} \pm 30 \text{ mV(rms)ac}$ @ 1 MHz, $V_{GS} = 0 \text{ Vdc}$ )	$C_{rss}$	—	1.3	—	pF
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**FUNCTIONAL TESTS** (In Motorola Test Fixture) (2)

Output Power, 1 dB Compression Point ( $V_{DD} = 26 \text{ Vdc}$ , $I_{DQ} = 250 \text{ mA}$ , $f = 1930 - 1990 \text{ MHz}$ )	P1dB	27	30	—	Watts
Common–Source Amplifier Power Gain @ 30 W ( $V_{DD} = 26 \text{ Vdc}$ , $I_{DQ} = 250 \text{ mA}$ , $f = 1930 - 1990 \text{ MHz}$ )	$G_{ps}$	13	14	—	dB
Drain Efficiency @ 30 W ( $V_{DD} = 26 \text{ Vdc}$ , $I_{DQ} = 250 \text{ mA}$ , $f = 1930 - 1990 \text{ MHz}$ )	$\eta$	46.5	50	—	%
Input Return Loss @ 30 W ( $V_{DD} = 26 \text{ Vdc}$ , $I_{DQ} = 250 \text{ mA}$ , $f = 1930 - 1990 \text{ MHz}$ )	IRL	—	–12	–9	dB
Output Mismatch Stress @ 30 W ( $V_{DD} = 26 \text{ Vdc}$ , $I_{DQ} = 250 \text{ mA}$ , $f_1 = 1930 - 1990 \text{ MHz}$ , VSWR = 5:1, All Phase Angles at Frequency of Tests)	$\Psi$	No Degradation In Output Power Before and After Test			

(1) Part is internally matched both on input and output.

(2) Device specifications obtained on a Production Test Fixture.



C1	1.8 pF, 100B Chip Capacitor	Z2	1.022" x 0.087" Microstrip
C2	0.8 pF, 100B Chip Capacitor	Z3	0.257" x 0.633" Microstrip
C3	0.8 pF, 100B Chip Capacitor	Z4	0.189" x 0.394" Microstrip
C4, C5	1.2 pF, 100B Chip Capacitors	Z5	0.335" x 0.394" Microstrip
C6, C7, C8	8.2 pF, 100B Chip Capacitors	Z6	0.616" x 0.087" Microstrip
C9	220 $\mu$ F, 63 V Electrolytic Capacitor	Z7	0.845" x 0.087" Microstrip
R1	1.0 k $\Omega$ , 1/8 W Chip Resistor (0805)	Z8	0.366" x 0.087" Microstrip
R2, R3	10 k $\Omega$ , 1/8 W Chip Resistors (0805)	Z9	$\approx$ 0.500" x 0.087" Microstrip
Z1	0.496" x 0.087" Microstrip		

Figure 1. 1930 – 1990 MHz Test Fixture Schematic

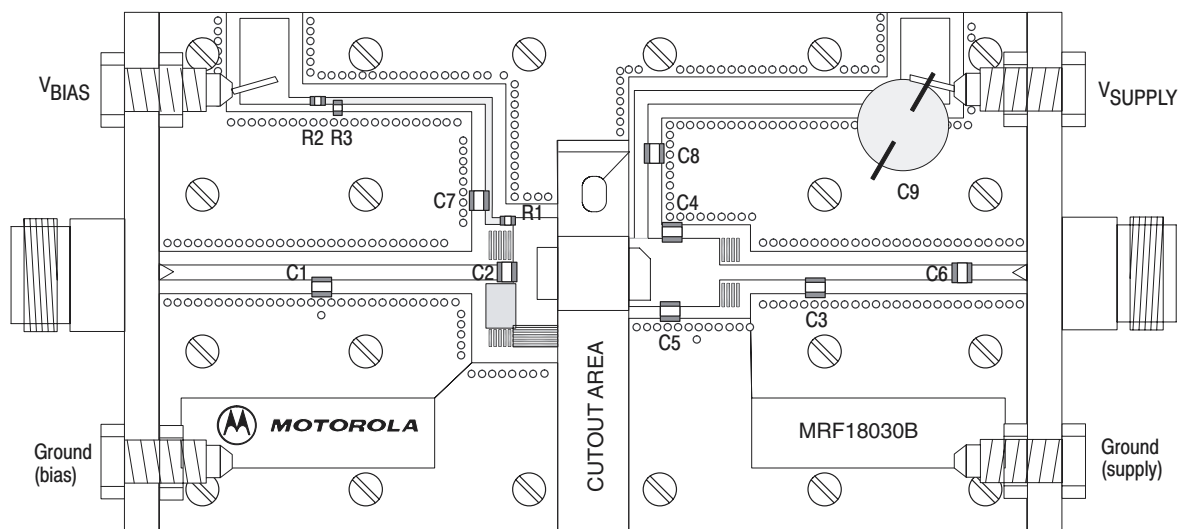


Figure 2. 1930 – 1990 MHz Test Fixture Component Layout

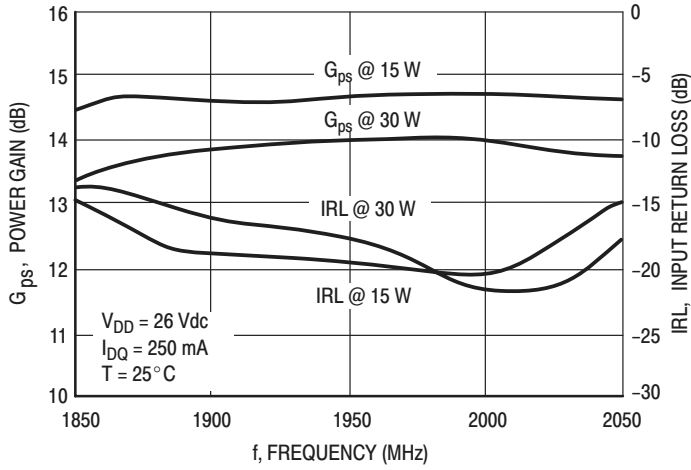


Figure 3. Wideband Gain and IRL at 30 W and 15 W Output Power

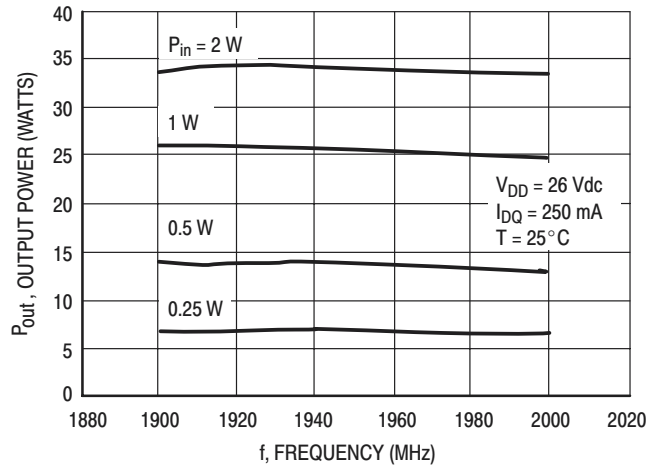


Figure 4. Output Power versus Frequency

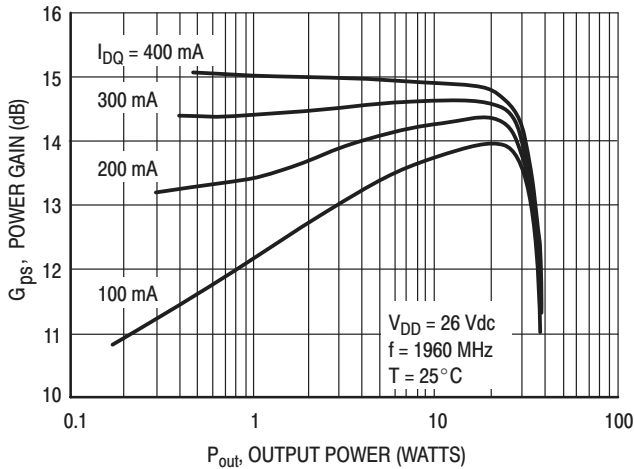


Figure 5. Power Gain versus Output Power

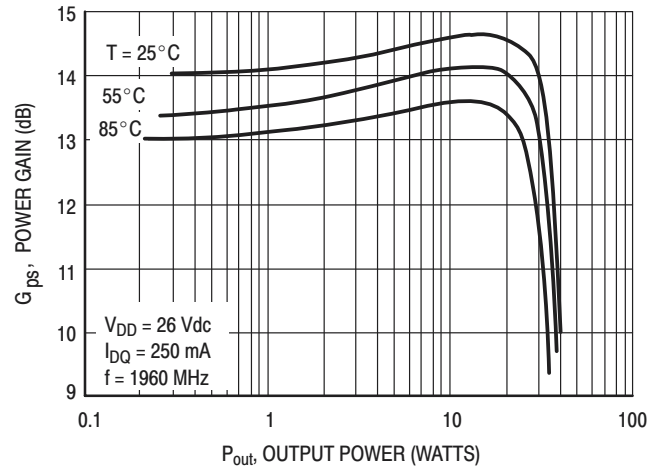


Figure 6. Power Gain versus Output Power

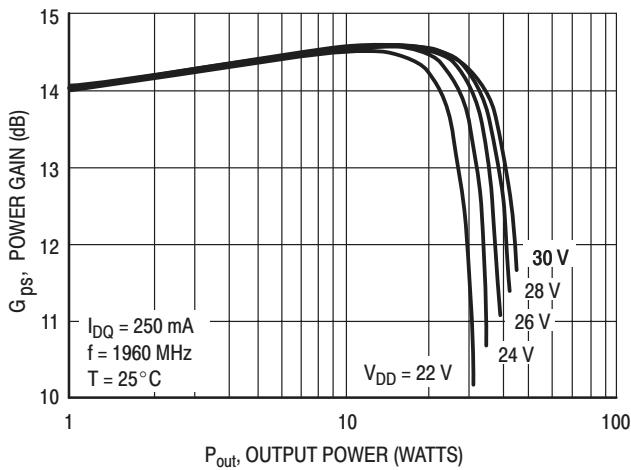


Figure 7. Power Gain versus Output Power

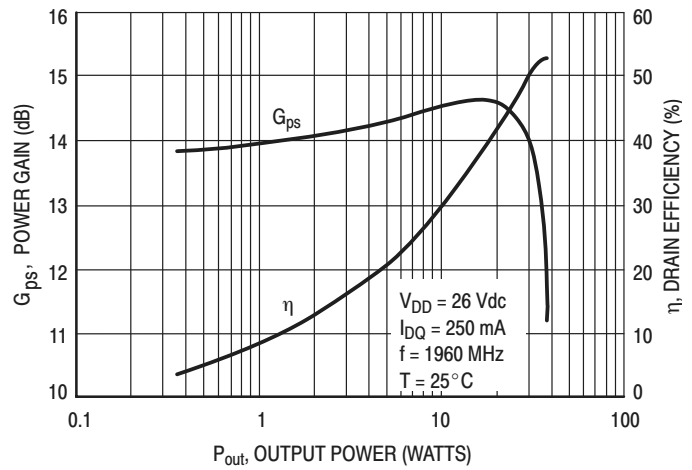
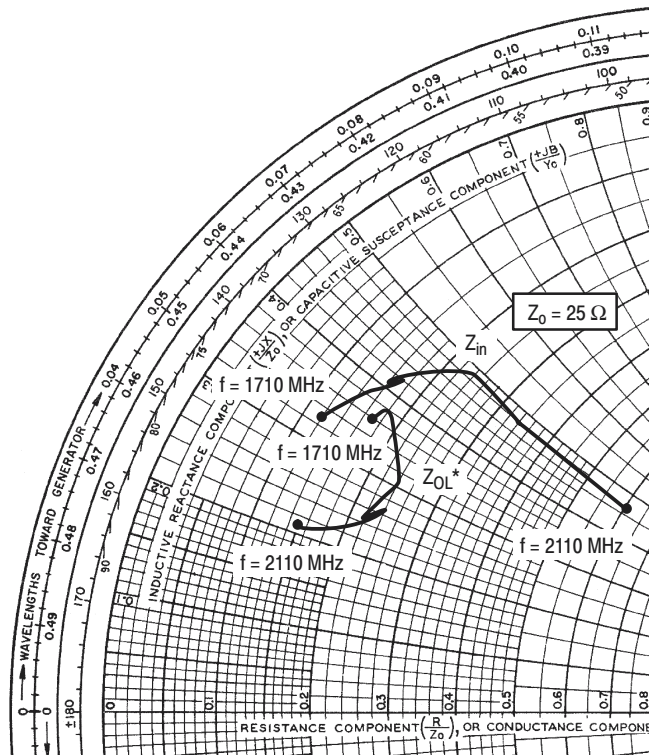


Figure 8. Power Gain and Efficiency versus Output Power



$V_{DD} = 26 \text{ V}$ ,  $I_{DQ} = 250 \text{ mA}$ ,  $P_{out} = 30 \text{ W (CW)}$

f MHz	$Z_{in}$ $\Omega$	$Z_{OL}^*$ $\Omega$
1710	$2.92 + j8.24$	$4.18 + j9.06$
1785	$3.84 + j9.75$	$4.59 + j9.46$
1805	$4.15 + j10.38$	$4.98 + j9.06$
1840	$4.04 + j10.22$	$6.10 + j7.63$
1880	$6.12 + j12.29$	$5.83 + j6.89$
1960	$6.20 + j12.29$	$5.55 + j6.33$
1990	$8.61 + j12.10$	$5.93 + j6.66$
2110	$15.19 + j11.85$	$3.82 + j5.33$

$Z_{in}$  = Complex conjugate of the source impedance.

$Z_{OL}^*$  = Complex conjugate of the optimum load impedance at a given power, voltage, bias current and frequency.

Note:  $Z_{OL}^*$  was chosen based on tradeoffs between gain, output power, and drain efficiency.

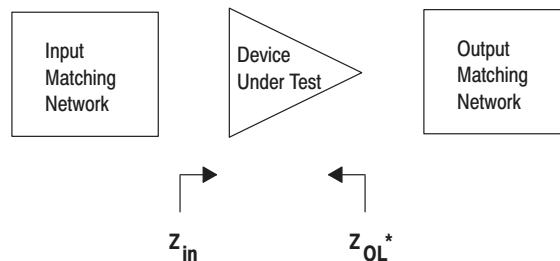
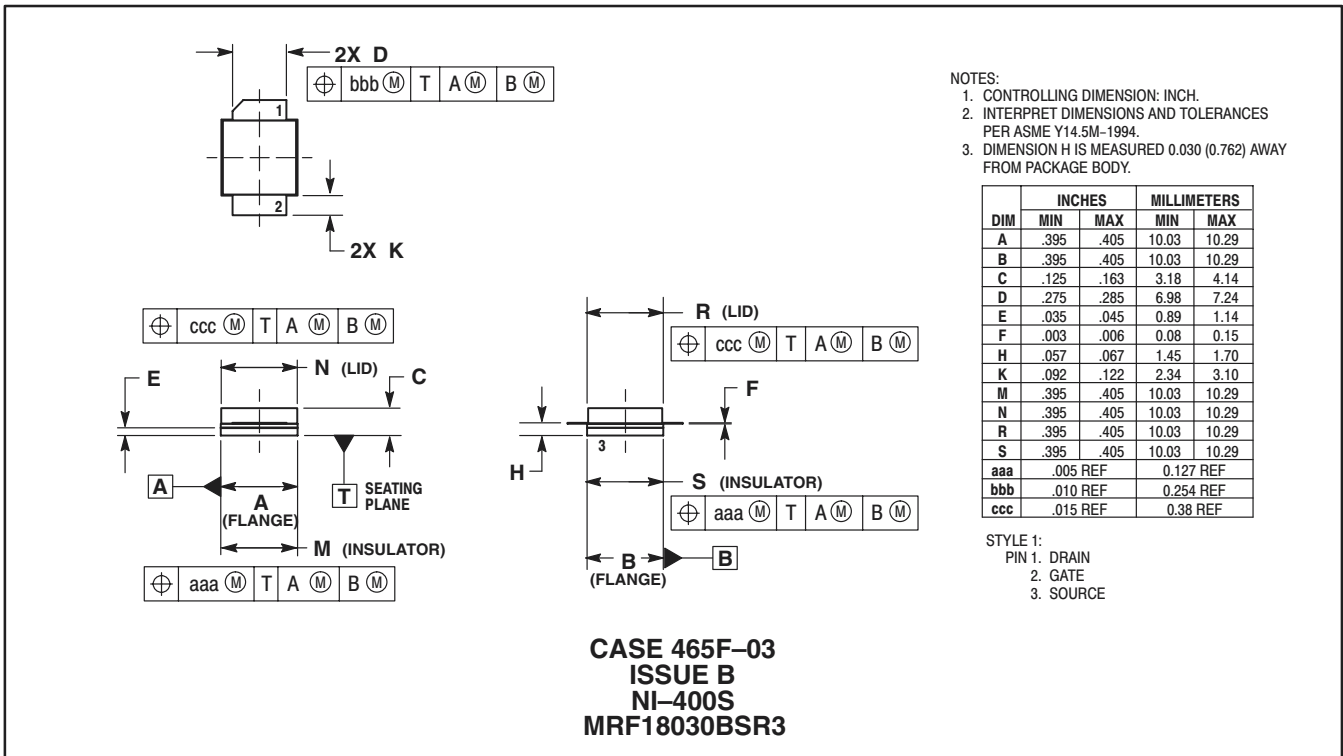
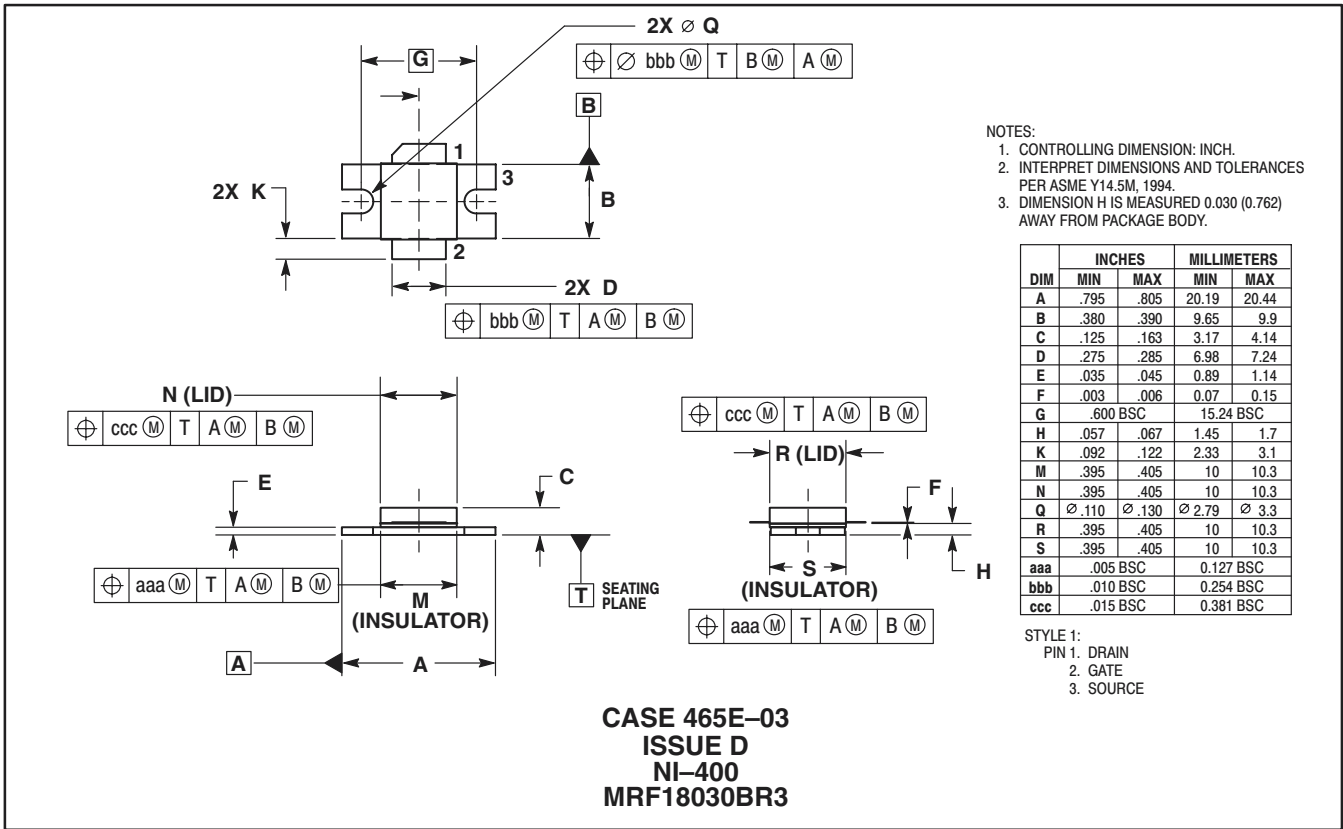



Figure 9. Series Equivalent Input and Output Impedance

# NOTES

## PACKAGE DIMENSIONS



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