**MX•COM, INC. MiXed Signal ICs**

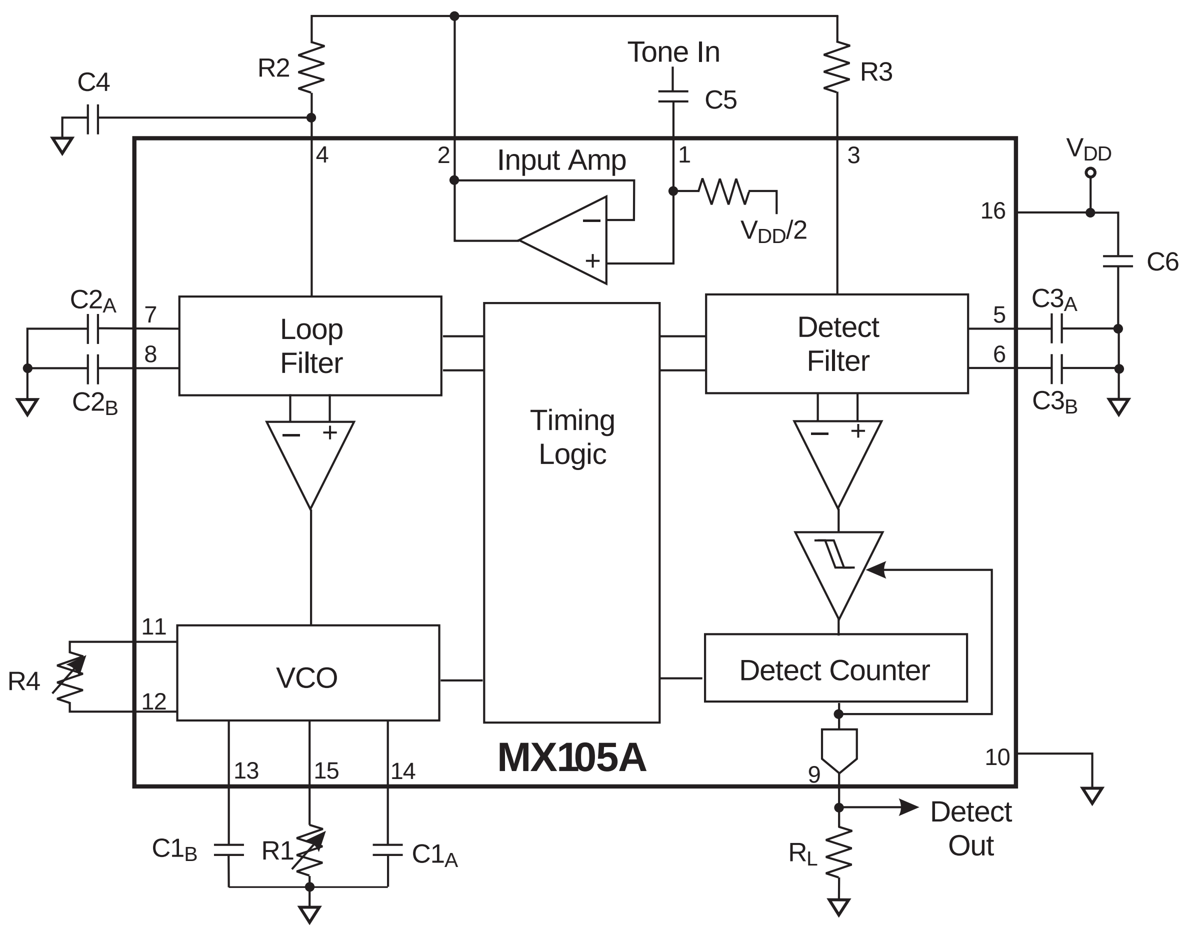
DATA BULLETIN

# MX105A Tone Detector

**PRELIMINARY INFORMATION**

- **FEATURES**
- **Operates in High Noise Conditions**
- **≥36 dB Signal Input Range**
- **High Sensitivity**
- **Low Power Operation 2.7 V to 5.5 V**
- **Adjustable Bandwidth**
- **Adjustable Frequency**

- **APPLICATIONS**
- **Single and Multitone System Applications**




The MX105A is a monolithic CMOS tone detector for tone decoding in single and multitone signaling systems. Using phase locked loop (PLL) decoding techniques, the MX105A recognizes tones in the presence of high noise levels and strong adjacent channel tones. Detection frequency and bandwidth can each be independently adjusted. The design is immune to high levels of harmonic and sub-harmonic noise. It also maintains excellent noise immunity and constant bandwidth over a wide range of input signal levels.

The MX105A requires a voltage supply of 2.7V to 5.5V and is available in the following package styles: 16-pin SOIC (MX105ADW), 16-pin PDIP (MX105AP), and 24-pin PLCC (MX105ALH).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# 1. Block Diagram

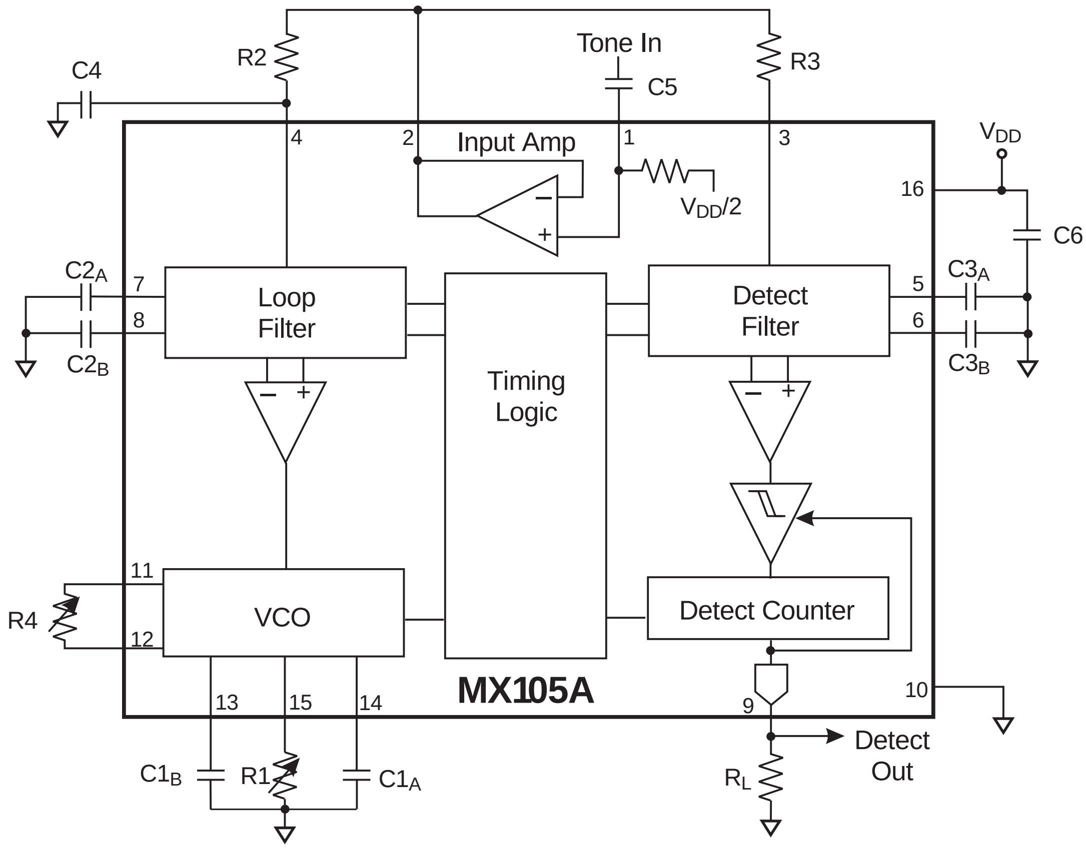


**Figure 1: Block Diagram**

## 2. Signal List

| Pin No. | Pin No. | Name | Type | Description |
|---|---|---|---|---|
| DW/P | LH | | | |
| 1 | 1 | INPUT AMP IN | input | AC couple to this input. Nominal input impedance is 200 kΩ. |
| 2 | 3 | INPUT AMP OUT | output | Nominal output impedance is 1 kΩ. |
| 3 | 5 | R3 | input | Detect filter resistor pin. |
| 4 | 6 | R2 | input | PLL loop filter resistor pin. For improved performance C4 may be chosen to provide 30° of phase shift at the loop filter input. |
| 5 | 7 | $C3_A$ | output | Detect filter capacitor pin A |
| 6 | 8 | $C3_B$ | output | Detect filter capacitor pin B |
| 7 | 10 | $C2_A$ | output | Loop filter capacitor pin A |
| 8 | 11 | $C2_B$ | output | Loop filter capacitor pin B |
| 9 | 13 | DETECT OUT | output | PMOS open drain output - active on detect. |
| 10 | 14 | $V_{SS}$ | power | Ground. |
| 11 | 16 | $R4_A$ | input | Bandwidth control resistor pin A |
| 12 | 17 | $R4_B$ | input | Bandwidth control resistor pin B |
| 13 | 19 | $C1_B$ | output | VCO capacitor B |
| 14 | 20 | $C1_A$ | output | VCO capacitor A |
| 15 | 22 | R1 | input | VCO discharge resistor. When potentiometer tuning is required, a series resistor is recommend to prevent possible shorting to ground. |
| 16 | 24 | $V_{DD}$ | power | Power supply. |


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# 3. External Components

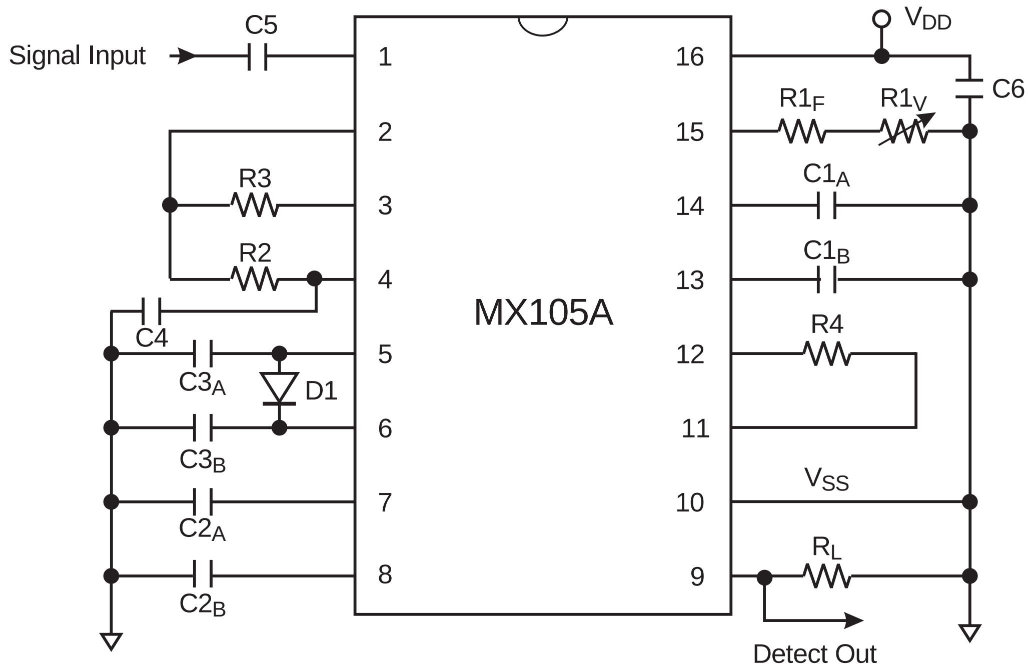


**Figure 2: Recommended External Components**

| | | | |
|---|---|---|---|
| $R1_F$ | See Section 5.2 | 300kΩ | |
| $R1_V$ | See Section 5.2 | 100kΩ | |
| R2 | See Section 5.6 | | |
| R3 | See Section 5.8 | | |
| R4 | See Section 5.5 | | |
| $R_L$ | Note 4 | 20kΩ | ±20% |
| $C1_A$ | See Section 5.2 Note 2 | | |
| $C1_B$ | See Section 5.2 Note 2 | | |

| | | | |
|---|---|---|---|
| $C2_A$ | See section 5.6 Note 2 | | |
| $C2_B$ | See Section 5.6 Note 2 | | |
| $C3_A$ | See Section 5.8 Note 2 | | |
| $C3_B$ | See Section 5.8 Note 2 | | |
| C4 | See Section 5.11 Note 1, 2 | | |
| C5 | | 0.27µF | ±20% |
| C6 | | 0.1µF | ±20% |
| D1 | See Section 5.9 Note 3 | small signal diode (1N914) | |

**External Components Notes:**

1. For improved performance, C4 may be chosen to provide 30° phase shift at the VCO loop filter input.
2. For compatibility with the MX105; capacitors (C1 - C4) may be connected to $V_{DD}$ instead of $V_{SS}$.
3. For improved de-response time, a diode (D1) may be added.
4. Any value load resistance ($R_L$) may be used, providing the maximum load current does not exceed the value given in 'Maximum Ratings Specifications'.

# 4. General Description

The MX105A implements a frequency detector with a phase locked loop (PLL) and a lock detector. The voltage controlled oscillator (VCO) center frequency, detection bandwidth, loop filter, and detect filter are all independently controlled by external components.

The MX105A provides a pair of pseudo-sinewave multipliers for splitting the input signal into approximately orthogonal components. These multipliers are implemented with commutating filters (cyclically sampling filters) which translate an in band AC input signal to DC. The commutating loop filter is used as the phase detector of the PLL while the commutating detect filter provides for lock detection. Each pseudo-sinewave has a cyclic form (1 1 0 -1 -1 0) to eliminate low order harmonic responses. The loop filter produces an error signal, which when applied to the VCO input allows frequency locking. A limiter between the loop filter output and the VCO input provides tunable control of the detection bandwidth (BW). Once lock is achieved the detect filter produces a DC value proportional to the input tone amplitude. An internally generated reference is compared to the detect filter output to determine whether the PLL is locked to an input tone. Once lock is determined the internal reference is reduced by 50% to minimize output chatter with marginal input signals.

The sampling clocks of the detect filter lag those of the loop filter by 60°. To improve performance, a capacitor (C4) can be used to phase shift the input to the loop filter by 30°. This shifts all sampling clocks an additional 30° relative to the input tone to phase align the detect filter sampling clocks with the amplitude peaks of the input tone.

Figure 3 shows the sampling clocks relative to an in band input tone; this figure represents the steady state 'locked' condition without C4.

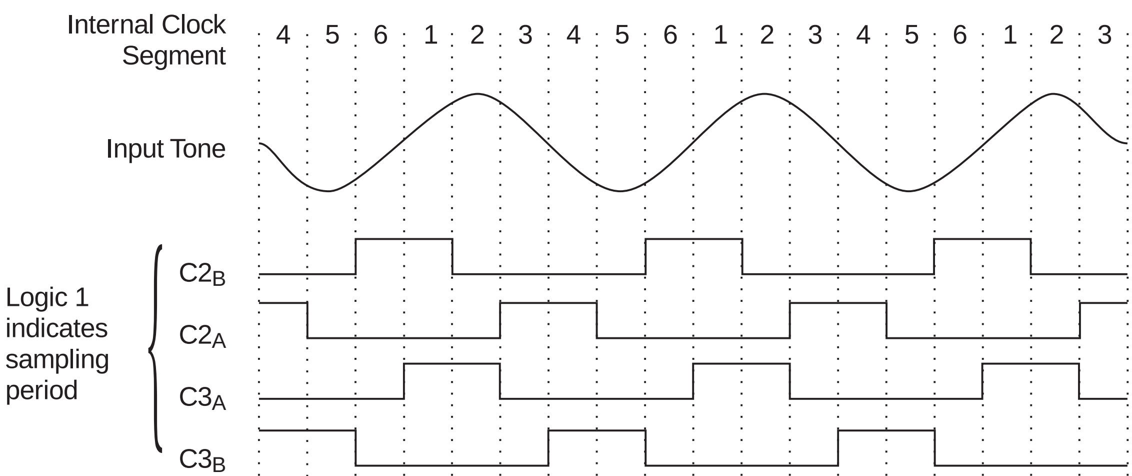


**Figure 3: Sampling Clocks of Commutating Filters**

# 5. Application

The external components shown in Figure 2 are used to adjust the various performance parameters of the MX105A. The signal-to-noise performance, response time and signal bandwidth are all interrelated factors which should be optimized to meet the requirements of the application.

By selecting component values in accordance with the following formulas, optimum circuit performance is obtained for any given application.

First define the following application parameters:

A. The center frequency to be detected ($f_0$).

B. The MX105A Minimum Usable Bandwidth (MUBW). This is obtained by taking into account the worst case tolerances on the input tone frequency and variations in the MX105A $f_0$ due to supply voltage and any temperature effect of the MX105A and its supporting components.

C. The maximum permissible MX105A response time.

D. The minimum input signal amplitude.

**Note:** Using this information the appropriate component values can be calculated, and the signal-to-noise performance can be read from a chart. Do not add large safety margins for response time and minimum signal amplitude; reasonable margins are already included in the formulas. Excessive margins may result in reduced noise immunity.

## 5.1 Method for Calculating External Component Values

The examples on the following pages demonstrate the calculation of component values for any given application. For the purpose of the examples, the values below are used:

A. $f_0$ = 2800 Hz

B. $\Delta$TEMP = 100 °C, $\Delta V_{DD}$ = 1V, $\Delta f_{IN}$ = 0.5%

C. Maximum allowed response time = 50ms

D. Minimum input signal amplitude = 200 $mV_{RMS}$.

## 5.2 Define $f_0$

The components R1, $C1_A$ and $C1_B$ set the free running frequency of the VCO and therefore the $f_0$ of the MX105A. As shown below, the frequency of 2800 Hz corresponds to a capacitor value of 220pF and a resistor value of 385 kΩ. This resistance can be achieved with a 300 kΩ fixed resistor for $R1_F$ and for $R1_V$ a 100 kΩ potentiometer. The capacitance of $C1_A$ and $C1_B$ should include 10-20pF parasitic capacitance due to the device and its package plus any board parasitic capacitance.

$$f_0 = \frac{1}{K \cdot R1(C1_A + C1_B)} \Rightarrow R1 \times C1_A = \frac{1}{2Kf_0}$$

$$\text{where: } K = 2.1 \pm 5\%$$
$$R1 = (R1_F + R1_V)$$

## 5.3 Calculate Minimum Usable Bandwidth

Minimum Usable Bandwidth (MUBW) is the TOTAL bandwidth required for the following:

A. Input signal frequency tolerance

B. MX105A $f_0$ temperature coefficient ($T_C$ = 100 ppm/°C)

C. MX105A $f_0$ supply voltage coefficient ($V_C$ = 5000 ppm/V)

**Note:** Add A, B and C and express as TOTAL bandwidth, not as a ± percentage (%) value.

$$\text{MUBW} = \Delta f_0 + T_C \Delta\text{TEMP} + V_C \Delta V$$
$$\text{MUBW} = 0.5 + 0.01 \times 100 + 0.5 \times 1 = 2\%$$

## 5.4 Calculate The Recommended Operating Bandwidth

$$BW = \frac{10 + \text{MUBW}}{2} = \frac{10 + 2}{2} = 6\%$$

## 5.5 Select R4 for Operating BW

$$R4 = \frac{4.8 \times BW}{10.35 - BW} = \frac{4.8 \times 6}{10.35 - 6} \approx 6.8k\Omega$$

The exact bandwidth given by any value of R4 will vary slightly. In applications where an exact bandwidth is required, R4 should be a variable resistor to permit adjustment.

## 5.6 Calculate $R2 \times C2_A$

$$R2 \times C2_A \approx \frac{100}{3 \times f_0 \times BW}$$

For a frequency of 2800 Hz, a bandwidth of 6%, and a choice of $C2_A = 0.01\mu F \Rightarrow R_V = 200k\Omega$.

**Note:** Use nearest preferred values.

## 5.7 Define Maximum Allowed Response Time

The maximum response time ($T_{ON}$) is the sum of the VCO lock time ($T_{LOCK}$) and the DETECT integration time ($T_{DETECT}$). The MX105A's $T_{ON}$ must not exceed the maximum time allowed for the application, but a value lying near the maximum gives the best S/N performance.

A. Calculate $T_{LOCK}$

$$T_{LOCK} = \frac{150}{f_0 \times BW}$$

Using the formula above, for a frequency of 2800 Hz and a bandwidth of 6% the approximate Lock time ($T_{LOCK}$) will be 9 ms. Since the maximum response time is 50 ms, a DETECT time of 41 ms is allowed.

**Note:** $T_{LOCK}$ may vary from near zero to the value given, causing corresponding variations in actual $T_{ON}$.

B. Calculate Maximum Allowable $T_{DETECT}$

$$T_{DETECT} = T_{ON_{MAX}} - T_{LOCK}$$

C. Define Minimum Expected Signal Amplitude $\left(V_{IN_{MIN}}\right)$

This is used in calculating $T_{DETECT}$ components.

## 5.8 Calculate $R3 \times C3_A$

$$R3 \times C3_A \approx \frac{T_{DETECT}}{-3 \times \ln\left(1 - \frac{V_{TH}}{V_{IN_{MIN}}}\right)}$$

where: $V_{TH}$ is the detect filter sensitivity.

**Note:**

1. For a signal amplitude of 200 $mV_{RMS}$, a resistor value R3 of 510 kΩ with a 0.1µF capacitor for $C3_A$ and $C3_B$ will yield a $T_{DETECT}$ time of 20ms. This in turn yields a response time of 9ms + 20 ms = 29ms.
2. Use nearest preferred values.

## 5.9 Calculate Maximum De-response Time

$$T_{OFF} \approx -3 \times \ln\left(\frac{V_{TH}}{V_{IN_{MAX}}}\right) R3 \times C3_A$$

where: $V_{TH}$ is the detect filter sensitivity.

For improved de-response time, a diode (1N914 or similar) can be placed between pins 5 and 6, as shown in Figure 3. The formula and figure below show the approximate time the MX105A will take to turn off after an in-band signal has been removed. The effect of this diode is to greatly reduce the turn-off time with signal input amplitudes greater than 300 $mV_{RMS}$. This graph is for $V_{DD}$ = 5V; for lower $V_{DD}$ KDT increases.

$$T_{OFF} \approx K_{DT} \times R3 \times C3_A$$

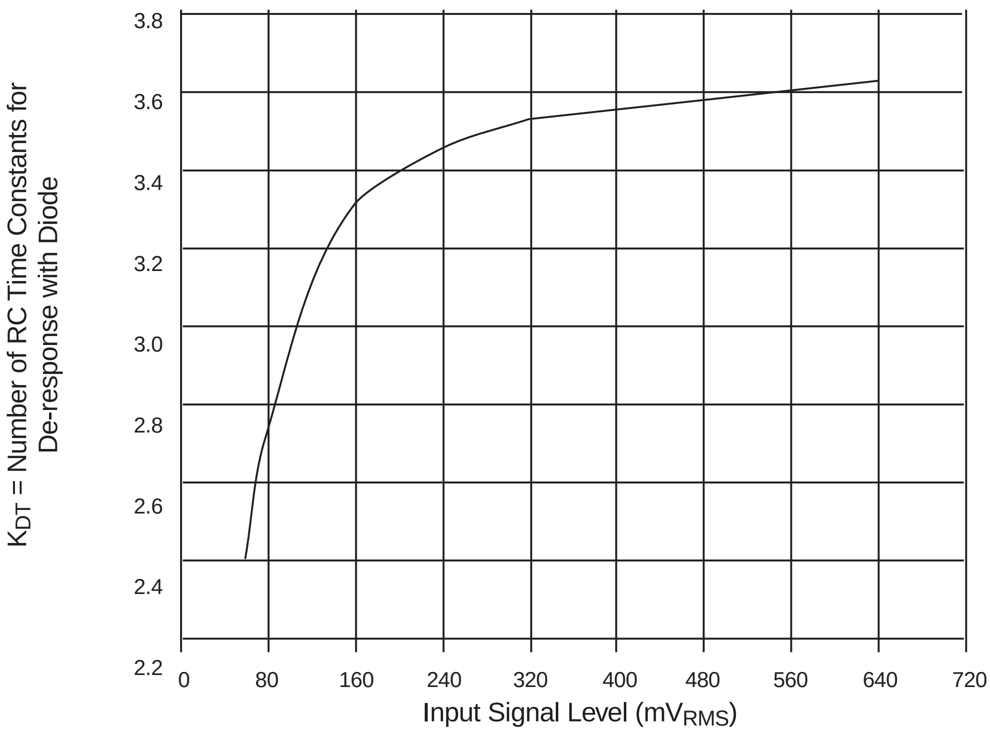


**Figure 4: $K_{DT}$ Factor for $T_{OFF}$ vs. Signal Input Amplitude**

## 5.10 Calculate Signal to Noise Performance

Worst-case S/N calculations depend on calculation of a value "M" using the formula shown below:

$$M = \frac{R3 \times C3_A}{3 \times R2 \times C2_A}$$

substituting example values,

$$M = \frac{510 \times 0.1}{3 \times 200 \times 0.01} = 8.5$$

By substituting this value for M in Figure 5, the minimum required S/N of an in band tone with respect to an adjacent interfering tone can be found. This then has to be increased depending on the input tone amplitude.

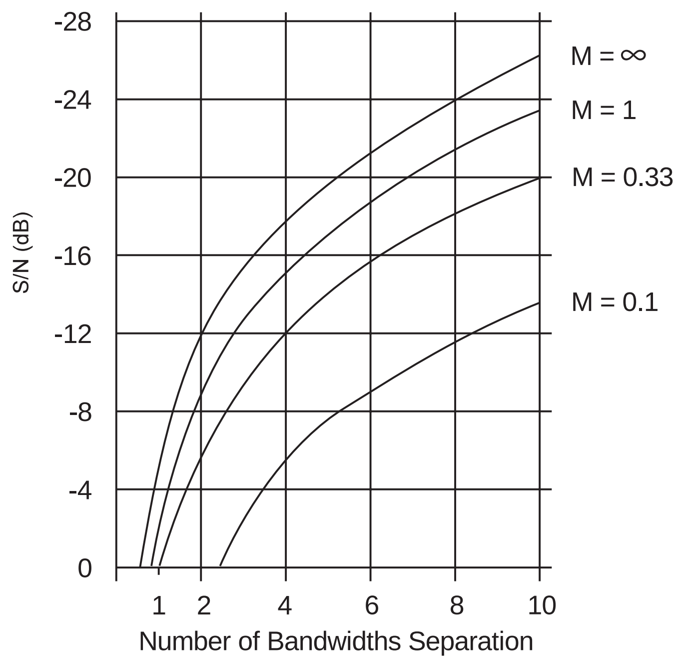


**Figure 5: S/N vs. BW Separation**

The following formula expresses the reduction in noise immunity as the input signal approaches the detect filter sensitivity $V_{TH}$.

$$\text{required } \frac{S}{N} = 20\log\left(\frac{V_{IN}}{V_{IN} - V_{TH}}\right) + \frac{S}{N}_{\text{Figure 5}}$$

If this S/N is better than required for the application, $R3 \times C3_A$ can be reduced, or the operating bandwidth can be increased to obtain a faster tone detection time.

If the S/N performance is not adequate, the operating bandwidth can be reduced toward the MUBW, or $R3C3_A$ can be increased to improve S/N performance at the expense of slower response time.

## 5.11 Calculate C4 for 30° Phase Shift

Capacitor C4 is used to phase shift the input to the VCO commutating filter by 30°, thereby shifting the sampling clocks by the same amount. This enables the Detect sampling filter to sample and integrate at the maximum and minimum of the input tone.

$$C4 = \frac{\tan(30^\circ)}{2\pi \times f_0 \times R_V} \approx \frac{0.092}{f_0 \times R_V} \approx 164\text{pF}$$

# 6. Performance Specification

## 6.1 Electrical Performance

### 6.1.1 Absolute Maximum Ratings

Exceeding these maximum ratings can result in damage to the device.

| **General** | **Min.** | **Max.** | **Units** |
|---|---|---|---|
| Supply ($V_{DD}$ - $V_{SS}$) | -0.3 | 7.0 | V |
| Voltage on any pin (wrt $V_{SS}$) | -0.3 | $V_{DD}$ + 0.3 | V |
| Current | | | |
| $V_{DD}$ | -30 | 30 | mA |
| $V_{SS}$ | -30 | 30 | mA |
| Any other pins | -20 | 20 | mA |
| Max. Output Switch Load Current | | 10 | mA |
| **P/LH/DW Package** | | | |
| Device Dissipation at $T_{AMB}$ = 25°C | | 800 | mW |
| Derating above 25°C | | 13 | mW/°C above 25°C |
| Storage Temperature | -40 | 85 | °C |
| Operating Temperature | -30 | 85 | °C |

### 6.1.2 Operating Limits

Correct operation of the device outside these limits is not implied.

| | **Notes** | **Min.** | **Typ.** | **Max.** | **Units** |
|---|---|---|---|---|---|
| Supply ($V_{DD}$ - $V_{SS}$) | | 2.7 | 3.3/5.0 | 5.5 | V |
| Operating Temperature | | -30 | | 85 | °C |


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### 6.1.3 Operating Characteristics

For the following conditions unless otherwise specified:

$V_{DD}$ = 5.0 V @ $T_{AMB}$ = 25°C
Load resistance on decoder output = 20kΩ.

| | Notes | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| **Static Parameters** | | | | | |
| $I_{DD}$ | | | 1.0 | | mA |
| Amplifier Input Impedance | | 160 | 200 | | kΩ |
| Digital Output Impedance | | | 500 | 1000 | Ω |
| Analog Output Impedance | | | 1000 | 1200 | Ω |
| **Dynamic Parameters** | | | | | |
| Input Signal | | | | | |
| Frequency | | 40 | | 20,000 | Hz |
| Lowest Must Detect Level | 1 | | 30 | | $mV_{RMS}$ |
| Highest Will Not Detect Level | 1 | | 20 | | $mV_{RMS}$ |
| Highest Will Not Detect $f_0/2$ | 1, 2 | | 30<br>790 | | dB<br>$mV_{RMS}$ |
| Highest Will Not Detect $5(f_0)$ | 1, 2 | | 20<br>250 | | dB<br>$mV_{RMS}$ |
| VCO | | | | | |
| Frequency | 3 | 120 | | 120,000 | Hz |
| Frequency Stability | | | 100<br>5000 | | ppm/°C<br>ppm/V |
| BW Limiter | | | | | |
| BW Range | | 2 | | 10 | $\%f_0$ |
| Amplifier | | | | | |
| Open Loop Gain | | | 60 | | dB |
| GBWP | | | 1.0 | | MHz |
| Closed Loop Gain | | | 0 | | dB |
| Detect Commutating Filter | | | | | |
| Sensitivity ($V_{TH}$) | 1 | | 25 | | $mV_{RMS}$ |

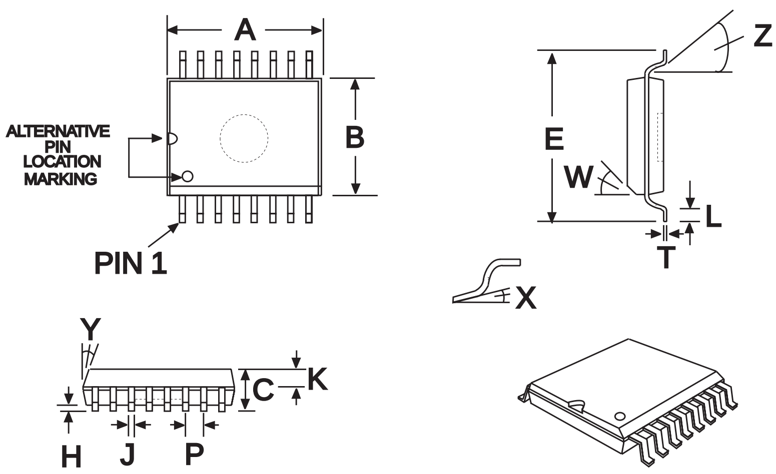
**Operating Characteristics Notes:**

1. Multiply by $V_{DD}$ /5V for other supply values.
2. The reference level is $V_{TH}$. The following formula converts dB to $mV_{RMS}$.

$$mV_{RMS} = 10^{(dB/20)} \times V_{TH}$$

3. Observing pins 13, 14, or 15 (DW/J package) will cause a frequency shift due to additional loading. If tuning center frequency by observing oscillator, design in a buffer amplifier between pin 15 and probe/calibration point and tune with no input signal. Otherwise, tune by observing detect output band edges while sweeping input signal. VCO center frequency is $6(f_0)$ at pin 15 while it is $3(f_0)$ at pins 13 and 14.

## 6.2 Packaging

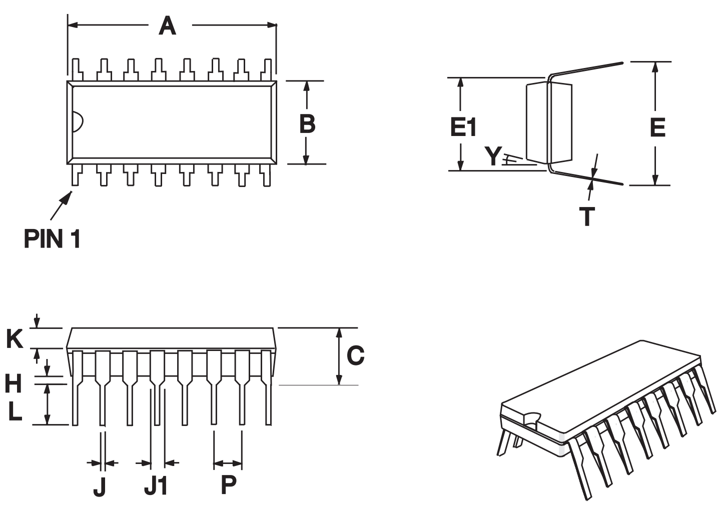



### Package Tolerances

| DIM. | MIN. | TYP. | MAX. |
|---|---|---|---|
| A | 0.395 (10.03) | | 0.413 (10.49) |
| B | 0.286 (7.26) | | 0.299 (7.59) |
| C | 0.093 (2.36) | | 0.105 (2.67) |
| E | 0.390 (9.90) | | 0.419 (10.64) |
| H | 0.003 (0.08) | | 0.020 (0.51) |
| J | 0.013 (0.33) | | 0.020 (0.51) |
| K | | 0.041 (1.04) | |
| L | 0.016 (0.41) | | 0.050 (1.27) |
| P | | 0.050 (1.27) | |
| T | 0.009 (0.23) | | 0.0125 (0.32) |
| W | | 45° | |
| X | 0° | | 10° |
| Y | 5° | | 7° |
| Z | | 5° | |

NOTE : All dimensions in inches (mm.)
Angles are in degrees

**Figure 6: 16-pin SOIC Mechanical Outline:** ***Order as part no. MX105ADW***

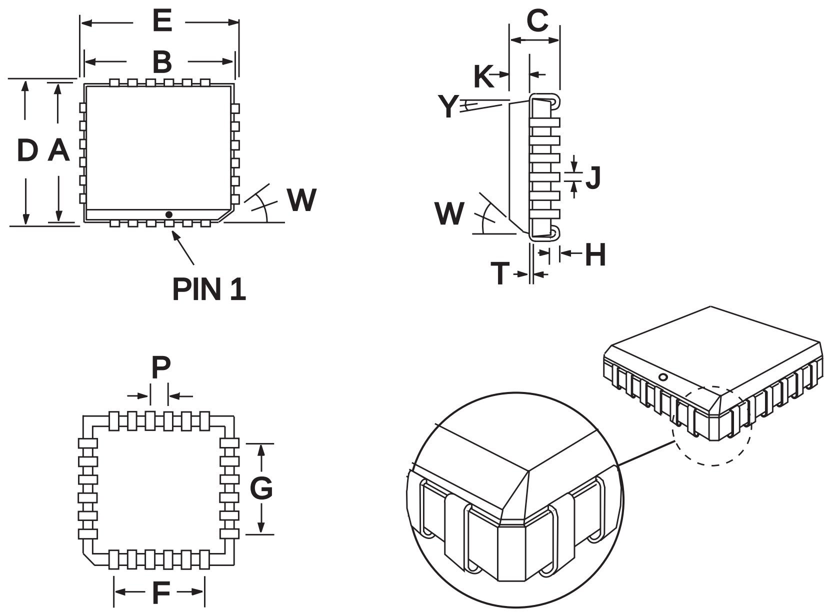



### Package Tolerances

| DIM. | MIN. | TYP. | MAX. |
|---|---|---|---|
| A | 0.740 (18.80) | | 0.810 (20.57) |
| B | 0.240 (6.10) | | 0.262 (6.63) |
| C | 0.135 (3.43) | | 0.200 (5.06) |
| E | 0.300 (7.62) | | 0.390 (9.91). |
| E1 | 0.290 (7.37) | | 0.325 (8.26) |
| H | 0.015 (0.38) | | 0.070 (1.77) |
| J | 0.014 (0.35) | | 0.023 (0.58) |
| J1 | 0.040 (1.02) | | 0.065 (1.65) |
| K | 0.056 (1.42) | | 0.064 (1.63) |
| L | 0.121 (3.07) | | 0.150 (3.81) |
| P | | 0.100 (2.54) | |
| T | 0.008 (0.20) | | 0.015 (0.38) |
| Y | | 7e | |

NOTE : All dimensions in inches (mm.)
Angles are in degrees

**Figure 7: 16-pin PDIP Mechanical Outline:** ***Order as part no. MX105AP***




## Package Tolerances

| DIM. | MIN. | TYP. | MAX. |
|---|---|---|---|
| A | 0.380 (9.61) | | 0.409 (10.40) |
| B | 0.380 (9.61) | | 0.409 (10.40) |
| C | 0.128 (3.25) | | 0.146 (3.70) |
| D | 0.417 (10.60) | | 0.435 (11.05) |
| E | 0.417 (10.60) | | 0.435 (11.05) |
| F | | 0.250 (6.35) | |
| G | | 0.250 (6.35) | |
| H | | 0.023 (0.58) | |
| J | 0.018 (0.45) | | 0.022 (0.55) |
| K | 0.047 (1.19) | | 0.048 (1.22) |
| P | 0.049 (1.24) | | 0.051 (1.30) |
| T | 0.006 (0.152) | | 0.009 (0.22) |
| W | 30° | 45° | |
| Y | | 6° | |

NOTE : All dimensions in inches (mm.)
Angles are in degrees

**Figure 8: 24-pin PLCC Mechanical Outline:** ***Order as part no. MX105ALH***

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# CML Product Data

In the process of creating a more global image, the three standard product semiconductor companies of CML Microsystems Plc *(Consumer Microcircuits Limited (UK), MX-COM, Inc (USA) and CML Microcircuits (Singapore) Pte Ltd)* have undergone name changes and, whilst maintaining their separate new names *(CML Microcircuits (UK) Ltd, CML Microcircuits (USA) Inc and CML Microcircuits (Singapore) Pte Ltd*), now operate under the single title **CML Microcircuits**.
These companies are all 100% owned operating companies of the CML Microsystems Plc Group and these changes are purely changes of name and do not change any underlying legal entities and hence will have no effect on any agreements or contacts currently in force.

## CML Microcircuits Product Prefix Codes

Until the latter part of 1996, the differentiator between products manufactured and sold from MXCOM, Inc. and Consumer Microcircuits Limited were denoted by the prefixes MX and FX respectively. These products use the same silicon etc. and today still carry the same prefixes. In the latter part of 1996, both companies adopted the common prefix: CMX.

This notification is relevant product information to which it is attached.

## CML Microcircuits (USA) [formerly MX-COM, Inc.] Product Textual Marking

On CML Microcircuits (USA) products, the **'MX-COM'** textual logo is being replaced by a **'CML'** textual logo.

Company contact information is as below:


**CML Microcircuits (UK) Ltd**
*COMMUNICATION SEMICONDUCTORS*

Oval Park, Langford, Maldon,
Essex, CM9 6WG, England
Tel: +44 (0)1621 875500
Fax: +44 (0)1621 875600
uk.sales@cmlmicro.com
www.cmlmicro.com

**CML Microcircuits (USA) Inc.**
*COMMUNICATION SEMICONDUCTORS*

4800 Bethania Station Road,
Winston-Salem, NC 27105, USA
Tel: +1 336 744 5050,
0800 638 5577
Fax: +1 336 744 5054
us.sales@cmlmicro.com
www.cmlmicro.com

**CML Microcircuits (Singapore) Pte Ltd**
*COMMUNICATION SEMICONDUCTORS*

No 2 Kallang Pudding Road, 09-05/
06 Mactech Industrial Building,
Singapore 349307
Tel: +65 7450426
Fax: +65 7452917
sg.sales@cmlmicro.com
www.cmlmicro.com


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