ACE93C46
Three-wire Serial EEPROM

Description

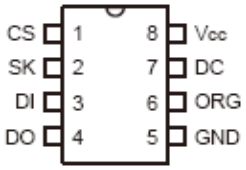
The ACE93C46 provides 1024 bits of serial electrically erasable programmable read only memory (EEPROM) organized as 64 words of 16 bits each, when the ORG pin is connected to VCC and 128 words of 8 bits each when it is tied to ground. The ACE93C46 is available in space-saving 8-lead PDIP, 8-lead TSSOP and 8-lead JEDEC SOIC packages. The ACE93C46 is enabled through the Chip Select pin (CS), and accessed via a 3-wire serial interface consisting of Data Input (DI), Data Output (DO), and Shift Clock (SK). Upon receiving a Read instruction at DI, the address is decoded and the data is clocked out serially on the data output pin DO. The WRITE cycle is completely self-timed and no separate erase cycle is required before write. The Write cycle is only enabled when it is in the Erase/Write Enable state. When CS is brought "high" following the initiation of a write cycle, the DO pin outputs the Ready/Busy status.

Features

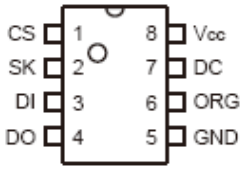
- Low-voltage operation – 1.8 (VCC=1.8 to 5.5V)
- Three-wire serial Interface
- 2MHz clock rate(5V) compatibility
- Self-timed write cycle (5 ms max)
- High-reliability – Endurance: 1 Million write cycles
  Data retention: 100 Years
- 8-lead PDIP, SOP-8, TSSOP-8 Packages

Packaging Type

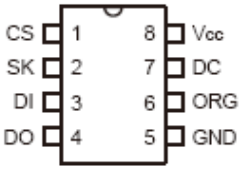
DIP-8



SOP-8



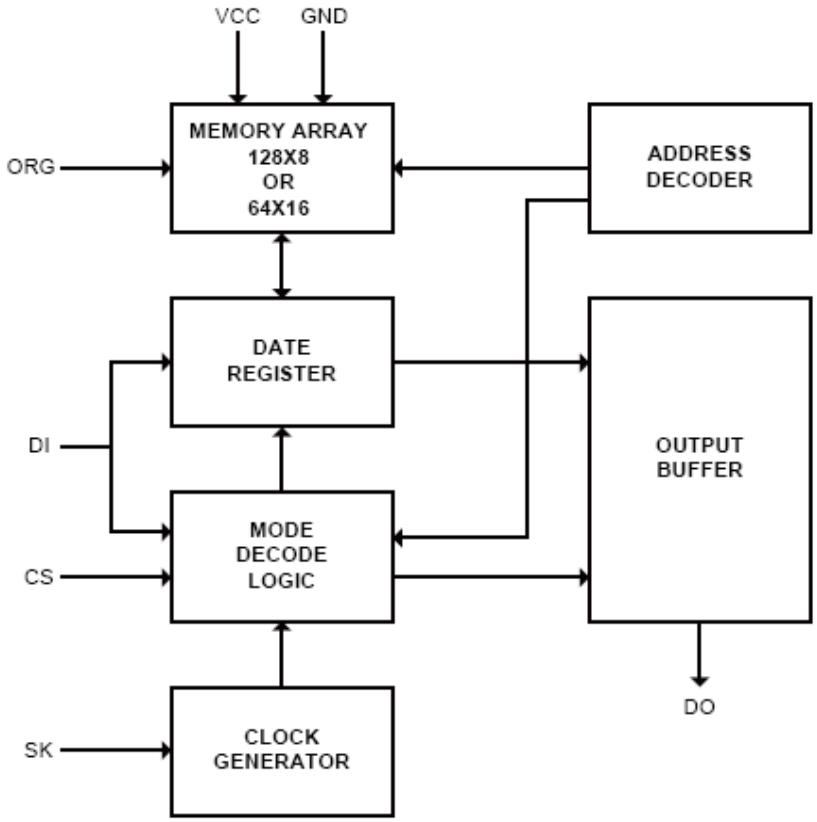
TSSOP-8



Pin Configurations

Pin Name	Function
CS	Chip select
SK	Serial Data Clock
DI	Serial Data Input
DO	Serial Data Output
GND	Ground
Vcc	Power Supply
ORG	Internal Organization
DC	Don't Connect

Block Diagram



Note: When the ORG pin is connected to VCC, the “x 16” organization is selected. When it is connected to ground, the “x 8” organization is selected. If the ORG pin is left unconnected and the application does not load the input beyond the capability of the internal 1 Meg ohm pullup, then the “x 16” organization is selected.

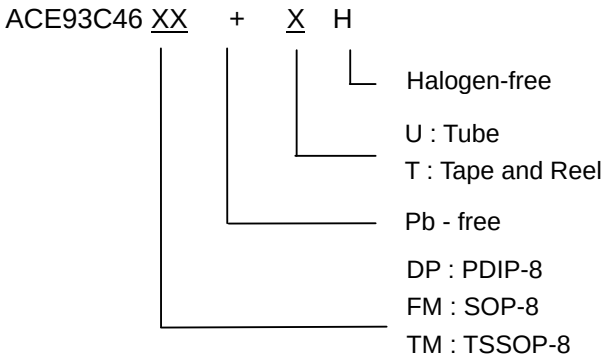
Absolute Maximum Ratings

DC Supply Voltage	-0.3 to 6.5V
Input / Output Voltage	GND -0.3 to Vcc 0.3V
Operating Ambient Temperature	-40 to 85℃
Storage Temperature	-65 to 150℃

*Notice: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to this device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied or intended. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

Ordering information

Selection Guide



Pin Capacitance

Applicable over recommended operating range from T_A=25℃, f=1.0MHz,VCC=+1.8V (unless otherwise noted)

Test Conditions	Symbol	Max	Unit	Conditions
Output Capacitance (DO)	COUT	5	pF	VOUT=0V
Input Capacitance (CS, SK, DI)	CIN	5	pF	VIN=0V

DC Characteristics

Applicable over recommended operating range from: T_A = -40℃ to +85℃, V_{CC} = +1.8V to +5.5V, (unless otherwise noted).

Symbol	Parameter	Test Condition	Min	Typ	Max	Units
V_{CC1}	Supply Voltage		1.8		5.5	V
V_{CC2}	Supply Voltage		2.7		5.5	V
V_{CC3}	Supply Voltage		4.5		5.5	V
I_{CC1}	Supply Current	V_{CC} = 5.0V, Read at 1.0MHz Write at 1.0MHz		0.2 0.9	2.0 3.0	mA
I_{SB1}	Standby Current	V_{CC} = 1.8V, CS=0V			1.0	μA
I_{SB2}	Standby Current	V_{CC} = 2.7V, CS=0V			1.0	μA
I_{SB3}	Standby Current	V_{CC} = 5.0V, CS=0V			1.0	μA
$I_{LI(1)}$	Input Leakage	V_{IN} = 0 to V_{CC}		0.1	1.0	μA
$I_{LI(2)}$	Input Leakage	V_{IN} = 0 to V_{CC}		2.0	3.0	μA
I_{OL}	Output Leakage	V_{IN} = 0 to V_{CC}		0.1	1.0	μA
$V_{IL1(3)}$	Input Low Voltage	2.7V≦Vcc≦5.5V	-0.3		0.8	V
$V_{IH1(3)}$	Input High Voltage	2.7V≦Vcc≦5.5V	2.0		Vcc+0.3	V

Symbol	Parameter	Test Condition	Min	Typ	Max	Units
$V_{IL2(3)}$	Input Low Voltage	1.8V≦Vcc≦2.7V	-0.3		Vcc+0.3	V
$V_{IH2(3)}$	Input High Voltage	1.8V≦Vcc≦2.7V	Vcc*0.7		Vcc+0.3	V
V_{OL1}	Output Low Voltage	2.7V≦Vcc≦5.5V IOL=2.1mA			0.4	V
V_{OH1}	Output High Voltage	IOH=-0.4mA	2.4			
V_{OL2}	Output Low Voltage	1.8V≦Vcc≦2.7V IOL=0.15mA			0.2	V
V_{OH2}	Output High Voltage	IOH=-100uA	Vcc-0.2			

Note: 1. DI.CS. SK input pin

2. ORG input pin

3. VIL min and VIH max are reference only and are not tested.

Applicable over recommended operating range from: T_A = -40℃ to +85℃, V_{CC} = +1.8V to +5.5V, CL=1TTL Gate and 100pF (unless otherwise noted).

Symbol	Parameter	Test Condition		Min	Typ	Max	Units
fsx	SK Clock Frequency	4.5≦Vcc≦5.5v 2.7≦Vcc≦5.5V 1.8V≦Vcc≦5.5V		0 0 0		2 1 0.25	MHz
tskh	SK High Time	4.5≦Vcc≦5.5v 2.7≦Vcc≦5.5V 1.8V≦Vcc≦5.5V		250 250 1000			ns
tskl	SK Low Time	4.5≦Vcc≦5.5v 2.7≦Vcc≦5.5V 1.8V≦Vcc≦5.5V		250 250 1000			ns
tcs	Minimum CS Low Time	4.5≦Vcc≦5.5v 2.7≦Vcc≦5.5V 1.8V≦Vcc≦5.5V		250 250 1000			ns
tcss	CS Setup Time	Relative to SK	4.5≦Vcc≦5.5v 2.7≦Vcc≦5.5V 1.8V≦Vcc≦5.5V	50 50 200			ns
tdis	DI Setup Time	Relative to SK	4.5≦Vcc≦5.5v 2.7≦Vcc≦5.5V 1.8V≦Vcc≦5.5V	100 100 400			ns
tcsh	CS Hold Time	Relative to SK		0			ns

Symbol	Parameter	Test Condition		Min	Typ	Max	Units
tdih	DI Hold Time	Relative to SK	4.5≦Vcc≦5.5v 2.7≦Vcc≦5.5V 1.8V≦Vcc≦5.5V	100 100 400			ns
tpd1	Output Delay to “1”	AC Test	4.5≦Vcc≦5.5v 2.7≦Vcc≦5.5V 1.8V≦Vcc≦5.5V			250 250 1000	ns
tpd0	Output Delay to “0”	AC Test	4.5≦Vcc≦5.5v 2.7≦Vcc≦5.5V 1.8V≦Vcc≦5.5V			250 250 1000	ns
tsv	CS to Status Valid	AC Test	4.5≦Vcc≦5.5v 2.7≦Vcc≦5.5V 1.8V≦Vcc≦5.5V			250 250 1000	ns
tdf	CS to DO in High Impedance	AC Test CS=VIL	4.5≦Vcc≦5.5v 2.7≦Vcc≦5.5V 1.8V≦Vcc≦5.5V			100 100 400	ns
twp	Write Cycle Time				1.5	5	ms
Endurance(1)	5.0V, 25℃			1M			Write Cycle

Note: 1. This parameter is characterized and is not 100% tested.

Functional Description

The ACE93C46 is accessed via a simple and versatile three-wire serial communication interface. Device operation is controlled by seven instructions issued by the host processor. A valid instruction starts with a rising edge of CS and consists of a start bit (logic“1”) followed by the appropriate op code and the desired memory address location.

Instruction Set for the ACE93C46

Instruction	SB	OP Code	Address		Data		Comments
			*8	*16	*8	*16	
READ	1	10	A_6-A_0	A_5-A_0			Read data stored in memory, at specified address
EWEN	1	00	11XXXXX	11XXXX			Write enable must precede all programming modes
REASE	1	11	A_6-A_0	A_5-A_0			Erase memory location An-A0
WRITE	1	01	A_6-A_0	A_5-A_0	D_7-D_0	D_{15}-D_0	Writes memory location An-A0
ERAL	1	00	10XXXXX	10XXXX			Erases all memory locations. Valid only at VCC=4.5V to 5.5V
WRAL	1	00	01XXXXX	01XXXX	D_7-D_0	D_{15}-D_0	Writes all memory locations. Valid

							only at VCC=4.5V to 5.5V
EWDS	1	00	00XXXXX	00XXXX			Disables all programming instructions

Notes: The X's in the address field represent don't care values and must be clocked.

READ (READ):

The Read (READ) instruction contains the address code for the memory location to be read. After the instruction and address are decoded, data from the selected memory location is available at the serial output pin DO. Output data changes are synchronized with the rising edges of serial clock SK. It should be noted that a dummy bit (logic "0") precedes the 8- or 16-bit data output string.

ERASE/WRITE (EWEN):

To assure data integrity, the part automatically goes into the Erase/Write Disable (EWDS) state when power is first applied. An Erase/Write Enable(EWEN) instruction must be executed first before any programming instructions can be carried out. Please note that once in the EWEN state, programming remains enabled until an EWDS instruction is executed or VCC power is removed from the part.

ERASE (ERASE):

The Erase (ERASE) instruction programs all bits in the specified memory location to the logical "1" state. The self-timed erase cycle starts once the ERASE instruction and address are decoded. The DO pin outputs the Ready/Busy status of the part if CS is brought high after being kept low for a minimum of 250 ns (TCS). A logic "1" at pin DO indicates that the selected memory location has been erased, and the part is ready for another instruction.

WRITE (WRITE):

The Write (WRITE) instruction contains the 8 or 16 bits of data to be written into the specified memory location. The self-timed programming cycle, tWP, starts after the last bit of data is received at serial data input pin DI. The DO pin outputs the Ready/Busy status of the part if CS is brought high after being kept low for a minimum of 250 ns (TCS). A logic "0" at DO indicates that programming is still in progress. A logic "1" indicates that the memory location at the specified address has been written with the data pattern contained in the instruction and the part is ready for further instructions. A Ready/Busy status cannot be obtained if the CS is brought high after the end of the selftimed programming cycle, TWP.

ERASE ALL (ERAL):

The Erase All (ERAL) instruction programs every bit in the memory array to the logic "1" state and is primarily used for testing purposes. The DO pin outputs the Ready/Busy status of the part if CS is brought high after being kept low for a minimum of 250 ns (TCS). The ERAL instruction is valid only at VCC = 5.0V ± 10%.

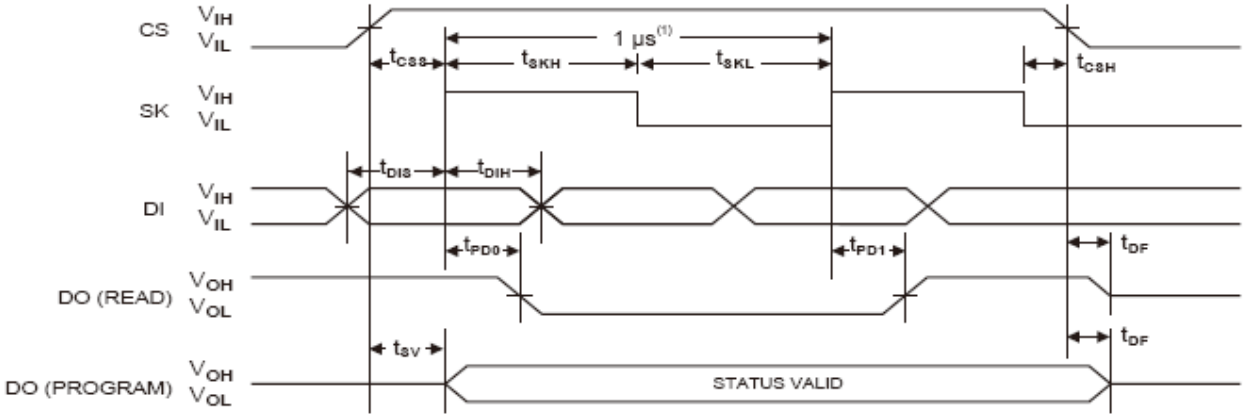
WRITE ALL (WRAL):

The Write All (WRAL) instruction programs all memory locations with the data patterns specified in the instruction. The DO pin outputs the Ready/Busy status of the part if CS is brought high after being kept low for a minimum of 250ns (TCS). The WRAL instruction is valid only at VCC = 5.0V ± 10%.

ERASE/WRITE DISABLE (EWDS):

To protect against accidental data disturb, the Erase/Write Disable (EWDS) instruction disables all programming modes and should be executed after all programming operations. The operation of the Read instruction is independent of both the EWEN and EWDS instructions and can be executed at any time.

Timing Diagrams



Note: This is the minimum SK period.

Figure 1: Synchronous Data Timing

Organization Key for Timing Diagrams

I/O	ACE93C46 (1K)	
	*16	*8
AN	A5	A6
DN	D15	D7

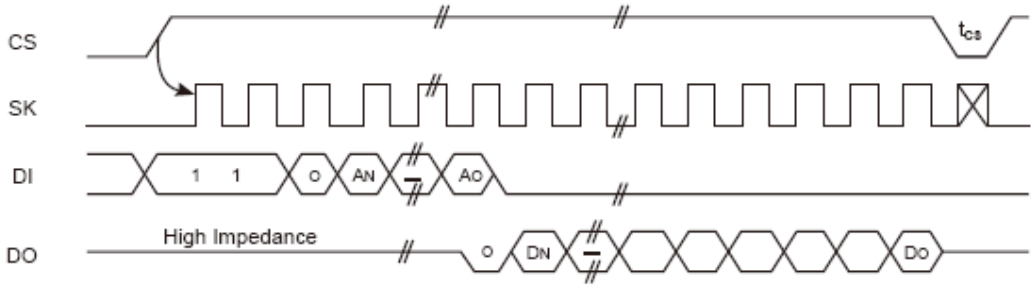


Figure 2: Read Timing

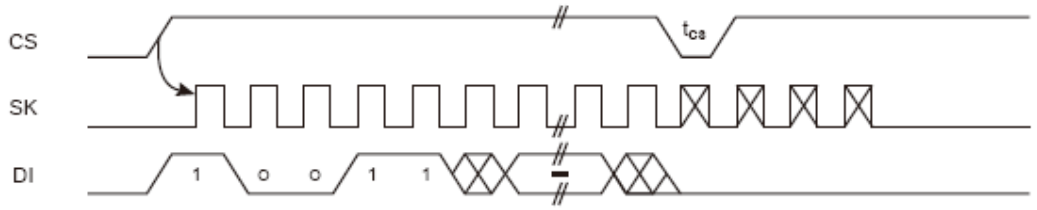


Figure 3: EWEN Timing

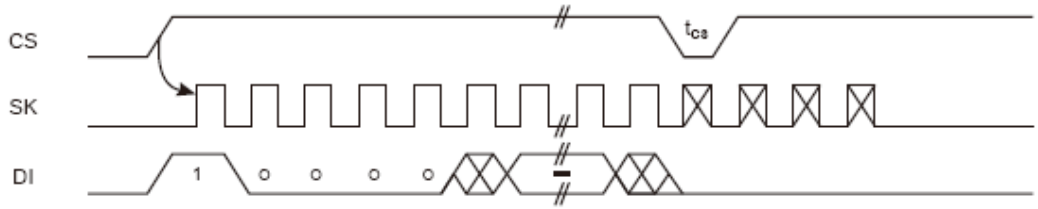


Figure 4: EWDS Timing

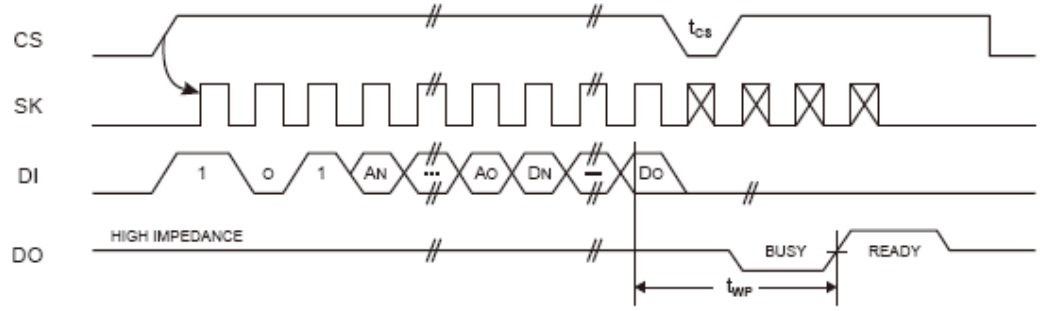
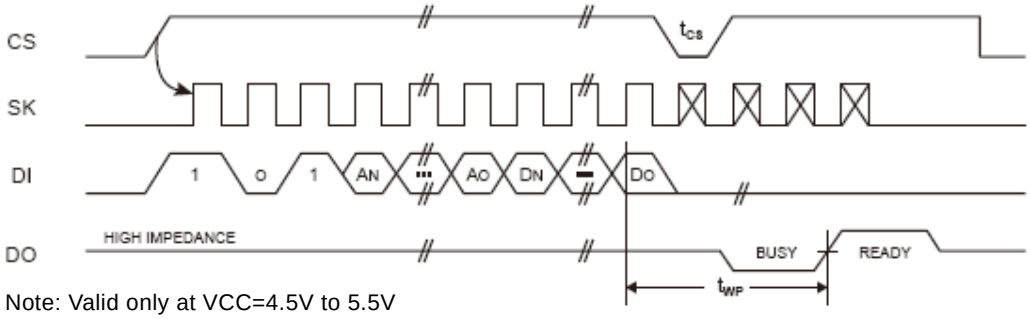


Figure 5: WRITE Timing



Note: Valid only at VCC=4.5V to 5.5V

Figure 6: WRAL Timing (1)

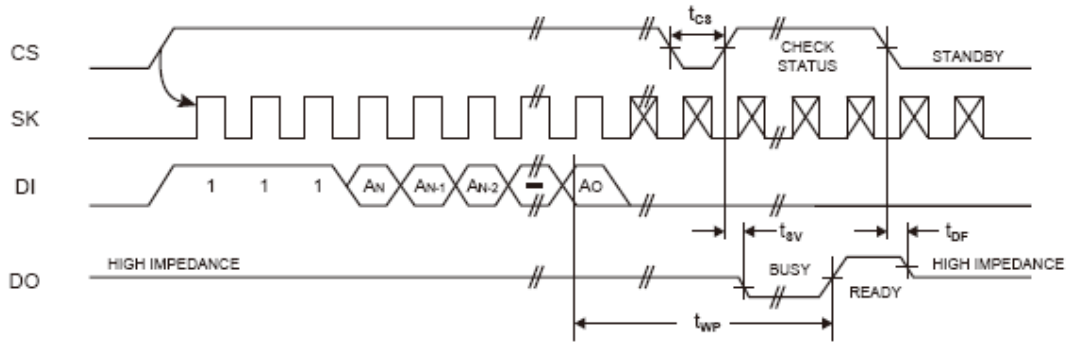
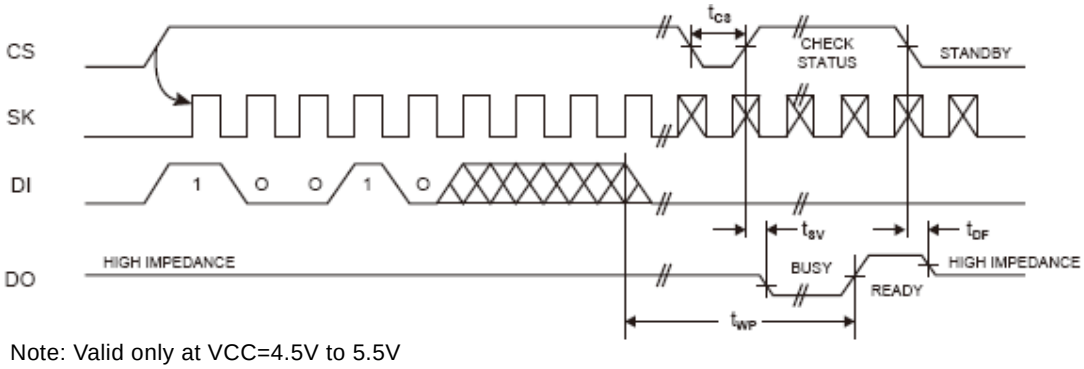


Figure 7: ERASE Timing

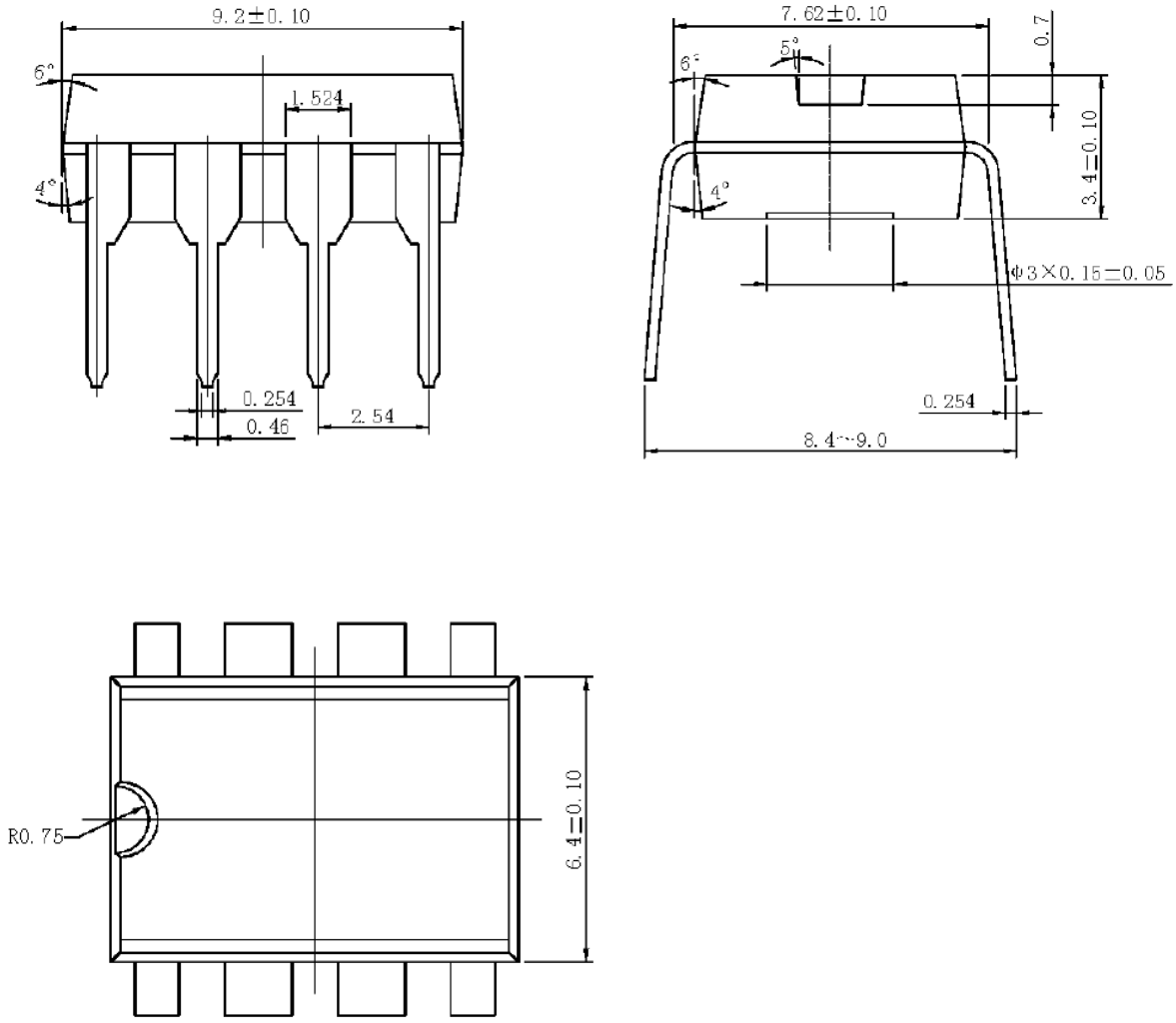


Note: Valid only at VCC=4.5V to 5.5V

Figure 8: ERAL Timing (1)

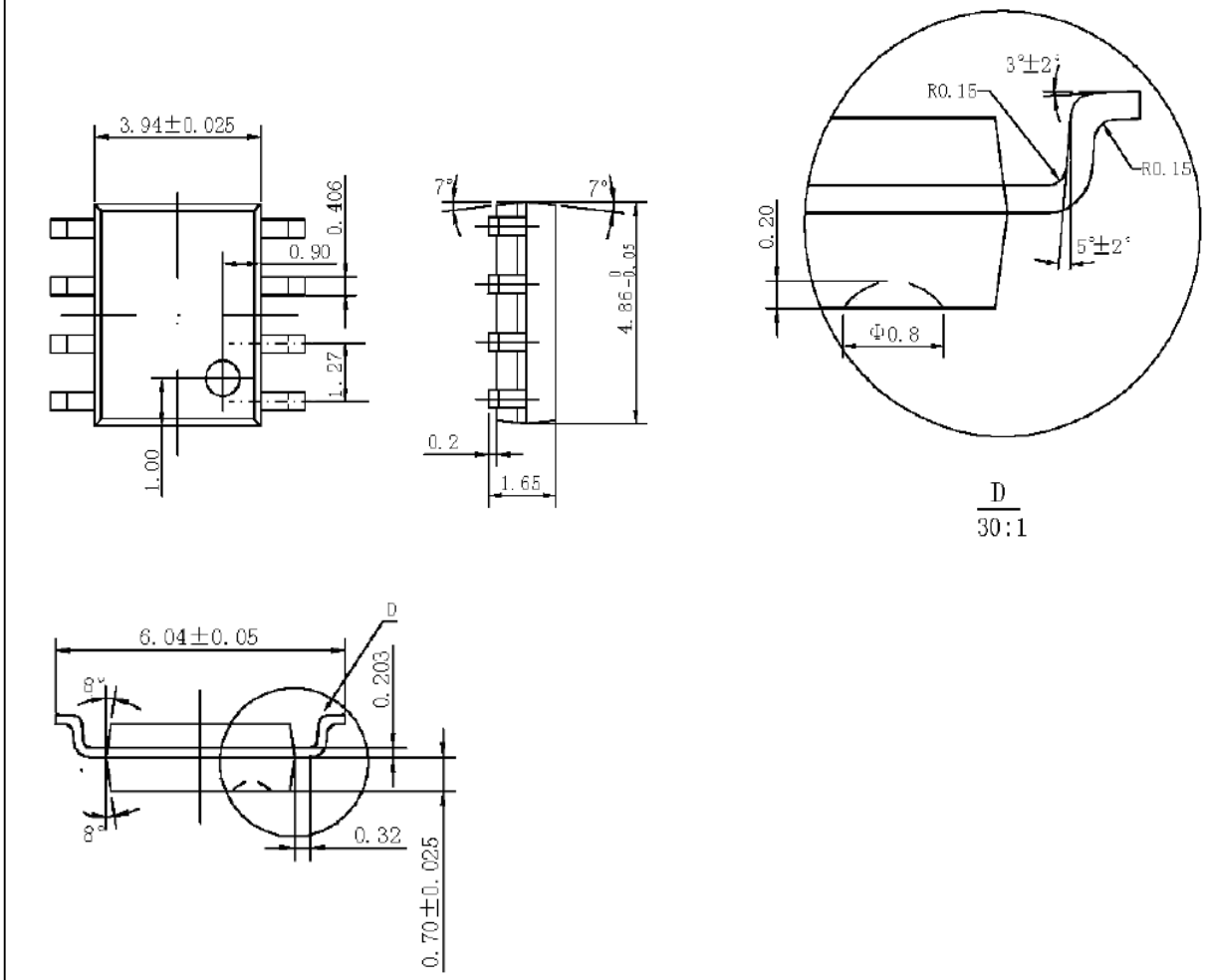
Packaging information

PDIP-8



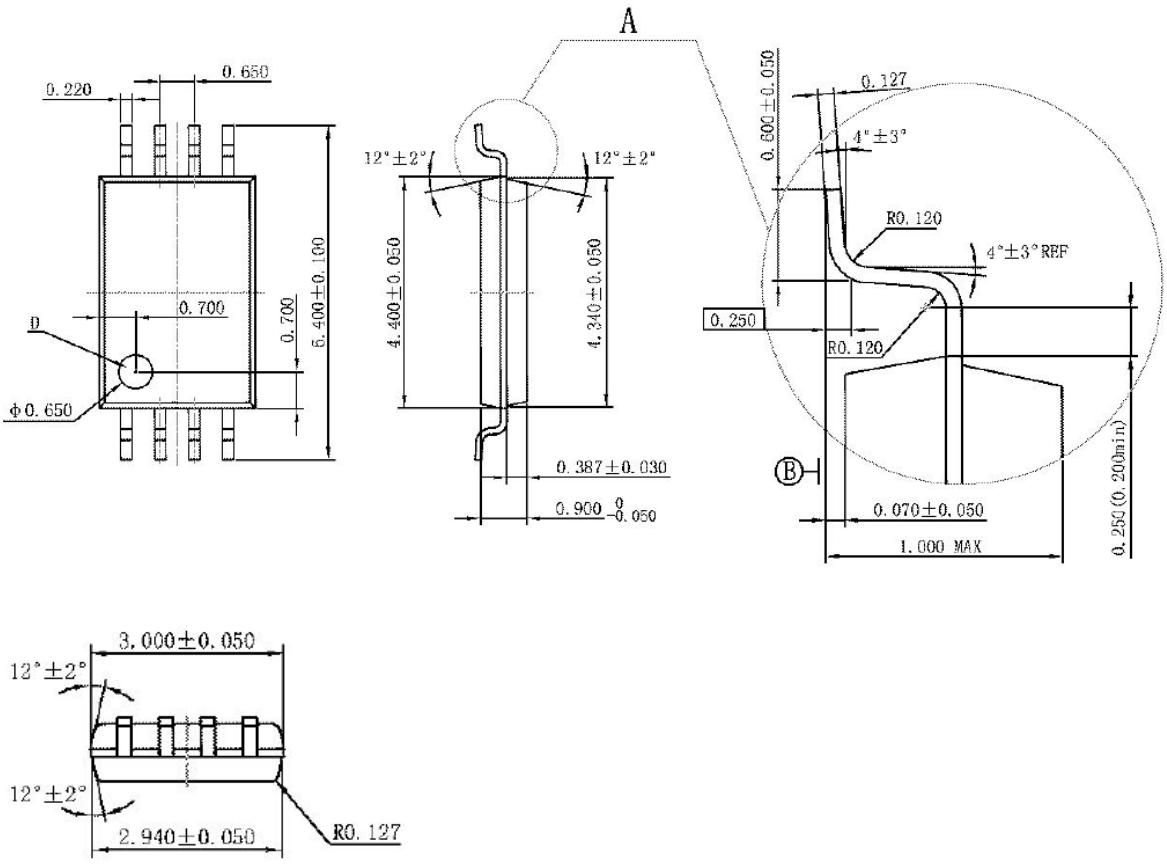
Note: Dimensions in Millimeters.

SOP-8



Note: Dimensions in Millimeters.

TSSOP-8



Note: Dimensions in Millimeters.

Notes

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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