INTRODUCTION

KS0073 is a dot matrix LCD driver & controller LSI which is fabricated by low power CMOS technology. It is capable of displaying 1, 2, or 4-lines with 5×8 or 6×8 dots format.

FUNCTIONS

- Character type dot matrix LCD driver & controller
- Internal driver: 34 common and 60 segment signal output
- Easy interface with 4-bit or 8-bit MPU
- Clock synchronized serial Interface
- 5×8 or 6x8 dot matrix possible
- Extension driver interface possible
- Bidirectional shift function
- All character reverse display
- Display shift per line
- Voltage converter for LCD drive voltage:
  13 V max (2 times / 3 times)
- Various instruction functions
- Automatic power on reset

FEATURES

- Internal Memory
  - Character Generator ROM (CGROM): 9600 bits. (240 characters × 5 × 8 dot)
  - Character Generator RAM (CGRAM): 64×8 bits. (8 characters × 5 × 8 dot)
  - Segment Icon RAM (SEGRAM): 16×8 bits. (96 icons max.)
  - Display Data RAM (DDRAM): 80×8 bits. (80 characters max.)
- Low power operation
  - Power supply voltage range: 2.7 to 5.5 V (VDD)
  - LCD Drive voltage range: 3.0 to 13.0 V (VDD to V5)
- CMOS process
- Programmable duty cycle: 1/17, 1/33 (Referto Table 1.)
- Internal oscillator with an external resistor
- Low power consumptio
- TCP or Bare chip available

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Table 1. Programmable duty cycles

1) 5-dot font width

Display Line Numbers	Duty Ratio	Single-chip Operation		With Extension Driver	
		Displayable characters	Possible icons	Displayable characters	Possible icons
1	1/17	1 line of 24 characters	60	1 line of 52 characters	80
2	1/33	2 lines of 24 characters	60	2 lines of 32 characters	80
4	1/33	4 lines of 12 characters	60	4 lines of 20 characters	80

2) 6-dot font width

Display Line Numbers	Duty Ratio	Single-chip Operation		With Extension Driver	
		Displayable characters	Possible icons	Displayable characters	Possible icons
1	1/17	1 line of 20 characters	60	1 line of 50 characters	96
2	1/33	2 lines of 20 characters	60	2 lines of 30 characters	96
4	1/33	4 lines of 10 characters	60	4 lines of 20 characters	96

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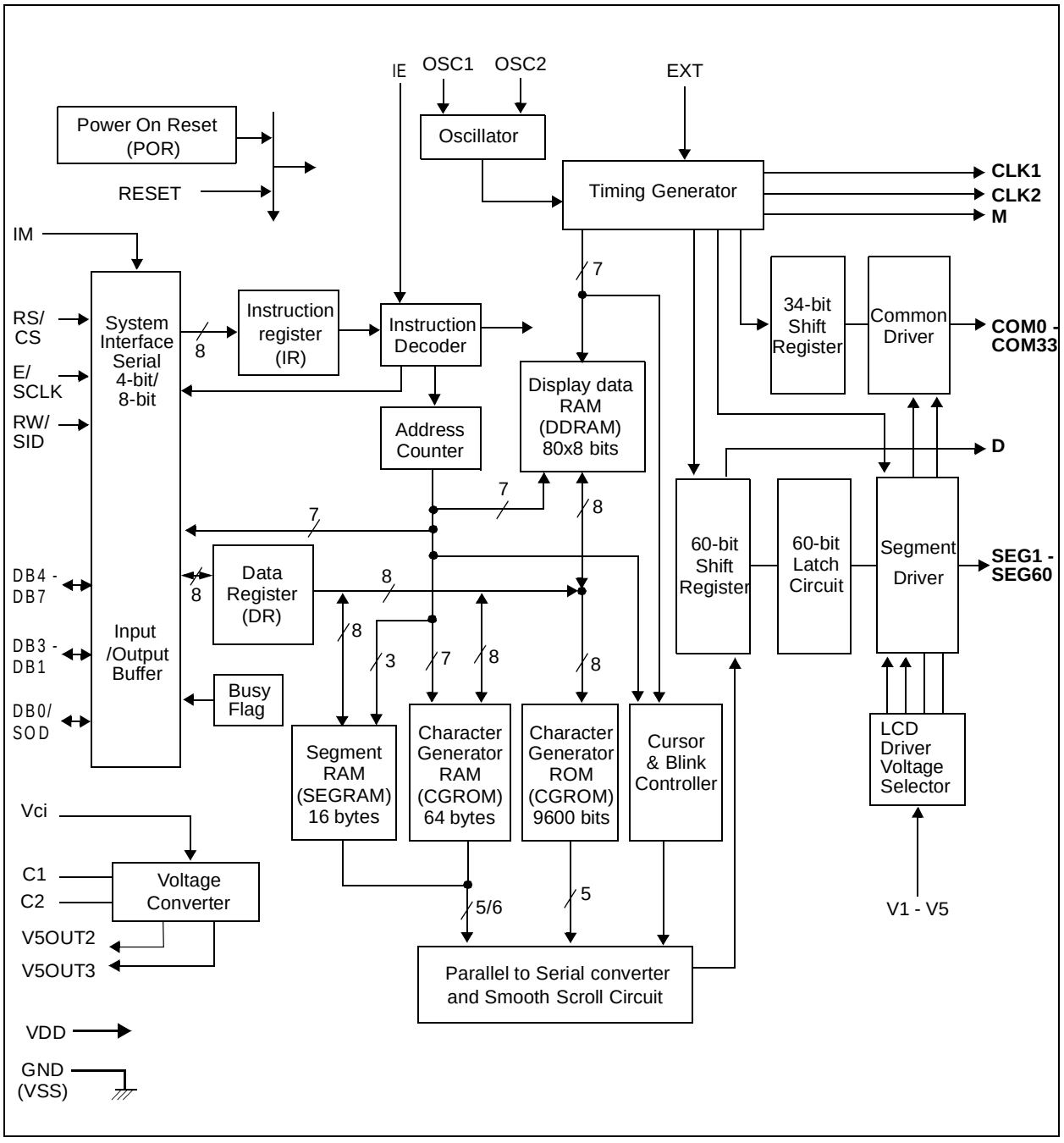
BLOCK DIAGRAM



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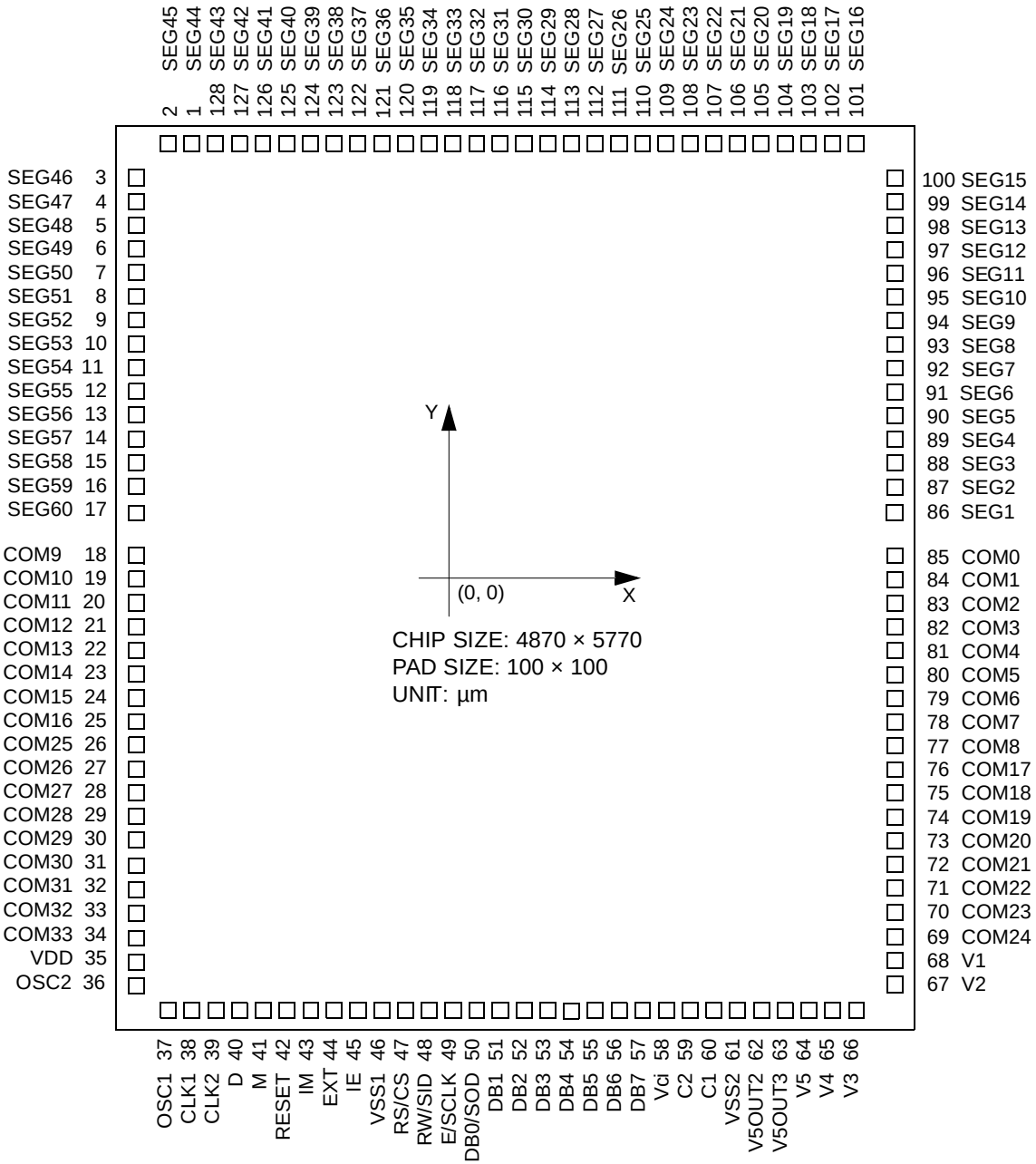
PAD CONFIGURATIO



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PAD COORDINATE

PAD NO	PAD NAME	COORDINATE		PAD NO	PAD NAME	COORDINATE		PAD NO	PAD NAME	COORDINATE		PAD NO	PAD NAME	COORDINATE	
		X	Y			X	Y			X	Y			X	Y
1	SEG44	-1687	2719	24	COM15	-2269	-616	47	RS/CS	-611	-2719	70	COM23	2269	-1741
2	SEG45	-1812	2719	25	COM16	-2269	-741	48	RW/SID	-486	-2719	71	COM22	2269	-1616
3	SEG46	-2269	2122	26	COM25	-2269	-866	49	E/SCLK	-361	-2719	72	COM21	2269	-1491
4	SEG47	-2269	1997	27	COM26	-2269	-991	50	DB0/SOD	-236	-2719	73	COM20	2269	-1366
5	SEG48	-2269	1872	28	COM27	-2269	-1116	51	DB1	-111	-2719	74	COM19	2269	-1241
6	SEG49	-2269	1747	29	COM28	-2269	-1241	52	DB2	14	-2719	75	COM18	2269	-1116
7	SEG50	-2269	1622	30	COM29	-2269	-1336	53	DB3	139	-2719	76	COM17	2269	-991
8	SEG51	-2269	1497	31	COM30	-2269	-1491	54	DB4	264	-2719	77	COM8	2269	-866
9	SEG52	-2269	1372	32	COM31	-2269	-1616	55	DB5	389	-2719	78	COM7	2269	-741
10	SEG53	-2269	1247	33	COM32	-2269	-1741	56	DB6	514	-2719	79	COM6	2269	-616
11	SEG54	-2269	1122	34	COM33	-2269	-1866	57	DB7	639	-2719	80	COM5	2269	-491
12	SEG55	-2269	997	35	VDD	-2269	-1991	58	Vci	764	-2719	81	COM4	2269	-366
13	SEG56	-2269	872	36	OSC2	-2269	-2116	59	C2	889	-2719	82	COM3	2269	-241
14	SEG57	-2269	747	37	OSC1	-1816	-2719	60	C1	1014	-2719	83	COM2	2269	-116
15	SEG58	-2269	622	38	CLK1	-1736	-2719	61	VSS2	1139	-2719	84	COM1	2269	9
16	SEG59	-2269	497	39	CLK2	-1611	-2719	62	V5 OUT2	1264	-2719	85	COM0	2269	134
17	SEG60	-2269	372	40	D	-1486	-2719	63	V5 OUT3	1389	-2719	86	SEG1	2269	372
18	COM9	-2269	134	41	M	-1361	-2719	64	V5	1514	-2719	87	SEG2	2269	497
19	COM10	-2269	9	42	RESET	-1236	-2719	65	V4	1639	-2719	88	SEG3	2269	622
20	COM11	-2269	-116	43	IM	-1111	-2719	66	V3	1764	-2719	89	SEG4	2269	747
21	COM12	-2269	-241	44	EXT	-986	-2719	67	V2	2269	-2116	90	SEG5	2269	872
22	COM13	-2269	-366	45	IE	-861	-2719	68	V1	2269	-1991	91	SEG6	2269	997
23	COM14	-2269	-491	46	VSS1	-736	-2719	69	COM 24	2269	-1866	92	SEG7	2269	1122

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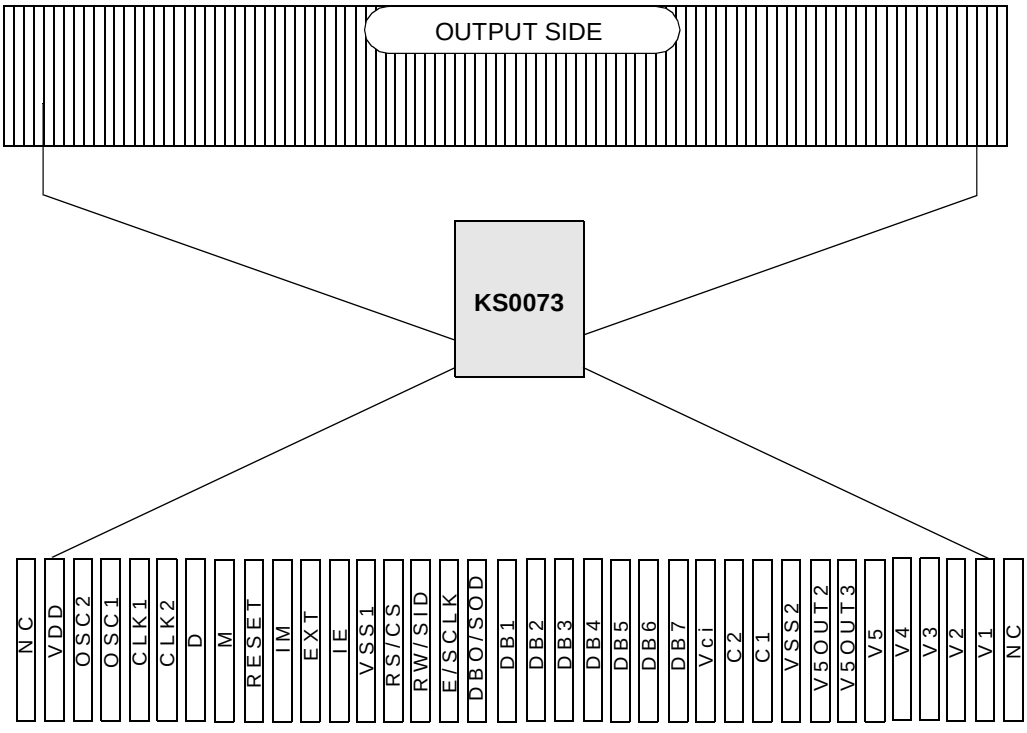
(PAD COORDINATE CONTINUED)

PAD NO.	PAD NAME	COORDINATE		PAD NO.	PAD NAME	COORDINATE		PAD NO.	PAD NAME	COORDINATE		PAD NO.	PAD NAME	COORDINATE	
		X	Y			X	Y			X	Y			X	Y
93	SEG8	2269	1247	102	SEG17	1688	2719	111	SEG26	563	2719	120	SEG35	-562	2719
94	SEG9	2269	1372	103	SEG18	1563	2719	112	SEG27	438	2719	121	SEG36	-687	2719
95	SEG10	2269	1497	104	SEG19	1438	2719	113	SEG28	313	2719	122	SEG37	-812	2719
96	SEG11	2269	1622	105	SEG20	1313	2719	114	SEG29	188	2719	123	SEG38	-937	2719
97	SEG12	2269	1747	106	SEG21	1188	2719	115	SEG30	63	2719	124	SEG39	-1062	2719
98	SEG13	2269	1872	107	SEG22	1063	2719	116	SEG31	-62	2719	125	SEG40	-1187	2719
99	SEG14	2269	1997	108	SEG23	938	2719	117	SEG32	-187	2719	127	SEG41	-1312	2719
100	SEG15	2269	2122	109	SEG24	813	2719	118	SEG33	-312	2719	127	SEG42	-1437	2719
101	SEG16	1813	2719	110	SEG25	688	2719	119	SEG34	-437	2719	128	SEG43	-1562	2719

PIN CONFIGURATION OF TCP

A) TCP OUTLINE



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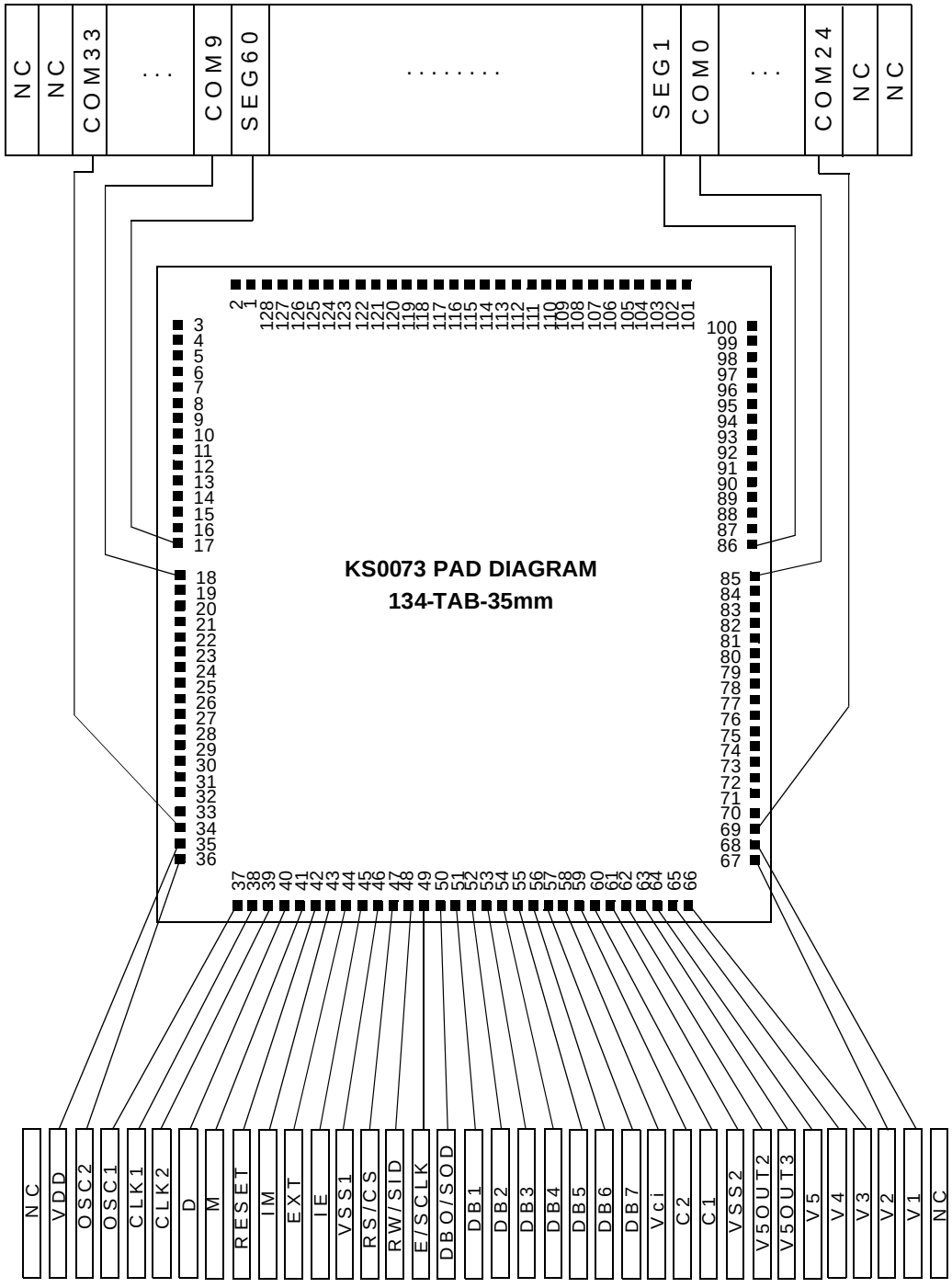

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PIN DESCRIPTION

Pin(No)	Input/ Output	Name	Description	Interface
VDD (35)	-	Power supply	for logical circuit (+3V, +5 V)	Power Supply
VSS1, VSS2 (46, 61)			0 V (GND)	
V1 ~ V5 (68~64)			Bias voltage level for LCD driving.	
Vci (58)	Input		Input voltage to the voltage converter to generate LCD drive voltage (Vci = 1.0 to 4.5 V).	
SEG1 ~ SEG6 (86~128, 1~17)	Output	Segment output	Segment signal output for LCD drive.	LCD
COM0 ~ COM33 (85~69,18~34)	Output	Common output	Common signal output for LCD drive.	LCD
OSC1,OSC2 (37,36)	Input (OSC1), Output (OSC2)	Oscillator	When using internal oscillator, connect external Rf resistor If external clock is used, connect it to OSC1.	External resistor / oscillator (OSC1)
CLK1,CLK2 (38,39)	Input	Latch(CLK1) / Shift(CLK2) clock	When EXT = “High”, each outputs latch clock and shift clock for extension driver.	Extensio driver
C1,C2 (60,59)	Input	External capacitance input	To use the voltage converter (2 times / times), these pins must be connected to the external capacitance.	External capacitor
M (41)	Output	Alternated signal for LCD driver out-put	When EXT = “High”, outputs the alternating signal to convert LCD driver waveform to AC for extension driver.	Extensio driver
D (40)	Output	Display data interface	When EXT = “High”, outputs extension driver data (the 61th dot's data)	Extensio driver
EXT (44)	Input	Extension driver control signal	When EXT = “High”, enables extension diver control signal, When EXT = “Low”, suppresses extra current consumption and CLK1/CLK2/M/D should be open.	-
RESET (42)	Input	Reset pin	Initialized to Low	-
IE (45)	Input	Selection pin of instruction set	When IE = “Low”, instruction set is selected as Table 10. When IE = “High”, instruction set is selected as Table 6.	-

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Pin(No)	Input/ Output	Name	Description	Interfac
V5OUT2 (62)	Output	Two times converter output	The value of Vci is converted twice. To use the three times converter, the same capacitance as that of C1-C2 should be connected here.	V5 pin/ capacitance
V5OUT3 (63)		Three times converter output	The value of Vci is converted three times.	V5 pin
IM (43)	Input	Interface mode selection	Select Interface mode with the MPU. When IM = “Low”: Serial mode, When IM = “High”: 4-bit/8-bit bus mode.	-
RS/CS (47)	Input	Register select / Chip select	In bus mode, used as register selection input. When RS/CS = “High”, Data register is selected. When RS/CS “Low”, Instruction register is selected. In serial mode, used as chip selection input. When RS/CS = “Low”, selected. When RS/CS = “High”, not selected (Low access enable).	MPU
RW/SID (48)	Input	Read, write / Serial input data	In bus mode, used as read/write selection input. When RW/SID = “High”, read operation. When RW/SID = “Low”, write operation. In serial mode, used for data input pin.	MPU
E/SCLK (49)	Input	Read, write enable/Serial clock	In bus mode, used as read/write enable signal. In serial mode, used as serial clock input pin.	MPU
DB0/SOD (50)	Input Output / Output	Data bus 0 bit / Serial output data	In 8-bit bus mode, used as lowest bidirectional data bit. During 4-bit bus mode, open this pin. In serial mode, used as serial data output pin. If not in read operation, open this pin.	MPU
DB1 ~ DB3 (51 ~ 53)	Input, Output	Data bus 1 ~ 7	In 8-bit bus mode, used as low order bidirectional data bus. During 4-bit bus mode or serial mode, open these pins.	MPU
DB4 ~ DB7 (54 ~ 57)			In 8-bit bus mode, used as high order bidirectional data bus. In 4-bit bus mode, used as both high and low order. DB7 used for Busy Flag output. During serial mode, open these pins.	MPU

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FUNCTION DESCRIPTION

System Interface

This chip has all three kinds of interface type with MPU: serial, 4-bit and 8-bit bus.
Serial and bus(4-bit/8-bit) are selected by IM input, and 4-bit bus and 8-bit bus are selected by the DL bit in the instruction register.

During read or write operation, two 8-bit registers are used. one is the data register (DR), the other is the instruction register(IR).

The data register(DR) is used as a temporary data storage place for being written into or read from DDRAM/CGRAM/SEGRAM. Target RAM is selected by RAM address setting instruction. Each internal operation, reading from or writing into RAM, is done automatically.
Hence, after MPU reads the DR data, the data in the next DDRAM/CGRAM/SEGRAM address is transferred into DR automatically. Also, after MPU writes data to DR, the data in DR is transferred into DDRAM/CGRAM/ SEGRAM automatically.

The Instruction register (IR) is used only to store instruction code transferred from MPU.
MPU cannot use it to read instruction data.

To select register, use the RS/CS input pin in 4-bit/8-bit bus mode (IM “High”) or the RS bit in serial mode (IM = “Low”).

Table 2. Various kinds of operations according to RS and R/W bits.

RS	R/W	Operation
0	0	Instruction Write operation (MPU writes Instruction code into IR)
0	1	Read Busy flag (DB7) and address counter (DB0 ~ DB6)
1	0	Data Write operation (MPU writes data into DR)
1	1	Data Read operation (MPU reads data from DR)

Busy Flag (BF)

When BF = “High”, it indicates that the internal operation is being processed. So during this time the next instruction cannot be accepted. BF can be read, when RS = “Low” and R/W = “High” (Read Instruction Operation), through the DB7 port. Before executing the next instruction, be sure that BF is not High.

Display Data RAM (DDRAM)

DDRAM stores display data of maximum 80×8 bits (80 characters).
DDRAM address is set in the address counter (AC) as a hexadecimal number (Refer to Fig-1).

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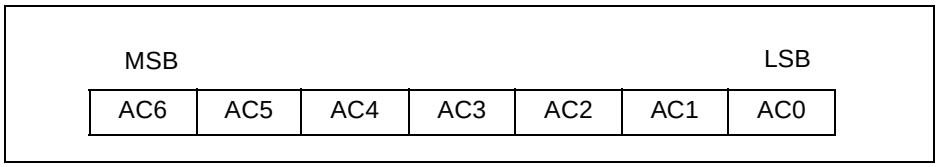

Fig-1. DDRAM Addres

1) Display of 5-dot font width character

(1) 5-dot 1 line display

In the case of a 1-line display with 5-dot font, the address range of DDRAM is 00H ~ 4FH (Refer to Fig-2).
When EXT "High", extension driver will be used.
Fig-3 shows the example with 40 segment extension drivers added.

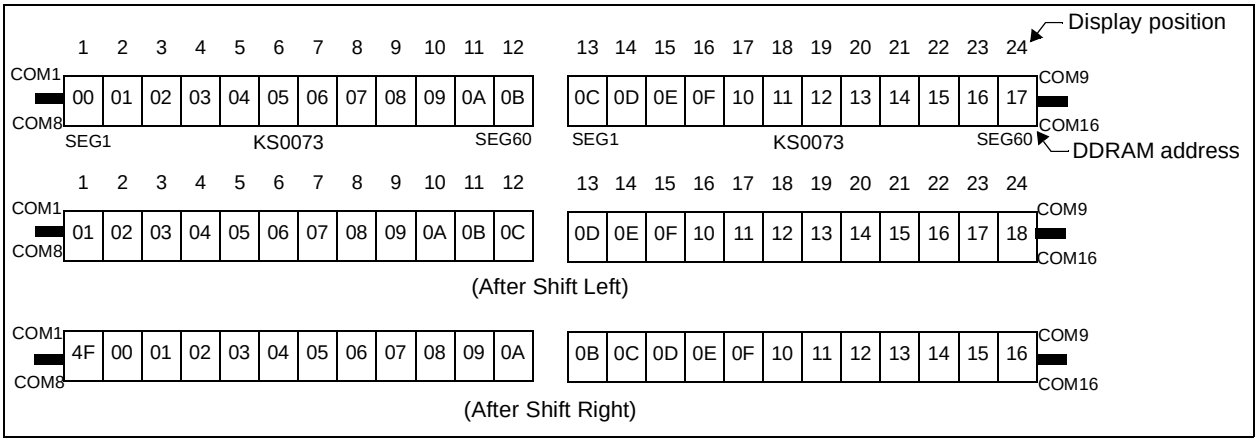

Fig-2. 1-line X 24 ch. display (5-dot font width)

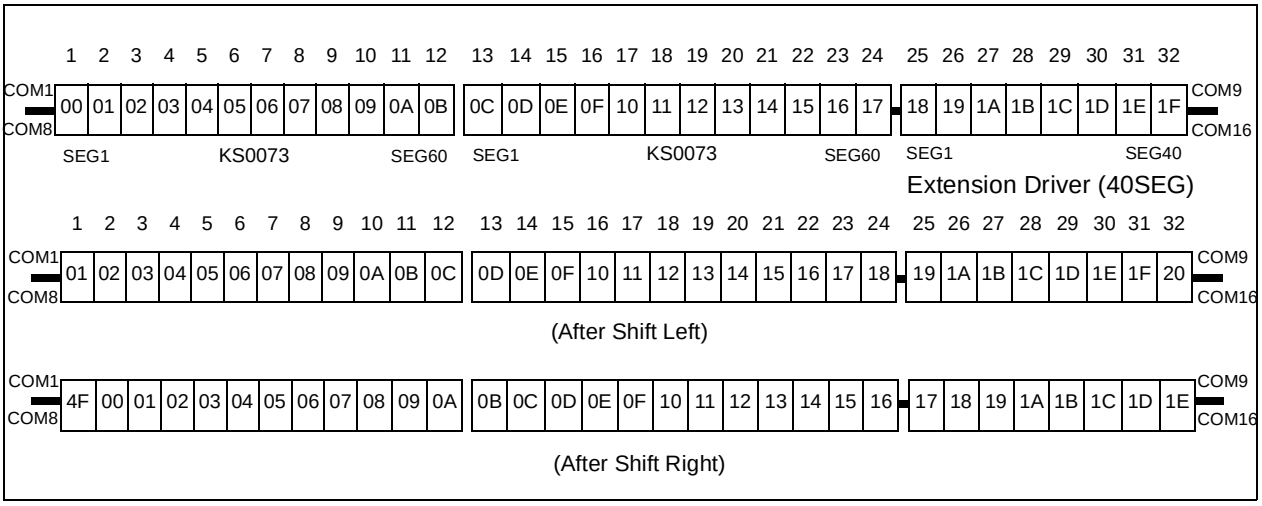

Fig-3. 1-line X 32 ch. display with 40 SEG. extension driver (5-dot font width)

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(2) 5-dot 2-line display

In the case of a 2-line display with 5-dot font, the address range of DDRAM is 00H–27H, and 40H–67H (Refer to Fig-4). When EXT = “High”, the extension driver will be used.
Fig-5 shows the example with 40 segment extension drivers added.

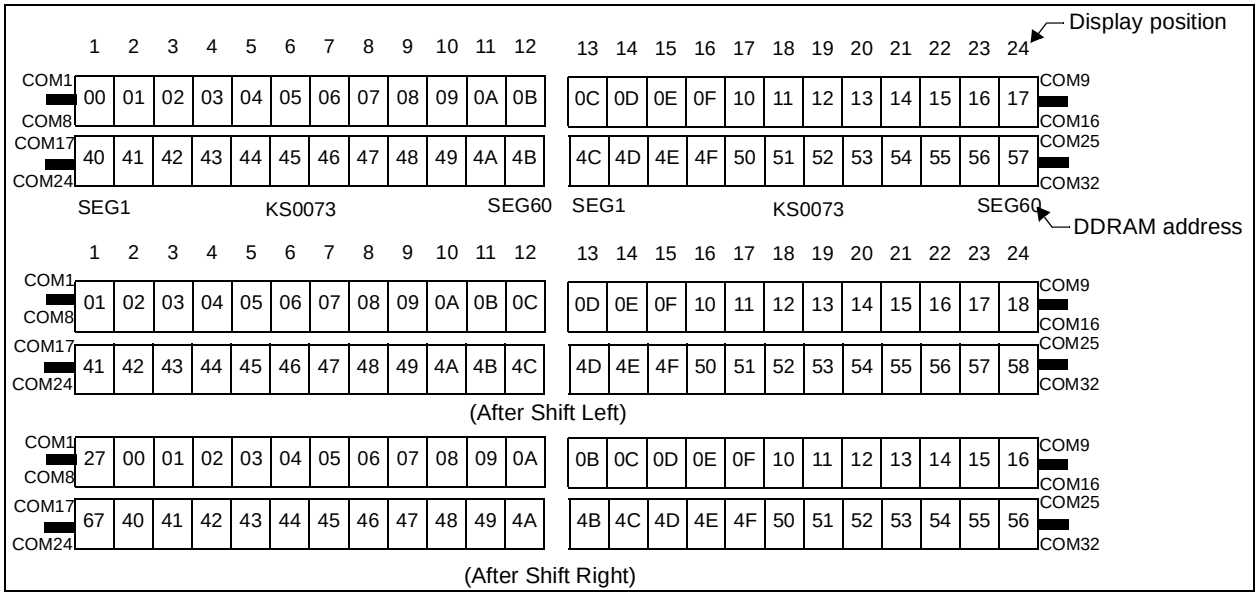

Fig-4. 2-line × 24 char. display (5-dot font width)

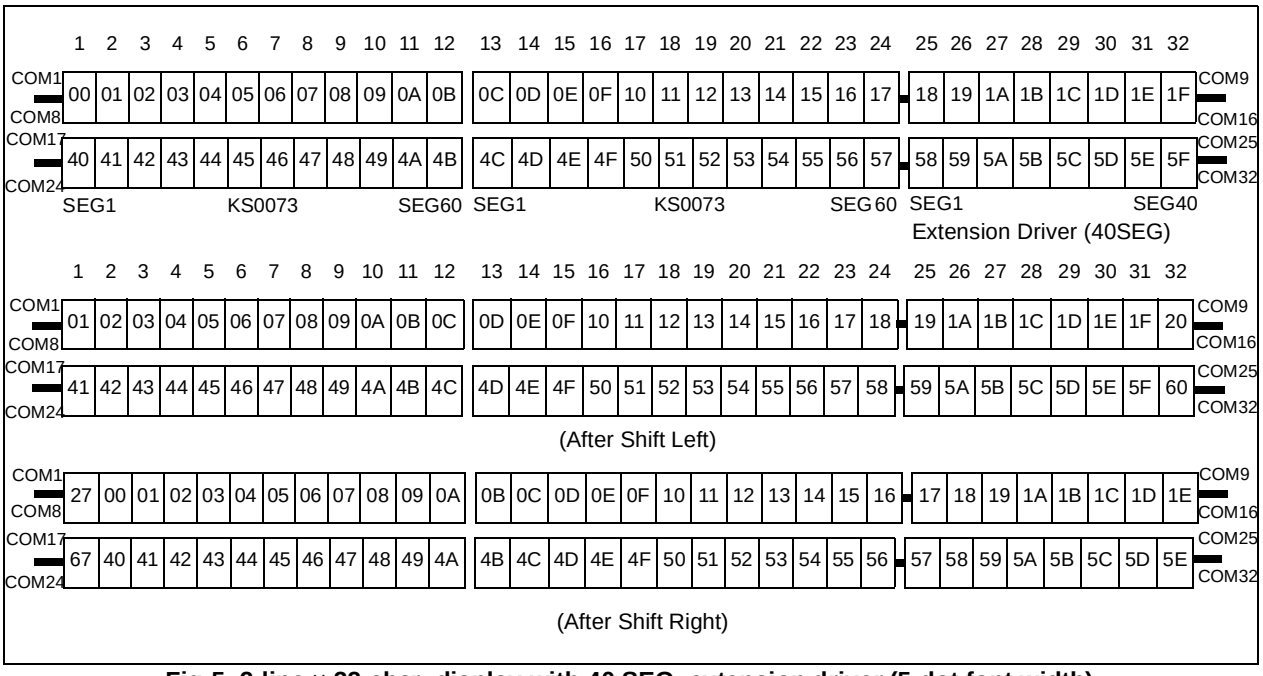

Fig-5. 2-line × 32 char. display with 40 SEG. extension driver (5-dot font width)

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(3) 5-dot 4-line display

In the case of a 4-line display with 5-dot font, the address range of DDRAM is 00H–13H, 20H–33H, 40H–53H, 60H–73H (Refer to Fig-6).

When EXT="High", extension driver will be used. Fig-7 shows the example with 40 segment extension drivers added.

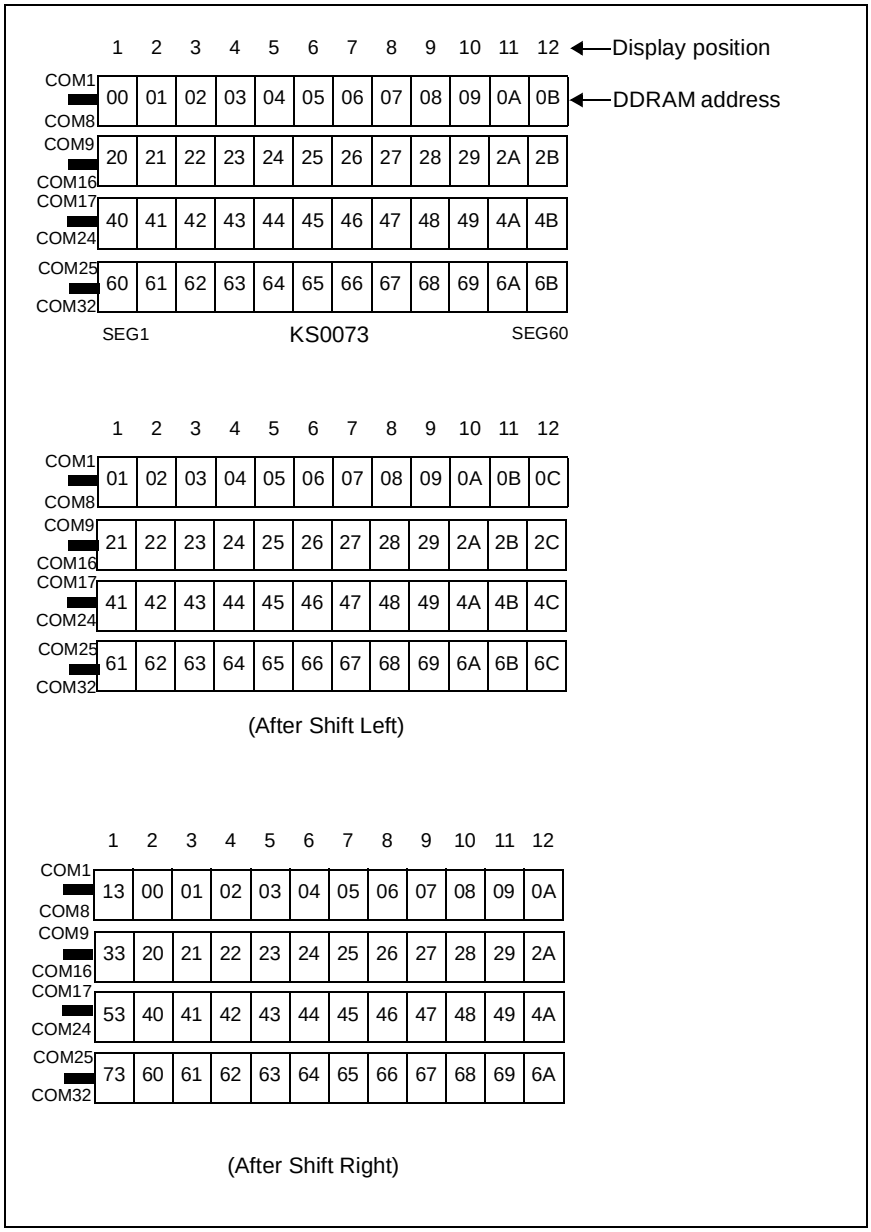

Fig-6. 4-line × 12 char. display (5-dot font width)

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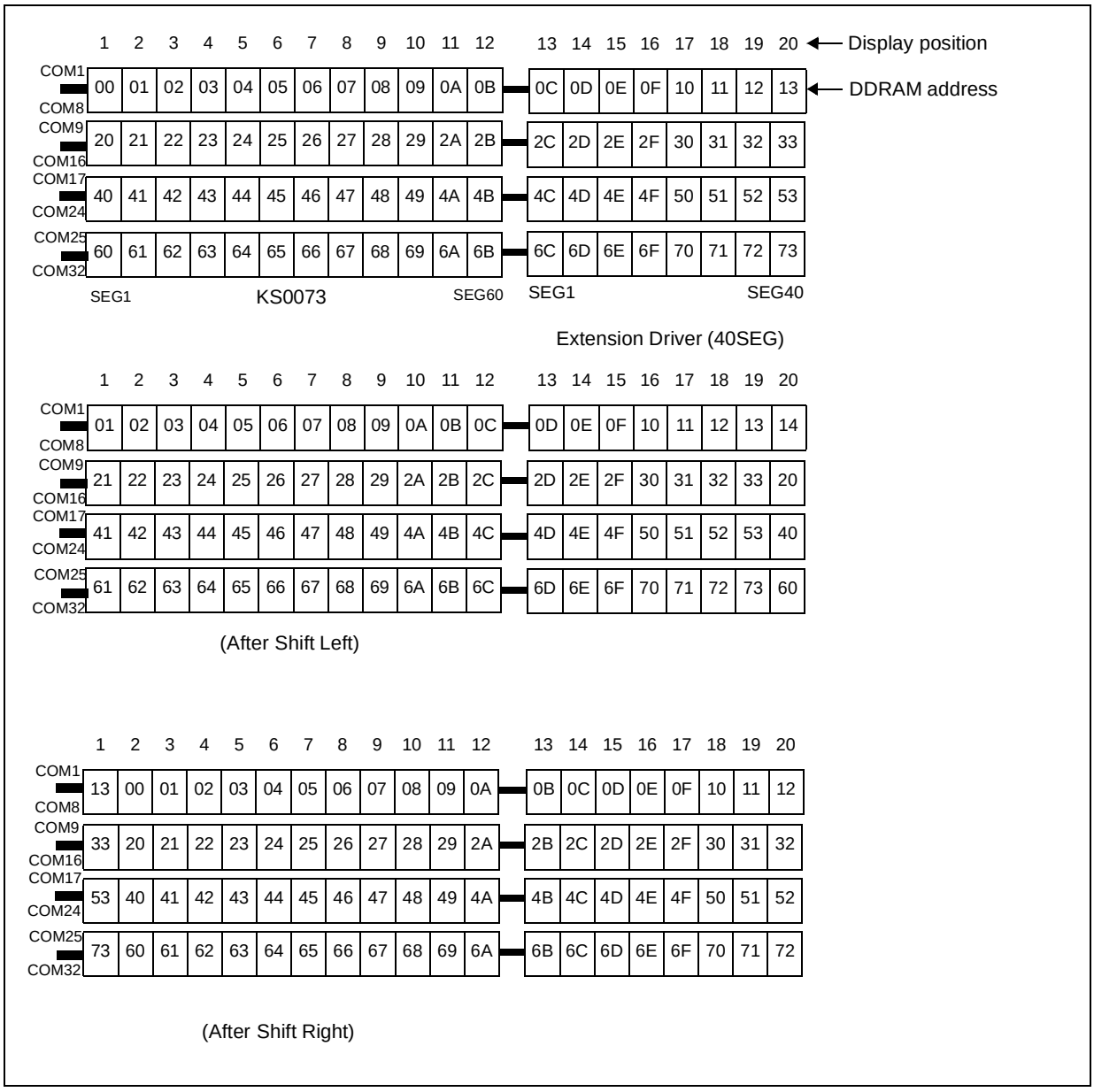

Fig-7. 4-line × 20 char. display with 40 SEG. extension driver (5-dot font width)

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2) Display of 6-dot font width character

(1) 6-dot 1-line display

In the case of a 1-line display with 6-dot font, the address range of DDRAM is 00H–4FH (Refer to Fig-8)
When EXT = “High”, extension driver will be used.
Fig-9 shows the example with 40 segment extension driver added.

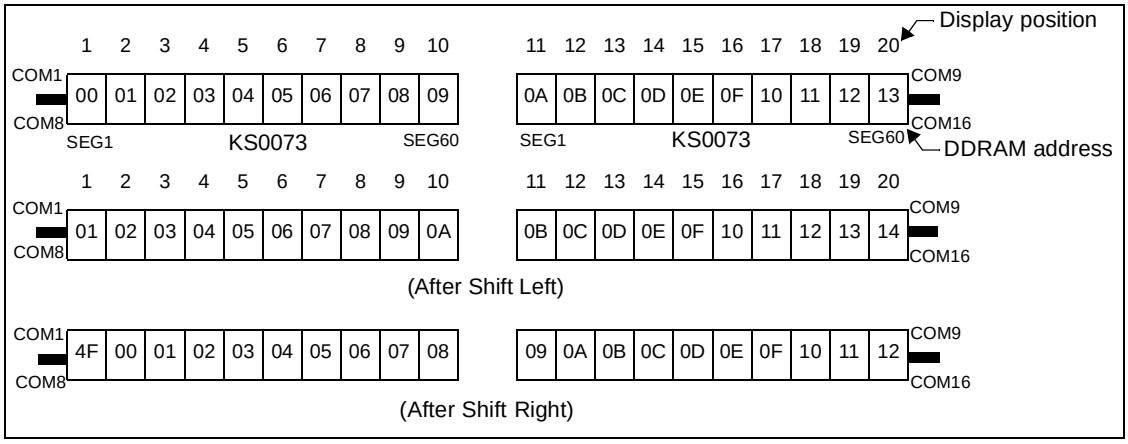

Fig-8. 1-line × 20 char. display (6-dot font width)

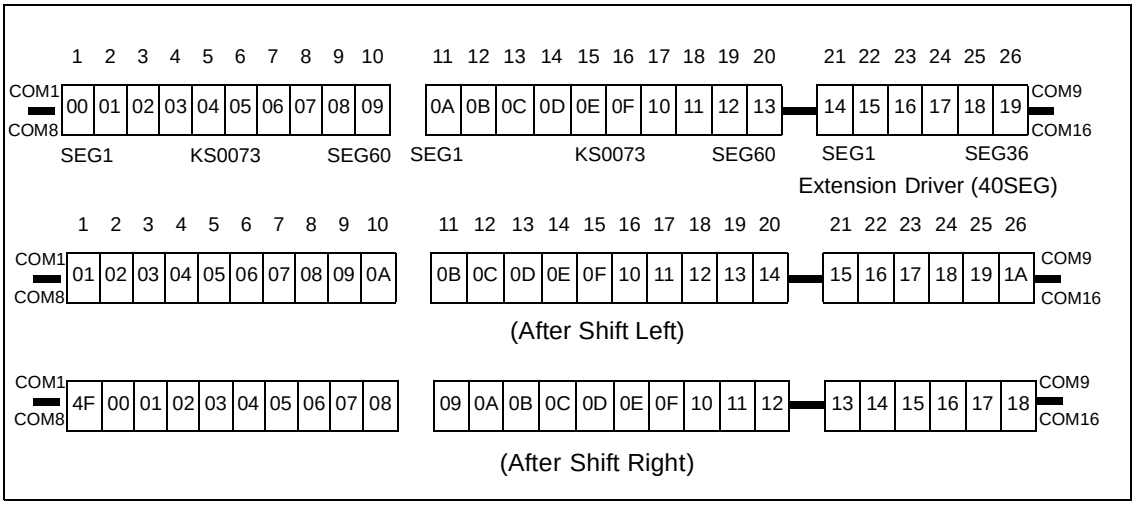

Fig-9. 1-line × 26char. display with 40 SEG. extension driver (6-dot font width)

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(2) 6-dot 2-line display

In the case of a 2-line display with 6-dot font, the address range of DDRAM is 00H–27H, and 40H–67H (Refer to Fig-10). When EXT = “High”, extension driver will be used.
Fig-11 shows an example with 40 segment extension drivers added.

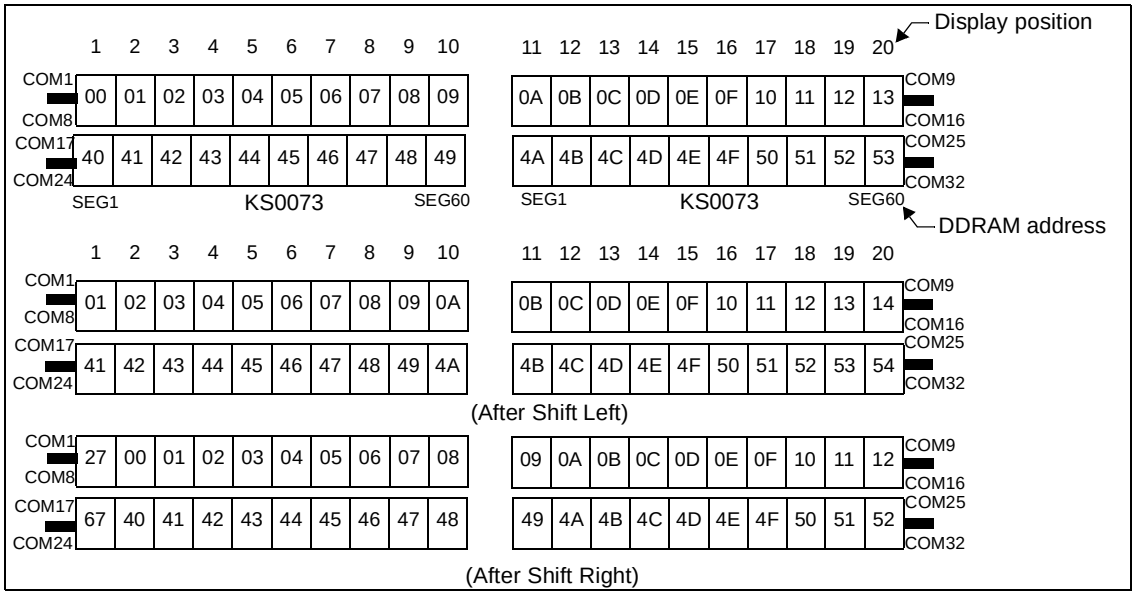

Fig-10. 2-line × 20char. display (6-dot font width)

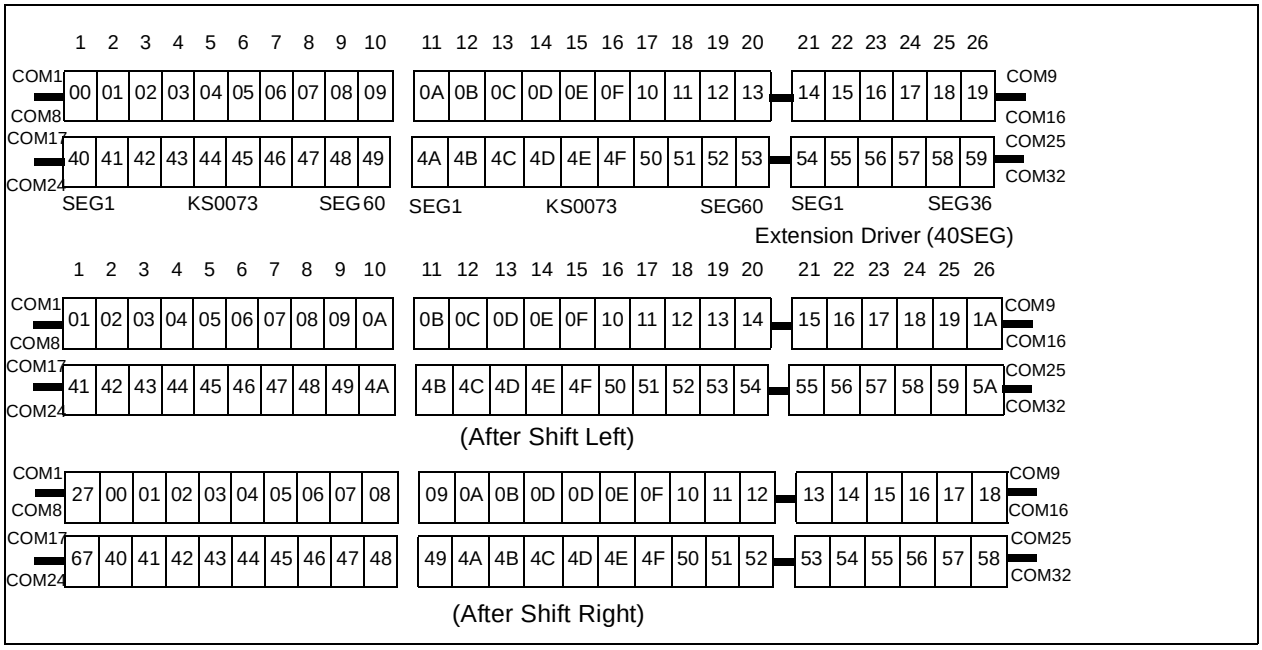

Fig-11. 2-line × 26 char. display with 40 SEG. extension driver (6-dot font width)

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(3) 6-dot 4-line display

In the case of a 4-line display with 6-dot font, the address range of DDRAM is 00H–13H, 20H–33H, 40H–53H, 60H–73H (Refer to Fig-12)
When EXT = “High”, the extension driver will be used.
Fig-13 shows the example with 40 segment extension drivers added.

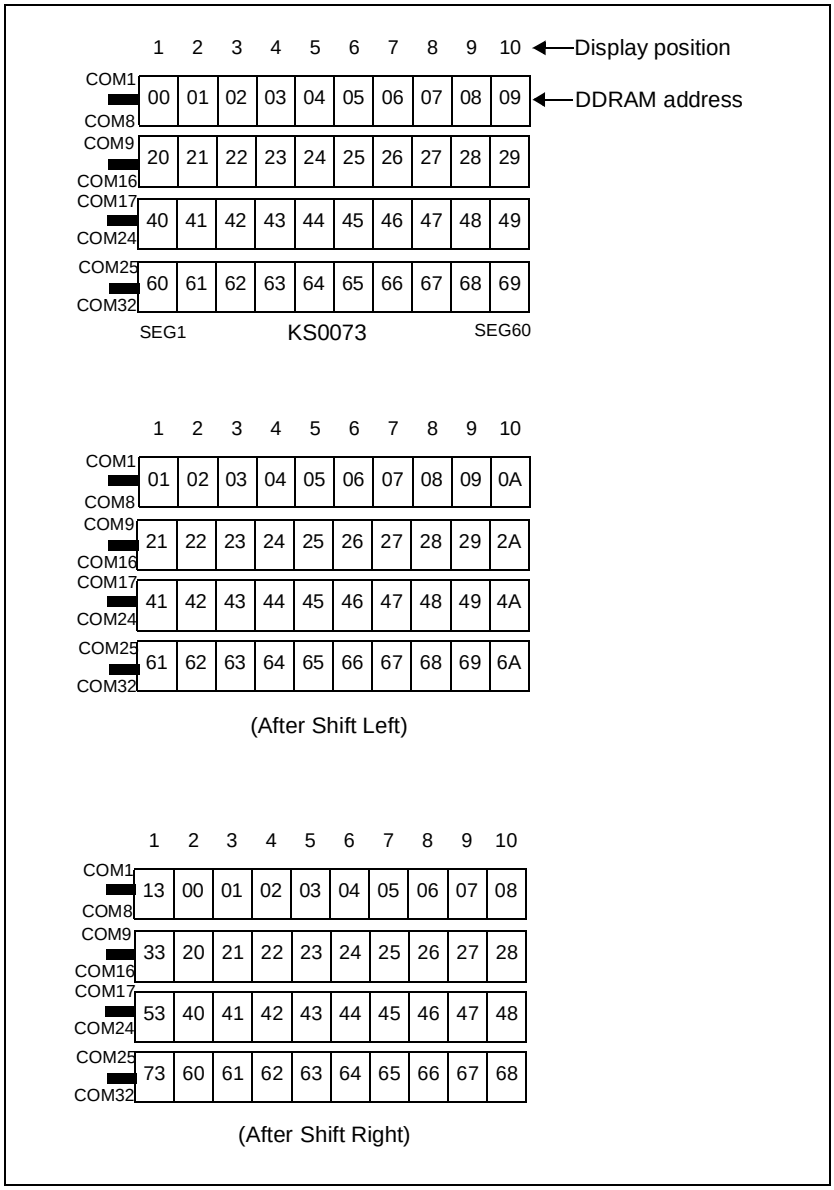

Fig-12. 4-line × 10char. display (6-dot font width)

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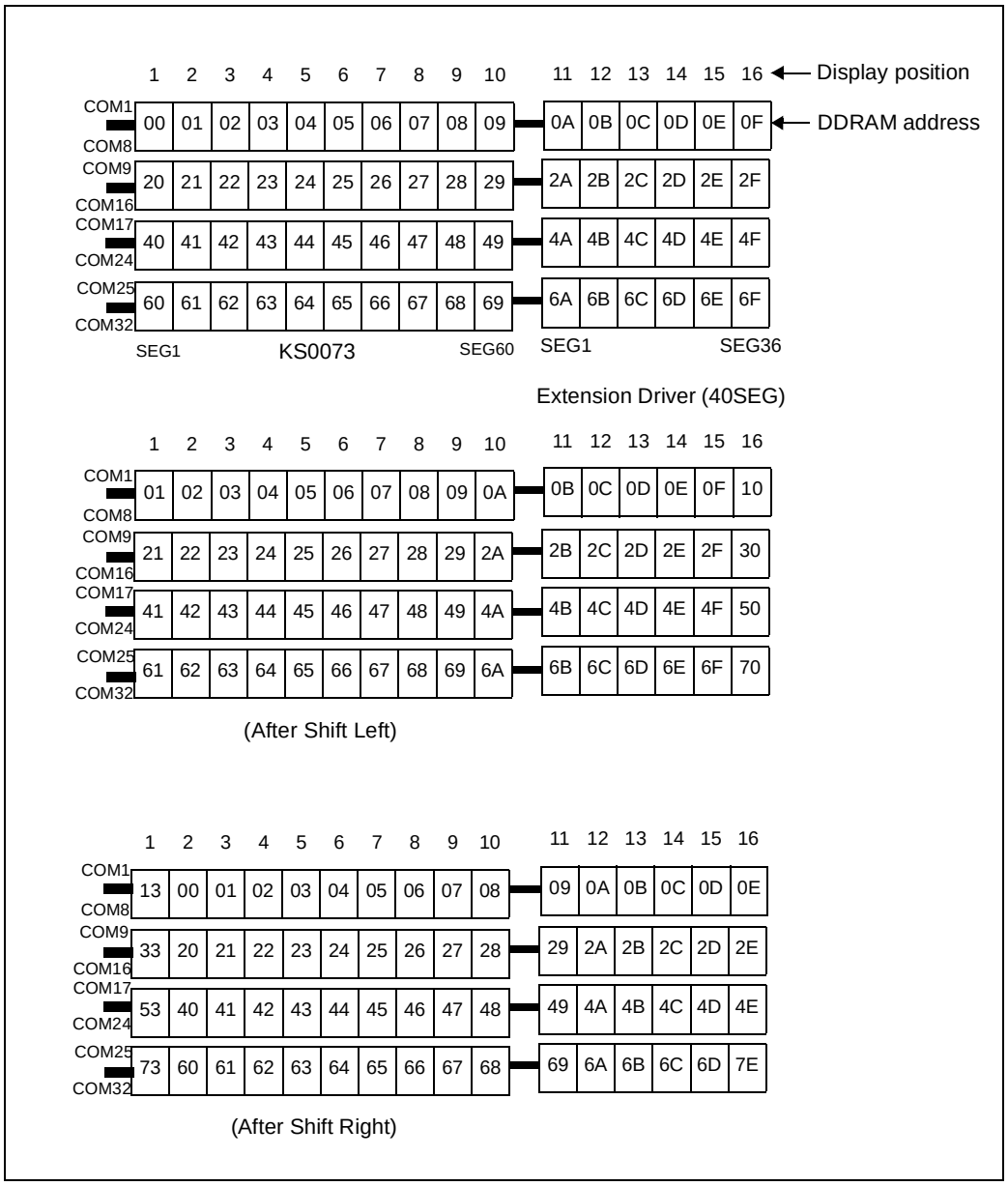

Fig-13. 4-line × 16 char. display with 40 SEG. extension driver (6-dot font width)

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Timing Generation Circuit
The timing generation circuit generates clock signals for internal operations.

Address Counter (AC)
The address Counter (AC) stores DDRAM/CGRAM/SEGRAM address, transferred from IR.
After writing into (reading from) DDRAM/CGRAM/SEGRAM, AC is automatically increased (decreased) by 1.
When RS "Low" and R/W = "High", AC can be read through DB0–DB6 ports.

Cursor/Blink Control Circuit
It controls cursor/blink ON/OFF and black/white inversion at cursor position.

LCD Driver Circuit
The LCD Driver circuit has 34 common and 60 segment signals for LCD driving.
Data from SEGRAM/CGRAM/CGROM is transferred to a 60-bit segment latch serially, which is then stored to a 60-bit shift latch. When each common is selected by a 34-bit common register, segment data also outputs throug a segment driver from a 100-bit segment latch.
In 1-line display mode, COM0 – COM17 have a 1/17 duty ratio, and in 2-line or 4-line mode, COM0 – COM33 hav a 1/33 duty ratio.

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CGROM (Character Generator ROM)
CGROM has 5 X 8-dot 240 characters pattern (Refer to Table 3).

Table 3. CGROM Character Code Table

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CGRAM (Character Generator RAM)

CGRAM has up to eight 5×8-dot characters. By writing font data to CGRAM, user defined character can be use (Refer to Table 4).

Table 4. Relationship between Character Code (DDRAM) and Character Pattern (CGRAM)

1) 5x8 dot Character pattern

Character Code (DDRAM data)								CGRAM address						CGRAM data								Pattern Number
D7	D6	D5	D4	D3	D2	D1	D0	A5	A4	A3	A2	A1	A0	P7	P6	P5	P4	P3	P2	P1	P	
0	0	0	0	X	0	0	0	0	0	0	0	0	0	B1	B0	X	0	1	1	1	0	pattern 1
											0	0	1				1	0	0	0	1	
											0	1	0				1	0	0	0	1	
											0	1	1				1	1	1	1	1	
											1	0	0				1	0	0	0	1	
											1	0	1				1	0	0	0	1	
											1	1	0				1	0	0	0	1	
											1	1	1				0	0	0	0	0	
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0	0	0	0	X	1	1	1	1	1	1	0	0	0	B1	B0	X	1	0	0	0	1	pattern 8
											0	0	1				1	0	0	0	1	
											0	1	0				1	0	0	0	1	
											0	1	1				1	1	1	1	1	
											1	0	0				1	0	0	0	1	
											1	0	1				1	0	0	0	1	
											1	1	0				1	0	0	0	1	
											1	1	1				0	0	0	0	0	

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2) 6x8 dot Character pattern

Character Code (DDRAM data)								CGRAM address						CGRAM data								Pattern Number
D7	D6	D5	D4	D3	D2	D1	D0	A5	A4	A3	A2	A1	A0	P7	P6	P5	P4	P3	P2	P1	P	
0	0	0	0	X	0	0	0	0	0	0	0	0	0	B1	B0	0	0	1	1	1	0	pattern 1
											0	0	1			0	1	0	0	0	1	
											0	1	0			0	1	0	0	0	1	
											0	1	1			0	1	1	1	1	1	
											1	0	0			0	1	0	0	0	1	
											1	0	1			0	1	0	0	0	1	
											1	1	0			0	1	0	0	0	1	
											1	1	1			0	0	0	0	0	0	
				.						.			.					.				.
				.						.			.					.				.
0	0	0	0	X	1	1	1	1	1	1	0	0	0	B1	B0	0	1	0	0	0	1	pattern 8
											0	0	1			0	1	0	0	0	1	
											0	1	0			0	1	0	0	0	1	
											0	1	1			0	1	1	1	1	1	
											1	0	0			0	1	0	0	0	1	
											1	0	1			0	1	0	0	0	1	
											1	1	0			0	1	0	0	0	1	
											1	1	1			0	0	0	0	0	0	

NOTE: 1. When BE (Blink Enable bit) = “High”, blink is controlled by B1 and B0 bit.
In displaying 5-dot font width, when B1 = “1”, enabled dots in P0 – P4 ports will blink, and when B1 = “0” and B0 = “1”, enabled dots in P4 port will blink.
When B1 = “0” and B0 = “0”, blinking will not occur.
In displaying 6-dot font width, when B1 = “1”, enabled dots of P0 – P5 ports will blink, and when B1 = “0” and B0 = “1”, enabled dots of P5 port will blink.
When B1 = “0” and B0 = “0”, blinking will not occur.

2. “X”: Don’t care

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SEGRAM (Segment Icon RAM)

SEGRAM has segment control data and segment pattern data. During 1-line display mode, COM0(COM17) enables the data of SEGRAM to display icons.
When used in 2/4-line display mode COM0(COM33) does that.
The higher 2-bits are blinking control data, and the lower 6-bits are pattern data (Refer to Table 5 and Fig-14).

Table 5. Relationship between SEGRAM address and display pattern

SEGRAM address	SEGRAM data display pattern	
	5-dot font width	6-dot font width
A3 A2 A1 A0	D7 D6 D5 D4 D3 D2 D1 D	D7 D6 D5 D4 D3 D2 D1 D0
0 0 0 0	B1 B0 X S1 S2 S3 S4 S5	B1 B0 S1 S2 S3 S4 S5 S6
0 0 0 1	B1 B0 X S6 S7 S8 S9 S10	B1 B0 S7 S8 S9 S10 S11 S12
0 0 1 0	B1 B0 X S11 S12 S13 S14 S15	B1 B0 S13 S14 S15 S16 S17 S18
0 0 1 1	B1 B0 X S16 S17 S18 S19 S20	B1 B0 S19 S20 S21 S22 S23 S24
0 1 0 0	B1 B0 X S21 S22 S23 S24 S25	B1 B0 S25 S26 S27 S28 S29 S30
0 1 0 1	B1 B0 X S26 S27 S28 S29 S30	B1 B0 S31 S32 S33 S34 S35 S36
0 1 1 0	B1 B0 X S31 S32 S33 S34 S35	B1 B0 S37 S38 S39 S40 S41 S42
0 1 1 1	B1 B0 X S36 S37 S38 S39 S40	B1 B0 S43 S44 S45 S46 S47 S48
1 0 0 0	B1 B0 X S41 S42 S43 S44 S45	B1 B0 S49 S50 S51 S52 S53 S54
1 0 0 1	B1 B0 X S46 S47 S48 S49 S50	B1 B0 S55 S56 S57 S58 S59 S60
1 0 1 0	B1 B0 X S51 S52 S53 S54 S55	B1 B0 S61 S62 S63 S64 S65 S66
1 0 1 1	B1 B0 X S56 S57 S58 S59 S60	B1 B0 S67 S68 S69 S70 S71 S72
1 1 0 0	B1 B0 X S61 S62 S63 S64 S65	B1 B0 S73 S74 S75 S76 S77 S78
1 1 0 1	B1 B0 X S66 S67 S68 S69 S70	B1 B0 S79 S80 S81 S82 S83 S84
1 1 1 0	B1 B0 X S71 S72 S73 S74 S75	B1 B0 S85 S86 S87 S88 S89 S90
1 1 1 1	B1 B0 X S76 S77 S78 S79 S80	B1 B0 S91 S92 S93 S94 S95 S96

NOTE: 1. B1, B0 : Blinking control bit

Control Bit	Blinking Port	
BE B1 B0	5-dot font width	6-dot font width
0 X X	No blink	No blink
1 0 0	No blink	No blink
1 0 1	D4	D5
1 1 X	D4 – D0	D5 – D0

2. S1 – S80: Icon pattern ON/OFF in 5-dot font width
   S1 – S96: Icon pattern ON/OFF in 6-dot font width
3. “X”: Don’t care

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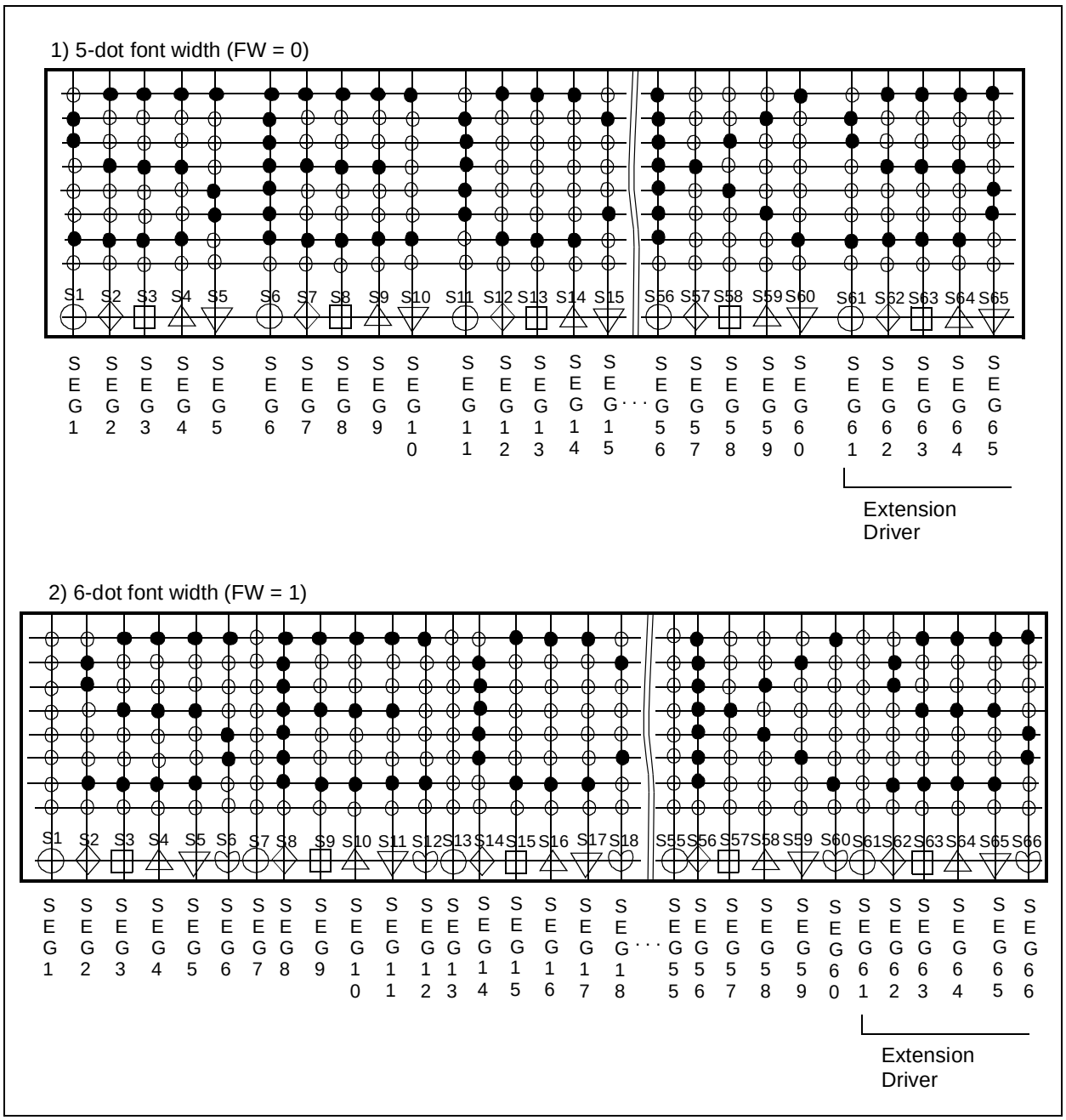

Fig-14. Relationship between SEGRAM and segment display

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INSTRUCTION DESCRIPTION

OUTLINE

To overcome the speed difference between the internal clock of KS0073 and the MPU clock, KS0073 performs internal operation by storing control information to IR or DR. The internal operation is determined according to th signal from MPU, composed of read/write and data bus (Refer to Table 6 and Table 10).
Instruction can be divided largely into four kinds,
(1) KS0073 function set instructions (set display methods, set data length, etc.)
(2) address set instructions to internal RAM
(3) data transfer instructions with internal RAM
(4) others.
The address of internal RAM is automatically increased or decreased by 1.

When IE "High", KS0073 is operated according to Instruction Set 1 (Table 6) and
when IE = "Low", KS0073 is operated according to Instruction Set 2 (Table 10).

NOTE: During internal operation, Busy Flag (DB7) reads High. Busy Flag check must precede the next instruction.
When an MPU program with Busy Flag (DB7) checking is made, 1/2Fosc is necessary for executing the next instruction by the falling edge of the 'E' signal after the Busy Flag (DB7) goes to "Low".

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(1) INSTRUCTION DESCRIPTION 1 (IE = "High")

Table 6. Instruction Set 1 (IE = "High")

Instruction	RE	Instruction Code										Description	Execution Time (fosc 270 kHz)
		RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		
Clear Display	X	0	0	0	0	0	0	0	0	0	1	Write "20H" to DDRAM. and set DDRAM address t "00H" from AC.	1.53 ms
Return Home	0	0	0	0	0	0	0	0	0	1	X	Set DDRAM address to "00H" from AC and return cursor to its original position if shifted. The contents of DDRAM ar not changed.	1.53 ms
Power Down Mode	1	0	0	0	0	0	0	0	0	1	PD	Set power down mode bit. (PD = "1":power down mode set, PD = "0":power down mode disable)	39 µs
Entry Mode Set	0	0	0	0	0	0	0	0	1	I/D	S	Assign cursor moving direction. (I/D = "1": increment, I/D = "0": decrement). and display shift enable bit. (S = "1": make display shift of the enabled lines by the DS4–DS1 bits in the Shift Enable instruction. S = "0":display shift disable)	39 µs
	1	0	0	0	0	0	0	0	1	1	BID	Segment bidirectional function. (BID = "1": Seg60→Seg1, BID = "0": Seg1→Seg60)	39 µs
Display ON/OFF Control	0	0	0	0	0	0	0	1	D	C	B	Set display/cursor/blink on/off (D = "1": display on, D = "0": display off, C = "1": cursor on, C = "0": cursor off, B = "1": blink on, B = "0": blink off).	39 µs
Extended function set	1	0	0	0	0	0	0	1	FW	B/W	NW	Assign font width, black/white inverting of cursor, and 4-line display mode control bit. (FW = "1": 6-dot font width, FW = "0": 5-dot font width, B/W = "1": black/white inverting of cursor enable, B/W = "0": black/white inverting of cursor disable NW "1": 4-line display mode, NW "0": 1-line or 2-line display mode)	39 µs

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(Table 6. continued)

Instruction	RE	Instruction Code										Description	Execution Time (fosc = 270 kHz)
		RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		
Cursor or Display Shift	0	0	0	0	0	0	1	S/C	R/L	X	X	Cursor or display shift. (S/C = “1”: display shift, S/C = “0”: cursor shift, R/L = “1”: shift to right, R/L = “0”: shift to left)	39 µs
Shift Enable	1	0	0	0	0	0	1	DS4	DS3	DS2	DS1	(When DH = “1”) Determine the line for display shift. (DS1 = “1/0”: 1st line display shift enable/disable DS2 = “1/0”: 2nd line display shift enable/disable DS3 = “1/0”: 3rd line display shift enable/disable DS4 = “1/0”: 4th line display shift enable/disable)	39 µs
Scroll Enable	1	0	0	0	0	0	1	HS4	HS3	HS2	HS1	(when DH = “0”) Determine the line for horizontal smooth scroll. (HS1 = “1/0”: 1st line dot scroll enable/disable HS2 = “1/0”: 2nd line dot scroll enable/disable HS3 = “1/0”: 3rd line dot scroll enable/disable HS4 = “1/0”: 4th line dot scroll enable/disable).	39 µs
Function Set	0	0	0	0	0	1	DL	N	RE (0)	DH	REV	Set interface data length, (DL = “1”: 8-bit, DL = “0”: 4-bit), numbers of display line when NW = “0”, (N = “1”: 2-line, N = “0”: 1-line), extension register, RE(“0”), shift/scroll enable, (DH = “1”: display shift enable DH = “0”: dot scroll enable), and reverse bit (REV = “1”: reverse display, REV = “0”: normal display)	39 µs
	1	0	0	0	0	1	DL	N	RE (1)	BE	LP	Set DL, N, RE(“1”) and CGRAM/SEGRAM blink enable (BE) (BE = “1/0”: CGRAM/SEGRAM blink enable/disable LP = “1”: low power mode, LP = “0”: normal operation mode)	39 µs

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(Table 6. continued)

Instruction	RE	Instruction Code										Description	Execution Time (fosc 270 kHz)
		RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		
Set CGRAM Address	0	0	0	0	1	AC5	AC4	AC3	AC2	AC1	AC0	Set CGRAM address in address counter.	39 µs
Set SEGRAM Address	1	0	0	0	1	X	X	AC3	AC2	AC1	AC0	Set SEGRAM address in address counter.	39 µs
Set DDRAM Address	0	0	0	1	AC6	AC5	AC4	AC3	AC2	AC1	AC0	Set DDRAM address in address counter.	39 µs
Set Scroll Quantity	1	0	0	1	X	SQ5	SQ4	SQ3	SQ2	SQ1	SQ0	Set the quantity of horizontal dot scroll.	39 µs
Read Busy Flag and Address	X	0	1	BF	AC6	AC5	AC4	AC3	AC2	AC1	AC0	Can be known whether during internal operation or not by reading BF. The contents of address counter can also be read. (BF = “1”: busy state, BF = “0”: ready state)	0 µs
Write Data	X	1	0	D7	D6	D5	D4	D3	D2	D1	D0	Write data into internal RAM (DDRAM/CGRAM/SEGRAM)	43 µs
Read Data	X	1	1	D7	D6	D5	D4	D3	D2	D1	D0	Read data from internal RAM (DDRAM/CGRAM/SEGRAM)	43 µs

* NOTE: When an MPU program with Busy Flag (DB7) checking is made, 1/2Fosc is necessary for executing the next instruction by the falling edge of the ‘E’ signal after the Busy Flag (DB7) goes to “Low”.

“X” : Don't care

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1) Display Clear

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	0	1

Clear all the display data by writing “20H” (space code) to all DDRAM address, and set DDRAM address to “00H” into AC (address counter). Return cursor to the original status, bringing the cursor to the left edge on first line of the display. Make entry mode increment (I/D = “1”).

2) Return Home: (RE = 0)

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	1	X

Return Home is a cursor return home instruction.
Set DDRAM address to “00H” into the address counter. Return cursor to its original site and return display to its original status, if shifted.
Contents of DDRAM does not change.

3) Power Down Mode Set: (RE = 1)

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	1	PD

Power down mode enable bit set instruction.
PD = “High”, it makes KS0073 suppress current consumption except the current needed for data storage by executing the next three functions.

1. make the output value of all the COM/SEG ports VDD
2. make the COM/SEG output value of the extension driver VDD by setting D output to “High” and M output to “Low”
3. disable voltage converter to remove the current through the divide resistor of power supply.
   This instruction can be used as power sleep mode.
   When PD = “Low”, power down mode becomes disabled.

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4) Entry Mode Set

(1) RE = 0

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	1	I/D	S

Set the moving direction of cursor and display.
I/D: Increment / decrement of DDRAM address (cursor or blink)
When I/D = “High”, cursor/blink moves to right and DDRAM address is increased by 1.
When I/D = “Low”, cursor/blink moves to left and DDRAM address is decreased by 1.
* CGRAM/SEGRAM operates the same as DDRAM, when reading from or writing to CGRAM/SEGRAM.

When S = “High”, after DDRAM write, the display of enabled line by DS1 - DS4 bits in the Shift Enabl instruction is shifted to the right (I/D = “0”) or to the left (I/D = “1”). But it will seem as if the cursor does not move.
When S = “Low”, or DDRAM read, or CGRAM/SEGRAM read/write operation, shift of display as the above function is not performed.

(2) RE = 1

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	1	1	BID

Set the data shift direction of segment in the application set.
BID: Data Shift Direction of Segment
When BID = “Low”, segment data shift direction is set to normal order, from SEG1 to SEG60.
When BID = “High”, segment data shift direction is set reversely. from SEG60 to SEG1.
By using this instruction, the efficiency of the application board area can be raised.
* The BID setting instruction is recommended to be set at the same time level as the function set instruction.
* DB1 bit must be set to “1”.

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5) Display ON/OFF Control (RE = 0)

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	1	D	C	B

Control display/cursor/blink ON/OFF 1 bit register.
D: Display ON/OFF control bit
When D = “High”, entire display is turned on.
When D = “Low”, display is turned off, but display data remains in DDRAM.

C: Cursor ON/OFF control bit
When C = “High”, cursor is turned on.
When C = “Low”, cursor is disappeared in current display, but I/D register preserves its data.

B: Cursor Blink ON/OFF control bit
When B “High”, cursor blink is on, that performs alternately between all the high data and display character at the cursor position. If fosc has a frequency of 270 kHz, blinking has a 370 ms interval.
When B “Low”, blink is off.

6) Extended Function Set (RE = 1)

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	1	F/W	B/W	NW

FW: Font Width control
When FW = “High”, display character font width is assigned to 6-dot, and the execution time becomes 6/5 times than that of the 5-dot font width.
The user font, specified in CGRAM, is displayed into 6-dot font width, bit-5 to bit-0, including the left space bit of CGRAM (Refer to Fig-15).
When FW = “Low”, 5-dot font width is set.

B/W: Black/White Inversion enable bit
When B/W = “High”, black/white inversion at the cursor position is set. In this case, C/B bit of display ON/OFF control instruction becomes a “don’t care” condition. If fosc has frequency of 270 kHz, inversion has 370 ms intervals.

NW: 4 Line mode enable bit
When NW = “High”, 4-line display mode is set. In this case, N bit of function set instruction becomes a “do ’t care” condition.

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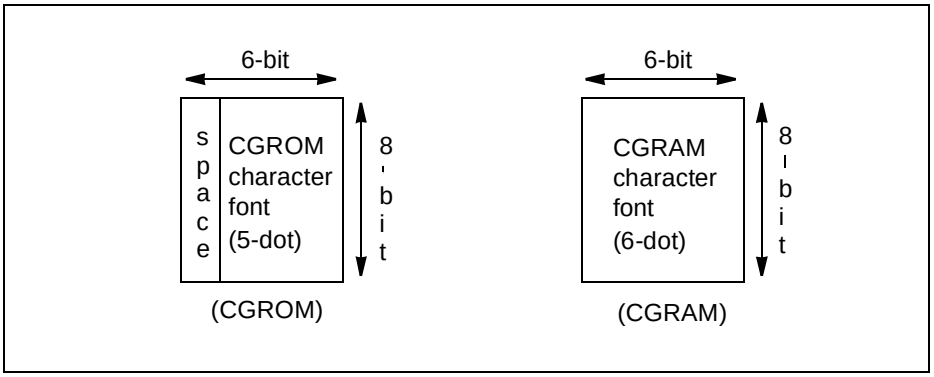

Fig-15. 6-dot font width CGROM/CGRAM

7) Cursor or Display Shift (RE = 0)

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	1	S/C	R/L	-	-

Shifts right/left cursor position or display without writing or reading of display data.
This instruction is used to correct or search display data (Refer to Table 7).
During 2-line mode display, cursor moves to the 2nd line after the 40th digit of the 1st line.
In 4-line mode, cursor moves to the next line, only after every 20th digit of the current line.
Note that display shift is performed simultaneously in all the lines enabled by DS1 - S4 in the Shift Enable instruction.
When displayed data is shifted repeatedly, each line is shifted individually.
When display shift is performed, the contents of the address counter are not changed.
During low power consumption mode, display shift may not be performed normally.

Table 7. Shift patterns according to S/C and R/L bits

S/C	R/L	Operation
0	0	Shift cursor to the left, ADDRESS COUNTER is decreased by 1
0	1	Shift cursor to the right, ADDRESS COUNTER is increased by 1
1	0	Shift all the display to the left, cursor moves according to the display
1	1	Shift all the display to the right, cursor moves according to the display

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8) Shift/Scroll Enable (RE = 1)

(1) DH = 0

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	1	HS4	HS3	HS2	HS1

HS: Horizontal Scroll per Line Enable
This instruction makes valid dot shifts by a display line unit.
HS1, HS2, HS3 and HS4 indicate each line to be dot scrolled, and each scroll is performed individually in each line.
If the line, in 1-line display mode or the 1st line in 2-line display mode is to be scrolled, set HS1 and HS2 to "High". If the 2nd line scroll is needed in 2-line mode, set HS3 and HS4 to "High" (Refer to Table 8).

(2) (DH = 1)

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	1	DS4	DS3	DS2	DS1

DS: Display Shift per Line Enable
This instruction selects the line to be shifted according to each line mode in display shift right/left instruction. DS1, DS2, DS3 and DS4 indicate each line to be shifted, and each shift is performed individually in each line.
If DS1 and DS2 are set to "High" (enable) in 2-line mode, only 1st line is shifted, and the 2nd line is not shifted. When only DS1 "High", only half of the 1st line is shifted. If all the DS bits (DS1 to DS4) are set to "Low" (disable), no display is shifted.

Table 8. Relationship between DS and COM signal

Enable bit	Enabled common signals during shift	Description
HS1/DS1	COM1 ~ COM8	The part of display line that corresponds to enabled common signal can be shifted.
HS2/DS2	COM9 ~ COM16	
HS3/DS3	COM17 ~ COM24	
HS4/DS4	COM25 ~ COM32	

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9) Function Set

(1) (RE = 0)

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	DL	N	RE (0)	DH	REV

DL: Interface data length control bit
When DL = “High”, it means 8-bit bus mode with MPU.
When DL = “Low”, it means 4-bit bus mode with MPU. Hence, DL is a signal to select 8-bit or 4-bit bus mode.
In 4-bit bus mode, it is required to transfer 4-bit data twice.

N: Display line number control bit
It is variable only when NW bit of extended function set instruction is Low.
When N = “Low”, 1-line display mode is set.
When N = “High”, 2-line display mode is set.
When NW = “High”, N bit is invalid, 4-line mode independent of N bit.

RE: Extended function registers enable bit
At this instruction, RE must be “Low”.

DH: Display shift enable selection bit.
When DH = “High”, enables display shift per line.
When DH = “Low”, enables smooth dot scroll.
This bit can be accessed only when IE pin input is “High”.

REV: Reverse enable bit
When REV = “High”, all the display data are reversed. i.e., all the white dots become black and black dots become white.
When REV = “Low”, the display mode is set to normal display.

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(2) (RE = 1)

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	DL	N	RE (1)	BE	LP

DL: Interface data length control bit
When DL = “High”, it means 8-bit bus mode with MPU.
When DL = “Low”, it means 4-bit bus mode with MPU. Hence, DL is a signal to select 8-bit or 4-bit bus mode.
When 4-bit bus mode, it is required to transfer 4-bit data twice.

N: Display line number control bit
It is variable only when NW bit of extended function set instruction is Low.
When N = “Low”, 1-line display mode is set.
When N = “High”, 2-line display mode is set.
When NW = “High”, N bit is invalid, 4-line mode independent of N bit.

RE: Extended function registers enable bit
When RE “High”, extended function set registers, SEGRAM address set registers, BID bit, HS/DS bits of shift/scroll enable instruction and BE bits of function set register can be accessed.

BE: CGRAM/SEGRAM data blink enable bit
BE = “High”, makes user font of CGRAM and segment of SEGRAM blinking. The quantity of blink is assigned the highest 2 bit of CGRAM/SEGRAM.

LP: Low power consumption mode enable bit
When EXT port input is “Low” (without extension driver) and LP bit is set to “High”, KS0073 operates in low power consumption mode.
During 1-line mode KS0073 operates on a 4-division clock, and in 2-line or 4-line mode it operates on 2-division clock. According to this instruction, execution time becomes 4 or 2 times longer.
Note not to use display shift instruction, as it may result in incorrect operation.
And the frame frequency is 5/6 times lower than that of normal operation.

10) Set CGRAM Address (RE = 0)

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	AC5	AC4	AC3	AC2	AC1	AC0

Set CGRAM address to AC.
This instruction makes CGRAM data available from MPU.

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11) Set SEGRAM Address (RE = 1)

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	-	-	AC3	AC2	AC1	AC0

Set SEGRAM address to AC.
This instruction makes SEGRAM data available from MPU.

12) Set DDRAM Address (RE = 0)

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	AC6	AC5	AC4	AC3	AC2	AC1	AC0

Set DDRAM address to AC.
This instruction makes DDRAM data available from MPU.
In 1-line display mode (N = 0, NW = 0), DDRAM address is from “00H” to “4FH”.
In 2-line display mode (N = 1, NW = 0), DDRAM address in the 1st line is from “00H” to “27H”, and DDRAM address in the 2nd line is from “40H” to “67H”.
In 4-line display mode (NW = 1), DDRAM address is from “00H” to “13H” in the 1st line, from “20H” to “33H” in the 2nd line, from “40H” to “53H” in the 3rd line and from “60H” to “73H” in the 4th line.

13) Set Scroll Quantity (RE = 1)

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	X	SQ5	SQ4	SQ3	SQ2	SQ1	SQ0

Setting SQ5 to SQ0, horizontal scroll quantity can be controlled in dot units. (Refer to Table 9)
In this case of KS0073 can show hidden areas of DDRAM by executing smooth scroll from 1 to 48 dots.

Table 9. Scroll quantity according to HDS bits

SQ5	SQ4	SQ3	SQ2	SQ1	SQ0	Function
0	0	0	0	0	0	No shift
0	0	0	0	0	1	shift left by 1-dot
0	0	0	0	1	0	shift left by 2-dot
0	0	0	0	1	1	shift left by 3-dot
:	:	:	:	:	:	:
1	0	1	1	1	1	shift left by 47-dot
1	1	X	X	X	X	shift left by 48-dot

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14) Read Busy Flag & Address

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	1	BF	AC6	AC5	AC4	AC3	AC2	AC1	AC0

This instruction shows whether KS0073 is in internal operation or not. If the resultant BF is High, the internal operation is in progress and should wait until BF to be Low, which by then the next instruction can be performed. In this instruction the value of address counter can also be read.

15) Write data to RAM

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	D7	D6	D5	D4	D3	D2	D1	D0

Write binary 8-bit data to DDRAM/CGRAM/SEGRAM.
The selection of RAM from DDRAM, CGRAM, or SEGRAM, is set by the previous address set instruction: DDRAM address set, CGRAM address set, SEGRAM address set.
RAM set instruction can also determine the AC direction to RAM.
After write operation, the address is automatically increased/decreased by 1, according to the entry mode.

16) Read data from RAM

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	1	D7	D6	D5	D4	D3	D2	D1	D0

Read binary 8-bit data from DDRAM/CGRAM/SEGRAM.
The selection of RAM is set by the previous address set instruction. If address set instruction of RAM is not performed before this instruction, the data that is read first is invalid, as the direction of AC is not determined. If RAM data is read several times without RAM address set instructions before read operation, the correct RAM data can be obtained from the second, but the first data would be incorrect, as there is no time margin to transfer RAM data. In DDRAM read operation, cursor shift instruction plays the same role as DDRAM address set instruction: it also transfers RAM data to output data register.
After read operation address counter is automatically increased/decreased by 1 according to the entry mode. After CGRAM/SEGRAM read operation, display shift may not be executed correctly.

* In the case of RAM write operation, AC is increased/decreased by 1 as in read operation after this. In this time, AC indicates the next address position, but the previous data can only be read by read instruction.

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(2) INSTRUCTION DESCRIPTION 1 (IE =”Low”)

Table 10. Instruction Set 2 (IE = “Low”)

Instruction	RE	Instruction Code										Description	Execution Time (fosc 270 kHz)
		RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		
Clear Display	X	0	0	0	0	0	0	0	0	0	1	Write “20H” to DDRAM an set DDRAM address to “00H” from AC.	1.53 ms
Return Home	X	0	0	0	0	0	0	0	0	1	X	Set DDRAM address to “00H” from AC and return cursor to its original position if shifted. The contents of DDRAM ar not changed.	1.53 ms
Entry Mode Set	X	0	0	0	0	0	0	0	1	I/D	S	Assign cursor moving direction, (I/D = “1”: increment, I/D = “0”: decrement) and display shift enable bit. (S = “1”: make entire display shift of all lines our- in DDRAM write, S = “0”: display shift disable)	39 µs
Display ON/OFF Control	0	0	0	0	0	0	0	1	D	C	B	Set display/cursor/blink on/off (D = “1”: display on, D = “0” : display off, C = “1” : cursor on, C = “0” : cursor off, B = “1” : blink on, B = “0” : blink off).	39 µs
Extended function Set	1	0	0	0	0	0	0	1	FW	BW	NW	Assign font width, black/white inverting of cursor, and 4-line display mode control bit. (FW = “1”: 6-dot font width, FW = “0”: 5-dot font width, B/W = “1”: black/white inverting of cursor enable, B/W = “0”: black/white inverting of cursor disable NW = “1”: 4-line display mode, NW = “0”: 1-line or 2-line display mode)	39 µs
Cursor or Display Shift	0	0	0	0	0	0	1	S/C	R/L	X	X	Cursor or display shift. (S/C = “1” : display shift, S/C = “0” : cursor shift, R/L = “1” : shift to right, R/L = “0” : shift to left).	39 µs

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(Table 10. continued)

Instruction	RE	Instruction Code										Description	Execution Time (fosc 270 kHz)
		RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		
Scroll Enable	1	0	0	0	0	0	1	HS4	HS3	HS2	HS1	Determine the line for horizontal smooth scroll. (HS1 = “1/0” : 1st line dot scroll enable/disabl HS2 = “1/0” : 2nd line dot scroll enable/disable HS3 = “1/0” : 3rd line dot scroll enable/disable HS4 = “1/0” : 4th line dot scroll enable/disable).	39 µs
Function Set	0	0	0	0	0	1	DL	N	RE (0)	X	X	Set interface data length (DL = “1” : 8-bit, DL = “0” : 4-bit), and numbers of display line when NW “0”, (N = “1” : 2-line, N = “0” : 1-line), extension register, RE(“0”)	39 µs
	1	0	0	0	0	1	DL	N	RE (1)	BE	LP	Set DL, N, RE(“1”) and CGRAM/SEGRAM blink enable (BE) (BE “1/0” : CGRAM/SEGRAM blink enable/disabl LP = “1” : low power mode, LP = “0” : normal operation mode)	39 µs
Set CGRAM Address	0	0	0	0	1	AC5	AC4	AC3	AC2	AC1	AC0	Set CGRAM address in address counter.	39 µs
Set SEGRAM Address	1	0	0	0	1	X	X	AC3	AC2	AC1	AC0	Set SEGRAM address in address counter.	39 µs

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Instruction	RE	Instruction Code										Description	Execution Time (fosc 270 kHz)
		RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		
Set DDRAM Address	0	0	0	1	AC6	AC5	AC4	AC3	AC2	AC1	AC0	Set DDRAM address in address counter.	39 µs
Set Scroll Quantity	1	0	0	1	X	SQ5	SQ4	SQ3	SQ2	SQ1	SQ0	Set the quantity of horizontal dot scroll.	39 µs
Read Busy flag and Address	X	0	1	BF	AC6	AC5	AC4	AC3	AC2	AC1	AC0	Can be known whether during internal operation or not by reading BF. The contents of address counter can also be read. (BF = "1": busy state, BF = "0": ready state)	0 µs
Write Data	X	1	0	D7	D6	D5	D4	D3	D2	D1	D0	Write data into internal RAM (DDRAM/CGRAM/SEGRAM)	43 µs
Read Data	X	1	1	D7	D6	D5	D4	D3	D2	D1	D0	Read data from internal RAM (DDRAM/CGRAM/SEGRAM)	43 µs

* NOTE: When an MPU program with Busy Flag(DB7) checking is made, 1/2Fosc (is necessary) for executing the next instruction by the falling edge of the 'E' signal after the Busy Flag(DB7) goes t "Low".

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1) Display Clear

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	0	1

Clear all the display data by writing “20H” (space code) to all DDRAM address, and set DDRAM address to “00H” into AC (address counter). Return cursor to the original status, namely, bring the cursor to the left edge on first line of the display.
And entry mode is set to increment mode (I/D = “High”).

2) Return Home

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	1	X

Return Home is the cursor return home instruction.
Set DDRAM address to “00H” into the address counter. Return cursor to its original site and return display to its original status, if shifted.
Contents of DDRAM does not change.

3) Entry Mode Set

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	1	I/D	S

Set the moving direction of cursor and display.
I/D : Increment / decrement of DDRAM address (cursor or blink)
When I/D = “High”, cursor/blink moves to right and DDRAM address is incr ased by 1.
When I/D = “Low”, cursor/blink moves to left and DDRAM address is decreased by 1.
* CGRAM/SEGRAM operates identically to the DDRAM, when reading from or writing to CGRAM/SEGRAM.

When S = “High”, after DDRAM write, the entire display of all lines is shifted to the right (I/D = “Low”) or to the left (I/D = “High”). But it will seem as if the cursor is not moving.
When S = “Low”, or DDRAM read, or CGRAM/SEGRAM read/write operation, shift of entire display is not performed.

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4) Display ON/OFF Control (RE = 0)

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	1	D	C	B

Control display/cursor/blink ON/OFF 1 bit register.
D : Display ON/OFF control bit
When D = “High”, entire display is turned on.
When D = “Low”, display is turned off, but display data remains in DDRAM.

C : Cursor ON/OFF control bit
When C = “High”, cursor is turned on.
When C = “Low”, cursor is disappeared in current display, but I/D register preserves its data.

B : Cursor Blink ON/OFF control bit
When B = “High”, cursor blink is on, which performs alternately between all the high data and display character at the cursor position. If fosc has 270 kHz frequency, blinking has 370 ms interval.
When B = “Low”, blink is off.

5) Extended Function Set (RE = 1)

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	1	FW	BW	NW

FW : Font Width control
When FW = “High”, display character font width is assigned to 6-dot and execution time becomes 6/5 times than that of 5-dot font width.
The user font, specified in CGRAM, is displayed into 6-dot font width, bit-5 to bit-0,including the left space bit of CGRAM.(Refer to Fig-16)
When FW = “Low”, 5-dot font width is set.

B/W : Black/White Inversion enable bit
When B/W = “High”, black/white inversion at the cursor position is set. In this case C/B bit of display ON/OFF control instruction becomes a don’t car condition. If fosc has frequency of 270 kHz, inversion has 370 ms intervals.

NW : 4 Line mode enable bit
When NW = “High”, 4 line display mode is set. In this case N bit of function set instruction becomes “don’t care” condition.

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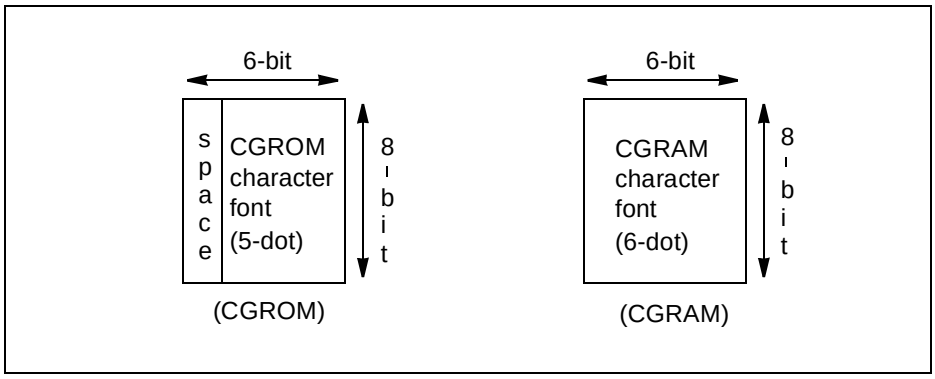

Fig-16. 6-dot font width CGROM/CGRAM

6) Cursor or Display Shift (RE = 0)

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	1	S/C	R/L	-	-

Shifting of right/left cursor position or display without writing or reading of display data.
This instruction is used to correct or search display data.(Refer to Table 7)
During 2-line mode display, cursor moves to the 2nd line after 40th digit of 1st line.
In 4-line mode, cursor moves to the next line, only after every 20th digit of the current line.
Note that display shift is performed simultaneously in all the lines.
When displayed data is shifted repeatedly, each line is shifted individually.
When display shift is performed, the contents of the address counter are not changed.

Table 11. Shift patterns according to S/C and R/L bits

S/C	R/L	Operation
0	0	Shift cursor to the left, ADDRESS COUNTER is decreased by
0	1	Shift cursor to the right, ADDRESS COUNTER is increased by 1
1	0	Shift the entire display to the left, cursor moves according to the display
1	1	Shift the entire display to the right, cursor moves according to the display

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7) Scroll Enable (RE = 1)

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	1	HS4	HS3	HS2	HS1

HS : Horizontal Scroll per Line Enable
This instruction makes valid dot shift by a display line unit.
HS1, HS2, HS3 and HS4 indicate each line to be dot scrolled, and each scroll is performed individually i each line.
If the line in 1-line display mode or the 1st line in 2-line display mode is to be scrolled, set HS1 and HS2 to "High". If the 2nd line scroll is needed in 2-line mode, set HS3 and HS4 t "High". (Refer to Table 8)

8) Function Set

(1) RE = 0

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	DL	N	RE (0)	-	-

DL : Interface data length control bit
When DL = "High", it means 8-bit bus mode with MPU.
When DL ="Low", it means 4-bit bus mode with MPU. Hence, DL is a signal to select 8-bit or 4-bit bus mode.
In 4-bit bus mode, it is required to transfer 4-bit data twice.

N : Display line number control bit
It is variable only when NW bit of extended function set instruction is Low.
When N = "Low", 1-line display mode is set.
When N = "High", 2-line display mode is set.
When NW = "High", N bit is invalid, 4-line mode independent of N bit.

RE : Extended function registers enable bit
At this instruction, RE must be "Low".

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(2) RE = 1

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	DL	N	RE (1)	BE	LP

DL : Interface data length control bit
When DL = “High”, it means 8-bit bus mode with MPU.
When DL = “Low”, it means 4-bit bus mode with MPU. Hence, DL is a signal to select 8-bit or 4-bit bus mode.
In 4-bit bus mode, it is required to transfer 4-bit data twice.

N : Display line number control bit
It is variable only when NW bit of extended function set instruction is Low.
When N = “Low”, 1-line display mode is set.
When N = “High”, 2-line display mode is set.
When NW = “High”, N bit is invalid, 4-line mode independent of N bit.

RE : Extended function registers enable bit
When RE “High”, extended function set registers, SEGRAM address set registers, HS bits of scroll enable instruction and BE bits of function set register can be accessed.

BE : CGRAM/SEGRAM data blink enable bit
BE = “High”, makes user font of CGRAM and segment of SEGRAM blinking. The quantity of blink is assigned the highest 2 bit of CGRAM/SEGRAM.

LP : Low power consumption mode enable bit
When EXT port input is “Low” (without extension driver) and LP bit is set to “High”, KS0073 operates i low power consumption mode.
During 1-line mode KS0073 operates on a 4-division clock, and in 2-line or 4-line mode it operates on 2-division clock. According to this instruction, execution time becomes 4 or 2 times longer.
Note not to use display shift instruction, as it may result in incorrect operation.
And the frame frequency is 5/6 times lower than that of normal operation.

9) Set CGRAM Address (RE = 0)

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	AC5	AC4	AC3	AC2	AC1	AC0

Set CGRAM address to AC.
This instruction makes CGRAM data available from MPU.

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10) Set SEGRAM Address (RE = 1)

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	-	-	AC3	AC2	AC1	AC0

Set SEGRAM address to AC.
This instruction makes SEGRAM data available from MPU.

11) Set DDRAM Address (RE = 0)

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	AC6	AC5	AC4	AC3	AC2	AC1	AC0

Set DDRAM address to AC.
This instruction makes DDRAM data available from MPU.
In 1-line display mode (N = 0, NW = 0), DDRAM address is from “00H” to “4FH”.
In 2-line display mode (N = 1, NW = 0), DDRAM address in the 1st line is from "00H" t “27H”, and DDRAM address in the 2nd line is from “40H” to “67H”.
In 4-line display mode (NW = 1), DDRAM address is from “00H” to “13H” in the 1st line, from “20H” to “33H” in the 2nd line, from “40H” to “53H” in the 3rd line and from “60H” to “73H” in the 4th line.

12) Set Scroll Quantity (RE = 1)

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	X	SQ5	SQ4	SQ3	SQ2	SQ1	SQ0

Setting SQ5 to SQ0, horizontal scroll quantity can be controlled in dot units. (Refer to Table 12).
In this case KS0073 executes dot smooth scroll from 1 to 48 dots.

Table 12. Scroll quantity according to HDS bits

SQ5	SQ4	SQ3	SQ2	SQ1	SQ0	Function
0	0	0	0	0	0	No shift
0	0	0	0	0	1	shift left by 1-dot
0	0	0	0	1	0	shift left by 2-dot
0	0	0	0	1	1	shift left by 3-dot
:	:	:	:	:	:	:
1	0	1	1	1	1	shift left by 47-dot
1	1	X	X	X	X	shift left by 48-dot

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13) Read Busy Flag & Address

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	1	BF	AC6	AC5	AC4	AC3	AC2	AC1	AC0

This instruction shows whether KS0073 is in internal operation or not. If the resultant BF is High, the internal operation is in progress and should wait until BF becomes “Low”, which by then the next instruction can be performed. In this instruction value of address counter can also be read.

14) Write data to RAM

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	D7	D6	D5	D4	D3	D2	D1	D0

Write binary 8-bit data to DDRAM/CGRAM/SEGRAM.
The selection of RAM from DDRAM, CGRAM, or SEGRAM, is set by the previous address set instruction : DDRAM address set, CGRAM address set, SEGRAM address set. RAM set instruction can also determines the AC direction to RAM.
After write operation, the address is automatically increased/decreased by 1, according to the entry mode.

15) Read data from RAM

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	1	D7	D6	D5	D4	D3	D2	D1	D0

Read binary 8-bit data from DDRAM/CGRAM/SEGRAM.
The selection of RAM is set by the previous address set instruction. If address set instruction of RAM is not performed before this instruction, the data which has been read first is invalid, as the direction of AC is not determined. If the RAM data several is read times without RAM address set instruction before read operation, the correct RAM data from the second, but the first data would be incorrect, as there is no time margin to transfer RAM data. In case of DDRAM read operation, cursor shift instruction plays the same role as DDRAM address set instruction : it also transfer RAM data to output data register.
After read operation address counter is automatically increased/decreased by 1 according to the entry mode. After CGRAM/SEGRAM read operation, display shift may not be executed correctly.

* In case of RAM write operation, AC is increased/decreased by 1 as in read operation after this. In this time, AC indicates the next address position, but the previous data can only be read by read instruction.

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INTERFACE WITH MPU

KS0073 can transfer data in bus mode (4-bit or 8-bit) or serial mode with MPU. Hence, both types, 4 or 8-bit MPU can be used. In case of 4-bit bus mode, data transfer is performed by twice to transfer 1 byte data.

(1) When interfacing data length are 4-bit, only 4 ports, from DB4 to DB7, are used as data bus.
At first, higher 4-bit (in case of 8-bit bus mode, the contents of DB4 - DB7) are transferred, and then lower 4-bit (in case of 8-bit bus mode, the contents of DB0 - DB3) are transferred. So transfer is performed by twice. Busy Flag outputs "High" after the second transfer is ended.

(2) When interfacing data length are 8-bit, transfer is performed at a time through 8 ports, from DB0 to DB7.

(3) If IM port is set to "Low", serial transfer mode is set.

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Interface with MPU in Bus Mode

1) Interface with 8-bit MPU

If 8-bit MPU is used, KS0073 can connect directly with that.
In this case, port E, RS, R/W and DB0 to DB7 need to interface each other.
Example of timing sequence is shown below.

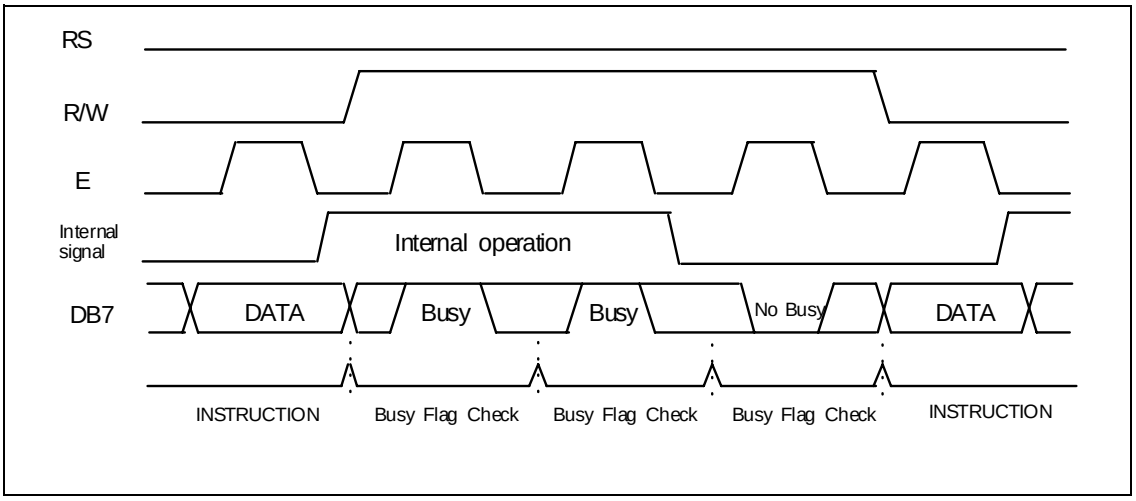

Fig-17. Example of 8-bit Bus Mode Timing Sequence

2) Interface with 4-bit MPU

If 4-bit MPU is used, KS0073 can connect directly with this.
In this case, port E, RS, R/W and DB4 to DB7 need to interface each other. The transfer is performed by twice.
Example of timing sequence is shown below.

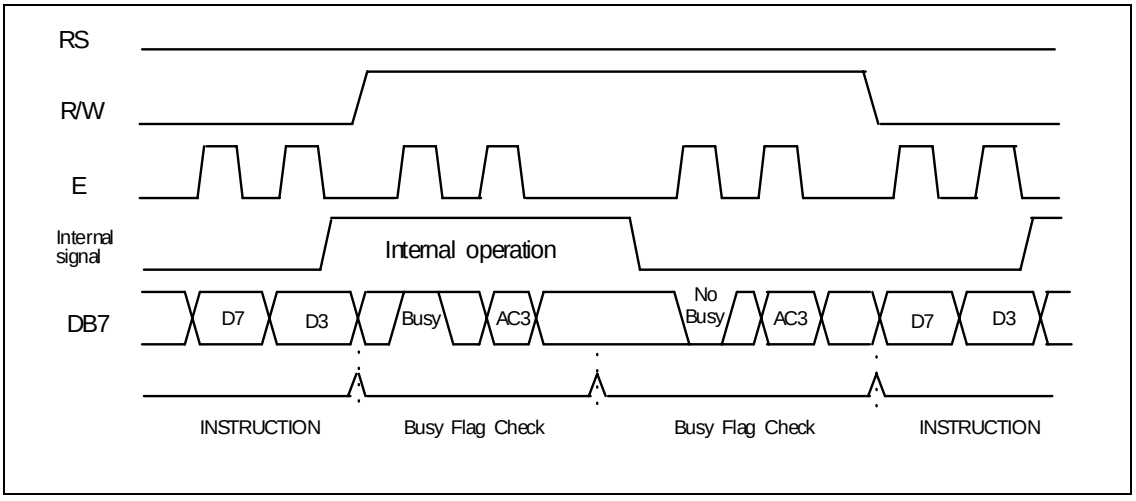

Fig-18. Example of 4-bit Bus Mode Timing Sequence

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Interface with MPU in Serial Mode

When IM port input is “Low”, serial interface mode is started. At this time, all three ports, SCLK (synchronizing transfer clock), SID (serial input data), and SOD (serial output data), are used. If KS0073 is to be used with other chips, chip select port (CS) can be used. By setting CS to “Low”, KS0073 can receive SCLK input. If CS is set to “High”, KS0073 resets the internal transfer counter.

Before transferring real data, start byte has to be transferred. It is composed of succeeding 5 “High” bits, read write control bit (R/W), register selection bit (RS), and end bit that indicates the end of start byte. Whenever succeeding 5 “High” bits are detected by KS0073, it resets the serial transfer counter and prepares to receive next informations.
The next input data is the register selection bit which determines which register is to be used, and read write control bit that determines the direction of data. Then end bit is transferred, which must have “Low” value t show the end of start byte. (Refer to Fig 19, Fig 20)

(1) Write Operation (R/W = 0)
After start byte is transferred from MPU to KS0073, 8-bit data is transferred which is divided into 2 bytes, each byte has 4 bit's real data and 4 bit's partition token data. For example, if real data is "10110001" (D0 - D7), then serially transferred data becomes "1011 0000 0001 0000" where 2nd and 4th 4 bits must be "0000" for safe transfer.
To transfer several bytes continuously without changing R/W bit and RS bit, start byte transfer is needed only at first starting time.
i.e., after the first start byte is transferred, real data succeeding can be transferred.

(2) Read Operation (R/W = 1)
After start byte is transferred to KS0073, MPU can receive 8-bit data through the SOD port at a time from the LSB. Waiting time is needed to insert between start byte and data reading, as internal reading from RAM requires some delay. Continuous data reading is possible such as serial write operation. It also needs only one start bytes, only if some delay between reading operations of each byte is inserted. During the reading operation, KS0073 observes succeeding 5 "High" from MPU. If detected, KS0073 restarts serial operation at once and prepares to receive RS bit. So in continuous reading operation, SID port must be "Low".

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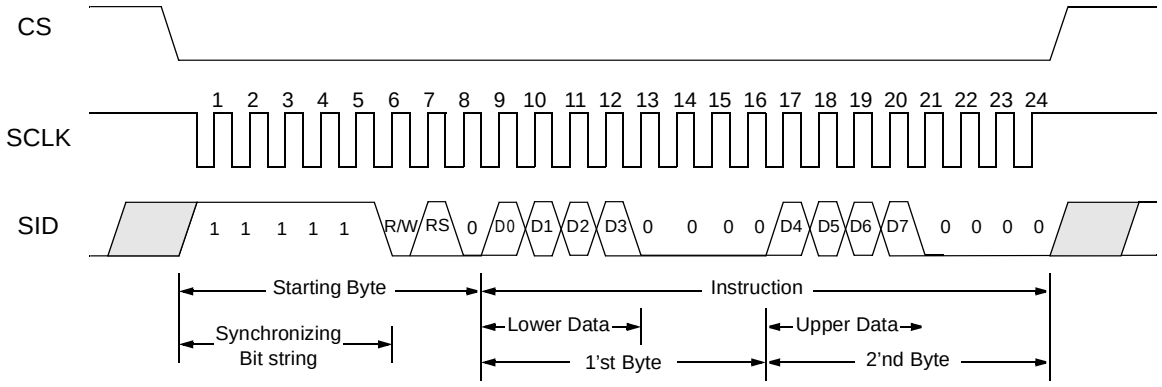
(1) Serial Write Operatio



(2) Serial Read Operation

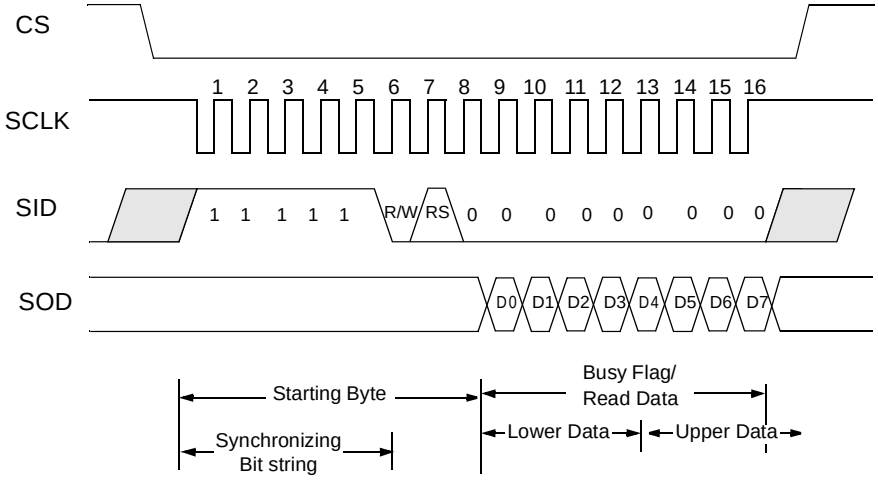


Fig-19. Timing Diagram of Serial Data Transfer

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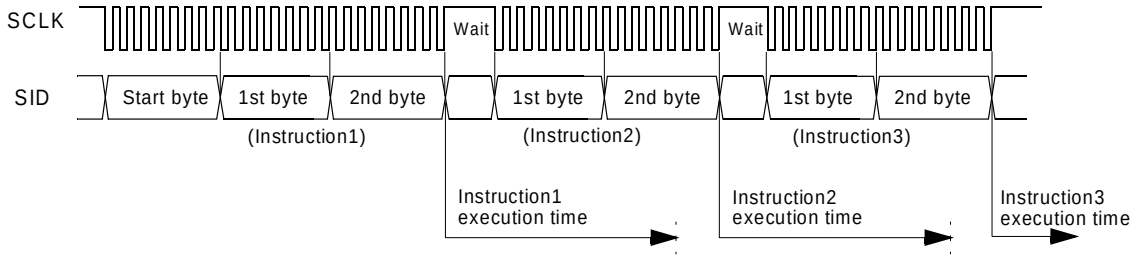
(1) Continuous Write Operation



(2) Continuous Read Operation

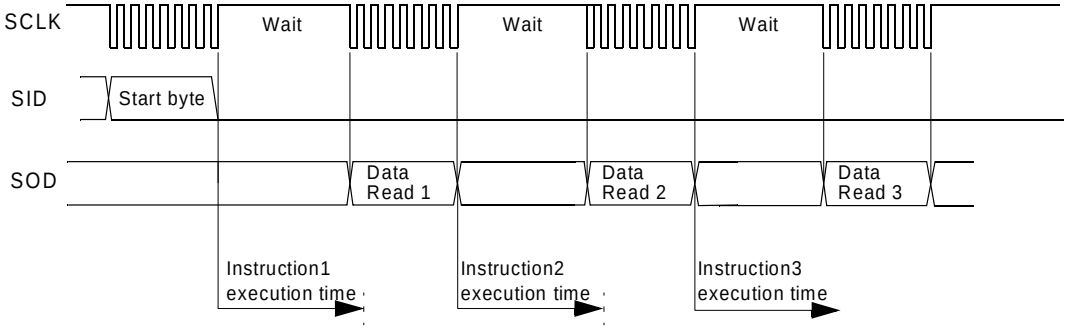


Fig-20. Timing Diagram of Continuous Data Transfer

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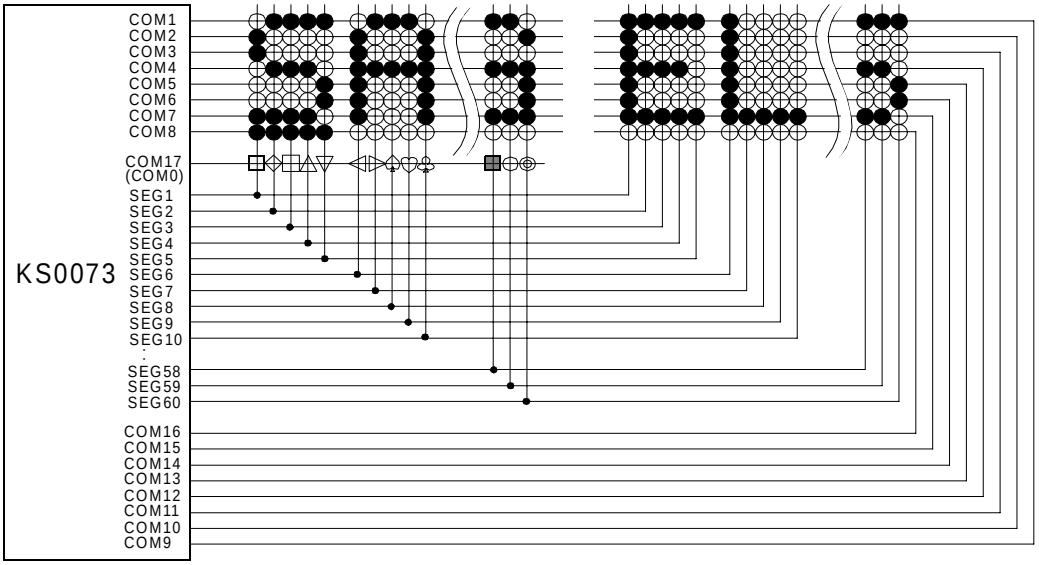
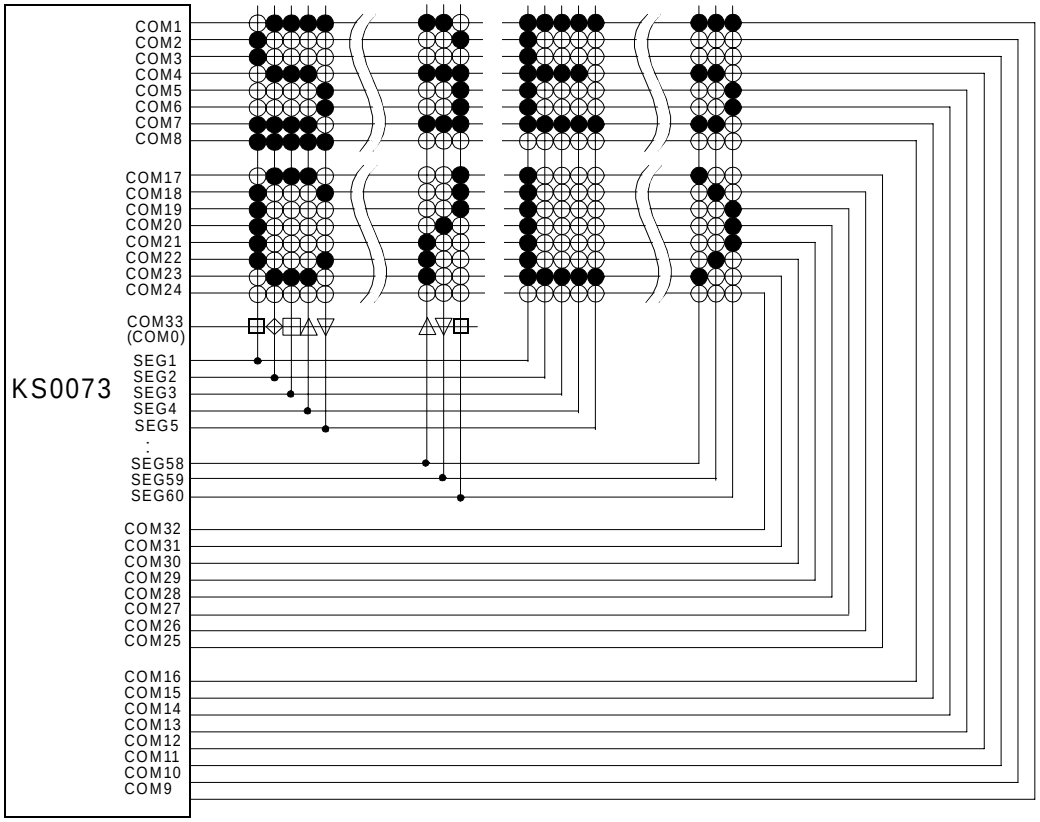
APPLICATION INFORMATION ACCORDING TO LCD

1) LCD Panel: 24 characters × 1-line format (5-dot font, 1/17 duty)



2) LCD Panel: 24 character × 2-line format (5-dot font, 1/33 duty)



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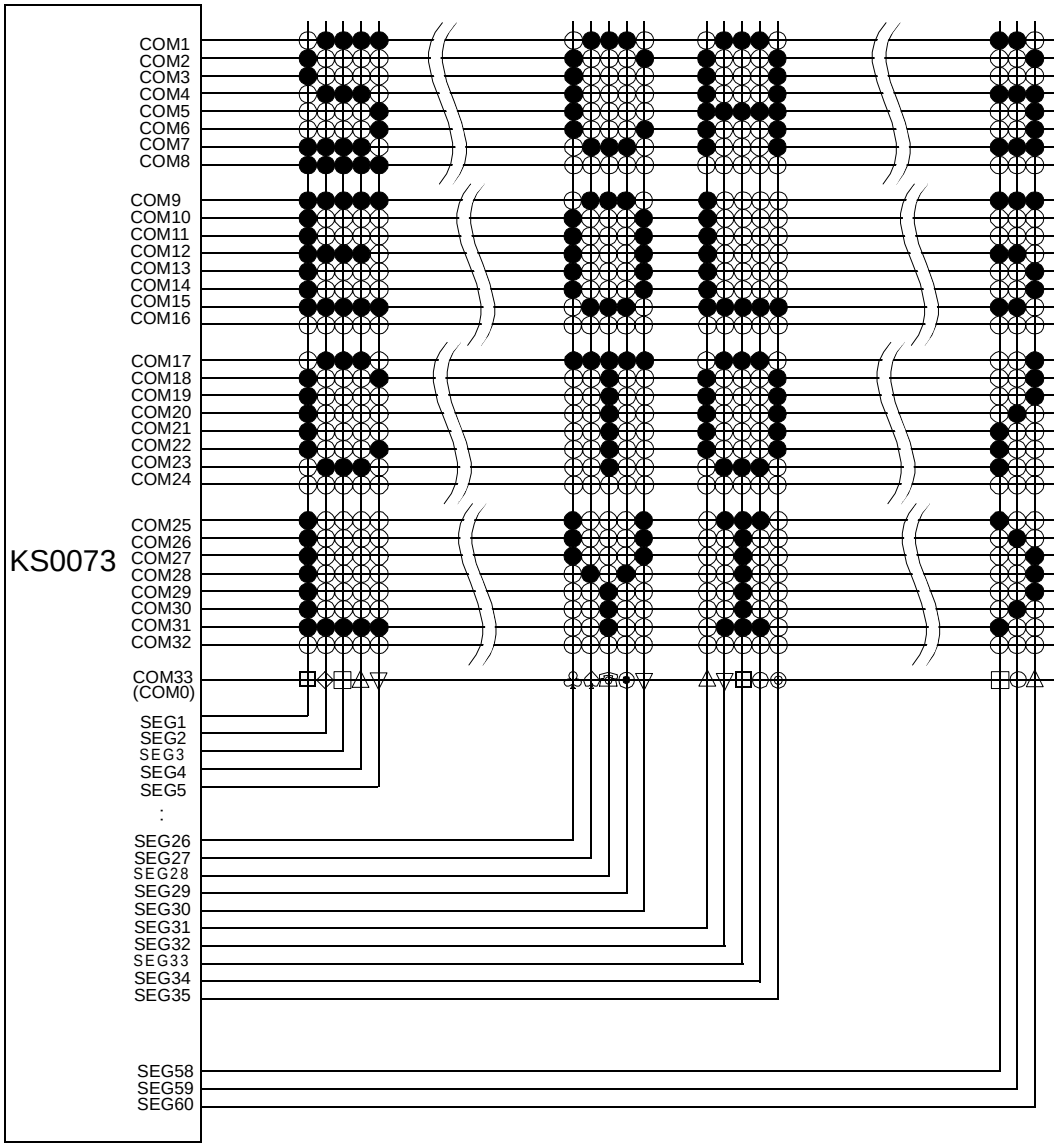
3) LCD Panel: 12 character × 4-line format (5-dot font, 1/33 duty)



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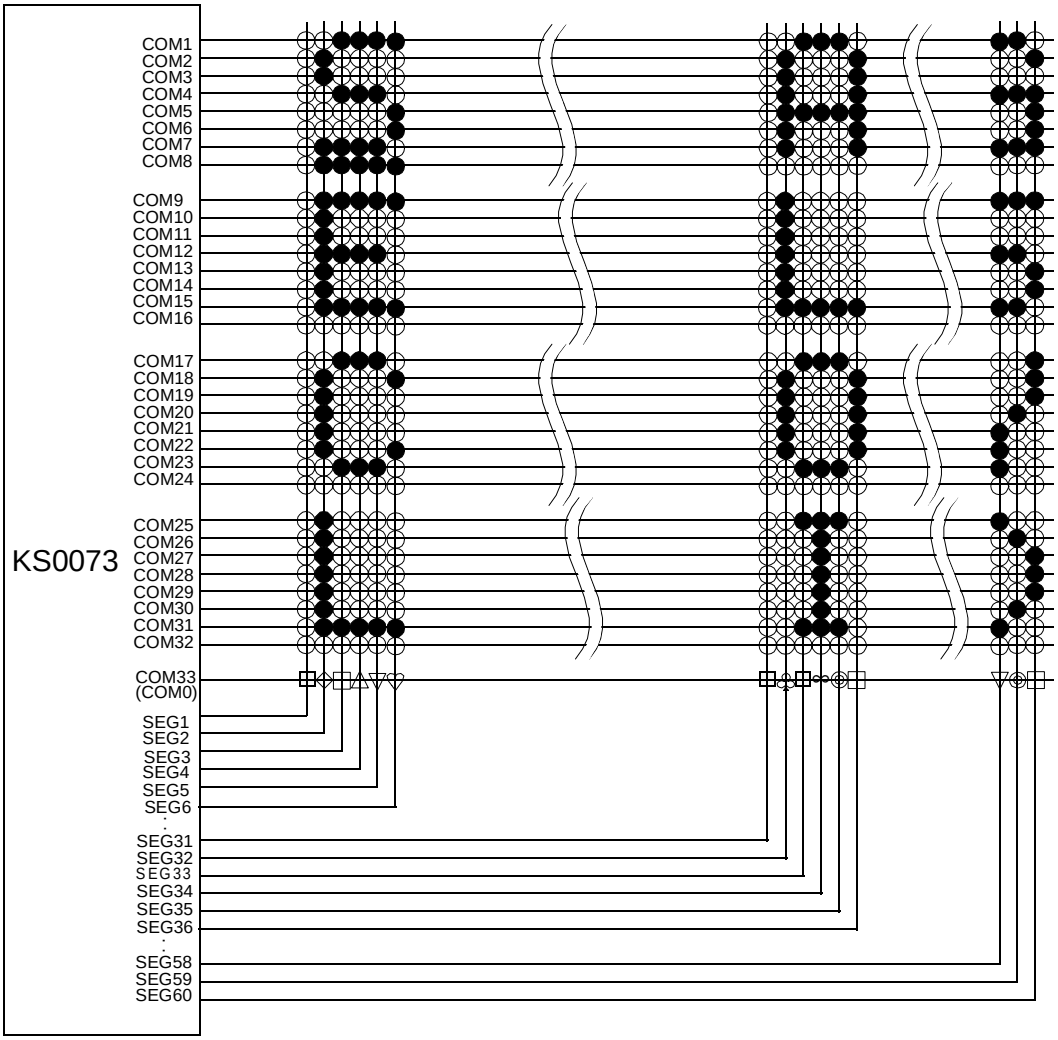
4) LCD Panel: 10 characters × 4-line format (6-dot font, 1/33 duty)



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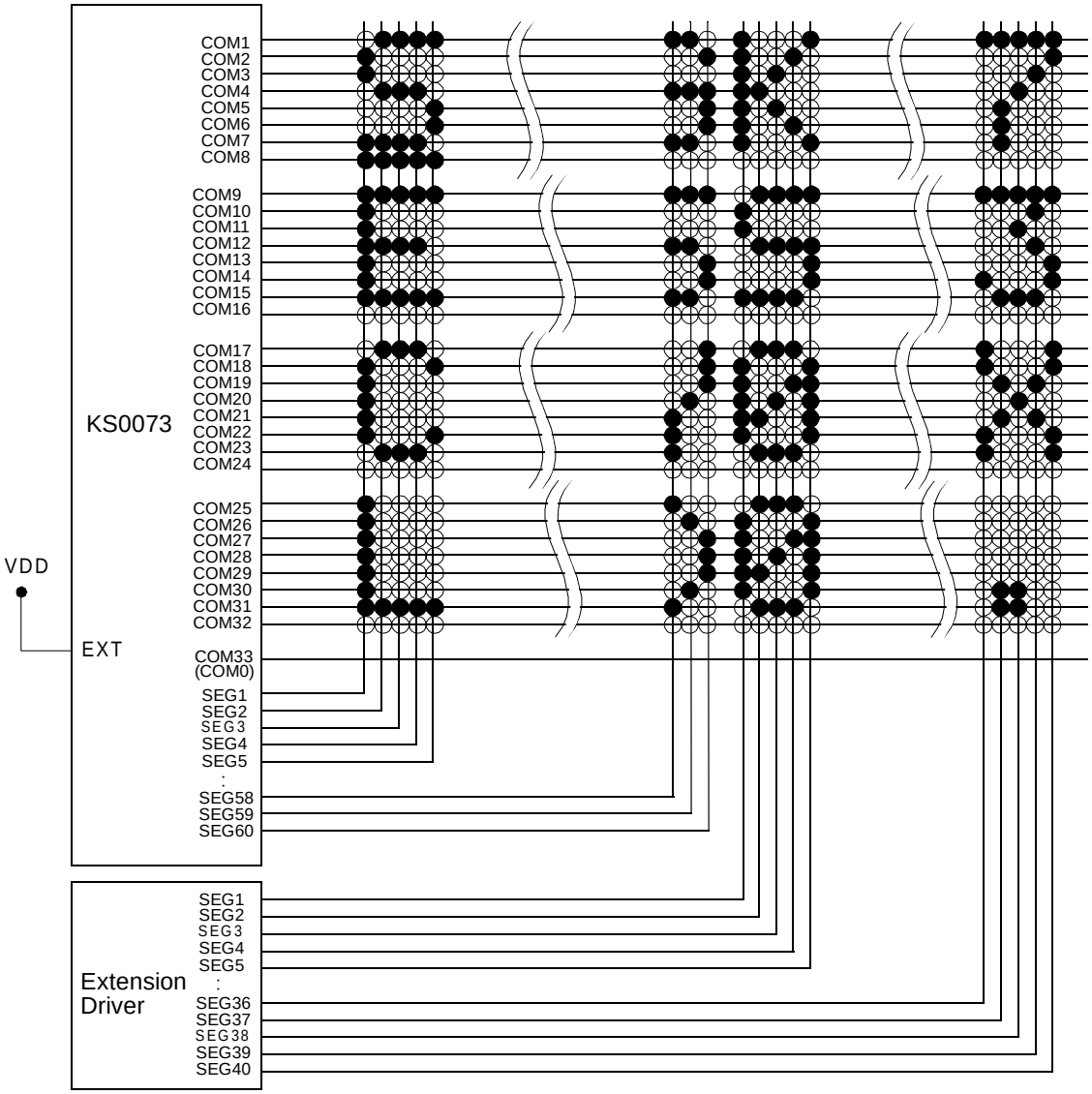
5) LCD Panel: 20 characters × 4-line format (5-dot font, 1/33 duty)



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INITIALIZING

1) Initializing by Internal Reset Circuit

When the power is turned on, KS0073 is initialized automatically by power on reset circuit.
During the initialization, the following instructions are executed, and BF(Busy Flag) is kept "High"(busy state) to the end of initialization.

(1) Display Clear instruction
Write "20H" to all DDRAM
(2) Set Functions instruction
DL = 1 : 8-bit bus mode
N = 1 : 2-line display mode
RE = 0 : Extension register disable
BE = 0 : CGRAM/SEGRAM blink OFF
LP = 0 : Operate in normal mode (Not in Low Power Mode)
DH = 0 : Horizontal scroll enable
REV = 0 : Normal display mode (Not reversed display)
(3) Control Display ON/OFF instructio
D = 0 : Display OFF
C = 0 : Cursor OFF
B = 0 : Blink OFF
(4) Set Entry Mode instruction
I/D = 1 : Increment by 1
S = 0 : No entire display shift
BID = 0 : Normal direction segment port
(5) Set Extension Function instruction
FW = 0 : 5-dot font width character display
B/W = 0 : Normal cursor (8th line)
NW = 0 : Not 4-line display mode, 2-line mode is set because of N("1")
(6) Enable Scroll/Shift instructio
HS = 0000 : Scroll per line disable
DS = 0000 : Shift per line disable
(7) Set scroll Quantity instruction
SQ = 000000 : Not scroll

2) Initializing by Hardware RESET input

When RESET pin = "Low", KS0073 can be initialized as in the case of power on reset.
During the power on reset operation, this pin is ignored.

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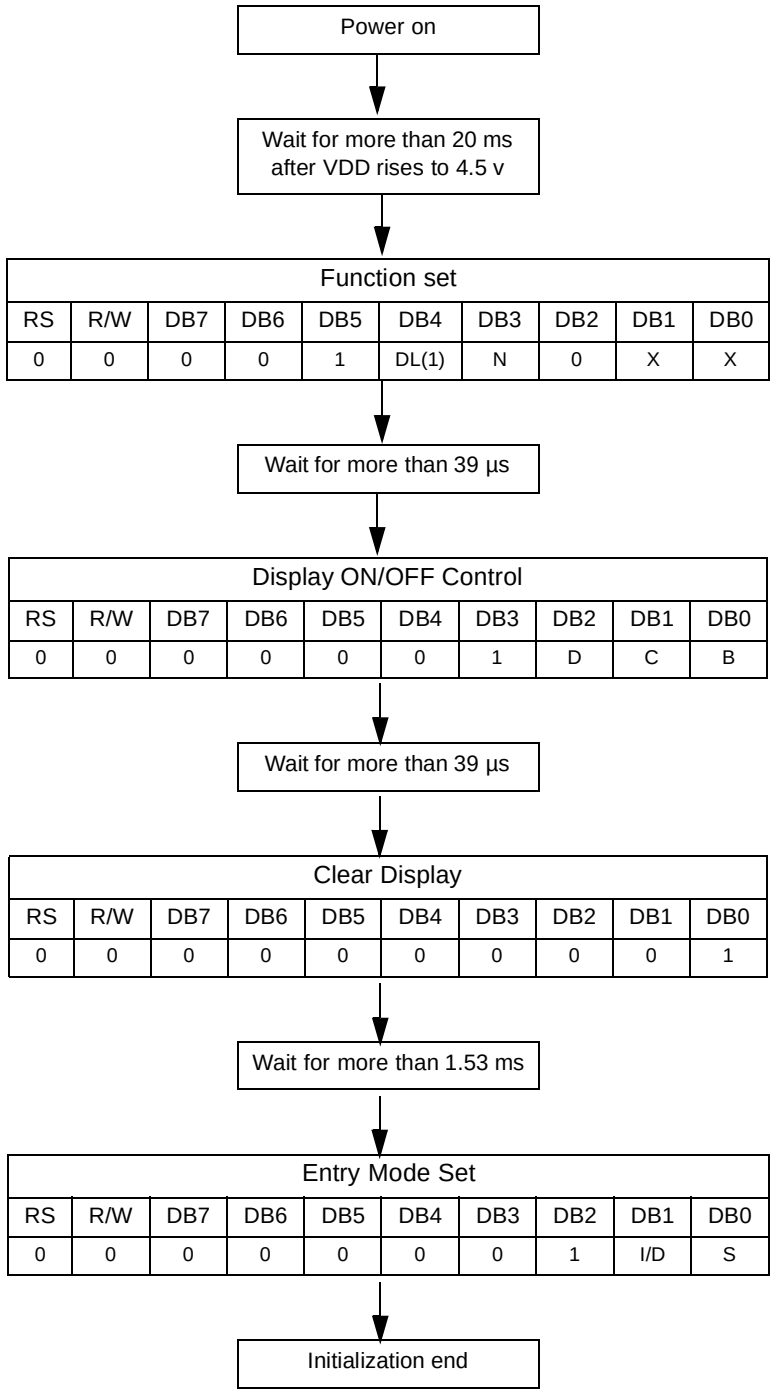
INITIALIZING BY INSTRUCTION

1) 8-bit interface mode



Condition : fosc=270kHz

DL	0	4-bit interface
	1	8-bit interface
N	0	1-line mod
	1	2-line mod
D	0	display off
	1	display on
C	0	cursor off
	1	cursor on
B	0	blink off
	1	blink on
I/D	0	decrement mode
	1	increment mode
S	0	entire shift off
	1	entire shift on

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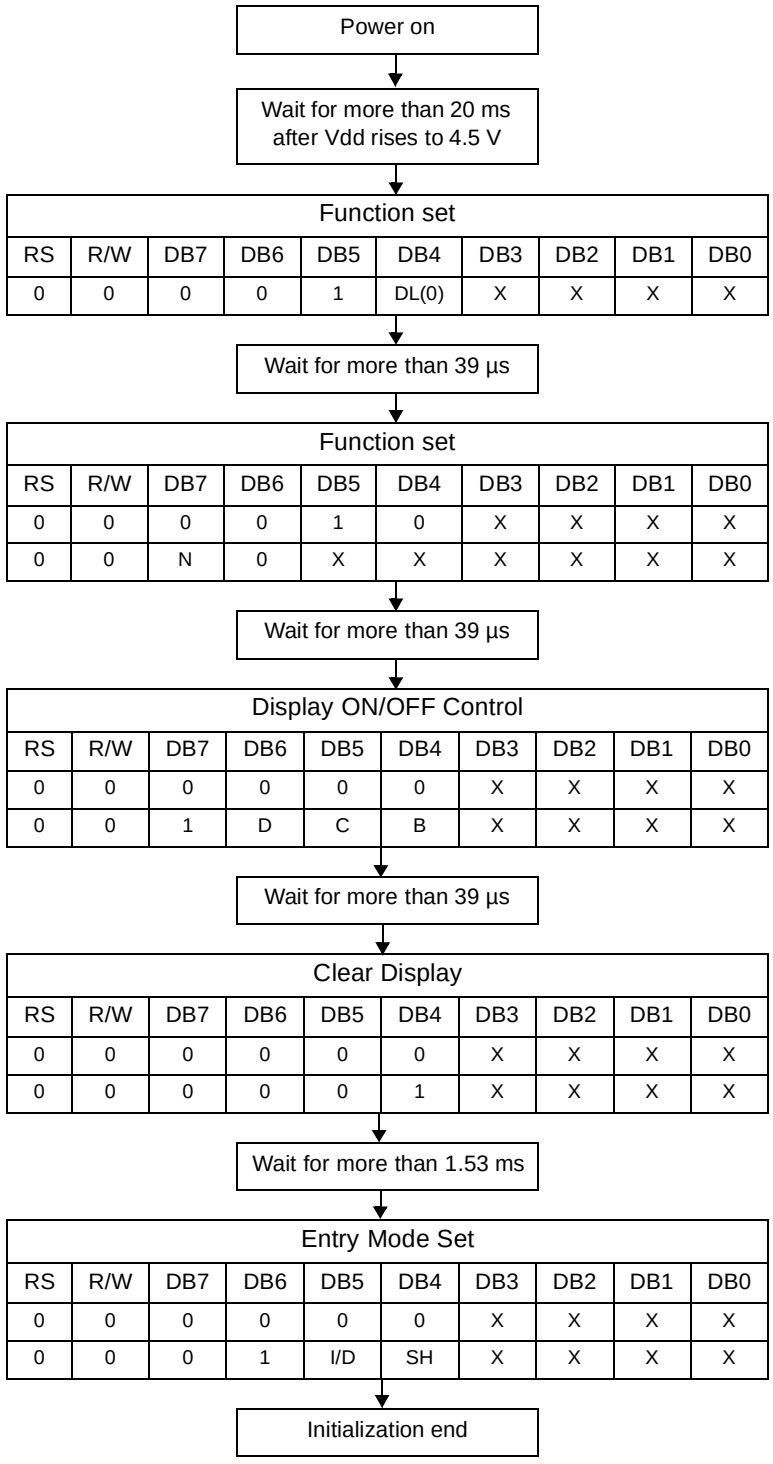
2) 4-bit interface mode



Condition : fosc=270kHz

DL	0	4-bit interface
	1	8-bit interface

N	0	1-line mode
	1	2-line mode

D	0	display off
	1	display on

C	0	cursor off
	1	cursor on

B	0	blink off
	1	blink on

I/D	0	decrement mode
	1	increment mode

SH	0	entire shift off
	1	entire shift o

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EXAMPLE OF INSTRUCTION AND DISPLY CORRESPONDENCE

1) IE='Low'

1. Power supply on: Initialized by the internal power on reset circuit

LCD DISPLAY

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0

2. Function Set: 8-bit, 1-line, RE(0)

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	1	0	0	X	X

3. Display ON/OFF Control: Display/Cursor on

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	1	1	1	0

_

4. Entry Mode Set: Increment

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	1	1	0

_

5. Write Data to DDRAM: Write S

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	0	1	0	1	0	0	1	1

S_

6. Write Data to DDRAM: Write A

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	0	1	0	0	0	0	0	1

SA_

7. Write Data to DDRAM: Write M

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	0	1	0	0	1	1	0	1

SAM_

8. Write Data to DDRAM: Write S

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	0	1	0	1	0	0	1	1

SAMS_

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9. Write Data to DDRAM: Write U

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	0	1	0	1	0	1	0	1

SAMSU_

10. Write Data to DDRAM: Write N

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	0	1	0	0	1	1	1	0

SAMSUN_

11. Write Data to DDRAM: Write G

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	0	1	0	0	0	1	1	1

SAMSUNG_

12. Cursor or Display Shift: Cursor shift to right

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	1	0	1	X	X

SAMSUNG _

13. Entry Mode Set: Entire display shift enable

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	1	1	1

SAMSUNG _

14. Write Data to DDRAM: Write K

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	0	1	0	0	1	0	1	1

AMSUNG K_

15. Write Data to DDRAM: Write S

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	0	1	0	1	0	0	1	1

MSUNG KS_

16. Write Data to DDRAM: Write

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	0	0	1	1	0	0	0	0

SUNG KS0_

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17. Write Data to DDRAM: Write

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	0	0	1	1	0	0	0	0

UNG KS00_

18. Write Data to DDRAM: Write

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	0	0	1	1	0	1	1	1

NG KS007_

19. Write Data to DDRAM: Write

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	0	0	1	1	0	0	1	0

G KS0072_

20. Cursor or Display Shift: Cursor shift to left

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	1	0	0	X	X

G KS0072

21. Write Data to DDRAM: Write 3

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	0	0	1	1	0	0	1	1

KS0073_

22. Return Home

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	1	X

SAMSUNG KS0073

23. Clear Display

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	0	1

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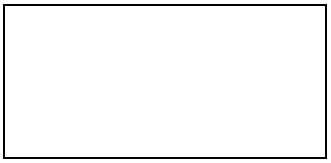
2) IE='High'

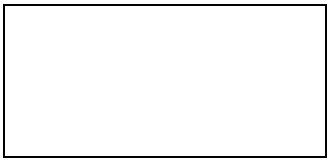
1. Power supply on: Initialized by the internal power on reset circuit

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0



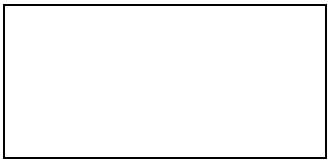
2. Function Set: 8-bit, RE(1)

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	1	1	1	0	0



3. Extended Function Set: 5-font, 4-lin

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	1	0	0	1

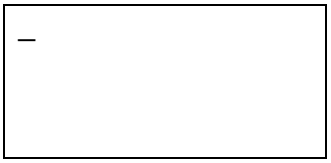


4. Function Set: RE(0)

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	1	1	0	0	0

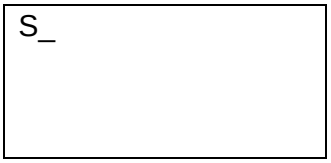
5. Display ON/OFF Control: Display/Cursor on

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	1	1	1	0



6. Write Data to DDRAM: Write S

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	0	1	0	1	0	0	1	1



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7. Write data to DDRAM: Write A

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	0	1	0	0	0	0	0	1

SA_

⋮

12. Write data to DDRAM: Write G

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	0	1	0	0	0	1	1	1

SAMSUNG_

13. Set DDRAM Address 20H

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	0	0	0	0

SAMSUNG
_

14. Write data to DDRAM: Write K

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	0	1	0	0	1	0	1	1

SAMSUNG
K_

⋮

19. Write data to DDRAM: Write 3

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	0	0	1	1	0	0	1	1

SAMSUNG
KS0073_

20. Set DDRAM Address 40H

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	0	0	0	0	0	0

SAMSUNG
KS0073
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21. Write data to DDRAM: Write L

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	0	1	0	0	1	1	0	0

SAMSUNG
KS0073
L_

30. Write data to DDRAM: Write R

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	0	1	0	1	0	0	1	0

SAMSUNG
KS0073
LCD DRIVER_

31. Set DDRAM Address 60H

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	0	0	0	0	0

SAMSUNG
KS0073
LCD DRIVER
_

43. Write data to DDRAM: Write R

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	0	1	0	1	0	0	1	0

SAMSUNG
KS0073
LCD DRIVER
& CONTROLLER_

44. Function Set: RE(0), DH(1)

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	1	1	0	1	0

SAMSUNG
KS0073
LCD DRIVER
& CONTROLLER_

45. Function Set: RE(1)

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	1	1	1	0	0

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LCD DRIVER
& CONTROLLER_

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46. Shift/Scroll Enable: DS4(1), DS3/2/1(0)

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	1	1	0	0	0

SAMSUNG
KS0073
LCD DRIVER
& CONTROLLER_

47. Function Set; RE(0

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	1	1	0	1	0

SAMSUNG
KS0073
LCD DRIVER
& CONTROLLER_

48. Cursor or Display Shift: Display shift to left

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	1	1	0	X	X

SAMSUNG
KS0073
LCD DRIVER
CONTROLLER_

49. Cursor or Display Shift: Display shift to left

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	1	1	0	X	X

SAMSUNG
KS0073
LCD DRIVER
CONTROLLER_

50. Cursor or Display Shift: Display shift to left

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	1	1	0	X	X

SAMSUNG
KS0073
LCD DRIVER
ONTROLLER_

51. Cursor or Display Shift: Display shift to left

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	1	1	0	X	X

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KS0073
LCD DRIVER
NTROLLER_

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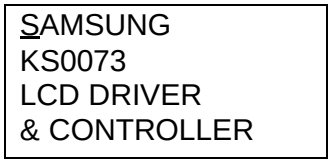
52. Return Home

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	1	X



53. Function Set; RE(0), REV(1)

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	1	1	0	1	1

54. Cursor or Display Shift: Display shift to right

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	1	1	1	X	X

55. Cursor or Display Shift: Display shift to right

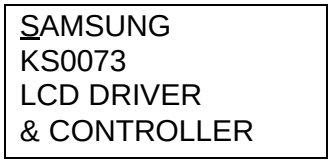
RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	1	1	1	X	X

56. Return Home

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	1	X

57. Function Set: RE(0), REV(0)

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	1	1	0	0	0



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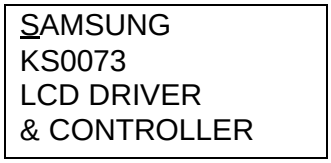
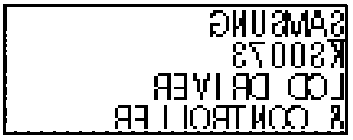
58. Function Set; RE(1

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	1	1	1	0	0



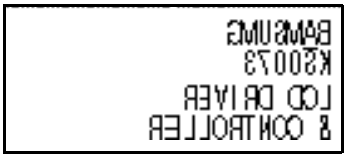
59. Entry Mode Set: BID(1)

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	1	1	1



60. Write Data to DDRAM: Write B

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	0	1	0	0	0	0	1	0



61. Write Data to DDRAM: Write I

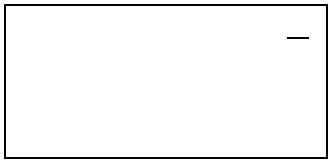
RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	0	1	0	0	1	0	0	1

62. Write Data to DDRAM: Write D

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	0	1	0	0	0	1	0	0

63. Clear Display

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	0	1



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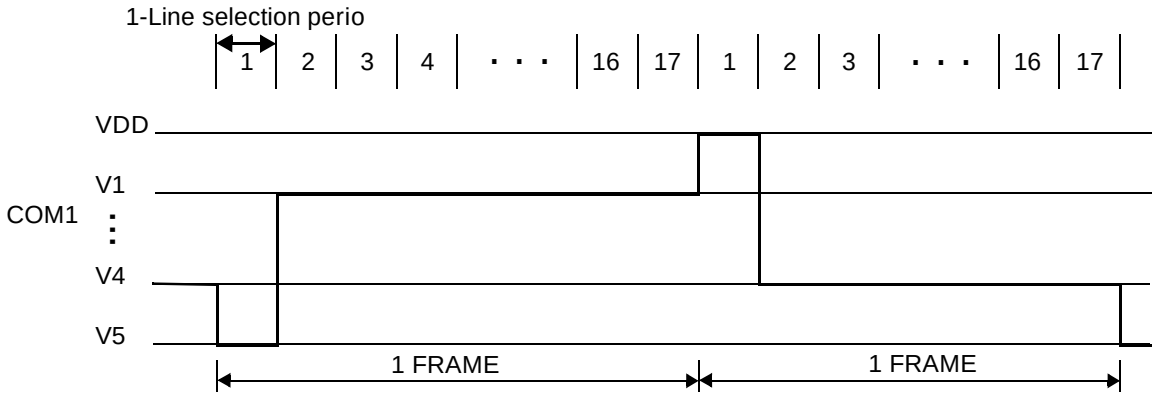
FRAME FREQUENCY

1) 1/17 Duty Cycle



Item	Normal Display Mode (LP=0)	
	5-dot font width	6-dot font widt
1-line selection perio	200 clocks	240 clocks
Frame frequency	79.4 Hz	66.2 Hz

Item	Normal Display Mode (LP=1)	
	5-dot font width	6-dot font widt
1-line selection perio	60 clocks	72 clocks
Frame frequency	66.2 Hz	55.1 Hz

* f_{OSC}=270 kHz (1 clock=3.7 μs)

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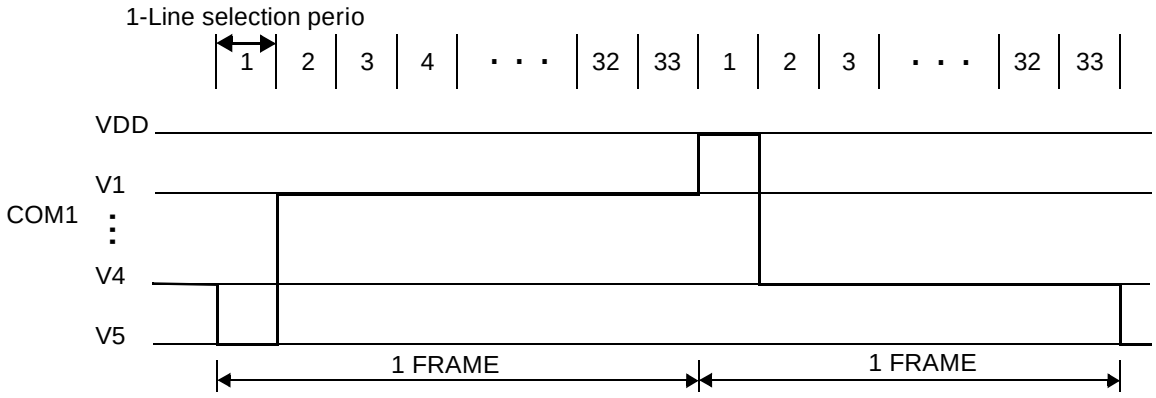
2) 1/33 duty cycle



Item	Normal Display Mode (LP=0)	
	5-dot font width	6-dot font widt
1-line selection perio	100 clocks	120 clocks
Frame frequency	81.8 Hz	68.2 Hz

Item	Normal Display Mode (LP=1)	
	5-dot font width	6-dot font widt
1-line selection perio	60 clocks	72 clocks
Frame frequency	68.2 Hz	56.8 Hz

* f_{OSC}=270 kHz (1 clock=3.7 μs)

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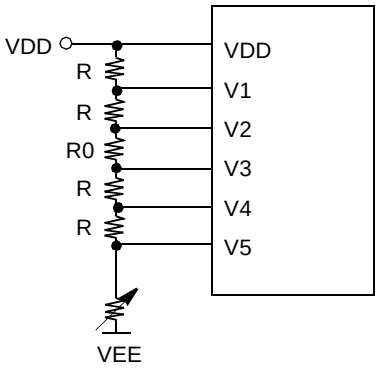
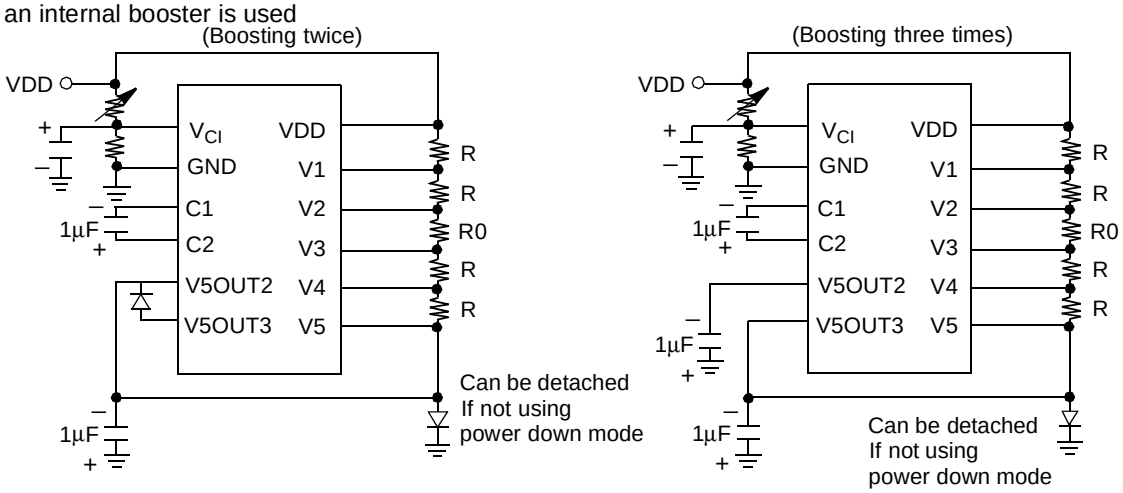
POWER SUPPLY FOR DRIVING LCD PANEL

1) When an external power supply is used



2) When an internal booster is used



* 1. Boosted output voltage should not exceed the maximum value (13 V) of the LCD driving voltage. Especially, a voltage of over 4.3V should not be supplied to the referenc voltage (Vci) when boosting three times.
  2. A voltage of over 5.5V should not be supplied to the reference voltage (Vci) when boosting twice.
  3. The value of resistance, according to the number of lines, duty ratio and the bias, is shown below. (Refer to Table 13)

Table 13. Duty Ratio and Power Supply for LCD Driving

Item		Data	
Number of lines		1	2 or
Duty ratio		1/17	1/33
Bias		1/5	1/6.7
Divided resistance	R	R	R
	R0	R	2.7R

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MAXIMUM ABSOLUTE RATE

Characteristi	Symbol	Value	Unit
Power supply voltage(1)	V_{DD}	-0.3 to +7.0	V
Power supply voltage(2)	V_{LCD}	VDD -15.0 to VDD +0.3	V
Input voltage	V_{IN}	-0.3 to VDD +0.	V
Operating temperature	Topr	-30 to +8	°C
Storage temperatur	Tstg	-55 to +125	°C

* Voltage greater than above may do damage to the circuit (VDD≥V1≥V2≥V3≥V4≥V5)

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ELECTRICAL CHARACTERISTICS

DC Characteristics

(V_{DD} = 2.7 to 5.5V, Ta = -30 to + 85 °C)

Item	Symbol	Condition	Min	Typ	Max	Unit
Operating Voltage	V_{DD}	-	2.7	-	5.5	V
Supply Current	I_{DD}	Internal oscillation or external clock. (V_{DD}=3.0V,fosc = 270kHz)	-	0.15	0.3	mA
Input Voltage (1) (except OSC1)	V_{IH1}	-	$0.7V_{DD}$	-	V_{DD}	V
	V_{IL1}	V_{DD} = 2.7 to 3.0	-0.3	-	$0.2V_{DD}$	
		V_{DD} = 3.0 to 5.5	-0.3	-	0.6	
Input Voltage (2) (OSC1)	V_{IH2}	-	$0.7V_{DD}$	-	V_{DD}	V
	V_{IL2}	-	-	-	$0.2V_{DD}$	
Output Voltage (1) (DB0 to DB7)	V_{OH1}	I_{OH} = -0.1mA	$0.75V_{DD}$	-	-	V
	V_{OL1}	I_{OL} = 0.1mA	-	-	$0.2V_{DD}$	
Output Voltage (2) (except DB0 to DB7)	V_{OH2}	I_O = -40µA	$0.8V_{DD}$	-	-	V
	V_{OL2}	I_O = 40µA	-	-	$0.2V_{DD}$	
Voltage Drop	Vd_{COM}	I_O = ± 0.1mA	-	-	1	V
	Vd_{SEG}		-	-	1	
Input Leakage Current	I_{IL}	V_{IN} = 0V to V_{DD}	-1	-	1	µA
Low Input Current	I_{IN}	V_{IN} = 0V, V_{DD} = 3V (PULL UP)	-10	-50	-120	
Internal Clock (external Rf)	f_{OSC}	Rf = 91kΩ ± 2% (V_{DD} = 5V)	190	270	350	kHz
External Clock	f_{EC}	-	125	270	410	kHz
	duty		45	50	55	%
	t_R, t_F		-	-	0.2	µs

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(DC Characteristics: continued)

Item	Symbol	Condition		Min	Type	Max	Unit
Voltage Converter Out2 (Vci = 4.5V)	V_{OUT2}	Ta = 25 °C, C = μF, I_{OUT} = 0.25 mA, fosc = 270kHz		-3.0	-4.2	-	V
Voltage Converter Out3 (Vci = 2.7V)	V_{OUT3}			-4.3	-5.1	-	
Voltage Converter Input	V_{ci}	-		1.0	-	4.5	V
LCD Driving Voltage	V_{LCD}	V_{DD}-V5	1/5 Bias	3.0	-	13.0	
			1/6.7 Bias	3.0	-	13.0	

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AC Characteristics

(V_{DD} = 4.5 to 5.5V, Ta = -30 to + 8 °C)

Mode	Item	Symbol	Min	Typ	Max	Unit
(1) Write Mode (Refer to Fig-21)	E Cycle Tim	tc	500	-	-	ns
	E Rise / Fall Time	tr,tf	-	-	20	
	E Pulse Width (High, Low)	tw	230	-	-	
	R/W and RS Setup Time	tsu1	40	-	-	
	R/W and RS Hold Time	th1	10	-	-	
	Data Setup Time	tsu2	60	-	-	
	Data Hold Time	th2	10	-	-	
(2) Read Mode (Refer to Fig-22)	E Cycle Tim	tc	500	-	-	ns
	E Rise / Fall Time	tr,tf	-	-	20	
	E Pulse Width (High, Low)	tw	230	-	-	
	R/W and RS Setup Time	tsu	40	-	-	
	R/W and RS Hold Time	th	10	-	-	
	Data Output Delay Tim	t_D	-	-	160	
	Data Hold Time	t_{DH}	5	-	-	
(3) Serial Interface Mod (Refer to Fig-23)	Serial Clock Cycle Time	tc	0.5	-	20	µs
	Serial Clock Rise/Fall Time	tr,tf	-	-	50	ns
	Serial Clock Width (High, Low)	tw	200	-	-	
	Chip Select Setup Time	tsu1	60	-	-	
	Chip Select Hold Time	th1	20	-	-	
	Serial Input Data Setup Tim	tsu2	100	-	-	
	Serial Input Data Hold Time	th2	100	-	-	
	Serial Output Data Delay Time	t_D	-	-	160	
	Serial Output Data Hold Time	t_{DH}	5	-	-	

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(AC Characteristics: continued) (V_{DD} = 2.7 to 4.5V, Ta = -30 to + 8 °C)

Mode	Item	Symbol	Min	Type	Max	Unit
(4) Write Mode (Refer to Fig-21)	E Cycle Tim	tc	100	-	-	ns
	E Rise / Fall Time	tr,tf	-	-	25	
	E Pulse Width (High, Low)	tw	450	-	-	
	R/W and RS Setup Time	tsu1	60	-	-	
	R/W and RS Hold Time	th1	20	-	-	
	Data Setup Time	tsu2	195	-	-	
	Data Hold Time	th2	10	-	-	
(5) Read Mode (Refer to Fig-22)	E Cycle Tim	tc	100	-	-	ns
	E Rise / Fall Time	tr,tf	-	-	25	
	E Pulse Width (High, Low)	tw	450	-	-	
	R/W and RS Setup Time	tsu	60	-	-	
	R/W and RS Hold Time	th	20	-	-	
	Data Output Delay Tim	t_D	-	-	360	
	Data Hold Time	t_{DH}	5	-	-	
(6) Serial Interface Mod (Refer to Fig-23)	Serial Clock Cycle Time	tc	1	-	20	µs
	Serial Clock Rise/Fall Time	tr,tf	-	-	50	ns
	Serial Clock Width (High, Low)	tw	400	-	-	
	Chip Select Setup Time	tsu1	60	-	-	
	Chip Select Hold Time	th1	20	-	-	
	Serial Input Data Setup Tim	tsu2	200	-	-	
	Serial Input Data Hold Time	th2	200	-	-	
	Serial Output Data Delay Time	t_D	-	-	360	
	Serial Output Data Hold Time	t_{DH}	5	-	-	

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(AC Characteristics: continued) (V_{DD} = 2.7 to 5.5 V, Ta = -30 to + 85°C)

Mode	Item	Symbol	Min	Typ	Max	Unit
(7) Interface Mode with Extension Driver (Refer to Fig-24)	Clock Pulse Width (High, Low)	tw	800	-	-	ns
	Clock Rise / Fall Time	tr,tf	-	-	100	
	Clock Setup Tim	tsu1	500	-	-	
	Data Setup Time	tsu2	300	-	-	
	Data Hold Time	t_{DH}	300	-	-	
	M Delay Time	t_{DM}	-1000	-	1000	

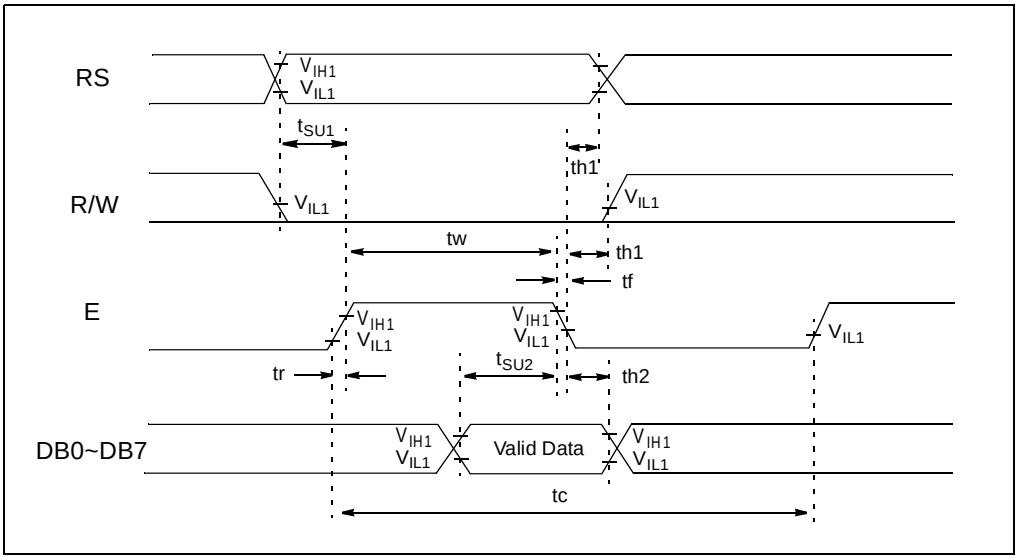

Fig-21. Write Mode

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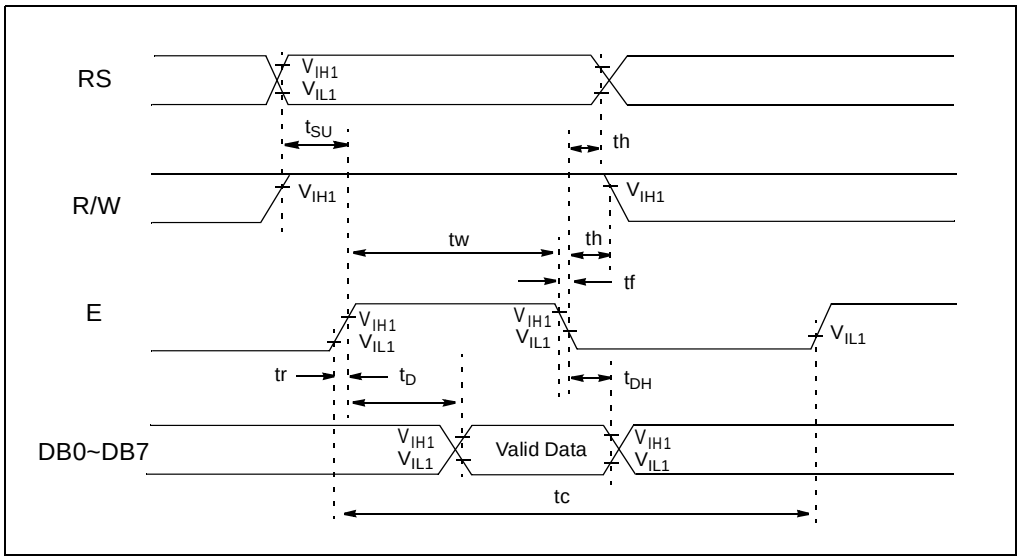

Fig-22. Read Mod

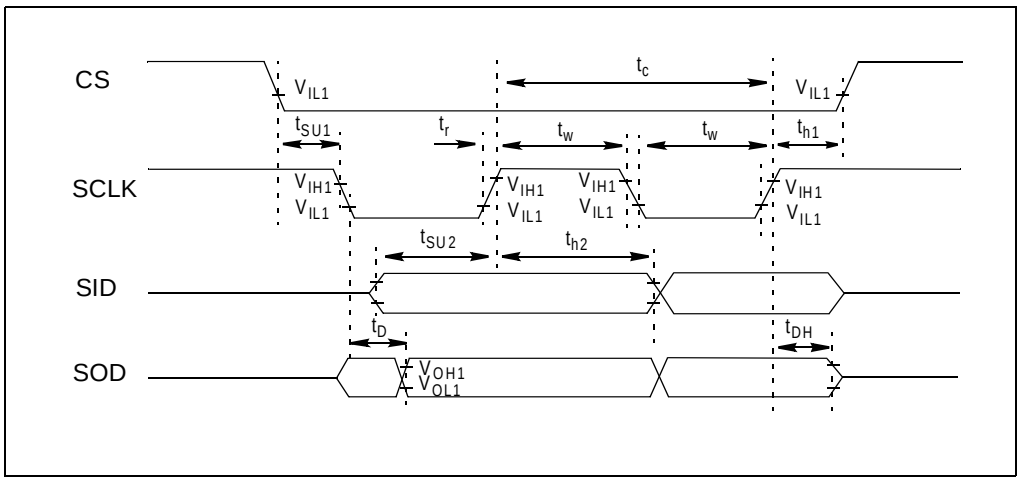

Fig-23. Serial Interface Mode

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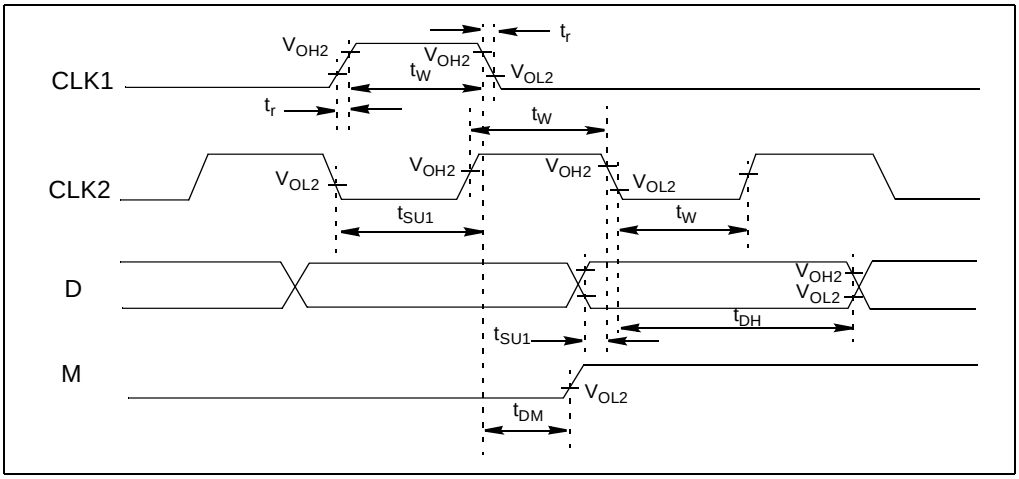

Fig-24. Interface Mode with Extensive Driver

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RESET TIMIN

(VDD=2.7V to 5.5V, Ta=-30°C to + 85°C)

Item	Symbol	Min	Typ	Max	Unit
Reset Low level width (Refer to Fig-25)	t_{RES}	10	–	–	ms

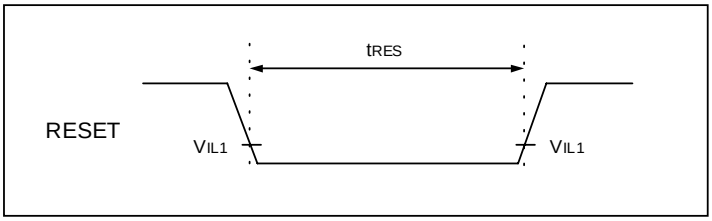

Fig-25. Reset TimingDiagram

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