The TMP68HC11A1T-3/TMP68HC11A0T-3 microcontroller (MCU) device is a high speed version of the TMP68HC11A1/A0 MCU device.

The entire data sheet of the TMP68HC11A8 MCU applies to the TMP68HC11A1T-3/TMP68HC11A0T-3 MCU with the exceptions provided in this appendix.

1. ELECTRICAL SPECIFICATIONS

1.1 MAXIMUM RATINGS

Raing	Symbol	Value	Unit
Supply Voltage	V_{DD}	− 0.3 to + 7.0	V
Input Voltage	V_{in}	− 0.3 to + 7.0	V
Operating Temperature Range TMP68HC11A0/A1x-3	T_A	T_L to T_H 0 to 70	℃
Storage Temperature Range	T_{stg}	− 55 to 150	℃
Current Drain per Pin* Excluding V_{DD}, V_{SS}, V_{RH}, and V_{RL}	I_D	25	mA

* One pin at a time, observing maximum power dissipation limits.

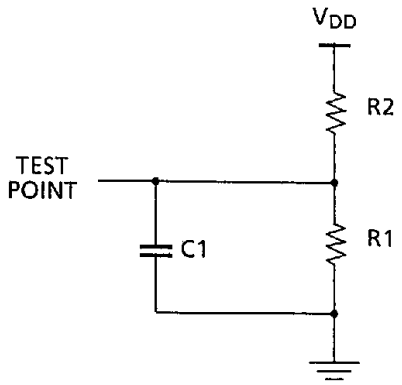
This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields;however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (e.g., either GND or V_{DD}).

1.2 DC ELECTRICAL CHARACTERISTICS (V_{DD}=5.0 Vdc±10%,V_{SS}=0 Vdc,T_A=T_L to T_H, unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
Output Voltage I_{Load} = ± 10.0μA (see Note 1)	All Outputs All Outputs Except $\overline{RESET}$ and MODA	VOL VOH	– V_{DD} – 0.1	0.1 –	V
Output High Voltage I_{Load} = -0.8mA, VDD = 4.5V (see Note 1)	All Outputs Except RESET, XTAL, and MODA	V_{OH}	V_{DD} – 0.8	–	V
Output Low Voltage I_{Load} = 1.6mA	All Outputs Except XTAL	V_{OL}	–	0.4	V
Input High Voltage	All Inputs Except $\overline{RESET}$ $\overline{RESET}$	V_{IH}	0.7 × V_{DD} 0.8 × V_{DD}	V_{DD} V_{DD}	V
Input Low Voltage	All Inputs	V_{IL}	V_{SS}	0.2 × V_{DD}	V
I/O Ports, Three-State Leakage V_{in} = V_{IH} or V_{IL}	PA7, PC0-PC7, PD0-PD5, AS/STRA, MODA LIR, RESET	I_{OZ}	–	± 10	μA
Input Current (see Note 2) V_{in} = V_{DD} or V_{SS} V_{in} = V_{DD} or V_{SS}	 PA0-PA2,$\overline{IRQ}$ $\overline{XIRQ}$ MODB/V_{STBY}	I_{in}	 – –	 ± 1 ± 10	μA
RAM Standby Voltage	Powerdown	V_{SB}	3.8	V_{DD}	V
RAM Standby Current	Powerdown	I_{SB}	–	20	μA
Total Supply Current(see Note 3) RUN: Single Chip Expanded Multiplexed WAIT: All Peripheral Functions Shut Down Single-Chip Mode Expanded Multiplexed Mode STOP: No Clocks, Single-Chip Mode		 I_{DD} W_{IDD} S_{IDD}	 – – – – –	 27 35 15 20 150	 mA mA mA mA μA
Input Capacitance	PA0-PA2, PE0-PE7, $\overline{IRQ}$, $\overline{XIRQ}$, EXTAL PA7, PC0-PC7, PD0-PD5, AS/STRA, MODA/$\overline{LIR}$, $\overline{RESET}$	C_{in}	– –	8 12	pF
Power Dissipation	Single Chip Mode Expanded Multiplexed Mode	P_D	– –	150 195	mW

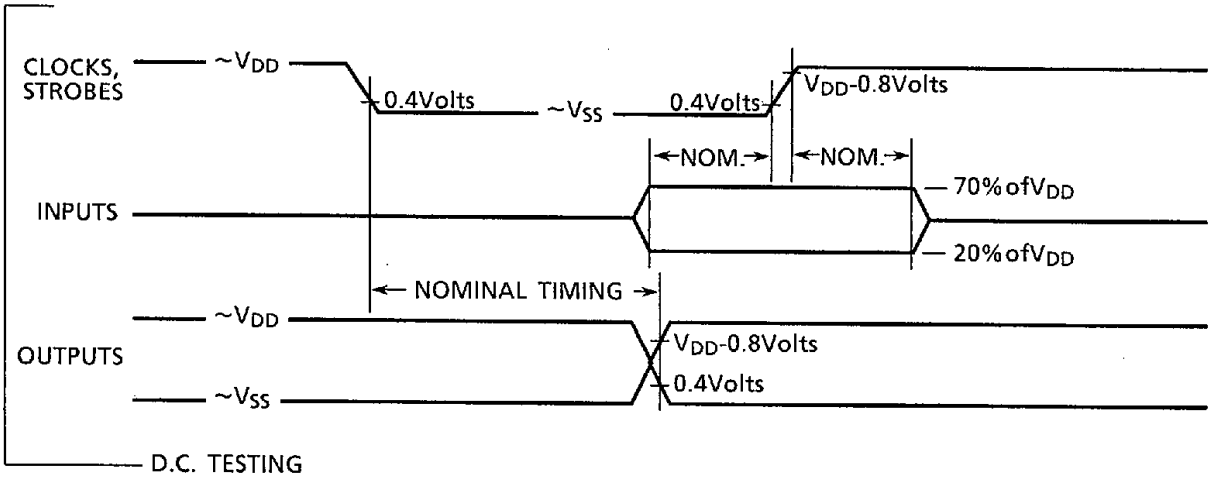
Notes :

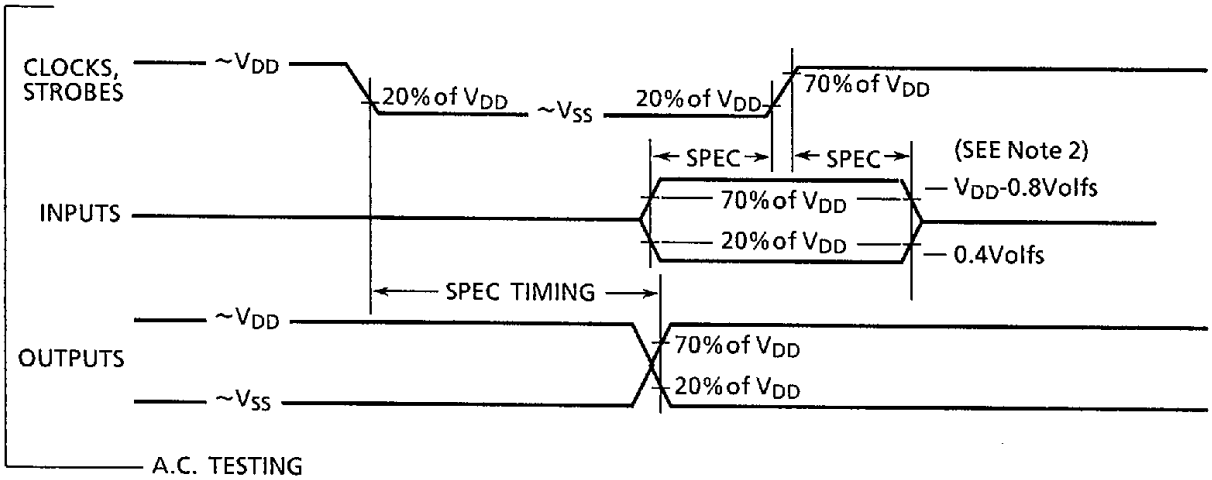
1. V_{OH} specification for $\overline{RESET}$ and MODA is not applicable because they are open-drain pins. V_{OH} specification not applicable to ports C and D in wire-OR mode.
2. See A/D specification for leakage current for port E.
3. All ports configured as inputs, $V_{IH} \geqq V_{DD} - 0.2$ V, $V_{IL} \leqq 0.2$V, No dc loads, EXTAL is driven with a square wave, and t_{cyc}=333 ns.



Equivalent Test Load (SEE Note 1)

Pins	R1	R2	C
PA3-PA7 PB0-PB7 PC0-PC7 PD0, PD5 E, AS; R/W	3.26kΩ	2.38kΩ	90pF
PD1-PD4	3.26kΩ	2.38kΩ	200pF





Notes:
1. Full test loads are applied during all dc electrical and ac timing measurements.
2. During ac timing measurements, inputs are driven to 0.4 volts and V_{DD}-0.8 volts while timing measurements are taken at the 20% and 70% of V_{DD} points.

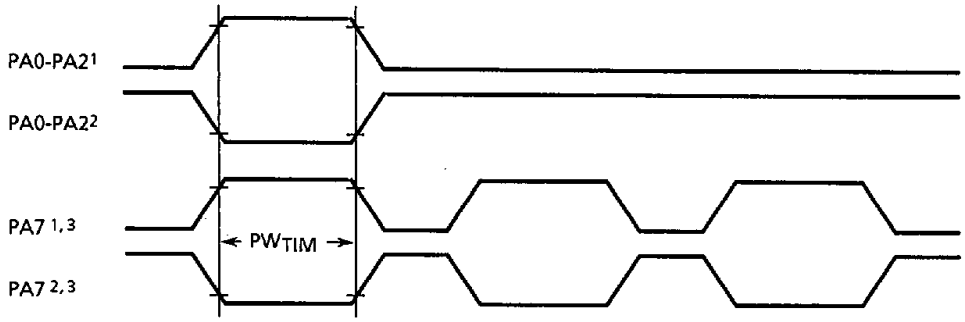
Figure 1.1 Test Methods

1.3 CONTROL TIMING (V_{DD} = 5.0 Vdc ± 10%, V_{SS} = 0 Vdc, $T_A = T_L$ to T_H)

Characteristic	Symbol	3.0MHz Min	3.0MHz Max	Unit
Frequency of Operation	f_O	dc	3.0	MHz
E Clock Period	t_{cyc}	333	–	ns
Crystal Frequency	f_{XTAL}	–	12.0	MHz
External Oscillator Frequency	$4f_O$	dc	12.0	MHz
Processor Control Setup Time (see Figures 1.3, 1.5, and 1.6)	t_{PCS}	30	–	ns
Reset Input Pulse Width (see Note 1 and Figure 1.3) (To Guarantee External Reset Vector)	PW_{RSTL}	8	–	t_{cyc}
(Minimum Input Time; May be Preempted by Internal Reset)		1	–	
Mode Programming Setup Time (see Figure 1.3)	t_{MPS}	2	–	t_{cyc}
Mode Programming Hold Time (see Figure 1.3)	t_{MPH}	10	–	ns
Interrupt Pulse Width, IRQ Edge Sensitive Mode (see Figures 1.4 and 1.6)	PW_{IRQ}	340	–	ns
Wait Recovery Startup Time (See Figure 1.5)	t_{WRS}	–	4	t_{cyc}
Timer Pulse Width Input Capture, Pulse Accumulator Input (see Figure 1.2)	PW_{TIM}	340	–	ns

Note : 1. $\overline{RESET}$ will be recognized during the first clock cycle it is held low. Internal circuity then drives the pin low for four clock cycles, releases the pin, and samples the pin level two cycles later to detemine the source of the interrupt.

2. All timing is shown with respect to 20% V_{DD} and 70% V_{DD} unless otherwise noted.



Notes :
1. Rising edge sensitive input
2. Falling edge sensitive input
3. Maximum pulse accumulator clocking rate is E frequency divided by 2.

Figure 1.2 Timer Inputs Timing Diagram

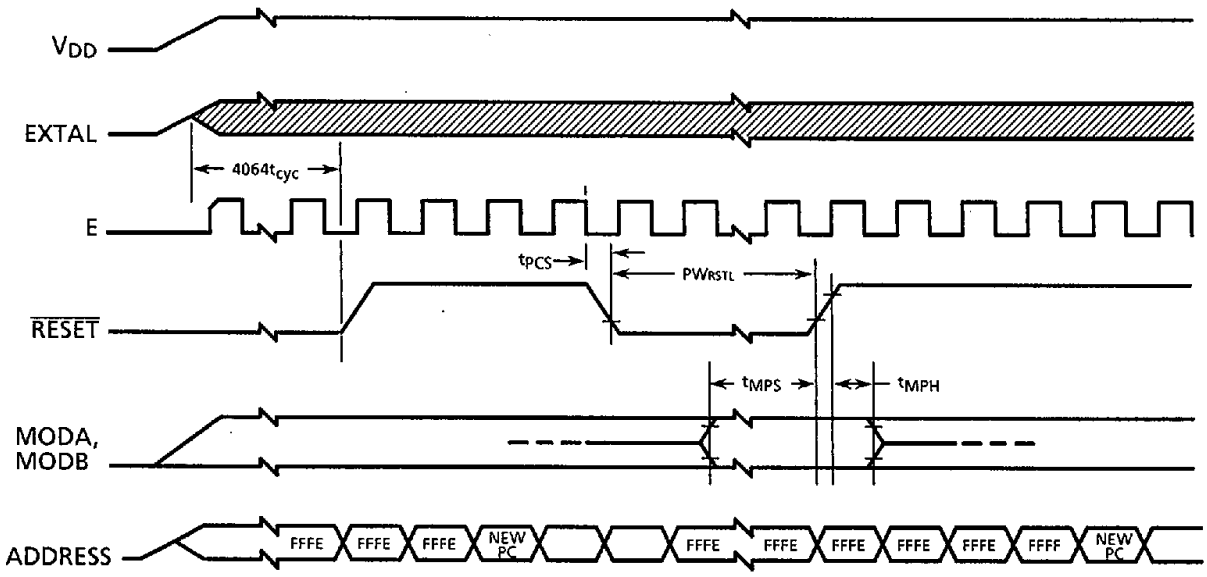
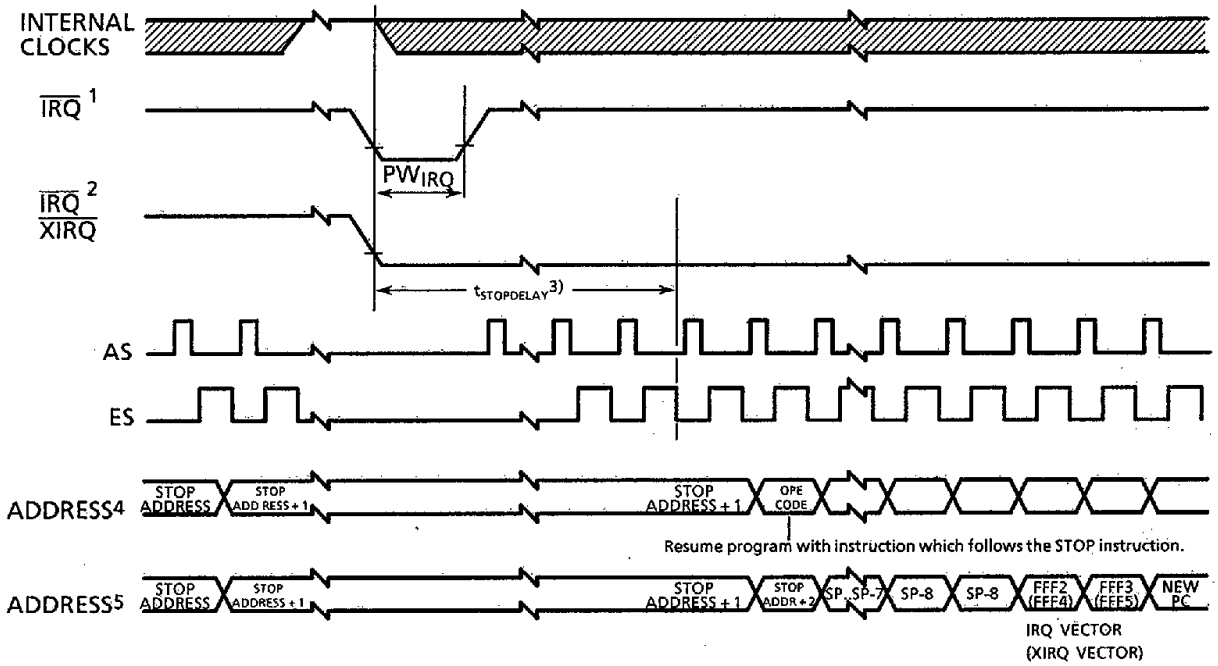
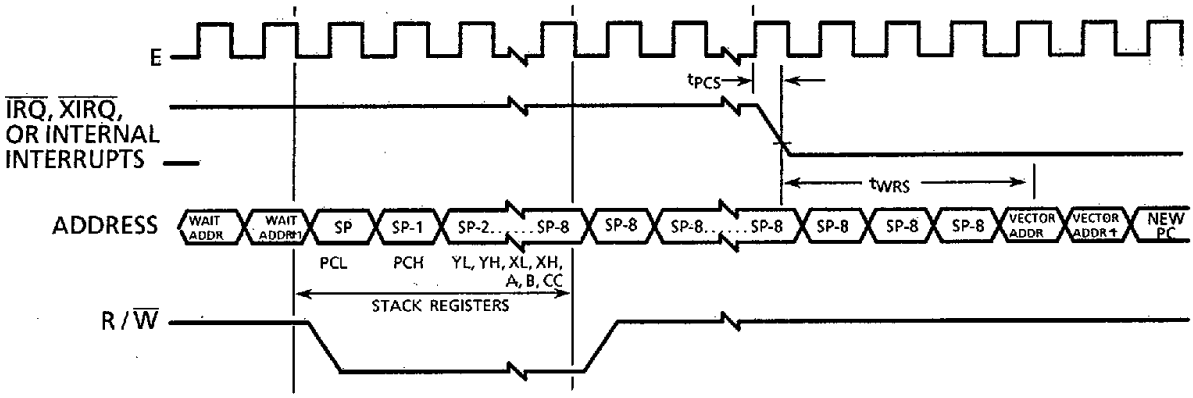


Figure 1.3 POR and External Reset Timing Diagram



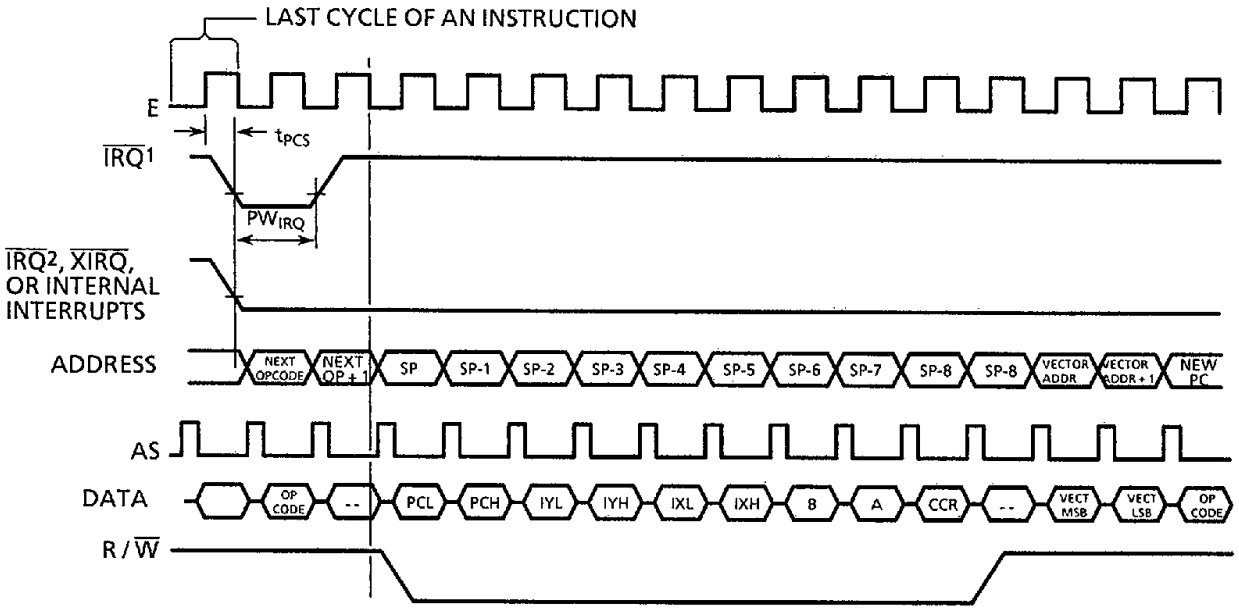
Notes :
1. Edge sensitive $\overline{IRQ}$ pin (IRQE bit = 1)
2. Level sensitive $\overline{IRQ}$ pin (IRQE bit = 0)
3. $t_{STOPDELAY} = 4064t_{cyc}$ if DLY bit = 1 or $4t_{cyc}$ if DLY = 0.
4. $\overline{XIRQ}$ with X bit CCR = 1 .
5. IRQ, or ($\overline{XIRQ}$ with X bit in CCR = 0) .

Figure 1.4 STOP Recovery Diagram



Notes :
$\overline{RESET}$ will also cause recovery from WAIT.

Figure 1.5 WAIT Recovery from Interrupt Timing Diagram



Notes :
1. Edge sensitive $\overline{IRQ}$ pin (IRQE bit = 1).
2. Level sensitive $\overline{IRQ}$ pin (IRQE bit = 0).

Figure 1.6 Interrupt Timing Diagram

1.4 PERIPHERAL PORT TIMING (V_{DD} = 5.0 Vdc ± 10%, V_{SS} = 0 Vdc, T_A = T_L to T_H)

Characteristic	Symbol	3.0MHz		Unit
		Min	Max	
E Clock Period	t_{cyc}	333	–	ns
Peripheral Data Setup Time (MCU Read of Ports A,C,D, and E) (see Figure 1.8)	t_{PDSU}	100	–	ns
Peripheral Data Hole Time (MCU Read of Ports A,C,D, and E) (see Figure 1.8)	t_{PDH}	50	–	ns
Delay Time, Peripheral Data Write (see Figures 1.7,1.9,1.12, and 1.13)	t_{PWD}			ns
MCU Write to Port A		–	200	
MCU Writes to Ports B,C, and D		–	185	
Input Data Setup Time(Port C) (see Figure 1.10 and 1.11)	t_{IS}	60	–	ns
Input Data Hold Time(Port C) (see Figure 1.10 and 1.11)	t_{IH}	100	–	ns
Delay Time, E Fall to STRB (see Figures 1.9,1.11,1.12,and 1.13)	t_{DEB}	–	180	ns
Setup Time, STRA Asserted to E Fall (see Note 1) (see Figures 1.11,1.12,and 1.13)	t_{AES}	0	–	ns
Delay Time, STRA Asserted to Port C Data Output Valid (see Figure 1.13)	t_{PCD}	–	100	ns
Hold Time, STRA Negated to Port C Data (see Figure 1.13)	t_{PCH}	10	–	ns
Three-State Hold Time (see Figure 1.13)	t_{PCZ}	–	150	ns

Notes :

1. If this setup time is met, STRB will acknowledge in the next cycle. If it is not met, the response may be delayed one more cycle.
2. Port C and D timing is valid for active drive (CWOM and DWOM bits not set in PIOC and SPCR registers respectively).
3. All timing is shown with respect to 20% V_{DD} and 70% V_{DD} unless otherwise noted.

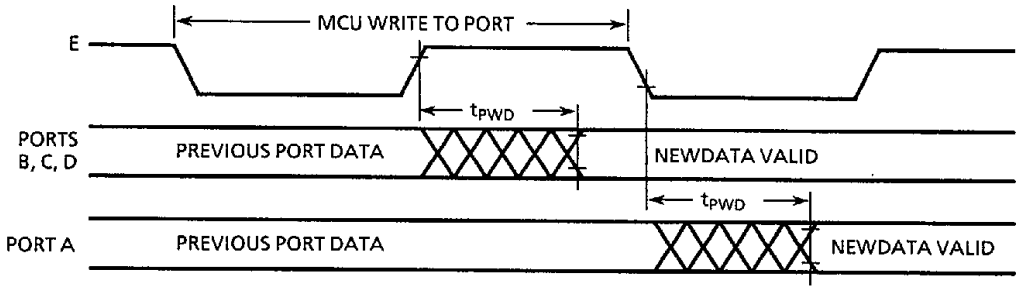
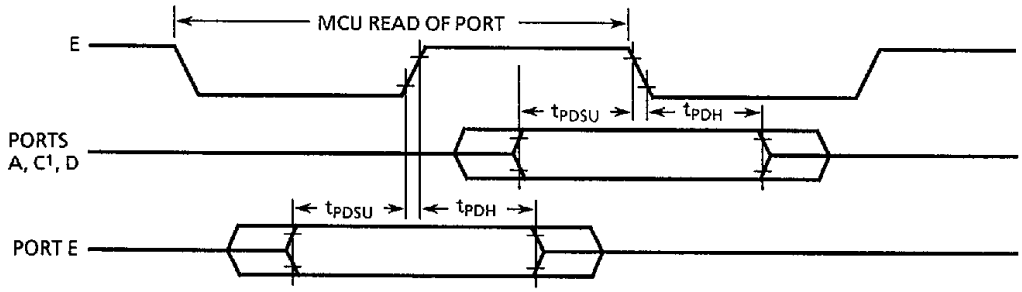


Figure 1.7 Port Write Timing Diagram



Note1 : For non-latched operation of Port C.

Figure 1.8 Port Read Timing Diagram

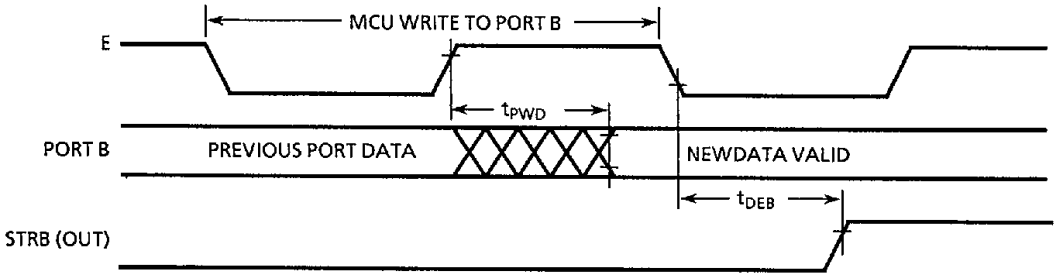


Figure 1.9 Simple Output Strobe Timing Diagram

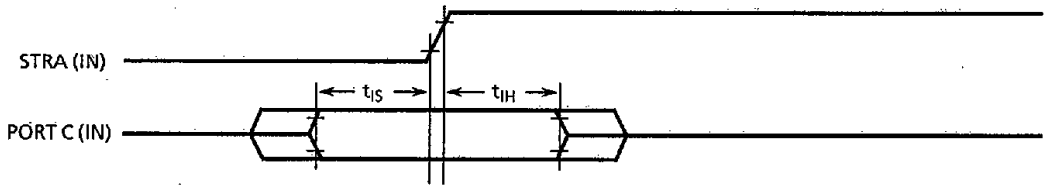
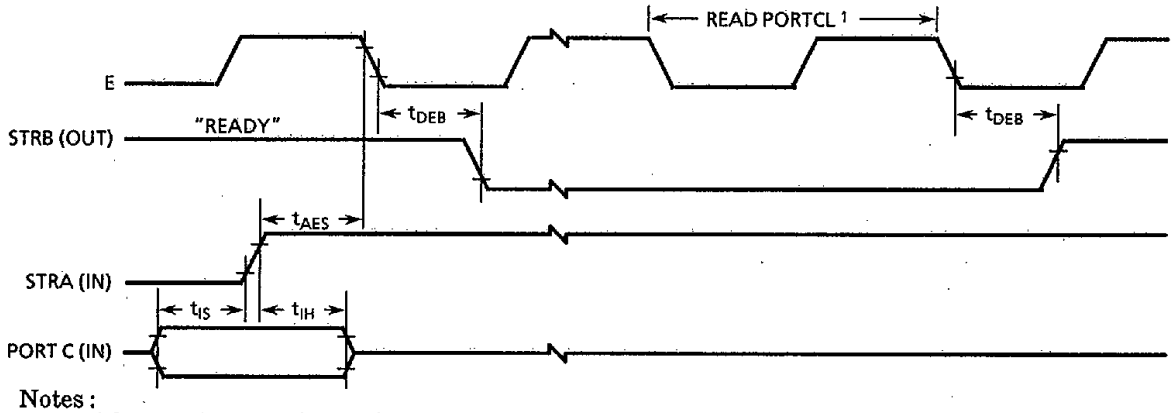
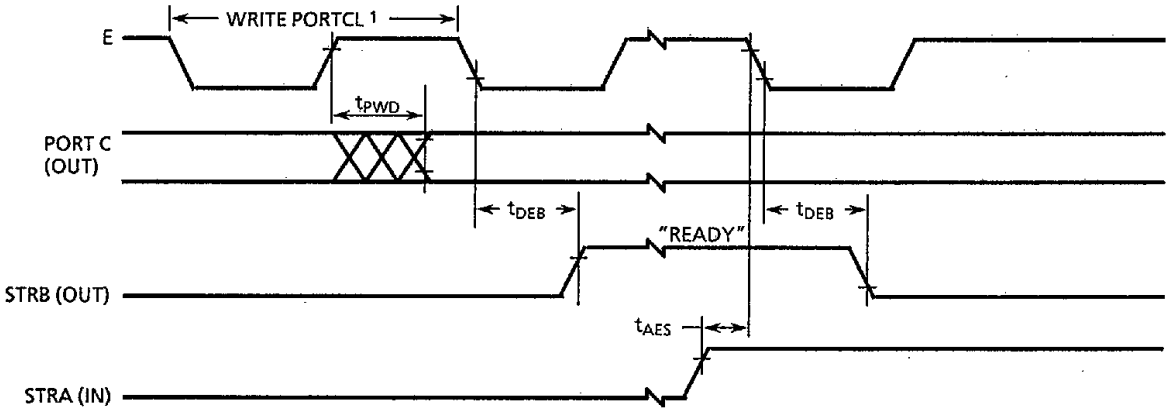


Figure 1.10 Simple Input Strobe Timing Diagram



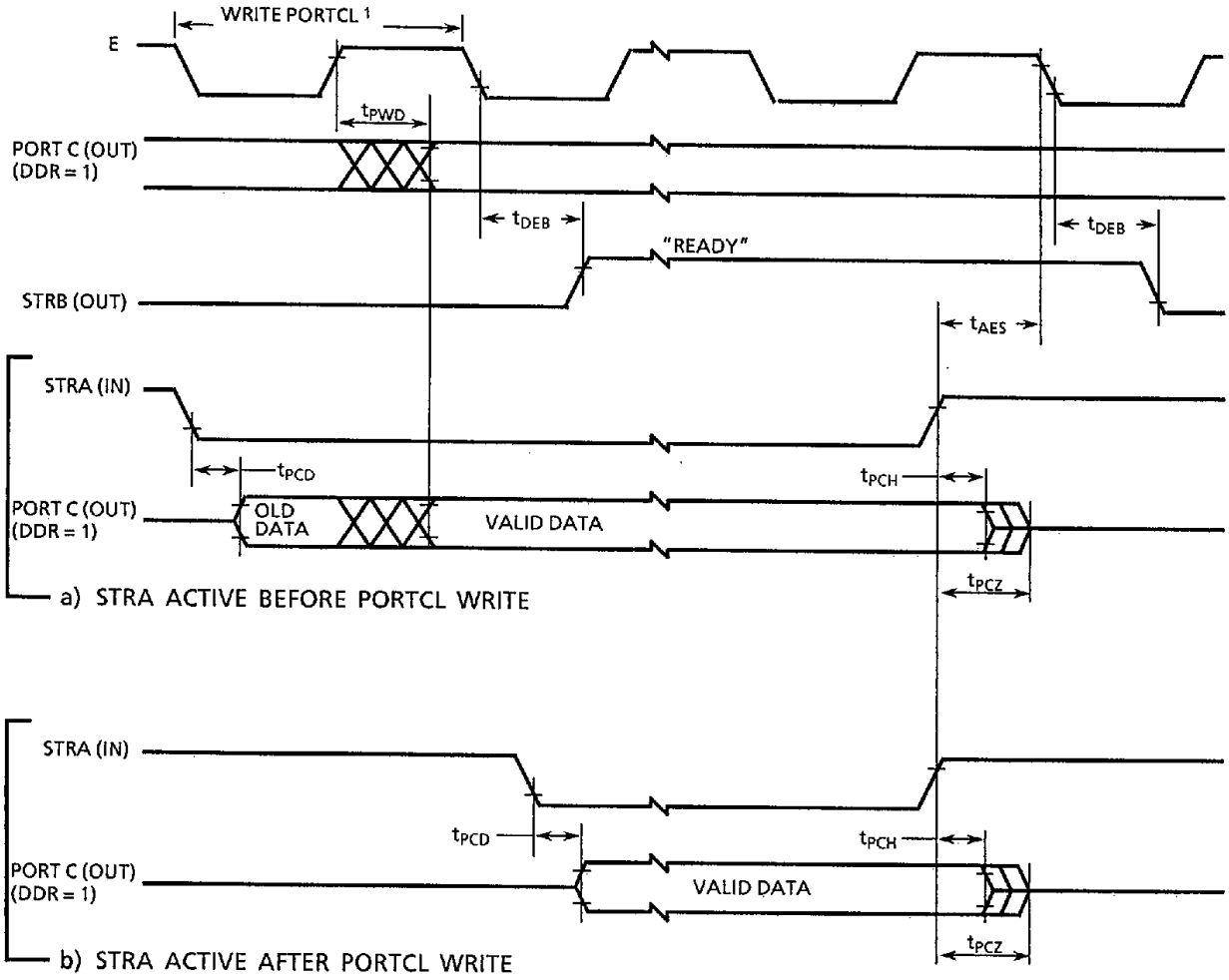
Notes :
1. After reading PIOC with STAF set.
2. Figure shows rising edge STRA (EGA = 1) and high true STRB (INVB = 1)

Figure 1.11 Port C Input Handshake Timing Diagram



Notes :
1. After reading PIOC with STAF set.
2. Figure shows rising edge STRA (EGA = 1) and high true STRB (INVB = 1)

Figure 1.12 Port C Output Handshake Timing Diagram



Notes :
1. After reading PIOC with STAF set.
2. Figure shows rising edge STRA (EGA = 1) and high true STRB (INVB = 1)

Figure 1.13 Three-State Variation of Output Handshake Timing Diagram (STRA Enables Output Buffer)

1.5 A/D CONVERTER CHARACTERISTICS(VDD=5.0 Vdc±10%, VSS=0Vdc, $T_A=T_L$ to T_H, 750kHz ≦ E ≦ 3.0MHz, unless otherwise noted)

Characteristic	Parameter	Min	Absolute	Max	Unit
Resolution	Number of Bits Resolved by the A/D	8	–	–	Bits
Non-Linearity	Maximum Deviation from the Ideal and an Actual A/D Transfer Characteristics	–	–	±1	LSB
Zero Error	Difference Between the Output of an Ideal and an Actual A/D for Zero Input Voltage	–	–	±1	LSB
Full Scale Error	Difference Between the Output of an Ideal A/D for Full-Scale Input Voltage	–	–	±1	LSB
Total Unadjusted Error	Maximum Sum of Non-Linearity, Zero Error, and Full-Scale Error	–	–	±1.5	LSB
Quantization Error	Uncertainty Due to Converter Resolution	–	–	±1/2	LSB
Absolute Accuracy	Difference Between the Actual Input Voltage and the Full-Scale Weighted Equivalent of the Binary Output Code, All Error Sources Included	–	–	±2	LSB
Conversion Range	Analog Input Voltage Range	V_{RL}	–	V_{RH}	V
V_{RH}	Maximum Analog Reference Voltage (see Note 2)	V_{RL}	–	$V_{DD}+0.1$	V
V_{RL}	Maximum Analog Reference Voltage (see Note 2)	$V_{SS}-0.1$	–	V_{RH}	V
ΔV_R	Maximum Difference between V_{RH} and V_{RL} (see Note 2)	3	–	–	V
Conversion Time	Total Time to Perform a Single Analog-to-Digital Conversion: a. E Clock b. Internal RC Oscillator	 – –	 32 –	 – tcyc + 32	 tcyc μs
Monotonicity	Conversion Result Never Decreases with an Increase in Input Voltage and has no Missing Codes		Guaranteed		
Zero Input Reading	Conversion Result when $V_{in}=V_{RL}$	00	–	–	Hex
Full Scale Reading	Conversion Result when $V_{in}=V_{RH}$	–	–	FF	Hex
Sample Acquisition Time	Analog Input Acquisition Sampling Time: a. E Clock b. Internal RC Oscillator	 – –	 12 –	 – 12	 tcyc μs
Sample/Hold Capacitance	Input Capacitance during Sample PE0-PE7	–	20 (Typ)	–	pF
Input Leakage	Input Leakage on A/D Pins PE0-PE7 V_{RL}, V_{RH}	– –	– –	400 1.0	nA μA

Notes :

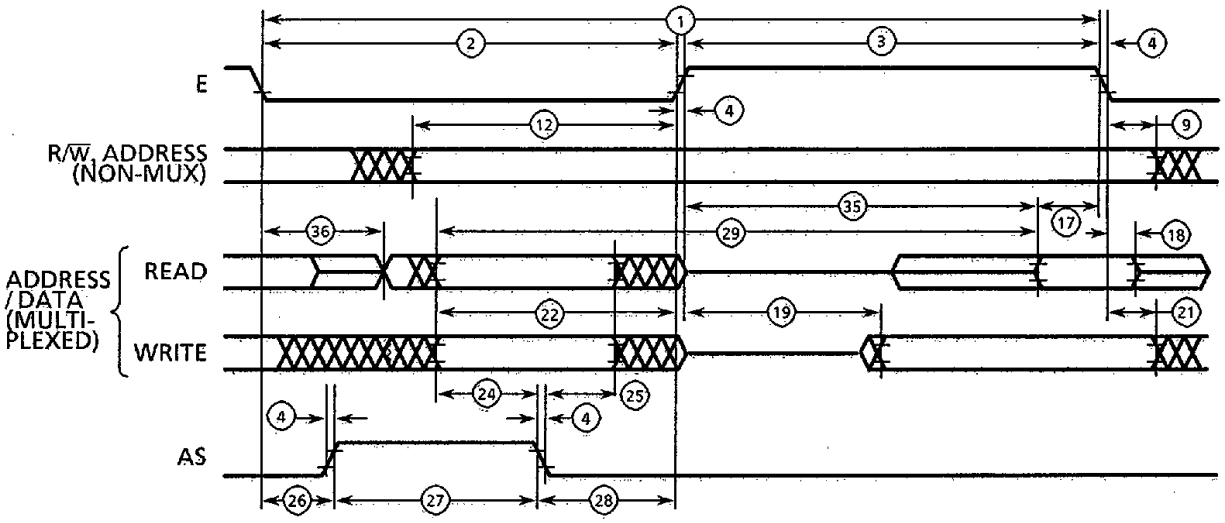
1. Source impedances greater than 10KΩ will adversely affect accuracy, due mainly to input leakage.
2. Performance verified down to 2.5V ΔV_R, but accuracy is tested and guaranteed at $\Delta V_R=5V\pm10\%$

1.6 EXPANSION BUS TIMING (V_{DD}=5.0 Vdc±10%,V_{SS}=0 Vdc,T_A=T_L to T_H, see Figure 1.14)

Num	Characteristic	Symbol	3.0MHz		Unit
			Min	Max	
1	Cycle Time	t_{cyc}	333	–	ns
2	Pulse Width, E Low	PW_{EL}	140	–	ns
3	Pulse Width, E High	PW_{EL}	135	–	ns
4	E and AS Rise and Fall Time	t_r, t_f	–	20	ns
9	Address Hold Time	t_{AH}	20	–	ns
12	Non-Muxed Address Valid Time to E Rise	t_{AV}	30	–	ns
17	Read Data Setup Time	t_{DSR}	30	–	ns
18	Read Data Hold Time	t_{DHR}	5	60	ns
19	Write Data Delay Time	t_{DDW}	–	80	ns
21	Write Data Hold Time	t_{DHW}	20	–	ns
22	Muxed Address Valid Time to E Rise	t_{AVM}	35	–	ns
24	Muxed Address Valid Time to As Fall	t_{ASL}	10	–	ns
25	Muxed Address Hold Time	t_{AHL}	20	–	ns
26	Delay Time,E to AS Rise	t_{ASD}	30	–	ns
27	Pulse Width, AS High	P_{WASH}	60	–	ns
28	Delay Time, AS to E Rise	t_{ASED}	30	–	ns
29	MPU Address Access Time	t_{ACCA}	160	–	ns
35	MPU Access Time	t_{ACCE}	–	110	ns
36	Muxed Address Delay (Previous Cycle MPU Read)	t_{MAD}	60	–	ns

Notes :

1. Input clocks with duty cycles other than 50% will affect bus performance. Timing parameters affected by input clock duty cycle are identified by (a) and (b). To recalculate the approximate bus timing values, substitute the follwing expressions in place of 1/8 t_{cyc} in the formulas where applicable:
   (a) (1-DC)×1/4tcyc
   (b) DC×1/4tcyc
   Where :
   DC is the decimal value of duty cycle percentage (high time)
2. All timing is shown with respect to 20% V_{DD} and 70% V_{DD} unless othewise noted.



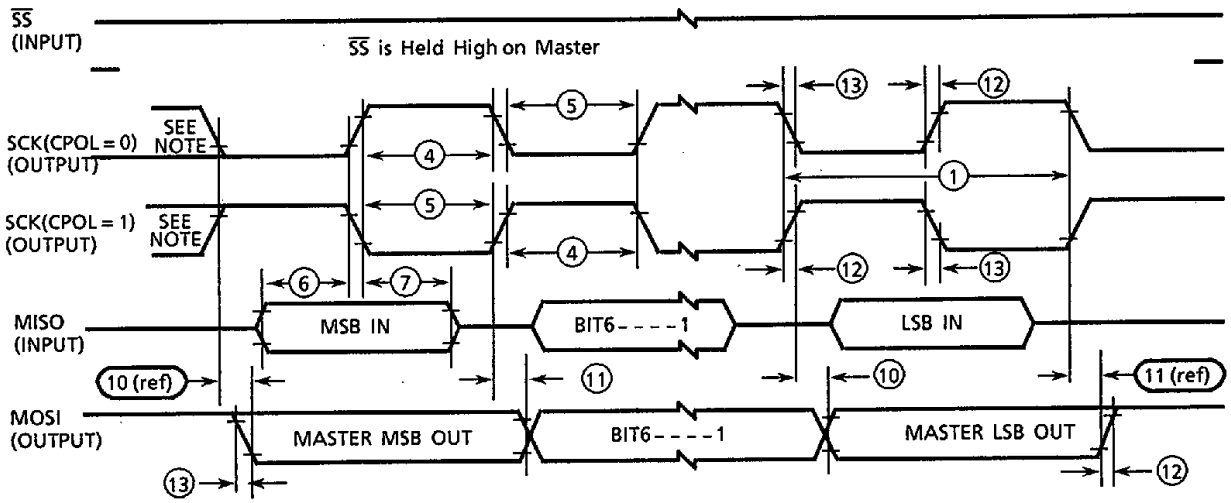
Note : Measurement point shown are 20% and 70% V_{DD}.

Figure 1.14 Expansion Bus Timing Diagram

1.7 SERIAL PERIPHERAL INTERFACE (SPI) TIMING(V_{DD}=5.0 Vdc±10%, V_{SS}=0 Vdc, T_A=T_L to T_H, see Figure 1.15)

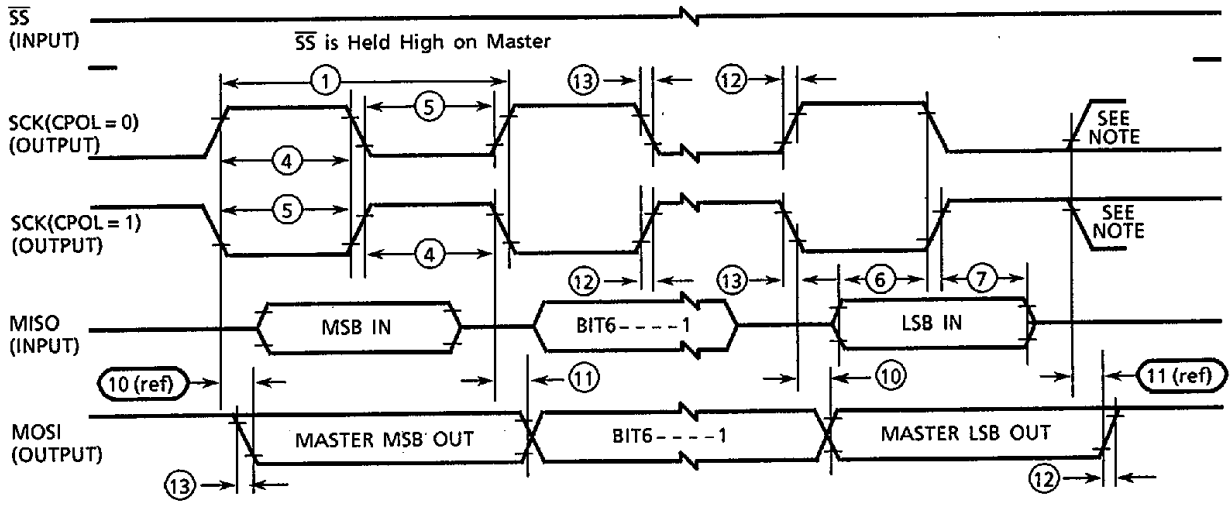
Num.	Characteristic	Symbol	Min	Max	Unit
	Operating Frequency Master Slave	 f_{OP} (m) f_{OP} (S)	 dc dc	 1.5 3.0	 MHz MHz
1	Cycle Time Master Slave	 f_{cyc} (m) f_{cyc} (S)	 2.0 334	 – –	 t_{cyc} ns
2	Enable Lead Time Master Slave	 t_{lead} (m) t_{lead} (S)	 * 240	 – –	 ns ns
3	Enable Lag Time Master Slave	 t_{lag} (m) t_{lag} (S)	 * 240	 – –	 ns ns
4	Clock (SCK) High Time Master Slave	 t_w (SCKH) $_m$ t_w (SCKH) $_s$	 227 127	 – –	 ns ns
5	Clock (SCK) Low Time Master Slave	 t_w (SCKL) $_m$ t_w (SCKL) $_s$	 227 127	 – –	 ns ns
6	Data Setup Time (Inputs) Master Slave	 t_{su} (m) t_{su} (s)	 100 100	 – –	 ns ns
7	Data Hold Time (Inputs) Master Slave	 t_h (m) t_h (s)	 100 100	 – –	 ns ns
8	Access Time (Time to Data Active from High-Impedance State) Slave	 t_a	 0	 120	 ns
9	Disable Time (Hold Time to High-Impedance State) Slave	 t_{dis}	 –	 167	 ns
10	Data Valid (After Enable Edge)**	t_v (S)	–	167	ns
11	Data Hold Time (Outputs) (After Enable Edge)	t_{ho}	0	–	ns
12	Rise Time (20% V_{DD} to 70% V_{DD}, C_L = 200pF) SPI Outputs(SCK, MOSI, and MISO) SPI Inputs (SCK, MOSI, MISO, and $\overline{SS}$)	 t_{rm} t_{rs}	 – –	 100 2.0	 ns μs
13	Fall Time (70% V_{DD} to 20% V_{DD}, C_L = 200pF) SPI outputs(SCK, MOSI, and MISO) SPI Inputs(SCK, MOSI, MISO, and $\overline{SS}$)	 t_{fm} t_{fs}	 – –	 100 2.0	 ns μs

* Signal production depends on software.
** Assumes 200 pF load on all SPI pins.
Note : All timing is shown with respect to 20% V_{DD} and 70% V_{DD}, unless otherwise noted.



Note : This first clock edge is generated internally but is not seen at the SCK pin.

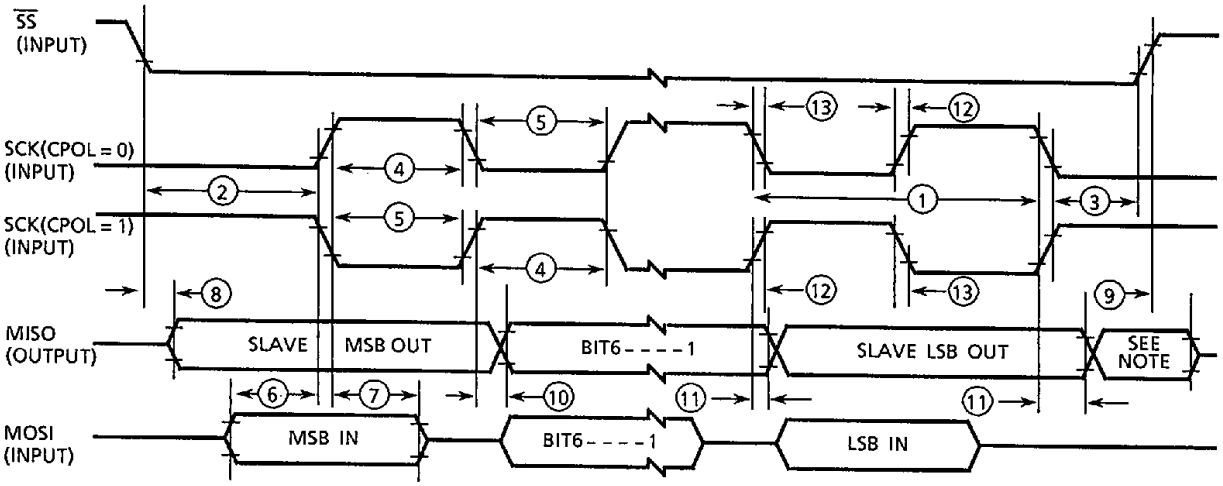
a) SPI MASTER TIMING (CPHA = 0)



Note : This last clock edge is generated internally but is not seen at the SCK pin.

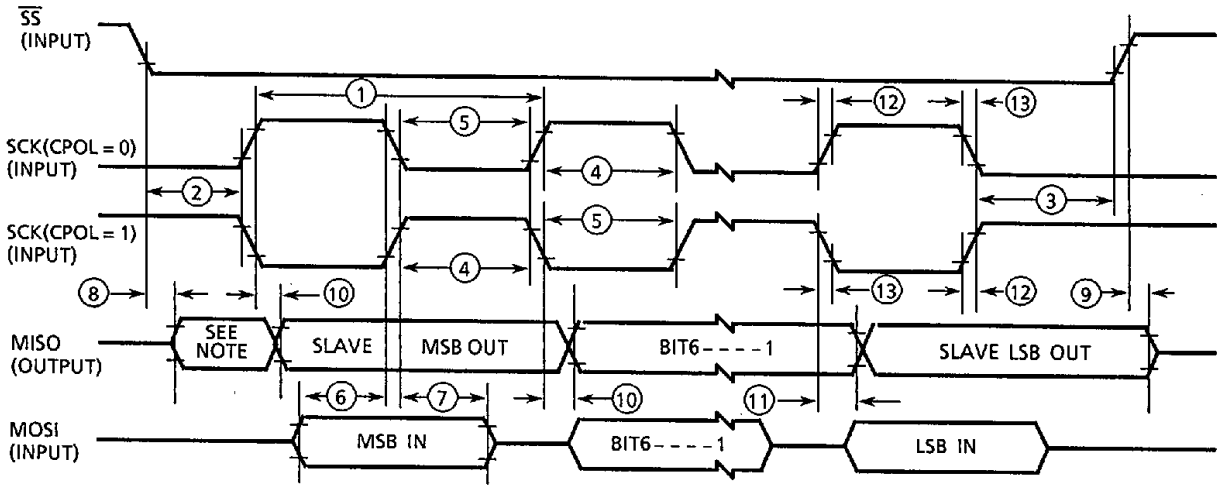
b) SPI MASTER TIMING (CPHA = 1)

Figure 1.15 SPI Timing Diagrams (Sheet 1 of 2)



Note : Not defined but normally MSB of character just received.

c) SPI SLAVE TIMING (CPHA = 0)



Note : Not defined but normally LSB of character previously transmitted.

d) SPI SLAVE TIMING (CPHA = 1)

Figure 1.15 SPI Timing Diagrams (Sheet 2 of 2)

1.8 EEPROM CHARACTERISTICS (V_{DD} = 5.0 Vdc ± 10%, V_{SS} = 0 Vdc, T_A = T_L to T_H)

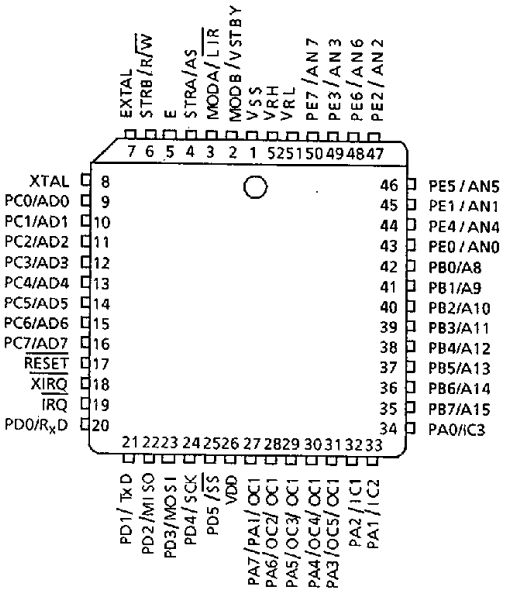
Characteristic	Temperature Range 0 to 70°C	Unit
Programming time (See Note 1) Under 1.0 MHz with RC Oscillator Enable 1.0 to 2.0 MHz with RC Oscillator Disabled 2.0 MHz (or Anytime RC Oscillator Enabled)	 10 20 10	ms
Erase Time (see Note 1) Byte, Row, and Bulk	10	ms
Write Erase Endurance	10, 000	Cycles
Data Retention	10	Years

Notes :

1. The RC oscillator must be enabled (by setting the CSEL bit in the OPTION register) for EEPROM programming and erasure when the E-clock frequency is below 1.0MHz.

2. PIN ASSIGNMENT

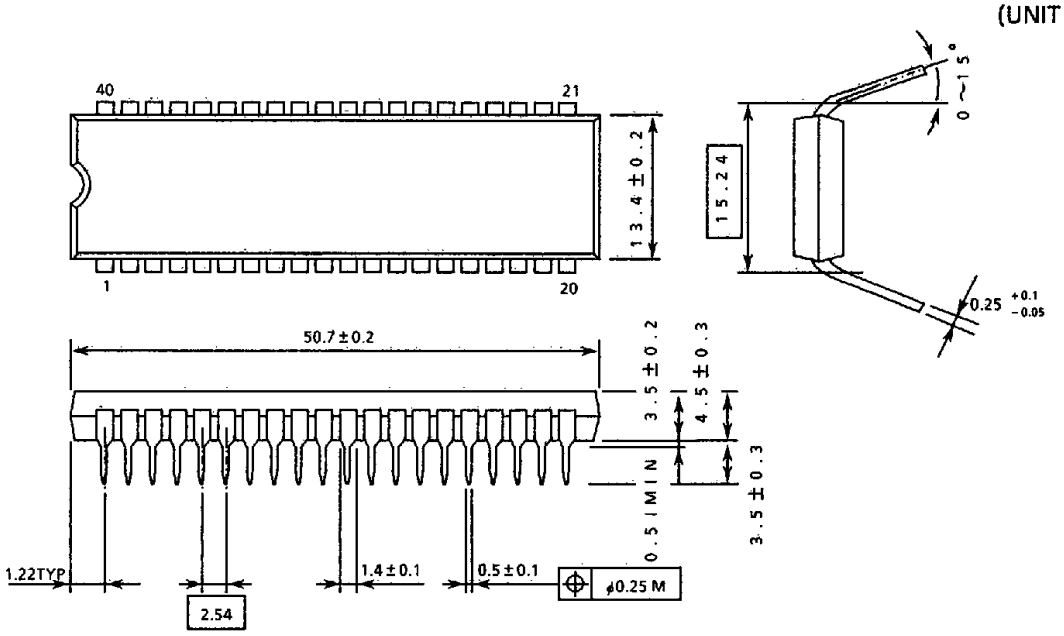
T SUFFIX
52 PIN PLCC



DIP40-P-600

P SUFFIX : 40PIN DIP (Dual Inline Package)

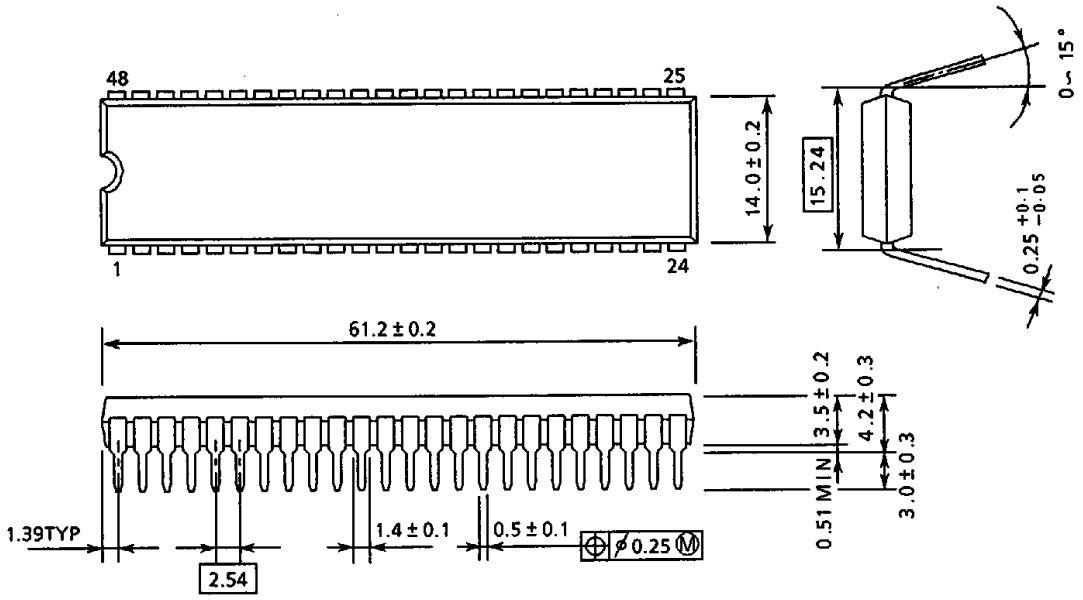
(UNIT : mm)



DIP48-P-600

(UNIT : mm)

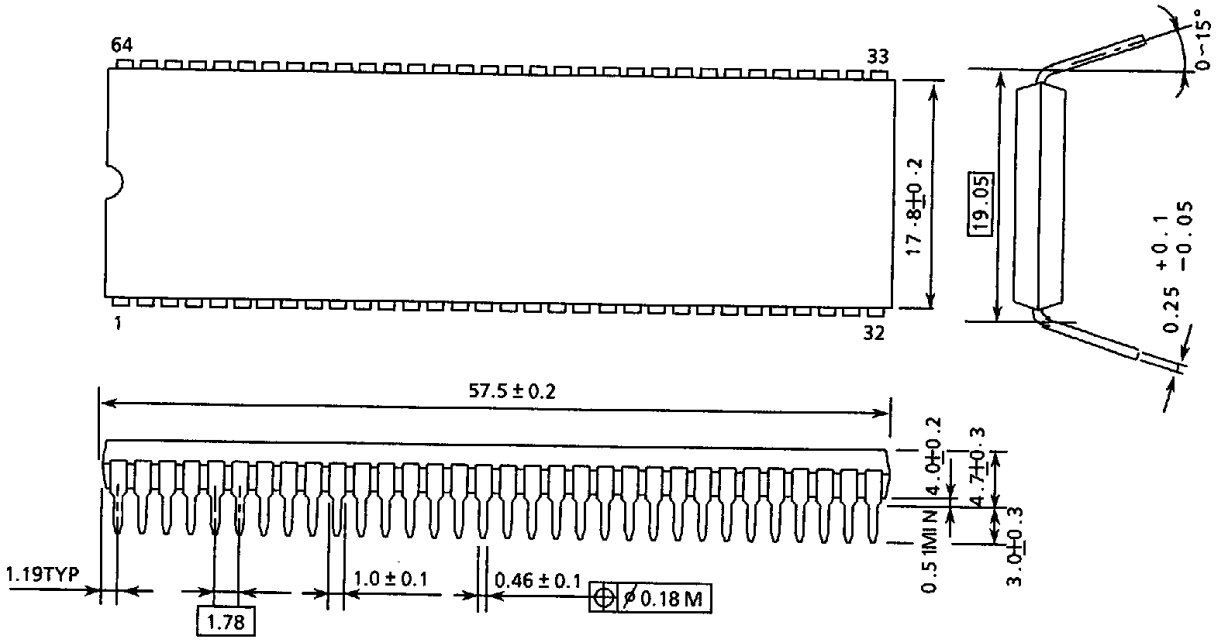
P SUFFIX : 48PIN DIP (Dual Inline Package)



SDIP64-P-750

N SUFFIX : 64PIN SDIP (Shrink Dual Inline Package)

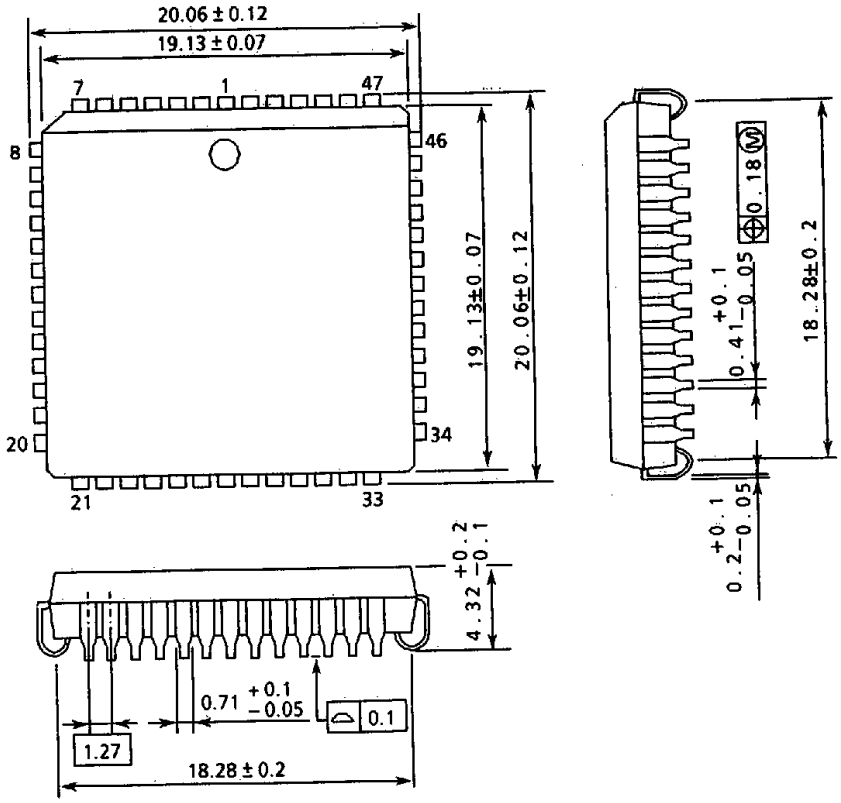
(UNIT : mm)



QFJ52-P-S750

T SUFFIX : 52PIN QFJ (Quad Flat J-leaded Package) (PLCC)

(UNIT : mm)



F SUFFIX 64 PIN QFP (Quad Flat Package) (UNIT : mm)