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PRODUCT OVERVIEW

INTRODUCTION

This manual describes SAMSUNG's S3C2410A 16/32-bit RISC microprocessor. This product is designed to provide hand-held devices and general applications with cost-effective, low-power, and high-performance microcontroller solution in small die size. To reduce total system cost, the S3C2410A includes the following components separate 16KB Instruction and 16KB Data Cache, MMU to handle virtual memory management, LCD Controller (STN & TFT), NAND Flash Boot Loader, System Manager (chip select logic and SDRAM Controller), 3-ch UART, 4-ch DMA, 4-ch Timers with PWM, I/O Ports, RTC, 8-ch 10-bit ADC and Touch Screen Interface, IIC-BUS Interface, IIS-BUS Interface, USB Host, USB Device, SD Host & Multi-Media Card Interface, 2-ch SPI and PLL for clock generation.

The S3C2410A was developed using an ARM920T core, 0.18um CMOS standard cells and a memory compier. Its low-power, simple, elegant and fully static design is particularly suitable for cost- and power-sensitive applications. It adopts a new bus architecture called Advanced Microcontroller Bus Architecture (AMBA).

The S3C2410A offers outstanding features with its CPU core, a 16/32-bit ARM920T RISC processor designed by Advanced RISC Machines, Ltd. The ARM920T implements MMU, AMBA BUS, and Harvard cache architecture with separate 16KB instruction and 16KB data caches, each with an 8-word line length.

By providing a complete set of common system peripherals, the S3C2410A minimizes overall system costs and eliminates the need to configure additional components. The integrated on-chip functions that are described in this document include:

- 1.8V/2.0V int., 3.3V memory, 3.3V external I/O microprocessor with 16KB I-Cache/16KB D-Cache/MMU
- External memory controller (SDRAM Control and Chip Select logic)
- LCD controller (up to 4K color STN and 256K color TFT) with 1-ch LCD-dedicated DMA
- 4-ch DMAs with external request pins
- 3-ch UART (IrDA1.0, 16-Byte Tx FIFO, and 16-Byte Rx FIFO) / 2-ch SPI
- 1-ch multi-master IIC-BUS/1-ch IIS-BUS controller
- SD Host interface version 1.0 & Multi-Media Card Protocol version 2.11 compatible
- 2-port USB Host /1- port USB Device (ver 1.1)
- 4-ch PWM timers & 1-ch internal timer
- Watch Dog Timer
- 117-bit general purpose I/O ports / 24-ch external interrupt source
- Power control: Normal, Slow, Idle and Power-off mode
- 8-ch 10-bit ADC and Touch screen interface
- RTC with calendar function
- On-chip clock generator with PLL

FEATURES

Architecture

- Integrated system for hand-held devices and general embedded applications
- 16/32-Bit RISC architecture and powerful instruction set with ARM920T CPU core
- Enhanced ARM architecture MMU to support WinCE, EPOC 32 and Linux
- Instruction cache, data cache, write buffer and Physical address TAG RAM to reduce the effect of main memory bandwidth and latency on performance
- ARM920T CPU core supports the ARM debug architecture.
- Internal Advanced Microcontroller Bus Architecture (AMBA) (AMBA2.0, AHB/APB)

System Manager

- Little/Big Endian support
- Address space: 128M bytes for each bank (total 1G bytes)
- Supports programmable 8/16/32-bit data bus width for each bank
- Fixed bank start address from bank 0 to bank 6
- Programmable bank start address and bank size for bank 7
- Eight memory banks:
 - Six memory banks for ROM, SRAM, and others.
 - Two memory banks for ROM/SRAM/ Synchronous DRAM
- Fully Programmable access cycles for all memory banks
- Supports external wait signals to expend the bus cycle
- Supports self-refresh mode in SDRAM for power-down
- Supports various types of ROM for booting (NOR/NAND Flash, EEPROM, and others)

NAND Flash Boot Loader

- Supports booting from NAND flash memory
- 4KB internal buffer for booting
- Supports storage memory for NAND flash memory after booting

Cache Memory

- 64-way set-associative cache with I-Cache (16KB) and D-Cache (16KB)
- 8words length per line with one valid bit and two dirty bits per line
- Pseudo random or round robin replacement algorithm
- Write-through or write-back cache operation to update the main memory
- The write buffer can hold 16 words of data and four addresses.

Clock & Power Manager

- On-chip MPLL and UPLL:
UPLL generates the clock to operate USB Host/Device.
MPLL generates the clock to operate MCU at maximum 266MHz @ 2.0V.
- Clock can be fed selectively to each function block by software.
- Power mode: Normal, Slow, Idle, and Power-off mode
Normal mode: Normal operating mode
Slow mode: Low frequency clock without PLL
Idle mode: The clock for only CPU is stopped.
Power-off mode: The Core power including all peripherals is shut down.
- Woken up by EINT[15:0] or RTC alarm interrupt from Power-Off mode

FEATURES (Continued)

Interrupt Controller

- 55 Interrupt sources (One Watch dog timer, 5 timers, 9 UARTs, 24 external interrupts, 4 DMA, 2 RTC, 2 ADC, 1 IIC, 2 SPI, 1 SDI, 2 USB, 1 LCD, and 1 Battery Fault)
- Level/Edge mode on external interrupt source
- Programmable polarity of edge and level
- Supports Fast Interrupt request (FIQ) for very urgent interrupt request

Timer with Pulse Width Modulation (PWM)

- 4-ch 16-bit Timer with PWM / 1-ch 16-bit internal timer with DMA-based or interrupt-based operation
- Programmable duty cycle, frequency, and polarity
- Dead-zone generation
- Supports external clock sources

RTC (Real Time Clock)

- Full clock feature: second, minute, hour, date, day, month, and year
- 32.768 KHz operation
- Alarm interrupt
- Time tick interrupt

General Purpose Input/Output Ports

- 24 external interrupt ports
- multiplexed input/output ports

UART

- 3-channel UART with DMA-based or interrupt-based operation
- Supports 5-bit, 6-bit, 7-bit, or 8-bit serial data transmit/receive (Tx/Rx)
- Supports external clocks for the UART operation (UEXTCLK)
- Programmable baud rate
- Supports IrDA 1.0
- Loopback mode for testing
- Each channel has internal 16-byte Tx FIFO and 16-byte Rx FIFO.

DMA Controller

- 4-ch DMA controller
- Supports memory to memory, IO to memory, memory to IO, and IO to IO transfers
- Burst transfer mode to enhance the transfer rate

A/D Converter & Touch Screen Interface

- 8-ch multiplexed ADC
- Max. 500KSPS and 10-bit Resolution

LCD Controller STN LCD Displays Feature

- Supports 3 types of STN LCD panels: 4-bit dual scan, 4-bit single scan, 8-bit single scan display type
- Supports monochrome mode, 4 gray levels, 16 gray levels, 256 colors and 4096 colors for STN LCD
- Supports multiple screen size
- Typical actual screen size: 640x480, 320x240, 160x160, and others
- Maximum virtual screen size is 4 Mbytes.
- Maximum virtual screen size in 256 color mode: 4096x1024, 2048x2048, 1024x4096, and others

TFT(Thin Film Transistor) Color Displays Feature

- Supports 1, 2, 4 or 8 bpp (bit-per-pixel) palette color displays for color TFT
- Supports 16 bpp non-palette true-color displays for color TFT
- Supports maximum 16M color TFT at 24 bpp mode
- Supports multiple screen size
- Typical actual screen size: 640x480, 320x240, 160x160, and others
- Maximum virtual screen size is 4Mbytes.
- Maximum virtual screen size in 64K color mode: 2048x1024, and others



FEATURES (Continued)**Watchdog Timer**

- 16-bit Watchdog Timer
- Interrupt request or system reset at time-out

IIC-Bus Interface

- 1-ch Multi-Master IIC-Bus
- Serial, 8-bit oriented and bi-directional data transfers can be made at up to 100 Kbit/s in Standard mode or up to 400 Kbit/s in Fast mode.

IIS-Bus Interface

- 1-ch IIS-bus for audio interface with DMA-based operation
- Serial, 8-/16-bit per channel data transfers
- 128 Bytes (64-Byte + 64-Byte) FIFO for Tx/Rx
- Supports IIS format and MSB-justified data format

USB Host

- 2-port USB Host
- Complies with OHCI Rev. 1.0
- Compatible with USB Specification version 1.1

USB Device

- 1-port USB Device
- 5 Endpoints for USB Device
- Compatible with USB Specification version 1.1

SD Host Interface

- Compatible with SD Memory Card Protocol version 1.0
- Compatible with SDIO Card Protocol version 1.0
- Bytes FIFO for Tx/Rx
- DMA based or Interrupt based operation
- Compatible with Multimedia Card Protocol version 2.11

SPI Interface

- Compatible with 2-ch Serial Peripheral Interface Protocol version 2.11
- 2x8 bits Shift register for Tx/Rx
- DMA-based or interrupt-based operation

Operating Voltage Range

- Core: 1.8V for 200MHz (S3C2410A-20)
2.0V for 266MHz (S3C2410A-26)
- Memory & IO: 3.3V

Operating Frequency

- Up to 266MHz

Package

- 272-FBGA