Product Technical Brief
S3C2443
Rev 2.1, June 2006

Overview

S3C2443X is a derivative product of Samsung's S3C24XXX family of microprocessors for mobile communication market. The S3C2443X's main enhancement over the baseline product, S3C2440A, is the integration of USB Device 2.0 and CFII+ Interface library to provide high speed connectivity and increase the system expendability respectively.

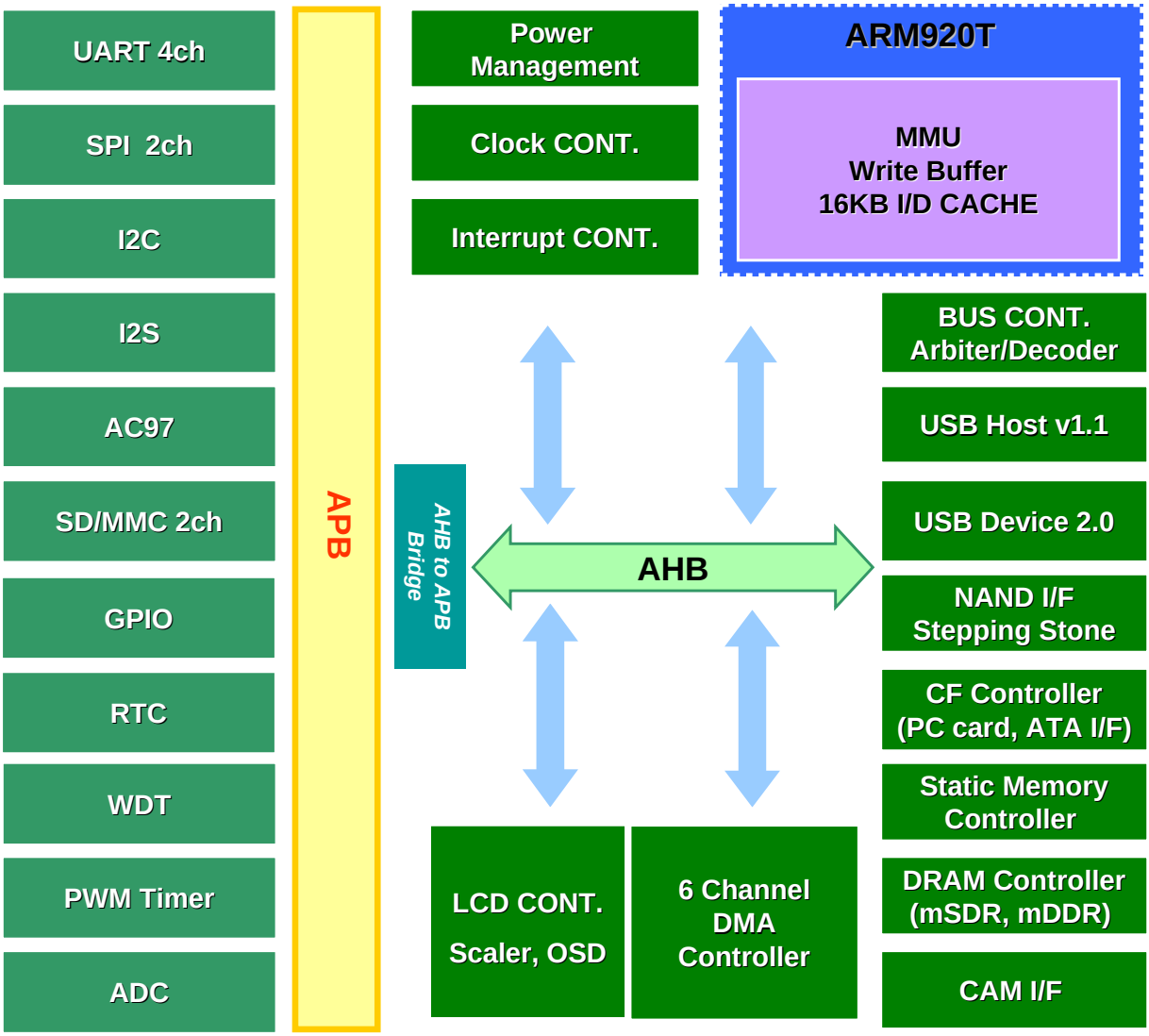
The S3C2443X features an ARM920T core, a 16/32-bit RISC microprocessor, to provide hand-held devices and general applications with cost-effective, low-power, and high performance micro-controller solution in a small form-factor. The S3C2443X is developed using 0.13 μm CMOS standard cell. In addition, it adopts a new bus architecture called Advanced Microcontroller Bus Architecture (AMBA).

By providing a comprehensive set of common system peripherals, the S3C2443X minimizes the overall system costs and eliminates the need to configure additional components.

Features Summary

- ARM920T core, 0.13 μm CMOS standard cells and a memory complier
- 16 KB I/D Cache / MMU
- Operating Frequency 400MHz / 533MHz
- Independent 2 External memory controller
- LCD controller (up to 4K color STN and 256K color TFT) with LCD dedicated DMA
- 2 port USB Host (Version 1.1 Complaint)
- 1 port USB Device (Version 2.0 Complaint)
- 6-channel general DMA with external request pins
- CF&ATA I/F
- 4-channel UART with IrDA 1.0 (Including 64-byte FIFO)
- 2-ch SPI (1-ch HS-SPI support)
- 1-ch multi-master IIC-BUS
- 1-ch IIS-BUS controller
- 1-ch AC97 controller
- 2-ch SD Host controller & Multi-Media Card protocol compatible (1-ch HS-MMC support)
- 4-ch PWM timers and 1-ch internal timer
- 147 general purpose I/O ports/24-ch external interrupt source
- 10-ch 10-bit ADC and touch screen interface
- Watchdog timer
- RTC with calendar function
- On-chip clock generator with PLL
- CAM I/F with BT 601/656 input

Functional Block Diagram



Product Details

❒ ARM Core

- ARM920T 32-bit RISC CPU
- Integrated system for hand-held devices and general embedded applications
- 16/32-Bit RISC architecture and powerful instruction set
- Enhanced ARM architecture MMU which supports WinCE, Symbian, Linux and Palm OS
- Instruction cache, data cache, write buffer and physical address TAG RAM to reduce the effect of main memory bandwidth and latency
- Internal Advanced Microcontroller Bus Architecture (AMBA) (AMBA2.0, AHB/APB)

❒Memory Subsystem

■ROM/SRAM/NAND/NOR interface

- NAND flash memory for boot loader and data storage
  - Supports booting from NAND flash memory
  - 4KB internal buffer (Stepping Stone)
  - Supports storage memory for NAND flash memory
- NAND Interface
  - Supports industry standard NAND interface
  - 1.8V, 2.5V or 3.3V interface voltage
  - x8(bootable), x16(storage only) data bus
  - Density Support: No density(size) limit
  - Supports small & large block NAND
- One-NAND/SRAM/ROM/NOR Flash Interface
  - x8, x16 data bus
  - Interface voltage : 1.8V / 2.5V / 3.3V

■ DRAM interface

- Standard/Mobile SDRAM interface
  - up to 133MHz bus speed
  - x32 data bus
  - Interface voltage :1.8V / 2.5V / 3.3V
  - Density support : up to 1Gbit
  - Mobile SDRAM feature (EMRS) support : DS (Driver Strength Control), TCSR (Temperature Compensated Self-Refresh Control) and PASR (Partial Array Self-Refresh Control)
- Standard/Mobile DDR SDRAM Interface
  - up to 133MHz bus speed
  - x16 data bus with 266Mbps/pin double data rate (DDR)
  - Interface voltage :1.8V / 2.5V / 3.3V
  - Density support : up to 1Gbit
  - Mobile DDR SDRAM feature (EMRS) support

❒Display Controller

■STN LCD interface

- Supports 3 types of LCD panels: 4-bit dual scan, 4-bit single scan, and 8-bit single scan display type
- Supports the monochrome, 4 gray levels, and 16 gray levels
- Supports 256 colors and 4096 colors for color STN LCD panel
- Supports multiple screen size
  - Typical actual screen size: 640x480, 320x240, 160x160, and others
  - Maximum virtual screen size is 4Mbytes.
  - Maximum virtual screen size in 256 color mode: 4096x1024, 2048x2048, 1024x4096, and others
- Supports 4bit/8bit LCD Driver I/F

■TFT LCD Interface

- 1/2/4/8bpp Palletized or 16bpp/24-bpp Non-Palletized Color-TFT support
- 320X240, 640x480 or other display resolutions up to 1024x1024
- Max. 2K x 2K virtual screen size
- 2 Layer OSD

■ Camera Interface

- 16-bit or 8-bit ITU-R601/ITU-R656 format input
- Up to 4M pixel for scaled or 16M pixel for unscaled resolution
- YCrCb 4:2:2 to 4:2:0 down-sampling, down-scaling for MPEG and JPEG
- RGB 24-bit or 16-bit output for preview
- Image windowing and zoom-in function
- Test pattern generation
- Image flip supports Y-mirror, X-mirror, 180’ rotation
- H/W Color Space Conversion

■A/D Converter and Touch Screen Interface

- 10-ch multiplexed ADC
- Max.500K samples/sec and 10-bit resolution

❒ Connectivity

■ I2S Bus Interface

- 1-ch IIS-bus for the audio-codec interface with DMA-based operation
- Serial, 8/16-bit per channel data transfers
- 64-Byte Tx FIFO and 64-Byte Rx FIFO
- Supports IIS format and MSB-justified data format

■ AC97 Interface

- 1-ch AC97 for audio interface with DMA-based operation
- 16-bit Stereo Audio

■ USB Host

- 2-port USB Host
- Complies with OHCI Rev. 1.0
- Compatible with USB Specification version 1.1

■ USB Device

- 1-port USB Device
- 9 End-points for USB Device
- Compatible with the USB Specification version 2.0

■UART

- 4-channel UART with DMA-based or interrupt-based operation
- Supports 5-bit, 6-bit, 7-bit, or 8-bit serial data transmit/receive
- Supports external clock for the UART operation (UEXTCLK)
- Programmable baud rate
- Supports IrDA 1.0 SIR (115.2Kbps) mode
- Each channel has internal 64-byte Tx FIFO and 64-byte Rx FIFO

■**SPI Interface**

- 2-ch Serial Peripheral Interface Protocol version 2.11 compatible (1-ch for HS-SPI)
- 16 byte TX
- DMA-based or interrupt-based operation

■ **I2C Bus Interface**

- 1-ch Multi-Master IIC-Bus
- Serial, 8-bit oriented and bi-directional data transfers can be made at up to 100 Kbit/s in the standard mode
- Up to 400 Kbit/s in the fast mode

■**MMC/SD/SDIO/HS-MMC**

- Multimedia Card Protocol version 4.0 compatible
- Compatible with SDIO card protocol version 1.0
- SD Memory Card Protocol version 1.0 compatible
- DMA based or Interrupt based operation
- 512 Bytes FIFO for Tx/Rx
- 2-ch SDIO/SD/MMC (1-ch for HS-MMC)

■ **CF/ATA I/F**

- Support CF+ and Compact Flash Spec. Ver3.0

❒System Peripheral

■ **Clock & Power Manager**

- On-chip MPLL and EPLL
  - EPLL generates the clock to operate several peripheral devices (IIS, UART, USB, ... etc.)
  - MPLL generates the clock to operate CPU at 400MHz @ ARM 1.3V, Internal 1.3V and at 533MHz @ ARM 1.375V, Internal 1.15V (typical condition)
- Clock can be fed selectively to each function block by software
  - Normal mode: normal operating mode
  - Idle mode: the clock for only CPU is stopped
  - Stop mode : All clock sources are stopped except RTC module
  - Sleep mode: CPU & all peripherals Power off
- Wake up by EINT[15:0], RTC alarm & tick interrupt or Battery fault from Sleep mode

■ **Interrupt Controller**

- 51 Interrupt sources (1 One Watch dog timer, 5 timers, 12 UARTs, 24 external interrupts, 6 DMA, 2 RTC, 2 ADC, 1IIC, 2 SPI, 2 SDI, 2 USB, 1 LCD, 1 Battery Fault, 1 NAND, and 2 Camera, etc)
- Level/Edge mode on external interrupt source
- Programmable polarity of edge and level
- Supports Fast Interrupt request (FIQ) for very urgent interrupt request

■ **Timer with Pulse Width Modulation (PWM)**

- 4-ch 16-bit Timer with PWM / 1-ch 16-bit internal timer with DMA-based or interrupt-based operation
- Programmable duty cycle, frequency, and polarity
- Dead-zone generation
- Supports external clock sources

■**Real Time Clock (RTC)**

- Full clock feature: msec, second, minute, hour, date, day, month, and year
- 32.768 KHz operation
- Alarm interrupt
- Time tick interrupt

■**DMA**

- 6-ch DMA controller
- Supports memory to memory, IO to memory, memory to IO, and IO to IO transfers
- Burst transfer mode to enhance the transfer rate

■**Watchdog Timer**

- 16-bit Watchdog Timer
- Interrupt request or system reset at time-out

■**GPIO**

- 24 external interrupt ports
- Total 147 Multiplexed input/output ports

■**Electrical Characteristics**

- Operating Conditions
  - Supply Voltage for Logic Core
    400MHz @1.3V, 533MHz @1.15V
  - External Memory Interface:
    1.8V/2.5V/3.3V
  - External I/O Interface:
    1.8V/2.5V/3.3V
    (depend on each power domain)
- Operational Core Frequency
  - 400MHz @1.3V, 533MHz @1.375V