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Preliminary

RF2052

HIGH PERFORMANCE WIDEBAND RF SYNTHESIZER/VCO WITH INTEGRATED RF MIXER

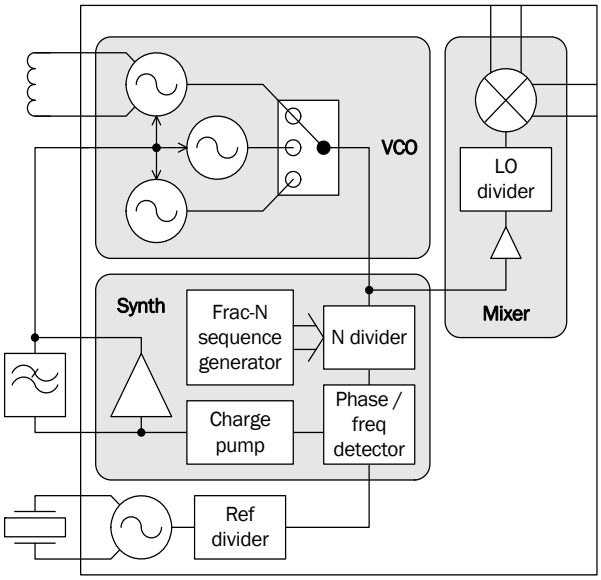
RoHS Compliant and Pb-Free Product
Package: QFN, 32-Pin, 5mmx5mm

Features

- 2.7V to 3.6V Operation
- 50MHz to 2.5GHz Frequency Range
- Fractional-N Synthesizer
- Low Phase Noise VCOs
- Very Fine Frequency Resolution
- On-chip Calibration
- Wide Range of Reference Frequencies
- Integrated RF Mixer
- Programmable Bias Conditions
- Three-wire Serial Control Interface

Applications

- Frequency Band Shifting
- Signal Generation
- Super-heterodyne Radios
- Satellite Communications
- Instrumentation and Test Equipment
- Wireless Infrastructure
- Wireless Repeaters
- Point-to-Point Radio Links
- PMR Systems



Functional Block Diagram

Product Description

The RF2052 is a very wideband RF frequency conversion chip with integrated local oscillator (LO) generation and an RF mixer. The RF synthesizer includes an integrated fractional-N phase locked loop with voltage controlled oscillators (VCOs) and dividers to produce a low-phase noise LO signal with a very fine frequency resolution. The LO output drives the built-in RF mixer which converts the signal into the required frequency band. The bias current can be programmed to optimize the supply current/performance trade-off. The LO generation blocks have been designed to continuously cover the frequency range from 300MHz to 2400MHz. The RF mixer is very broad band and operates from 50MHz to 2500MHz at the RF ports of the device. An external crystal of between 10MHz and 52MHz or an external reference source of between 10MHz and 104MHz can be used with the RF2052 to accommodate a variety of reference frequency options.

The device is programmed using a true three-wire serial interface. The RF2052 is designed for 2.7V to 3.6V operation for compatibility with portable, battery powered devices. It is available in a plastic 32-pin, 5mmx5mm QFN package.

Optimum Technology Matching® Applied

☐ GaAs HBT	☐ SiGe BiCMOS	☐ GaAs pHEMT	☐ GaN HEMT
☐ GaAs MESFET	☐ Si BiCMOS	☑ Si CMOS	☐ RF MEMS
☐ InGaP HBT	☐ SiGe HBT	☐ Si BJT	

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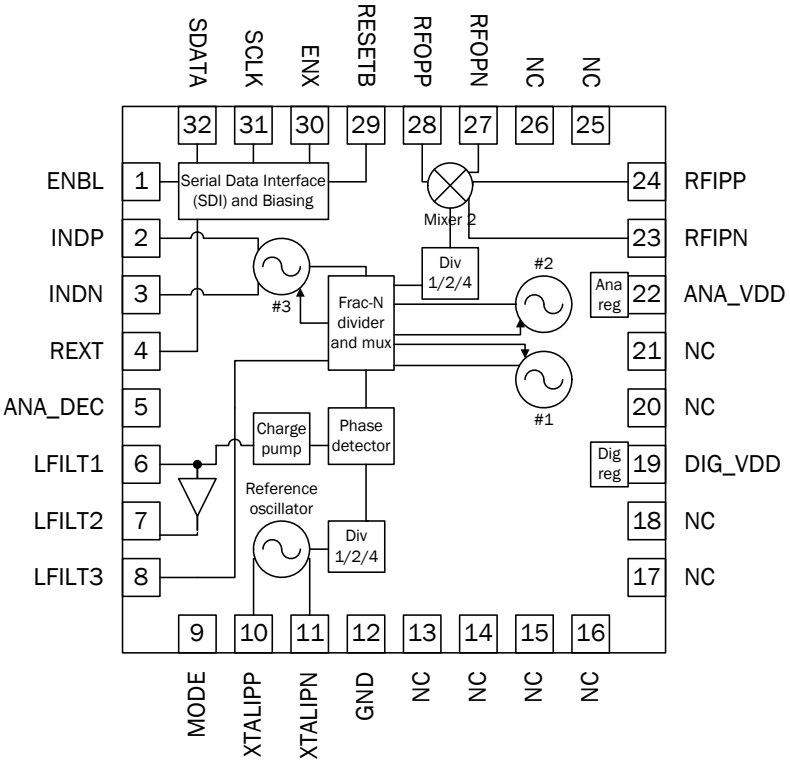
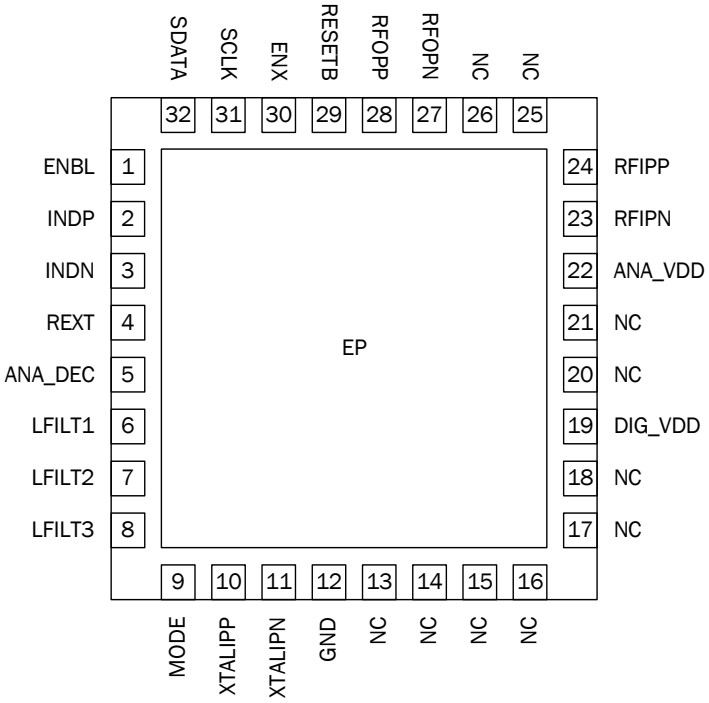
Detailed Functional Block Diagram



Pin Out



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Pin	Function	Description
1	ENBL	Device enable input. An RC low-pass filter could be used to reduce digital noise.
2	INDP	Low frequency VCO differential inductor. This is an RF pin and all normal layout precautions should be observed.
3	INDN	Low frequency VCO differential inductor. This is an RF pin and all normal layout precautions should be observed.
4	REXT	External bandgap bias resistor. This could be a sensitive low frequency noise injection point.
5	ANA_DEC	Analog supply decoupling capacitor. Apply RF decoupling to a good quality ground as close to the pin as possible.
6	LFILT1	Phase detector output. Low-frequency noise-sensitive node.
7	LFILT2	Loop filter op-amp output. Low-frequency noise-sensitive node.
8	LFILT3	VCO control input. Low-frequency noise-sensitive node.
9	MODE	Mode select pin. An RC low-pass filter can be used to reduce digital noise.
10	XTALIPP	Reference crystal / reference oscillator input. Should be AC-coupled if an external reference is used.
11	XTALIPN	Reference crystal / reference oscillator input. Should be AC-coupled to ground if an external reference is used.
12	GND	Connect to ground.
13	NC	
14	NC	
15	NC	
16	NC	
17	NC	
18	NC	
19	DIG_VDD	Digital supply. Should be decoupled as close to the pin as possible.
20	NC	
21	NC	
22	ANA_VDD	Analog supply. Should be decoupled as close to the pin as possible.
23	RFIPN	Differential input. See note 1.
24	RFIPP	Differential input. See note 1.
25	NC	
26	NC	
27	RFOPN	Differential output. See note 2.
28	RFOPP	Differential output. See note 2.
29	RESETB	Chip reset (active low). Connect to DIG_VDD if external reset is not required.
30	ENX	Serial interface select (active low). An RC low-pass filter could be used to reduce digital noise.
31	SCLK	Serial interface clock. An RC low-pass filter could be used to reduce digital noise.
32	SDATA	Serial interface data. An RC low-pass filter could be used to reduce digital noise.
EP	Exposed pad	Connect to ground. This is the ground reference for the circuit. All decoupling should be connected here through low impedance paths.

Note 1: The signal should be connected to this pin such that DC current cannot flow into or out of the chip, either by using an AC coupling capacitor as part of lumped element matching network or by use of a transformer (see application circuit).

Note 2: DC current needs to flow from ANA_VDD into this pin, either through RF choke inductor or transformer (see application circuit).

Absolute Maximum Ratings

Parameter	Rating	Unit
Supply Voltage (V_{DD})	-0.5 to +3.6	V
Input Voltage (V_{IN}), any pin	-0.3 to V_{DD}+0.3	V
Storage Temperature (T_{STG})	-40 to +150	°C

Caution! ESD sensitive device.

Exceeding any one or a combination of the Absolute Maximum Rating conditions may cause permanent damage to the device. Extended application of Absolute Maximum Rating conditions to the device may reduce device reliability. Specified typical performance or functional operation of the device under Absolute Maximum Rating conditions is not implied.

RoHS status based on EUDirective2002/95/EC (at time of this document revision).

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
ESD Requirements					
Human Body Model					
General	2000			V	
RF Pins	1000			V	
Machine Model					
General	200			V	
RF Pins	100			V	
Operating Conditions					
Supply Voltage (V_{DD})	2.7	3.0	3.6	V	
Temperature (T_{OP})	-40		85	°C	
Static					
Programmable Supply Current (I_{DD})					
Low Current Setting		55		mA	Only one mixer operating.
High Linearity Setting		72		mA	Only one mixer operating.
Standby		3		mA	Reference oscillator and bandgap only.
Power Down Current		140		µA	ENBL=0
Mixer					
Gain		-2		dB	
Noise Figure					
Low Current Setting		9.5		dB	
High Linearity Setting		12		dB	
IIP_3					
Low Current Setting		12		dBm	
High Linearity Setting		18		dBm	
RF and IF Port Frequency Range	50		2500	MHz	
RF and IF Port Return Loss		10		dB	maximal, 100Ω differential

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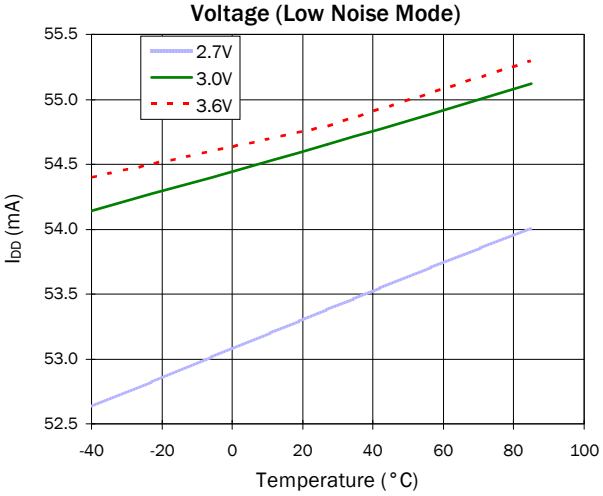
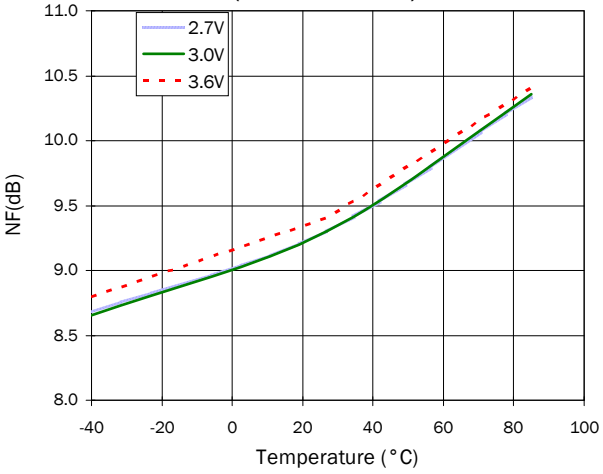
Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Voltage Controlled Oscillator					
Open Loop Phase Noise at 1MHz Offset					
2GHz LO Frequency		-130		dBc/Hz	
1GHz LO Frequency		-135		dBc/Hz	
500MHz LO Frequency		-140		dBc/Hz	
Reference Oscillator					
Xtal Frequency	10		52	MHz	
Reference Input	10		104	MHz	
Phase Detector Frequency			52	MHz	

Typical Operating Characteristics

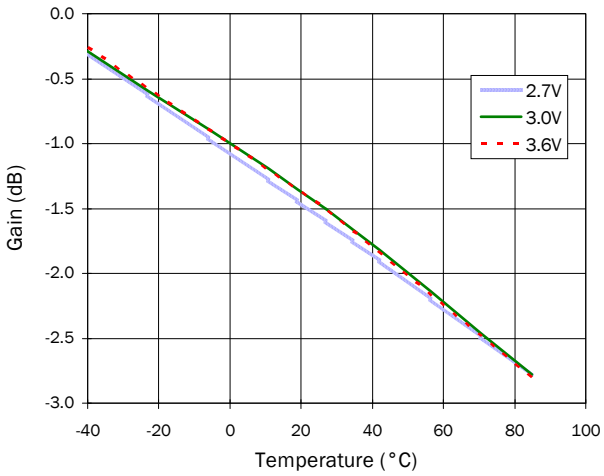
Supply Current versus Temperature and Supply Voltage (Low Noise Mode)



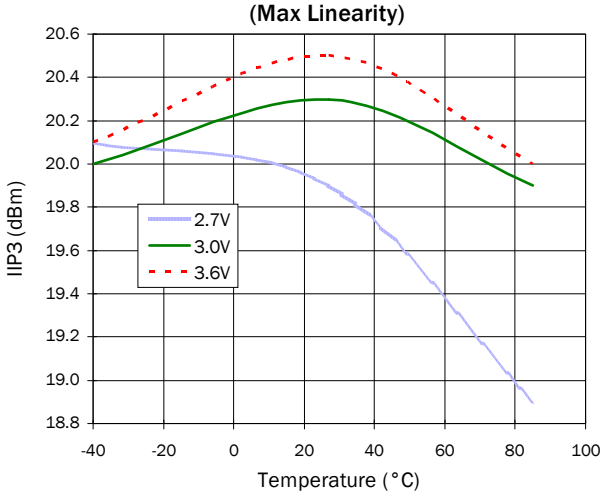
NF versus Temperature and Supply Voltage (Low Noise Mode)



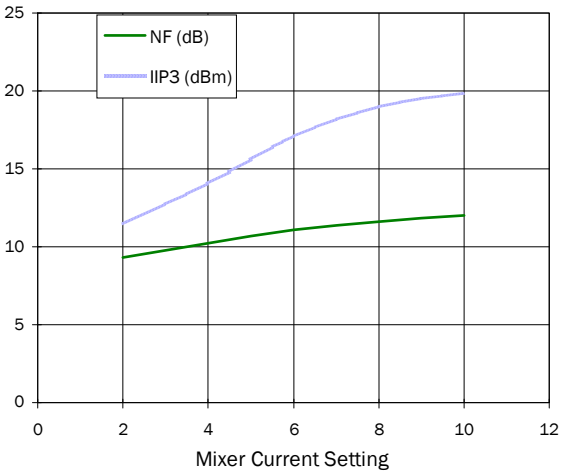
Gain versus Temperature and Supply Voltage



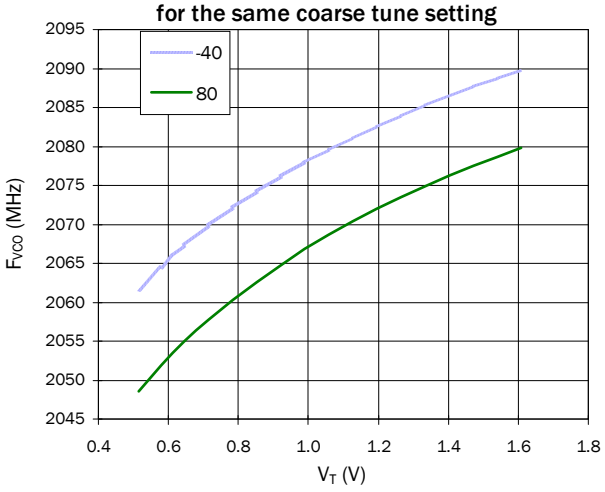
IIP3 versus Temperature and Supply Voltage (Max Linearity)



NF and IIP3 versus Mixer Current Setting



VCO1 F_{VCO} versus V_T for the same coarse tune setting



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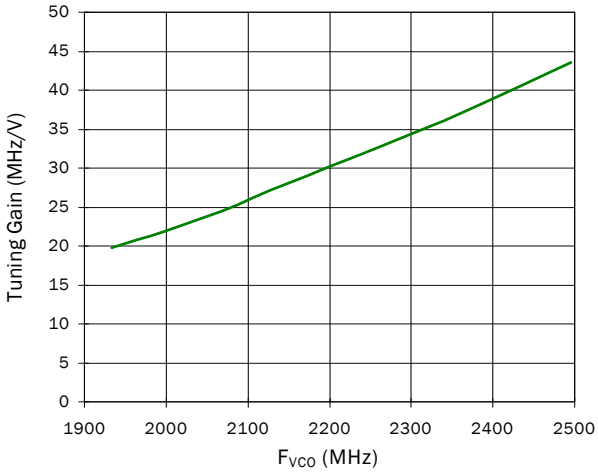
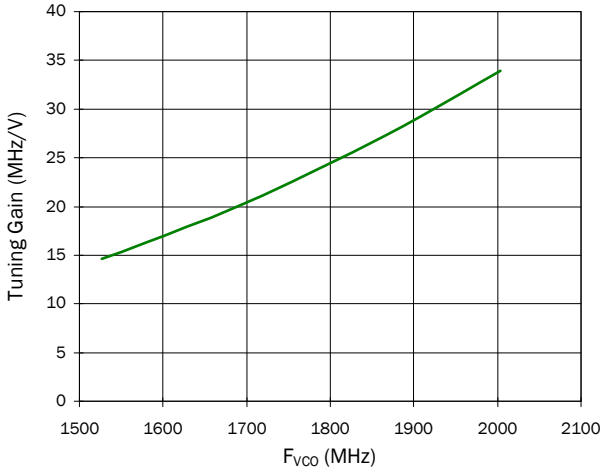
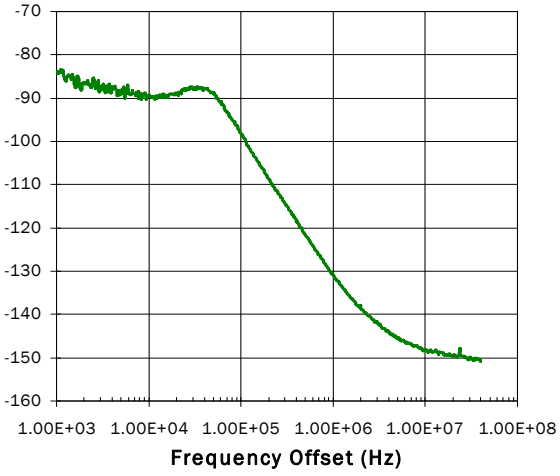
VCO1 Tuning Gain versus Frequency



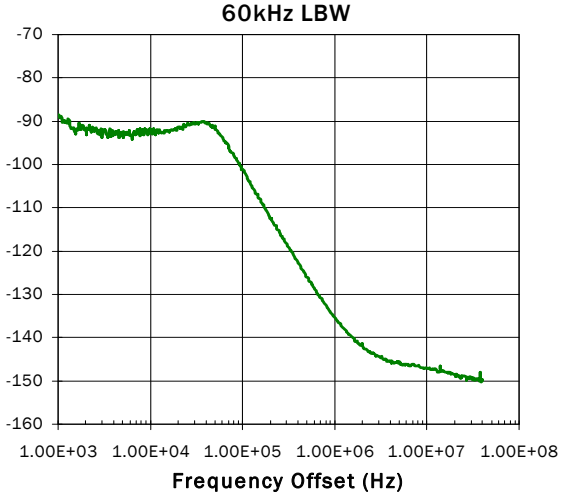
VCO2 Tuning Gain versus Frequency



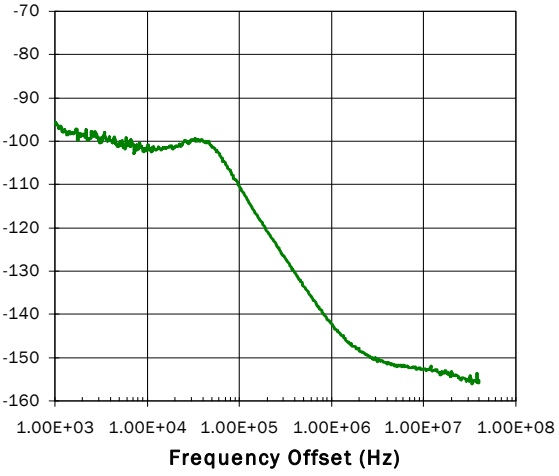
Phase Noise (dBc/Hz) @ 2000MHz
60kHz LBW



Phase Noise (dBc/Hz) @ 1000MHz
60kHz LBW



Phase Noise (dBc/Hz) @ 500MHz
60kHz LBW



Detailed Description

The RF2052 includes a wideband fractional-N phase-locked loop, an op-amp to enable an active loop filter (if required), a wideband frequency generation (VCO) capability, a wideband mixer, and a low-noise crystal oscillator circuit.

A true 3-wire serial interface is provided for synthesizer programming, device configuration and control. Various diagnostic indicators are also available using the read function of the serial bus if required. Hardware controls for power-down and mixer selection are also provided.

Wideband Mixer

RF2052 includes a wideband mixer. It supports RF/IF frequencies of 50MHz to 2500MHz using the internal VCO to provide the LO frequency of 300MHz to 2400MHz. The mixer has in input port and an output port that can be used for either the IF or the RF ports. The mixer current can be programmed allowing a trade-off between power consumption and linearity. The majority of the mixer current is sourced through the output pins via either a centre-tapped balun or an RF choke in the external matching circuitry to the supply. This can be programmed to between 5mA and 20mA depending on linearity requirements, using the MIX2_IDD<3:0> word in the CFG2 register.

The RF mixer input and output ports are differential and require simple matching circuits optimized to the specific application frequencies. A conversion gain of approximately -3dB to 0dB is achieved with 100Ω differential input impedance, and the outputs driving 500Ω to 50Ω differential impedance match at the pins.

VCO

In the RF2052 three VCOs are used to cover the whole tuning range requirement. VCO1 uses an integrated inductor, and is optimized for use between 1972MHz and 2400MHz. VCO2 also has an internal inductor and is optimized for use between 1556MHz and 1972MHz. The third, low frequency, VCO uses an external strip-line resonator that may be configured by the user, but which is intended for use between 1200MHz and 1556MHz. The VCO is selected using the P1_VCOSEL<1:0> and P2_VCOSEL<1:0> control words in the PLL1x0 or PLL2x0 registers (depending on mode). The VCO current may also be programmed using the P1_VCOI or P2_VCOI control words in the PLL1x1 and PLL2x1 registers respectively. This allows optimization of VCO performance for a particular frequency. A divide-by 1/2/4 block follows the VCO, to allow a LO frequency from 300MHz to 2400MHz to be obtained. The divide ratio is set by the P1_LODIV<1:0> and P2_LODIV<1:0> control words in the RxPLLx0 and TxPLLx0 registers.

Fractional-N PLL

The IC contains a charge-pump based, fractional-N phase locked loop (PLL) for controlling the three VCOs. The PLL includes automatic calibration systems to counteract the effects of process and environmental variations, ensuring repeatable lock-time and noise performance. The PLL is intended to use a reference frequency signal of 10MHz to 104MHz. A reference divider (divide by 1, 2, or 4) is supplied and should be programmed to limit the frequency at the phase detector to a maximum of 52MHz.

The PLL will lock the VCO to the frequency F_{VCO} according to:

$$F_{VCO} = 2*N*F_{OSC}/R$$

where N is the programmed fractional N divider value consisting of N and NUM, F_{OSC} is the reference signal frequency at the OSCA pin, and R is the programmed R divider value (1, 2, or 4).

The N divider is a fractional divider, containing a dual-modulus prescaler and a digitally spur-compensated fractional sequence generator to allow fine frequency steps. The N divider is programmed using the N(9:0) and NUM(23:0) bits as follows:

First determine the desired, effective N divider value, N_{EFF}:

$$N_{EFF} = F_{VCO}*R/F_{OSC}$$

N(9:0) should be set to the integer part of N_{EFF}. NUM should be set to the fractional part of N_{EFF} multiplied by $2^{24} = 16777216$.

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Example: VCO1 operating at 2220MHz, 23.92MHz reference frequency, the desired effective divider value is:

$$N_{EFF} = F_{VCO} * R / F_{OSC} = 2220 * 1 / 23.92 = 92.8093645495.$$

The N value is set to 92, equal to the integer part of N_{EFF}, and the NUM value is set to the fractional portion of N_{EFF} multiplied by 2^{24}:

$$NUM = 0.8093645495 * 2^{24} = 13,578,884.$$

Converting N and NUM into binary results in the following:

N=0 0101 1100
NUM=1100 1111 0011 0010 1000 0100

So the registers would be programmed:

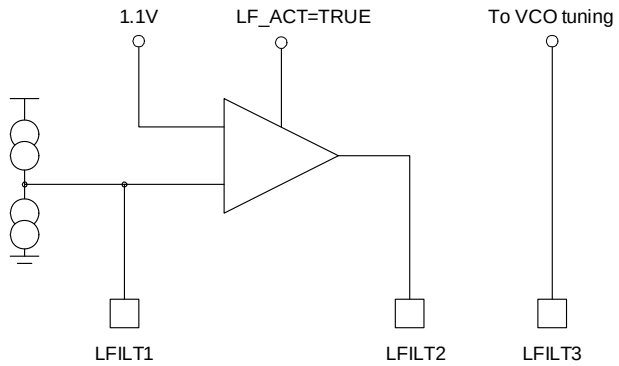
P1_N (or P2_N)=0 0101 1100
P1_NUM_MSB (or P2_NUM_MSB)=1100 1111 0011 0010
P1_NUM_LSB (or P2_NUM_LSB)=1000 0100

The maximum N_{EFF} is 127, and the minimum N_{EFF} is 12. The minimum step size is $F_{OSC}/2^{24}$. Thus for a 23.92MHz reference, the frequency step size would be 1.4Hz. The minimum reference frequency that could be used to program a frequency of 2400MHz (using VCO1) is 2400/127, 18.898MHz (approx).

Two PLL programming banks are provided, the first bank is superseded by the label PLL1 and the second bank is superseded by the label PLL2. For the RF2052 either these banks may be used to the LO frequency, and can be selected using the MODE pin.

Loop Filter

The PLL may be designed to use an active or a passive loop filter as required. The internal configuration of the chip is shown below. If the CFG1:LF_ACT bit is asserted high, the op-amp will be enabled. If the CFG1:LF_ACT bit is asserted low, the internal op-amp is disabled and a high impedance is presented to the LFILT1 pin. The RFSlice evaluation software can assist with loop filter designs. Because the op-amp is used in an inverting configuration in active mode, when the passive loop filter mode is selected the phase-detector polarity should be inverted. For active mode, CFG1:PDP=1, for passive mode, CFG1:PDP=0.



Crystal Oscillator

The PLL may be used with an external reference source, or its own crystal oscillator. If an external source (such as a TCXO) is being used it should be AC-coupled into one of the XO inputs, and the other input should be AC-coupled to ground.

A crystal oscillator typically takes many milliseconds to settle, and so for applications requiring rapid pulsed operation of the PLL (such as a TDMA system, or Rx/Tx half-duplex system) it is necessary to keep the XO running between bursts. However, when the PLL is used less frequently, it is desirable to turn off the XO to minimize current draw. The REFSTBY register is provided to allow for either mode of operation. If REFSTBY is programmed high, the XO will continue to run even when ENABLE is

asserted low. Thus the XO will be stable and a clock is immediately available when ENABLE is asserted high, allowing the chip to assume normal operation. On cold start, or if REFSTBY is programmed low, the XO will need a warm-up period before it can provide a stable clock. The length of this warm-up period will be dependent on the crystal characteristics.

Serial Interface

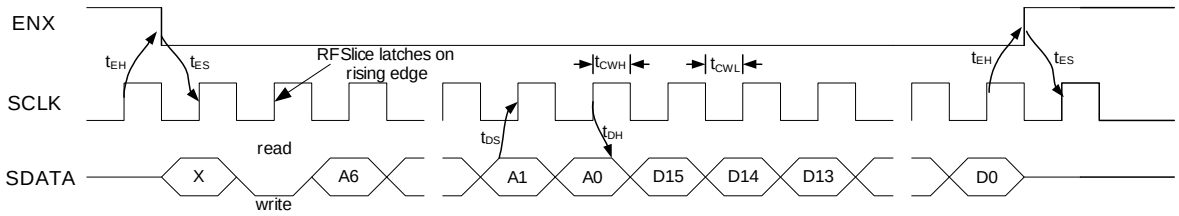
The RF2052 is programmed using a 3-wire serial bus. The programming interface supports both write and read operations.

Write

Initially ENX is high and SDATA is high impedance. The write operation begins with the controller starting SCLK. On the first falling edge of SCLK the baseband asserts ENX low. The second rising edge of SCLK is reserved to allow the SDI to initialize, and the third rising edge is used to define whether the operation will be a write or a read operation. In write mode the baseband will drive SDATA for the entire telegram. RF2052 will read the data bit on the rising edge of SCLK.

The next 7 data bits are the register address, MSB first. This is followed by the payload of 16 data bits for a total write mode transfer of 24 bits. Data is latched into RF2052 on the last rising edge of SCLK (after ENX is asserted high).

Serial Bus Write



t_{EH} > 20ns, t_{ES} >20ns, t_{DS} >20ns, t_{DH} > 20ns, t_{CWH} > 40ns, t_{CWL} >40ns

Read

Initially ENX is high and SDATA is high impedance. The read operation begins with the controller starting SCLK. The controller is in control of the SDATA line during the address write operation. On the first falling edge of SCLK the baseband asserts ENX low. The second rising edge of SCLK is reserved to allow the SDI to initialize, and the third rising edge is used to define whether the operation will be a write or a read operation. In read mode the baseband will drive SDATA for the address portion of the telegram, and then control will be handed over to RF2052 for the data portion. RF2052 will read the data bits of the address on the rising edge of SCLK. After the address has been written, control of the SDATA line is handed over to RF2052. One and a half clocks are reserved for turn-around, and then the data bits are presented by RF2052. The data is set up on the rising edge of SCLK, and the controller latches the data on the falling edge of SCLK. At the end of the data transmission, RF2052 will release control of the SDATA line, and the controller asserts ENX high. The SDATA port on RF2052 transitions from high impedance to low impedance on the first rising edge of the data portion of the transaction (for example, 3 rising edges after the last address bit has been read), so the controller chip should be presenting a high impedance by that time.

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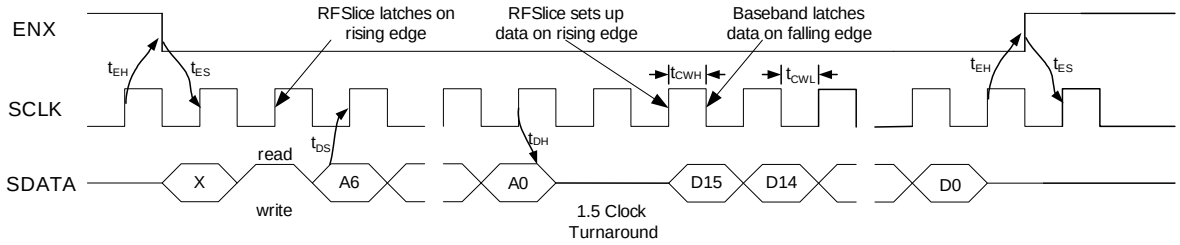
Serial Bus Read



t_{EH} > 20ns, t_{ES} >20ns, t_{DS} >20ns, t_{DH} > 20ns, t_{CWH} > 40ns, t_{CWL} >40ns

Hardware Control

Three hardware control pins are provided: ENBL, MODE and RESETB. ENBL will enable the part when asserted high. This enables all circuitry except for the digital, which is always active providing a power supply is present. If the CFG3:REFSTBY bit is not set, ENBL will also control the activation of the XO and biasing circuitry. IF CFG3:REFSTBY bit is asserted high, the XO and biasing circuitry will always be active.

The RESETB pin is a hardware reset control that will reset all digital circuits to their start-up state when asserted low. The device includes a POR function, so this pin should not normally be required, in which case it should be connected to the positive supply.

The MODE pin controls which mixer and PLL programming register block is active.

Calibration

Two calibration functions are included in the device; a frequency calibration function and a VCO tuning gain calibration function.

The frequency calibration is enabled using the PLL1x0:P1_CT_EN and PLL2x0:P2_CT_EN control words. When enabled, the calibration is performed whenever ENABLE is asserted. The device will perform a coarse tuning function whereby fixed capacitance elements are progressively connected to the VCO resonant circuit until the VCO is oscillating at approximately the correct frequency. The output of this calibration is made available in the RB1:CT_CAL read-back register. A value of 128 or 0 in this register indicates that the coarse tune was unsuccessful. This will only occur if the user is trying to program a frequency that is outside of the VCO operating range. A value between 0 and 128 indicates a successful calibration, and will be dependent on the desired frequency, as well as process variation for a particular device. The calibration operation takes approximately 50µs. If start-up time is a critical parameter, and the user is always programming the same frequency for the PLL, the calibration result may be read back from the RB1:CT_CAL register, and written to the PLL1x2:P1_CT_DEF or PLL2x2:P2_CT_DEF registers (depending on desired programming block). The calibration function may then be disabled using the PLL1x0:P1_CT_EN or PLL2x0:P2_CT_EN control words.

The VCO tuning gain calibration is enabled using the PLL1x1:P1_KV_EN or PLL2x1:P2_KV_EN registers. The tuning gain of the VCO will vary according to the desired oscillation frequency (see performance graphs). When the synthesizer is only required to generate a narrow range of frequencies, it is sufficient to simply look up the tuning gain of the VCO for that frequency range, and design the loop filter accordingly. However, if a wide range of frequencies is required, there is some risk that the variation in tuning gain will result in an unacceptable variation in the PLL loop bandwidth and may even result in loop instability. The tuning gain calibration will compensate for VCO tuning gain variation by modifying the charge pump current such that the ratio between the tuning gain and the charge pump current remains constant. This calibration requires approximately 100µs. The result of the calibration will be returned to the RB1:CP_CAL read-back register. The charge pump current may be controlled directly by the user by disabling the calibration using the PLL1x1:P1_KV_EN or PLL2x1:P2_KV_EN registers and writing the required value to the PLL1x0:P1_CP_DEF or PLL2x0:P2_CP_DEF registers.

Start-up

When starting from cold REFSTBY=0, REFSTBY should be asserted high approximately 500µs before ENABLE is taken high. This is to allow the XO to settle and will depend on XO characteristics. The various calibration routines will also take some time depending on whether they are enabled or not. Coarse tuning calibration takes about 50µs and VCO tuning gain compensation takes about 100µs. Additionally, time for the PLL to settle will be required. All of these timings will be dependent application specific factors such as loop filter bandwidth, reference clock frequency, XO characteristics and so on. The fastest turn-on and lock time will be obtained by leaving REFSTBY asserted high, disabling all calibration routines, and setting the PLL loop bandwidth as wide as possible.

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Programming Registers

CFG1 (00h)

Bit Name	Bit	Function
LD_EN	[15]	Enable lock detector circuitry
LD_LEV	[14]	Modify lock range for lock detector
PDP	[8]	Phase detector polarity: 0=positive; 1=negative
LF_ACT	[7]	Active loop filter enable, 1=Active 0=Passive
CPL	[6:5]	Charge pump leakage current: 00=no leakage; 01=setting 1; 10=setting 2; 11=setting 3
CT_POL	[4]	Polarity of VCO coarse-tune word: 0=positive; 1=negative

CFG2 (01h)

Bit Name	Bit	Function
MIX2_IDD	[10:8]	Mix 2 current (mA): 000=OFF; 001=5; 010=10; 011=15; 100=20
NBR_CT_AVG	[3:2]	Number of averages during CT cal
NBR_KV_AVG	[1:0]	Number of averages during KV cal

CFG3 (02h)

Bit Name	Bit	Function
TKV1	[15:12]	Settling time for first measurement in LO KV compensation
TKV2	[11:8]	Settling time for second measurement in LO KV compensation
FLL_FACT	[3:2]	
CT_CPOL	[1]	
REFSTBY	[0]	Reference oscillator state in standby mode 0=XO is off; 1=XO is on

CFG4 (03h)

Bit Name	Bit	Function
CLK_DIV	[15:12]	Reference divider: b0001=div by 1; b0100=div by 2; b1000=div by 4
XO_CT	[11:8]	XO coarse tune
XO_CR_S	[5]	XO additional fixed capacitance

PLL1x0 (08h)

Bit Name	Bit	Function
P1_VCOSEL	[15:14]	VCO band select, Mode 1: 00=VCO1; 01=VCO2; 10=VCO3; 11=Reserved
P1_CT_EN	[13:12]	VCO coarse tune enable, Mode 1: 00=disabled; 11=full
P1_KV_EN	[11:10]	VCO tuning gain calibration enable, Mode 1: 00=disabled; 11=full
P1_LODIV	[9:8]	LO divider setting, Mode 1: 00=div by 1; 01=div by 2; 10=div by 4; 11=Reserved
P1_CP_DEF	[5:0]	Charge pump setting. If P1_KV_EN=1 this value sets charge pump current during Kv compensation measurement. If P1_KV_EN=0, this value is used at all times.

PLL1x1 (09h)

Bit Name	Bit	Function
P1_NUM_MSB	[15:0]	Most significant bits of VCO divider numerator value, Mode 1

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PLL1x2 (0Ah)

Bit Name	Bit	Function
P1_NUM_LSB	[15:8]	Least significant bits of VCO divider numerator value, Mode 1
P1_CT_DEF	[7:1]	VCO coarse tuning default value, Mode 1

PLL1x3 (0Bh)

Bit Name	Bit	Function
P1_N(8:0)	[15:7]	VCO divider integer value, Mode 1
P1_VCOI(2:0)	[2:0]	VCO bias setting - Mode 1

PLL2x0 (10h)

Bit Name	Bit	Function
P2_VCOSEL	[15:14]	VCO band select, Mode 2: 00=VCO1; 01=VCO2; 10=VCO3; 11=Reserved
P2_CT_EN	[13:12]	VCO coarse tune enable, Mode 2: 00=disabled; 11=full
P2_KV_EN	[11:10]	VCO tuning gain calibration enable, Mode 2: 00=disabled; 11=full
P2_LODIV	[9:8]	LO divider setting, Mode 2: 00=div by 1; 01=div by 2; 10=div by 4; 11=Reserved
P2_CP_DEF	[5:0]	Charge pump setting. If P2_KV_EN=1 this value sets charge pump current during Kv compensation measurement. If P2_KV_EN=0, this value is used at all times.

PLL2x1 (11h)

Bit Name	Bit	Function
P2_NUM_MSB	[15:0]	Most significant bits of VCO divider numerator value, Mode 2

PLL2x2 (12h)

Bit Name	Bit	Function
P2_NUM_LSB	[15:8]	Least significant bits of VCO divider numerator value, Mode 2
P2_CT_DEF	[7:1]	VCO coarse tuning default value, Mode 2

PLL2x3 (13h)

Bit Name	Bit	Function
P2_N	[15:7]	VCO divider integer value, Mode 2
P2_VCOI	[2:0]	VCO bias setting - Mode 2

RB1 (1Ch)

Bit Name	Bit	Function
LOCK	[15]	PLL Lock detector, 0=Pll locked, 1=Pll unlocked
CT_CAL(6:0)	[14:8]	CT setting (either result of CT cal, or CT_DEF,dep. on state of CT_EN). Mode 1/Mode 2 dep on MODE
CP_CAL(6:0)	[7:0]	CP setting (either result of KV cal, or CP_DEF,dep on state of KV_EN). Mode 1/Mode 2 dep on MODE

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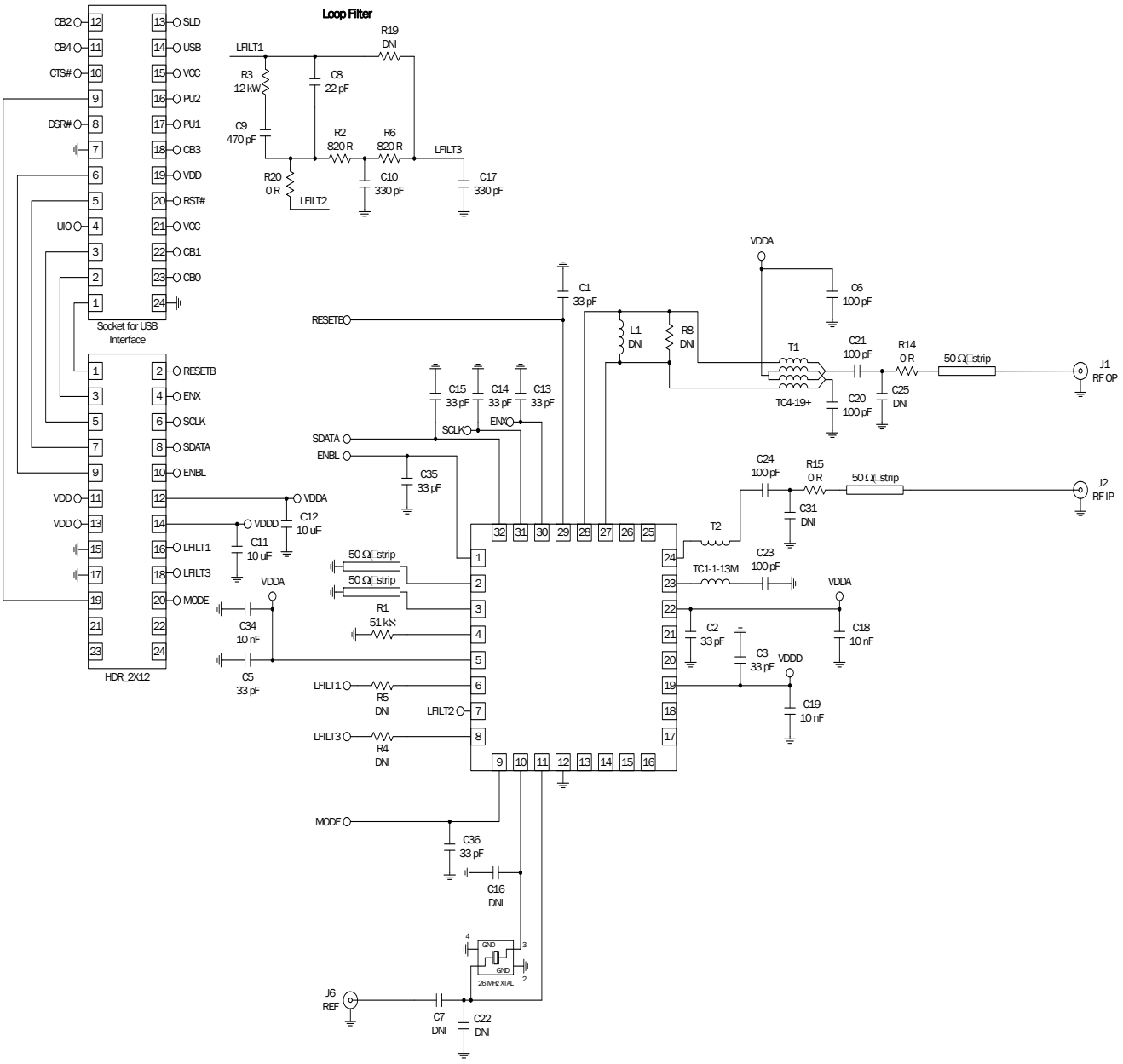
Evaluation Board

The following diagrams show the schematic of the RF2052 evaluation board and the PCB layout for the RF section of the circuit. Application notes have been produced showing how the device is matched and details of board layouts. The documentation supplied with the design kit provides a complete circuit diagram for the board and associated information on programming the device.

Evaluation Board Schematic



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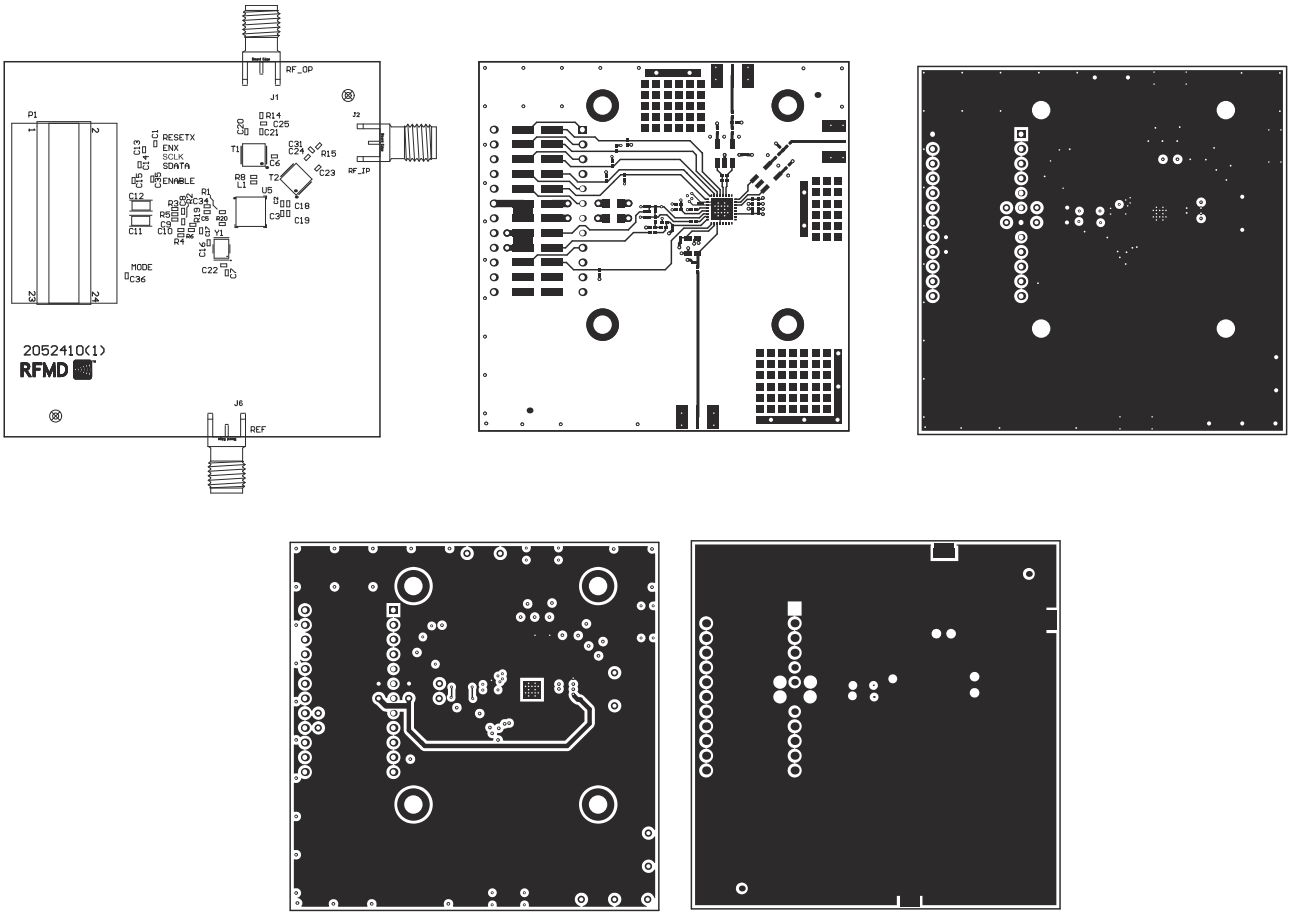
Evaluation Board Layout
Board Size 2.5”x2.5”
Board Thickness 0.040”, Board Material FR-4



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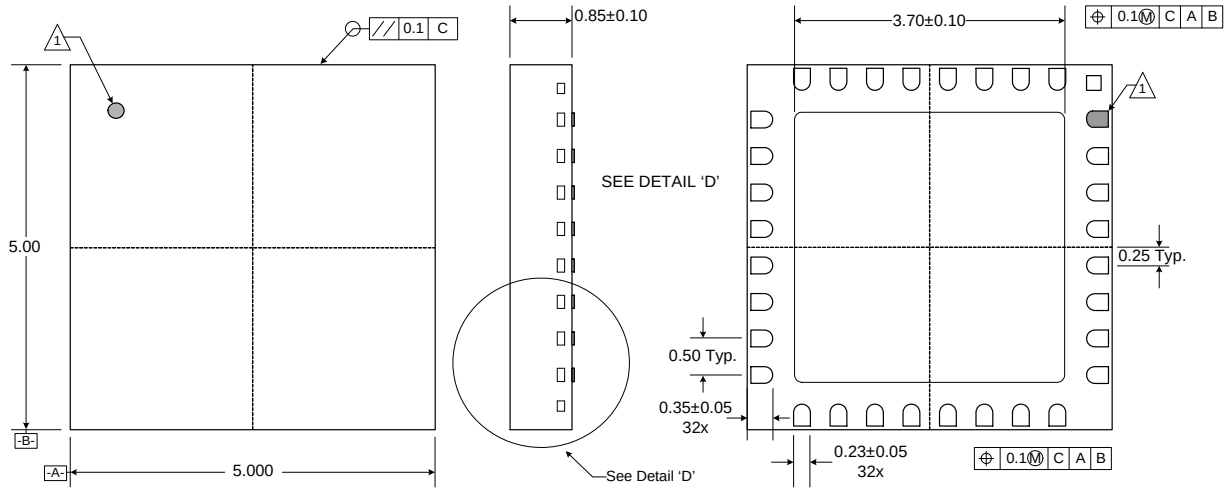
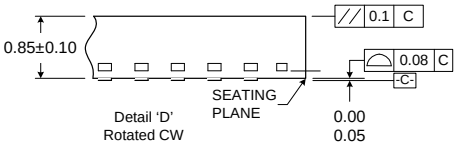
Package Drawing
QFN, 32-Pin, 5mmx5mm





Dimensions in mm.
Shaded area indicates pin 1.

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Ordering Information

RF2052	High Performance Wideband RF Synthesizer/VCO with Integrated RF Mixer
DK2052	Design Kit Including Evaluation Board, Cables, Connectors, and Software

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