1.5 GHz Low Noise Self-Biased Transistor Amplifier

Technical Data

INA-12063

Features

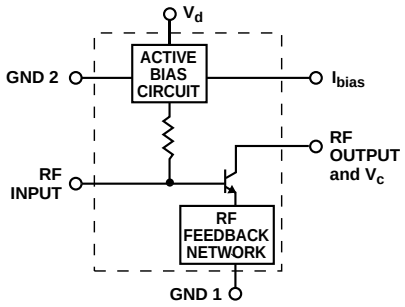
- **Integrated, Active Bias Circuit**
- **Single Positive Supply Voltage (1.5 – 5V)**
- **Current Adjustable, 1 to 10mA**
- **2 dB Noise Figure at 900 MHz**
- **16 dB Gain at 900 MHz**
  25 dB Gain at 100 MHz

Applications

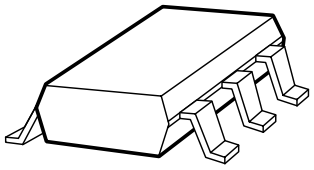
- **Amplifier Applications for Cellular, Cordless, Special Mobile Radio, PCS, ISM, and Wireless LAN Applications**

Equivalent Circuit

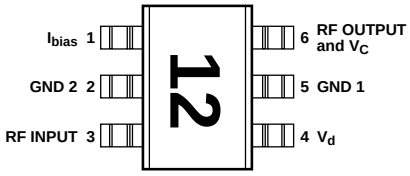
(Simplified)



Surface Mount Package SOT-363 (SC-70)



Pin Connections and Package Marking



Note:
Package marking provides orientation and identification.

Description

Hewlett-Packard's INA-12063 is a Silicon monolithic self-biased transistor amplifier that offers excellent gain and noise figure for applications to 1.5 GHz. Packaged in an ultra-miniature SOT-363 package, it requires half the board space of a SOT-143 package.

The INA-12063 is a unique RFIC that combines the performance flexibility of a discrete transistor with the simplicity of using an integrated circuit. Using a patented bias circuit, the performance and operating current of the INA-12063 can be adjusted over the 1 to 10 mA range.

The INA-12063 is fabricated using HP's 30 GHz f_{MAX} ISOSAT™ Silicon bipolar process which uses nitride self-alignment submicrometer lithography, trench isolation, ion implantation, gold metalization, and polyimide intermetal dielectric and scratch protection to achieve superior performance, uniformity, and reliability.

INA-12063 Absolute Maximum Ratings

Symbol	Parameter	Units	Absolute Maximum[1]
V_d	Supply Voltage, to Ground	V	7
V_c	Collector Voltage	V	7
I_c	Collector Current	mA	15
P_{in}	CW RF Input Power	dBm	13
T_j	Junction Temperature	°C	150
T_{STG}	Storage Temperature	°C	-65 to 150

Thermal Resistance[2]:
$\theta_{j\text{-}c} = 170°C/W$

Notes:
1. Operation of this device above any one of these limits may cause permanent damage.
2. $T_C = 25°C$ (T_C is defined to be the temperature at the package pins where contact is made to the circuit board).

Electrical Specifications, $T_C = 25°C$, $V_d = 3$ V, unless noted

Symbol	Parameters and Test Conditions		Units	Min.	Typ.	Max.	Std.Dev.[3]
G_P	Power Gain ($\|S_{21}\|^2$)	f = 900 MHz[1] f = 250 MHz[2]	dB	14.5	16 19		0.36
NF	Noise Figure	f = 900 MHz[1] f = 250 MHz[2]	dB		2.0 5.0	2.6	0.2
P_{1dB}	Output Power at 1 dB Gain Compression	f = 900 MHz[1] f = 250 MHz[2]	dBm		0 -7		
IP_3	Third Order Intercept Point	f = 900 MHz[1] f = 250 MHz[2]	dBm		15 2		
I_{dd}	Device Current[4]	900 MHz LNA[1] 250 MHz IF Amp[2]	mA		5 1.5	7	0.6

Notes:
1. See Test Circuit in Figure 32.
2. See Test Circuit in Figure 33.
3. Standard deviation number is based on measurement of at least 500 parts from three non-consecutive wafer lots during the initial characterization of this product, and is intended to be used as an estimate for distribution of the typical specification.
4. I_{dd} is the total current into Pins 1, 4, and 6 of the device, i.e. $I_{dd} = I_c + I_{bias} + I_d$.

INA-12063 Typical Performance, 900 MHz LNA (900 MHz Test Circuit, see Figure 32)

$T_C = 25°C, Z_O = 50\,\Omega, V_d = 3\,V, I_C = 5\,mA$, unless noted

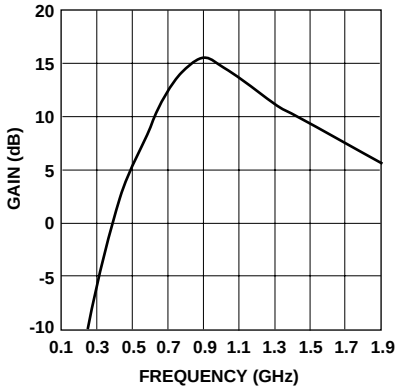


Figure 1. Gain vs. Frequency.

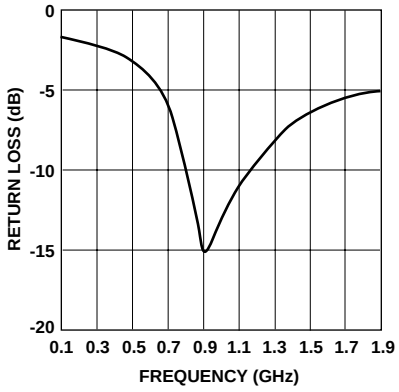


Figure 2. Input Return Loss vs. Frequency.

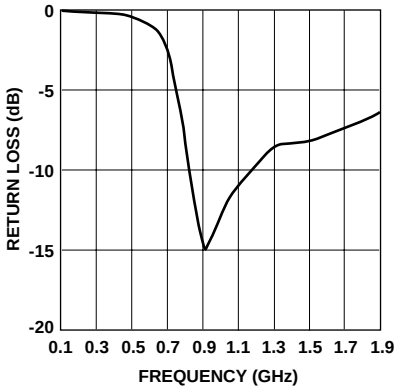


Figure 3. Output Return Loss vs. Frequency.

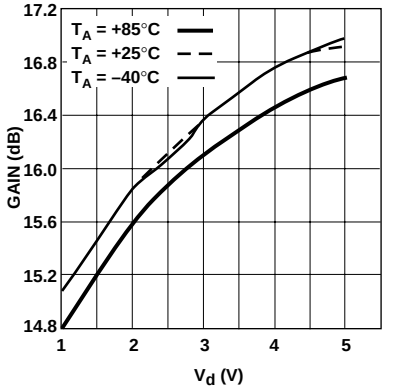


Figure 4. Gain at 900 MHz vs. Voltage and Temperature.

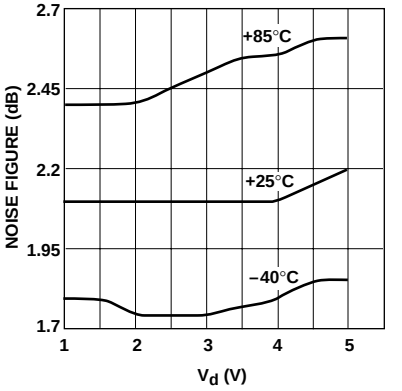


Figure 5. Noise Figure at 900 MHz vs. Voltage and Temperature.

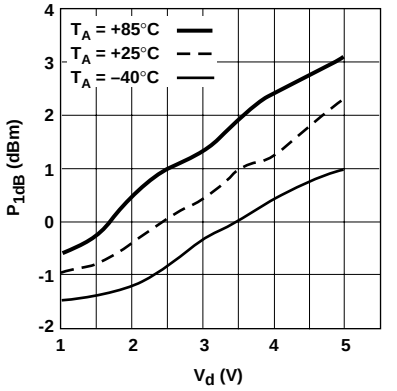


Figure 6. Output P_{1dB} at 900 MHz vs. Voltage and Temperature.

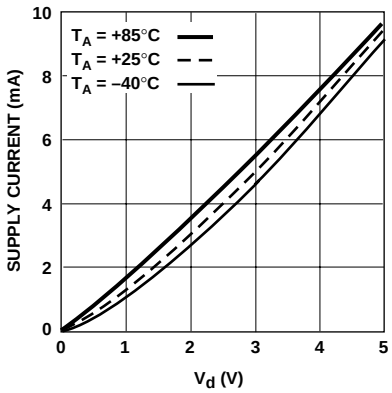


Figure 7. Supply Current vs. Voltage and Temperature.

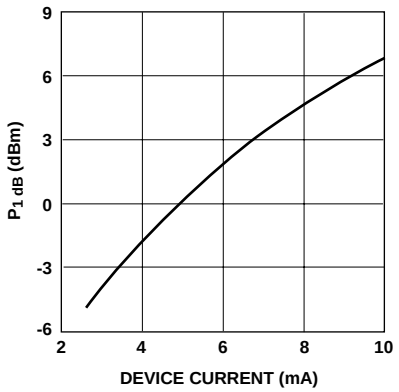


Figure 8. Output $P_{1\,dB}$ at 900MHz vs. Device Current for V_d = 3 V.

INA-12063 Typical Scattering Parameters[1], I_C = 1.5 mA

$T_C = 25°C, Z_O = 50\Omega, V_d = 3.0V$

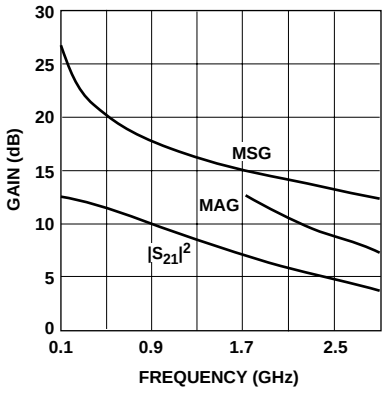
Freq.	S_{11}		S_{21}			S_{12}			S_{22}	
GHz	Mag.	Ang.	dB	Mag.	Ang.	dB	Mag.	Ang.	Mag.	Ang.
0.1	0.93	-8	12.6	4.26	172	-42.2	0.01	86	0.99	-3
0.2	0.92	-16	12.5	4.20	164	-36.2	0.02	79	0.99	-7
0.3	0.90	-24	12.3	4.11	157	-32.8	0.02	73	0.98	-10
0.4	0.89	-32	12.0	4.00	149	-30.5	0.03	69	0.96	-13
0.5	0.83	-38	11.7	3.83	141	-29.1	0.04	64	0.94	-16
0.6	0.79	-45	11.3	3.69	135	-27.9	0.04	60	0.93	-19
0.7	0.75	-52	10.9	3.49	128	-26.8	0.05	56	0.91	-21
0.8	0.72	-58	10.4	3.32	122	-26.1	0.05	53	0.89	-23
0.9	0.69	-64	10.1	3.18	116	-25.5	0.05	50	0.87	-26
1.0	0.65	-69	9.6	3.03	111	-24.9	0.06	47	0.86	-28
1.1	0.61	-74	9.2	2.89	106	-24.5	0.06	45	0.84	-30
1.2	0.59	-80	8.7	2.72	102	-24.2	0.06	43	0.83	-32
1.3	0.55	-84	8.4	2.64	97	-23.9	0.06	41	0.82	-34
1.4	0.52	-89	8.1	2.54	92	-23.6	0.07	40	0.81	-35
1.5	0.49	-94	7.7	2.43	88	-23.3	0.07	38	0.80	-37
1.6	0.47	-98	7.3	2.33	84	-23.2	0.07	36	0.79	-39
1.7	0.44	-103	7.0	2.23	80	-22.9	0.07	35	0.78	-40
1.8	0.42	-107	6.6	2.15	77	-22.9	0.07	35	0.77	-42
1.9	0.40	-112	6.4	2.08	73	-22.5	0.07	34	0.77	-44
2.0	0.38	-116	6.0	1.99	69	-22.3	0.08	33	0.76	-45
2.1	0.36	-120	5.7	1.93	66	-22.1	0.08	32	0.75	-47
2.2	0.34	-124	5.3	1.83	63	-22.0	0.08	29	0.74	-49
2.3	0.31	-129	5.2	1.82	59	-21.9	0.08	30	0.74	-51
2.4	0.31	-133	4.7	1.72	57	-22.0	0.08	29	0.73	-52
2.5	0.29	-137	4.6	1.70	54	-21.7	0.08	31	0.73	-54
2.6	0.28	-144	4.3	1.65	50	-21.4	0.08	30	0.73	-56
2.7	0.27	-149	4.1	1.60	47	-21.0	0.09	29	0.72	-58
2.8	0.25	-154	3.7	1.54	44	-20.7	0.09	27	0.71	-60
2.9	0.23	-156	3.5	1.50	41	-20.9	0.09	24	0.70	-61
3.0	0.24	-162	3.5	1.49	39	-21.0	0.09	28	0.71	-63

Note:

1. Reference plane per Figure 31 in Applications Information section.

Typical Noise Parameters @ 900 MHz, I_C = 1.5 mA

Fmin (dB)	Γ_{opt} Mag.	Γ_{opt} Ang.	R_N (Ω)
1.4	0.6	36	23



INA-12063 Typical Scattering Parameters[1], I_C = 2.5 mA

$T_C = 25°C, Z_O = 50\Omega, V_d = 3.0V$

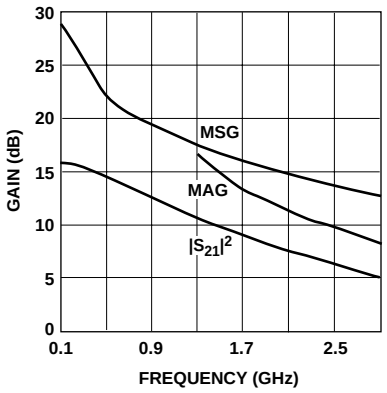
Freq.	S_{11}		S_{21}			S_{12}			S_{22}	
GHz	Mag.	Ang.	dB	Mag.	Ang.	dB	Mag.	Ang.	Mag.	Ang.
0.1	0.90	-10	16.0	6.33	171	-42.2	0.01	87	0.99	-4
0.2	0.88	-18	15.8	6.19	161	-36.2	0.02	79	0.98	-8
0.3	0.85	-27	15.5	5.98	153	-33.2	0.02	73	0.96	-11
0.4	0.82	-35	15.2	5.74	144	-31.1	0.03	68	0.94	-15
0.5	0.76	-42	14.6	5.37	135	-29.6	0.03	62	0.91	-18
0.6	0.71	-49	14.1	5.07	128	-28.4	0.04	59	0.90	-20
0.7	0.67	-56	13.5	4.73	122	-27.5	0.04	55	0.87	-23
0.8	0.62	-62	12.9	4.43	116	-26.6	0.05	53	0.85	-25
0.9	0.59	-67	12.4	4.18	110	-26.1	0.05	51	0.83	-27
1.0	0.54	-72	11.9	3.93	104	-25.6	0.05	49	0.82	-29
1.1	0.51	-76	11.4	3.71	100	-25.1	0.06	48	0.80	-30
1.2	0.49	-81	10.8	3.47	95	-24.8	0.06	46	0.79	-32
1.3	0.45	-84	10.4	3.31	91	-24.5	0.06	44	0.77	-34
1.4	0.42	-89	10.0	3.15	87	-24.1	0.06	44	0.76	-35
1.5	0.39	-93	9.5	2.98	83	-23.6	0.07	42	0.76	-37
1.6	0.37	-96	9.1	2.84	79	-23.5	0.07	41	0.74	-39
1.7	0.35	-100	8.7	2.72	76	-23.3	0.07	40	0.73	-40
1.8	0.33	-104	8.3	2.60	72	-23.0	0.07	41	0.73	-42
1.9	0.31	-108	8.0	2.51	69	-22.5	0.07	40	0.72	-43
2.0	0.29	-112	7.6	2.40	66	-22.2	0.08	40	0.72	-45
2.1	0.27	-115	7.3	2.31	62	-22.0	0.08	38	0.72	-47
2.2	0.25	-119	6.8	2.20	59	-21.8	0.08	36	0.71	-49
2.3	0.24	-122	6.6	2.15	56	-21.6	0.08	36	0.70	-50
2.4	0.23	-126	6.2	2.05	54	-21.7	0.08	36	0.69	-52
2.5	0.22	-131	6.1	2.01	51	-21.2	0.09	38	0.69	-53
2.6	0.20	-136	5.8	1.95	48	-20.7	0.09	36	0.69	-55
2.7	0.19	-142	5.5	1.89	45	-20.4	0.10	35	0.68	-57
2.8	0.18	-145	5.2	1.81	42	-20.0	0.10	32	0.68	-60
2.9	0.16	-146	4.9	1.75	39	-20.2	0.10	29	0.66	-60
3.0	0.17	-153	4.8	1.75	37	-20.1	0.10	32	0.68	-62

Note:

1. Reference plane per Figure 31 in Applications Information section.

Typical Noise Parameters @ 900 MHz, I_C = 2.5 mA

Fmin (dB)	Γ_{opt} Mag.	Γ_{opt} Ang.	R_N (Ω)
1.5	0.54	36	20



INA-12063 Typical Scattering Parameters[1], I_C = 5 mA

$T_C = 25°C, Z_O = 50\,\Omega, V_d = 3.0\,V$

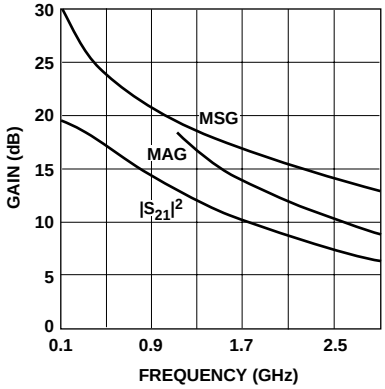
Freq.	S_{11}		S_{21}			S_{12}			S_{22}	
GHz	Mag.	Ang.	dB	Mag.	Ang.	dB	Mag.	Ang.	Mag.	Ang.
0.1	0.86	-11	19.6	9.56	168	-42.2	0.01	79	0.98	-5
0.2	0.82	-22	19.3	9.18	157	-36.8	0.01	73	0.96	-10
0.3	0.78	-31	18.7	8.65	146	-33.8	0.02	71	0.93	-13
0.4	0.73	-40	18.1	8.07	137	-31.7	0.03	68	0.90	-17
0.5	0.65	-46	17.3	7.34	128	-30.4	0.03	62	0.86	-20
0.6	0.59	-53	16.6	6.75	120	-28.7	0.04	61	0.85	-22
0.7	0.55	-59	15.8	6.18	114	-28.0	0.04	59	0.82	-24
0.8	0.50	-64	15.1	5.68	108	-27.2	0.04	56	0.80	-26
0.9	0.46	-68	14.4	5.26	103	-26.9	0.04	55	0.78	-27
1.0	0.43	-72	13.8	4.88	97	-26.3	0.05	52	0.77	-29
1.1	0.40	-76	13.2	4.55	93	-25.8	0.05	52	0.74	-30
1.2	0.37	-79	12.6	4.24	89	-25.3	0.05	52	0.74	-32
1.3	0.35	-81	12.0	3.99	85	-24.8	0.06	51	0.72	-34
1.4	0.33	-85	11.5	3.76	81	-24.3	0.06	50	0.72	-35
1.5	0.30	-87	11.0	3.55	78	-23.9	0.06	48	0.71	-36
1.6	0.28	-90	10.5	3.37	75	-23.5	0.07	48	0.70	-38
1.7	0.27	-94	10.1	3.21	71	-23.2	0.07	47	0.69	-39
1.8	0.25	-95	9.7	3.05	68	-22.9	0.07	48	0.69	-41
1.9	0.23	-99	9.3	2.93	64	-22.2	0.08	46	0.69	-42
2.0	0.22	-101	9.0	2.81	61	-22.0	0.08	45	0.68	-44
2.1	0.20	-104	8.5	2.67	58	-21.6	0.08	43	0.67	-45
2.2	0.18	-104	8.1	2.55	56	-21.3	0.09	41	0.67	-48
2.3	0.17	-107	7.8	2.47	53	-21.1	0.09	41	0.66	-50
2.4	0.17	-109	7.5	2.37	51	-20.8	0.09	41	0.66	-51
2.5	0.15	-114	7.3	2.31	48	-20.5	0.09	42	0.65	-53
2.6	0.14	-118	7.0	2.24	45	-20.0	0.10	40	0.66	-55
2.7	0.13	-123	6.7	2.17	42	-19.6	0.11	39	0.64	-56
2.8	0.12	-125	6.4	2.08	39	-19.3	0.11	36	0.63	-59
2.9	0.11	-126	6.1	2.02	37	-19.3	0.11	33	0.62	-59
3.0	0.11	-133	6.0	2.00	35	-19.3	0.11	35	0.64	-61

Note:

1. Reference plane per Figure 31 in Applications Information section.

Typical Noise Parameters @ 900 MHz, I_C = 5 mA

Fmin (dB)	Γ_{opt} Mag.	Γ_{opt} Ang.	R_N (Ω)
1.8	0.41	38	16



INA-12063 Typical Scattering Parameters[1], I_C = 8 mA

$T_C = 25°C, Z_O = 50\Omega, V_d = 3.0V$

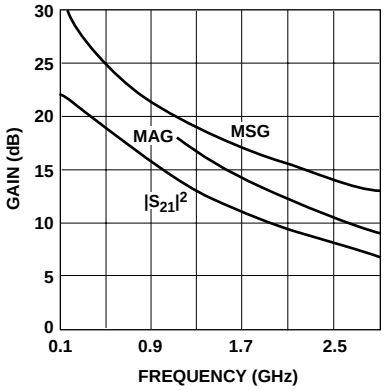
Freq.	S_{11}		S_{21}			S_{12}			S_{22}	
GHz	Mag.	Ang.	dB	Mag.	Ang.	dB	Mag.	Ang.	Mag.	Ang.
0.1	0.80	-13	22.3	12.97	166	-41.9	0.01	73	0.98	-5
0.2	0.76	-24	21.7	12.17	152	-37.4	0.01	72	0.94	-11
0.3	0.69	-35	20.9	11.10	141	-33.9	0.02	75	0.90	-15
0.4	0.63	-44	20.1	10.06	130	-32.2	0.02	69	0.86	-18
0.5	0.55	-49	19.0	8.89	121	-30.6	0.03	64	0.83	-21
0.6	0.50	-55	18.1	8.00	114	-29.6	0.03	64	0.80	-23
0.7	0.45	-59	17.1	7.20	107	-28.9	0.04	59	0.77	-24
0.8	0.41	-64	16.3	6.56	102	-28.0	0.04	59	0.76	-25
0.9	0.37	-67	15.6	6.02	97	-26.9	0.05	58	0.73	-26
1.0	0.34	-69	14.9	5.53	92	-26.5	0.05	58	0.71	-29
1.1	0.32	-72	14.1	5.08	88	-25.9	0.05	57	0.71	-30
1.2	0.30	-76	13.5	4.72	84	-25.4	0.05	56	0.70	-31
1.3	0.28	-76	12.9	4.40	81	-24.7	0.06	55	0.69	-33
1.4	0.26	-79	12.4	4.18	77	-24.1	0.06	53	0.68	-34
1.5	0.24	-82	11.7	3.86	74	-23.5	0.07	53	0.67	-36
1.6	0.23	-81	11.4	3.71	71	-23.4	0.07	52	0.65	-38
1.7	0.21	-84	10.8	3.48	68	-22.8	0.07	52	0.66	-39
1.8	0.20	-85	10.5	3.34	65	-22.7	0.07	51	0.66	-41
1.9	0.19	-89	9.9	3.14	62	-22.0	0.08	50	0.67	-42
2.0	0.17	-88	9.6	3.01	59	-21.5	0.08	48	0.66	-44
2.1	0.17	-91	9.2	2.89	56	-21.2	0.09	47	0.64	-45
2.2	0.15	-91	8.8	2.77	53	-21.0	0.09	44	0.63	-47
2.3	0.14	-93	8.6	2.68	51	-20.6	0.09	43	0.64	-49
2.4	0.14	-94	8.3	2.59	48	-20.4	0.09	43	0.64	-49
2.5	0.13	-98	8.0	2.51	47	-19.9	0.10	43	0.63	-51
2.6	0.12	-102	7.7	2.42	43	-19.5	0.11	42	0.61	-53
2.7	0.11	-103	7.3	2.32	40	-19.0	0.11	41	0.61	-56
2.8	0.10	-107	7.1	2.25	37	-18.6	0.12	38	0.61	-58
2.9	0.10	-101	6.7	2.17	36	-18.7	0.12	34	0.58	-60
3.0	0.09	-110	6.8	2.18	34	-18.7	0.12	35	0.61	-60

Note:

1. Reference plane per Figure 31 in Applications Information section.

Typical Noise Parameters @ 900 MHz, I_C = 8 mA

Fmin (dB)	Γ_{opt} Mag.	Γ_{opt} Ang.	R_N (Ω)
2.0	0.30	41	15



INA-12063 Applications Information

Introduction

The INA-12063 is a unique RFIC configuration that combines the performance flexibility of a discrete transistor with the simplicity of using an integrated circuit.

The INA-12063 is an integrated circuit that combines three functions: (1) a silicon bipolar RF transistor, (2) an RF feedback network, and (3) a patented[1] bias regulation circuit. A simplified schematic diagram of the INA-12063 is shown in Figure 9. The result is a versatile gain stage that can be operated from a single +1.5 to +5 volt power supply with the device current set by the user.

The INA-12063 is designed for use in battery powered equipment demanding high performance with low supply voltages and minimal current drain. Typical applications for the INA-12063 include low noise RF amplifiers, IF amplifiers, gain and buffer stages through 2 GHz. The INA-12063 is an excellent choice for use in cellular and cordless telephones, PCS, W/LAN's, RF modems and other commercial wireless equipment.

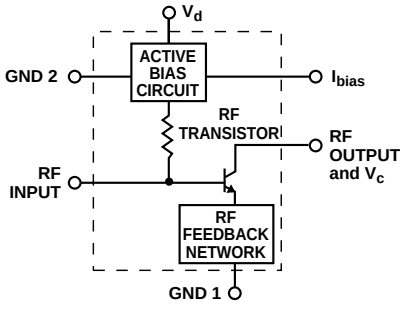


Figure 9. INA-12063 Schematic.

Description

The *active bias circuit* solves three problems normally encountered with traditional approaches for biasing discrete transistors. First, as an active bias circuit, the emitter of the RF transistor is DC grounded. This permits the collector current to be controlled without the need for resistors and/or bypass capacitors in the emitter that may degrade RF performance.

Second, the internal bias circuit greatly simplifies the design tasks commonly associated with biasing transistors, such as accurately regulating the collector current, allowing for variations in h_{FE}, making a non-intrusive DC connection to the base of the transistor, and stabilizing current over temperature.

And, third, the integrated bias circuit eliminates the cost, parts count, and associated PCB space required for as many as 8 additional DC components.

The integrated bias control circuit is very easy to use. For most applications, the collector current for the RF transistor can be set with a single resistor.

The geometry of the integrated *RF transistor* is designed to provide an excellent balance between low noise figure, high gain, and good dynamic range while retaining practical impedance matching levels. The operating current is typically in the 1 to 10 mA range.

The *integrated RF feedback* contains an inductive element in the emitter circuit of the RF transistor. This series feedback configuration is of the type often implemented in discrete transistor designs for the purpose of improving stability and bringing the optimum noise match at the input of the transistor closer to 50 Ω. The result is that for many applications, a simple, series inductor is often all that is needed to adequately match the input of the INA-12063 to 50 Ω.

In contrast to amplifiers that use resistive feedback to achieve broadband 50 Ω input and output matches, the INA-12063 leaves the designer with the flexibility of optimizing performance for a particular frequency band. For example, frequency selective input and output impedance matching circuits can be used to tune for optimum NF, maximum output power, low input VSWR, or to tailor the passband response to eliminate undesirable gain responses.

Setting the Bias Current

The integrated, active bias circuit is a 10:1 current mirror. The current mirror forces the collector current in the RF transistor to be approximately 10 times the current supplied to the I_{bias} pin.

In normal use, a voltage between +1.5 and +5 volts, is applied to both the V_d and V_c terminals of the INA-12063. Although normally connected to the same supply voltage, it is not necessary that both V_d and V_c be at the same voltage.

The collector current of the RF transistor is then set by injecting a small control current into the I_{bias} pin that is approximately 1/10 of the desired collector current.

[1] U.S. Patent Number 5436595

While there are any number of means of supplying the I_{bias} control current, the simplest way is to merely place a resistor between the V_d and I_{bias} terminals, shown as "R_{bias}" in Figure 10. R_{bias} will be sufficiently high to act as a current source. The value for R_{bias} is calculated as follows:

$$R_{bias} = 10\left(\frac{V_d - 0.8}{I_c}\right) \quad (1)$$

where V_d is the device voltage, I_c is the desired collector current, and R_{bias} is the value of the bias determining resistor. For example, for a desired collector current of 1.5 mA and a power supply of 2.7 volts, the value of R_{bias} would be 12.7 KΩ.

Power Down

A power-down function for the INA-12063 can be conveniently implemented by switching the I_{bias} current. This method has the advantage of switching only a very small current since I_{bias} is typically only a fraction of a mA.

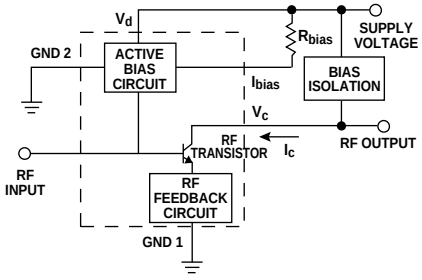


Figure 10. Single-Resistor Bias Circuit.

Amplifier Application Guidelines

This section describes the general approach for designing amplifiers using the INA-12063. This is a generic design approach and is applicable for most low noise RF or IF amplifiers or for general purpose gain and buffer stages.

The following "10-step" program is suggested as the design sequence:

1. Determine performance goals.
2. Select the bias condition.
3. Choose PCB material.
4. Check stability.
5. Determine required DC connections.
6. Design the input impedance matching network.
7. Design the output impedance matching network.
8. Layout the printed circuit board.
9. Computer optimization and performance verification.
10. Fabricate, assemble, and test.

Each of these steps in the design sequence will now be discussed in the following sections.

Step 1. Establish Performance Goals

The first step in the design of an INA-12063 amplifier stage is to establish performance goals. It may be necessary to consider performance tradeoffs between some amplifier parameters, such as Noise Figure, Input VSWR, Gain, Output Power, Output VSWR, Stability, and DC power consumption.

Some of these parameters are counterposed, for example, increased output power requires greater DC power consumption. The tradeoff decisions may require consideration of the choice of DC bias which is discussed in the next section. The final design will often be a balance between system-critical performance and those parameters of lesser significance.

Step 2. Choose Bias Conditions

The second step of the design process is to choose the bias conditions, i.e., the RF transistor operating voltage (V_c) and current (I_c). The bias conditions are chosen at this step in the design sequence since many of the RF design characteristics (e.g., S-parameters and noise parameters) are dependent on current and/or voltage.

The choice of bias *voltage* is often preemptive as it is normally fixed by available system resources, such as a battery voltage or system power supply. The INA-12063 will operate from supply voltages from 1.5 to 5volts, with +3 volts considered to be the typical operating voltage.

Although noise figure and gain are somewhat insensitive to device voltage as an independent variable, some increase in output power can be realized with higher device voltages.

The bias *current* has the greatest effect on RF performance and the following tradeoffs should be considered:

Noise Figure increases with device current. The data in the Typical Noise Parameter tables shows an increase in F_{min} of from 1.4 dB at 1.5 mA of bias current to 2.0 dB at 8 mA.

Gain – Transducer gain, $|S_{21}|^2$, increases significantly in proportion to device current.

Output Power – One of the benefits of increased device current is greater output power. A typical increase in current from 1.5 to 8 mA results in a corre-

sponding increase in P_{1dB} of -5.2 dBm to +4.6 dBm. The data sheet curve in Figure 8 characterizes the P_{1dB} - I_c tradeoff.

Impedance Match – While it is not a parameter per se, the degree of difficulty of impedance match may also be a consideration in the selection of bias current. Generally, the higher the device current, the less "severe" the impedance match, i.e., Γ_{opt}, Γ_{ms}, Γ_{ml} are all closer to 50 Ω.

Step 3. Selection of PCB Material

If the selection of PCB material has not been preordained by other factors (e.g., system standards) then it should be chosen at this stage of the design process. The printed circuit board material is chosen at this step since it will have an effect on the next step of the stability analysis and on the subsequent design of the impedance matching networks.

Key factors to consider in the selection of board material are dielectric constant, RF loss characteristics, board thickness, and cost.

The dielectric constant and board thickness together contribute to the physical geometry of the circuit, an important consideration for miniaturization. Higher dielectric constant material enables the construction of more compact circuits since the physical dimensions of transmission lines are smaller.

In addition to transmission line widths, PCB board thickness also influences the quality of ground vias. Ground vias in excessively thick PCBs result in high inductance paths to ground. For some active devices, poor grounding can result in performance degradation or reduced stability.

Dielectric loss is not a significant factor for the moderate frequency ranges over which the INA-12063 is normally used. Low loss, low dielectric constant "microwave" type materials are usually reserved for applications demanding the very lowest noise figures (minimum circuit loss) and/or for frequencies above 2GHz.

An overall good choice for most low cost wireless applications using devices such as the INA-12063 is a fiberglass-epoxy material such as FR-4 or G-10 with a thickness in the range of 0.020 to 0.031 inches.

Step 4. Stability Analysis

A stability analysis is the next step in the design process. The purpose of this step is to examine the circuit's tendency to oscillate. A linear CAD program, such as Hewlett-Packard's *Touchstone* should be used to calculate the stability factor, K, and stability measure, B1. The factors K and B1 are both derived from the S-parameters for the INA-12063 at the previously established bias voltage and current. The conditions for unconditional stability are:

$$K > 1 \text{ and } B1 > 0$$

While a simple analysis based only on the S-parameters is often adequate at this point, a slightly more rigorous analysis is recommended that includes the parasitic elements in the device's path to ground. At this stage in the design, a reasonable estimation (guess) of this electrical path and the construction of the ground vias are adequate. For the INA-12063, bear in mind that Pin 5 of the package is the critical connection for "RF" grounding. A typical RF path to ground consists of a short length of transmission line terminated in one or more ground vias. (The length of the PCB pad between the INA-12063 ground pin and the ground should be modeled as a microstripline ("MLIN" in *Touchstone*), and the plated through ground holes as "VIA" elements.)

When evaluating stability, it is a good practice to calculate K and B1 over the full frequency range for which S-parameters are available. The reason for this is that even though K and B1 may indicate stability over the frequency band of interest, the possibility exists for a circuit to oscillate at frequencies that are far outside of the band of interest.

While unconditional stability requires a positive, non-zero value of B1, most of the following stability analysis will focus on the K factor since the value of K indicates the degree of stability. What should the minimum value of K be to ensure stability? While K = 1.001 is stable, some margin is prudent to allow for component tolerances, temperature effects, and manufacturing variations. Typical rules of thumb suggest that K should be at least 1.2 to 1.5.

There are three possible cases resulting from the CAD analysis:

- *Case 1* – K > 1 over the entire frequency range.
- *Case 2* – K > 1 within the band of interest and K < 1 for some frequencies outside of the band of interest.
- *Case 3* – K < 1 within the band of interest.

If the CAD analysis indicates there is a potential instability issue ($K < 1$ and/or $B1 \leq 0$ for any frequency) as in Case 2 or Case 3 above, then some stability countermeasures will be needed.

There are four basic techniques for handling potential instability:

(a) Live with it. If the source and load impedances that will be presented to the amplifier are well defined, the finesse approach of using stability circles may be used. Stability circles (calculated by a program such as *Touchstone*) are plotted on a Smith chart and define regions of loads that could cause a circuit to oscillate. An amplifier is safe from oscillation if the expected amplifier terminations lie well outside of the unstable regions on both the input and output impedance planes. Since the possibility of oscillation could exist at any frequency for which the INA-12063 has gain, stability circles must be checked at frequencies over a wide frequency range when this method is used.

(b) Resistive feedback. The use of resistive feedback is often used to create stable, wideband, amplifiers. While effective in stabilizing active devices, this method will not be considered here since a significant penalty is often paid in degraded NF, less gain, and lowered output power performance.

(c) Lossless feedback. Reactive feedback elements can also be used to stabilize amplifiers. The INA-12063 already incorporates one type of reactive feedback in the emitter of the RF transistor, with a resulting improvement in stability. Further use of the lossless feedback technique is not suggested for most INA-12063 amplifier applications since this method adds considerable design complexity as well as additional parts count and board space to the circuit.

(d) Resistive loading. Resistive loading can be used at either the input or output of the INA-12063 to create an unconditionally stable amplifier. This is the brute-force method of ensuring stability. It is fairly fail-safe and is also the simplest to implement. The addition of a resistive element to either the amplifier input or output creates RF loss which manifests itself as lower gain plus either increased NF (if the resistance is added to the input) or lower output power (if the resistance is placed at the output.)

In keeping with the goals of low cost (i.e., circuit simplicity), the resistive loading method is the technique suggested for producing an unconditionally stable amplifier for most applications of the INA-12063.

The resistive loading can be applied in either series or shunt and can be added to either the input or output of the amplifier. The choice of series or shunt resistive load may be dictated by whether the real part of the output impedance of the amplifier device is greater or less than 50 Ω. The logical choice is to use a shunt resistor when the amplifier impedance is >50 Ω and a series resistor for the case of >50 Ω. This technique will bring the overall impedance closer to 50 Ω, thus simplifying the match. In some cases, excessive voltage drop across the stabilizing resistor due to the DC current into the device may preclude the use of the series configuration. Shunt resistance is usually the most straightforward solution to implement since it can be easily bypassed to ground with a capacitor without disturbing the bias.

For gain or buffer stages requiring maximum output power, the loading is applied to the amplifier input. If the performance goal is low noise figure, the resistive loading is implemented on the output side of the INA-12063 as shown in Figure 11.

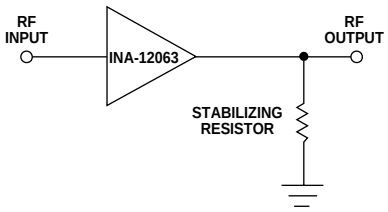


Figure 11. Shunt Stabilizing Resistor for LNA.

A simple manual optimization may be used to determine a starting value for the stabilizing resistor. By adding a shunt resistor to the output of the INA-12063 in the circuit file used in the previous stability analysis, K may be observed while adjusting the value of the resistor. The shunt resistor should be the highest value that will adequately stabilize the circuit.

The three possible cases resulting from the stability analysis will now be considered.

Case 1 ($K > 1$ over the entire frequency range) is always the hoped for situation since it is the easiest to deal with. If K is greater than unity by a comfortable margin, then no further action is needed at this point.

Case 2 (K>1 within the band of interest; K<1 for some frequencies outside of the band of interest) is the next simplest case to handle. Since K>1 in the band of interest, little or no performance tradeoffs may be needed to make the amplifier unconditionally stable.

By using R-C or R-L combinations, frequency selective resistive loading can be applied only over the frequency range for which K < 1 in order to stabilize the amplifier without adversely affecting in-band performance.

Case 3 (K<1 in the band of interest) requires tradeoffs in NF or output power to achieve an unconditionally stable amplifier stage.

The INA-12063 typically falls into either Case 2 or Case 3, depending on the bias current, circuit grounding, and frequency band of interest.

In all cases, a final check of stability should be done in the analysis of the completed amplifier design. This is done as part of Step 9 in the design sequence.

Step 5. DC Connections
The DC connections to the INA-12063 are considerations in the next two steps in which the input and output impedance matching networks are chosen. The goal is economy of components by integrating as many of the DC connections into the matching circuits as practical. For example the use of a series C in an impedance matching network could double as a DC blocking capacitor. Or, a shunt L can be used to apply the required supply voltage to the output of the INA-12063.

One of the advantages of the active bias circuit in the INA-12063 is that there is no need for an external DC bias connection to the RF Input. If desired, the input may be connected directly to matching networks using a series capacitor as the first element.

Pins 4 and 6 are connected to the supply voltage and Pins 2 and 5 are DC grounded. Pins 1 and 4 should be bypassed to ground. A high value resistor from Pin 1 to Pin 6 is a simple and convenient method for setting the device operating current. Pin 3, has an internal voltage present and is normally connected to a DC blocking capacitor. The only DC connection which could affect RF performance is that of applying the supply voltage to the RF Output pin.

Step 6. Designing the Input Match
The input impedance match is generally designed to achieve either of two goals, either lowest noise figure or maximum power transfer. The maximum power transfer match provides maximum gain and corresponds to minimum VSWR. In some cases, noise circles in combination with constant gain circles are used to design an intermediate match point to achieve a compromise in performance between low noise figure and low input VSWR.

If the design goal is to obtain lowest NF, the input of the INA-12063 is matched to the conjugate of Γ_{opt}. Γ_{opt} is the reflection coefficient of the source termination that results in F_{min}, the lowest possible device noise figure. Γ_{opt} design data are found in the tables of Typical Noise Parameters. Alternatively Γ_{opt} can be calculated using the same CAD circuit file used in the stability analysis in Step 4 above. This method is slightly more accurate since it takes the feedback effects of device grounding and stabilization components into account.

If the design goal is to obtain maximum power transfer (maximum gain/minimum input VSWR), then the input of the INA-12063 is matched to Γ_{ms}. Γ_{ms} is the source impedance resulting from the simultaneous conjugate match of the input and output of the device. Since Γ_{ms} is only defined for devices/circuits with K > 1, the CAD circuit file from design Step 4, including any stabilizing resistors, is used to calculate Γ_{ms}.

For most communication systems operating over relatively small bandwidths, a single frequency match approach is usually adequate. As a general rule, the selection of high pass networks for the input (and output) matching circuits is desirable to reduce excess gain at low frequencies.

As a final note in the choice of the input matching structure, the use of a series C element is possible at the input of the INA-12063 since the internal bias circuit obviates the need for an external DC connection to the input.

The choice of using either lumped element or distributed (transmission line) matching elements is mainly dictated by size and frequency constraints as well as by cost considerations. While distributed elements are “free” since they are etched onto the PCB, they usually use more board space than an equivalent lumped element (chip) component.

Before proceeding to the next step, circuit stability and out-of-band gain should be re-checked.

Step 7. Designing the Output Match

The output of the INA-12063 is normally matched for maximum power transfer (maximum gain and lowest output VSWR.) Maximum power transfer occurs when the output is matched to the conjugate of Γ_{ml}. Γ_{ml} is computed from the same CAD circuit file as used for determining Γ_{ms} in the design of the input matching network in the previous step. A typical LNA is matched for Γ_{opt} at the input and Γ_{ml} at the output.

Note: The small signal match for maximum power transfer should not be confused with matching the output of the INA-12063 for the *highest* output power. As output power is increased, the device becomes nonlinear resulting in a shift away from the Γ_{ml} match. While various load pull types of measurements exist to determine the optimum impedance match for maximum output power under nonlinear conditions, these tests are fairly tedious and an empirical tuning approach is often more expedient to arrive at a solution. The Γ_{ml} match may be used as a starting point in tuning for maximum output power.

The same comments regarding single frequency match, high pass networks, and lumped vs. distributed elements referred to in the input matching step above are applicable to the output matching circuit.

Once again, out-of-band gain and stability should be checked.

Step 8. RF Layout

Up to this point, we have completed the RF electrical design, the choice of circuit board material, and the DC circuit. The next step is to lay out the printed circuit board. While the layout is not critical, some precautions should be considered.

A recommended PCB pad layout for the miniature SOT-363 (SC-70) package used by the INA-12063 is shown in Figure 12 (dimensions are in inches). This layout provides ample allowance for package placement by automated assembly equipment without adding parasitics that could impair the high frequency RF performance of the INA-12063. The layout is shown with a footprint of a SOT-363 package superimposed on the PCB pads for reference.

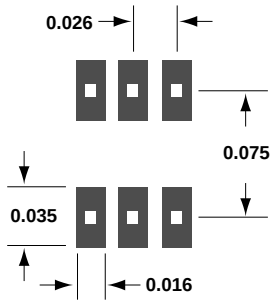


Figure 12. PCB Pad Layout for INA-12063 Package (dimensions in inches).

Starting with the package pad layout in Figure 12, an RF layout similar to the one in Figure 13 is suggested as a starting point for the INA-12063 amplifier.

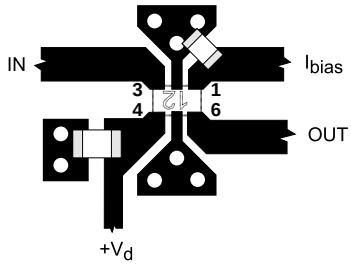


Figure 13. RF Layout.

This layout shows the direct grounding of Pin 5 (the device RF ground) which should be connected to ground through as short a path as practical, unless additional shunt feedback is desired. Capacitive bypasses should be placed on the DC connections at Pins 1 and 4 to prevent possible feedback and/or oscillation in the active bias circuit. Multiple vias are used to ensure good RF grounding.

It is recommended that the PCB pads for the two ground pins *not* be connected together. Each ground pin should have its own separate path to ground, otherwise, unintentional feedback could lead to potential instability in the RF transistor or internal bias circuit.

Step 9. Final CAD Analysis and Optimization

Following the completion of the amplifier electrical design and layout, it is advisable to do a final CAD analysis and circuit optimization. The analysis at this point will take into account such things as component parasitics (e.g., series L in chip caps), actual transmission line dimensions and interconnections, effects of ground vias, etc.

The circuit should be analyzed over the full range of the provided S-parameters to re-verify amplifier stability and ensure well-behaved out-of-band performance. With the full circuit parasitics and losses taken into account, it may be necessary to adjust the value of the shunt stabilizing resistor.

The results of this final analysis and optimization are then used to make final adjustments to component values and the PCB layout as

well as to ensure that the performance goals in Step 1 will be met.

Step 10. Build and Test
The final step is to fabricate circuit boards and assemble amplifiers for testing and verification of performance. Some adjustment in component values and transmission lines may be done at this step to allow for imperfections in the computer simulation. This completes the amplifier design.

900 MHz LNA Design Example
As an application example, the design of a low noise amplifier stage for 900 MHz using the INA-12063 will be described. This amplifier design would be representative for use in many low-cost, battery power receiver applications such as LNAs for cellular telephones or 900 MHz ISM/spread spectrum systems.

This example will follow the above design sequence.

1. Performance goals. As a receiver front end stage, the primary design goals for this example amplifier are: (1) noise figure less than 2 dB, and, (2) a input 3rd order intercept (IP_3) point of at least -10 dBm. Secondary goals are low output VSWR and minimum DC current drain. The resulting input VSWR and stage gain will be accepted. Low cost is always a design goal.

Results of this step:

Constrain:

NF ≤ 2 dB
Input IP_3 ≥ -10 dBm
Low cost

Optimize:

Minimize output VSWR
Minimize DC power

Accept:

Gain
Input VSWR

2. Select bias conditions. For this example, the supply voltage is constrained by an assumed battery supply of 3 volts, leaving device current as the only remaining bias variable. The current is selected based on output power which is driven by the IP_3 requirement. The table of Electrical Specifications provides a starting point. Using the typical gain of 16 dB and a difference of 15 dB between the output IP_3 and P_{1dB}, the design goal of an input 3rd order intercept point of -10 dBm is translated to a 1-dB compressed output power requirement of -9 dBm. Figure 8 indicates a current of 2.5 mA will meet this P_{1dB} requirement with adequate design margin.

Results of this step:

Bias: 3 volts, 2.5 mA

3. Choose PCB material. FR-4 with a thickness of 0.031 inches is chosen as the printed circuit board material. FR-4 meets the requirement of low cost while providing acceptable low loss performance at 900 MHz.

A thickness of 0.031 inches is suitable for the miniaturization of microstriplines and thin enough to allow for low inductance ground vias. With a relative dielectric constant (ε_r) of 4.8, the width of a 50 Ω microstripline on 0.031 inch FR-4 is 0.056 inches, which is a convenient size for mounting chip components.

Results of this step:

PCB Material: 0.031-inch FR-4

4. Evaluate stability. Stability factor is calculated from the set of S-parameters closest to the chosen bias condition, which in this example is 3 volts and 2.5 mA. For the required accuracy in the stability analysis, a short length of transmission line (0.030-inch long, 0.015-inch wide) is added to connect the RF ground pin (Pin 5) of the INA-12063 to a 0.025-inch diameter ground via.

Hewlett-Packard's *Touchstone* CAD program was used to calculate the stability factor (K), stability measure (B1), and gain over the full S-parameter frequency range of 0.1 to 3.1 GHz. The results show a value of K < 1 at 900 MHz, corresponding the "Case 3" situation described in the stability discussion in design Step 4 above. To preserve NF, the stabilizing resistor, R1, shown in Figure 14, was added from the output of the INA-12063 to ground. Since the real part of the output impedance of the INA-12 is > 50 Ω, a resistor in the shunt configuration is used to move the overall impedance closer to 50 Ω.

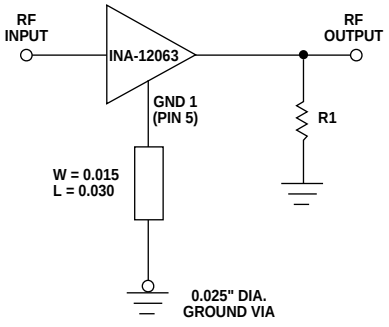


Figure 14. Stabilizing Resistor on Output.

The *Touchstone* circuit file for this step is shown in Figure 15.

```
DIM
  FREQ GHZ
  RES  OH
  LNG  IN
CKT
  MSUB ER=4.8 H=0.031
       T=0.001 RHO=1 RGH=0
  S2P  1  2  3  TYP25B.S2P
  MLIN 3  4  W=0.015 L=0.030
  VIA  4  0  D1=0.025
       D2=0.025 H=0.031
       T=0.001
  RES  2  0  R=600  ! R1
  DEF2P  1  2  INA12
TERM
   Z0 = 50
OUT
  INA12   K
  INA12   B1
  INA12   DB[S21]
  INA12   DB[GMAX]
!  INA12   MAG[GMN]
!  INA12   ANG[GMN]
!  INA12   MAG[GM2]
!  INA12   ANG[GM2]
FREQ
  SWEEP  0.1  3.1   0.1
```

Figure 15. CAD File for Stability Analysis and Conjugate Match.

The value of the shunt resistor, R1, is varied while observing the resulting K. While a 600 Ω resistor is found to stabilize the circuit at 900 MHz (K = 1.46), there still exists a possibility of oscillation at 100 MHz with the worst case value of K = 0.72. There are two options at this point: (a) lower the value of the shunt resistor, which trades additional stability for circuit gain and output power, or (b) use a frequency selective circuit to resistive load the device only at lower frequencies.

In the interest of circuit simplicity (meeting the objective of low cost) the shunt resistor value was lowered to 290 Ω. This value resulted in a K > 1 over the full frequency range at a trade-off in gain of 1.7 dB. (The stability measure criteria, B1 > 0, was also verified.)

Results of this step:

A 290 Ω shunt resistor was added to the output of the INA-12063 for stability.

5. Allow for DC connections. The required DC connections to be made to this example amplifier are: +3 volts to the RF Output and V_d terminals (Pins 4 & 6), a suitable bias current into I_{bias} (Pin 1), and Pins 2 and 5 to ground. The RF Input (Pin 3) and RF Output should have blocking capacitors if the amplifier is to be cascaded with stages that do not have a DC open circuit.

To set the INA-12063 operating current to 2.5 mA, a 9.1 K Ω resistor will be connected between the +3 volt supply and the I_{bias} pin. The DC schematic for the LNA is shown in Figure 16.

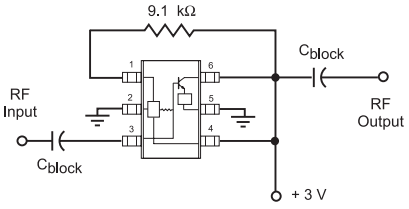


Figure 16. 900 MHz LNA DC Schematic.

Results of this step:

The DC connections were identified and will be considered in choosing the input & output matching circuits.

6. Design of the input impedance matching network. Commensurate with the primary design objective of low noise figure, the 50 Ω input to the amplifier stage will be matched to the conjugate of Γ_{opt}. The value of Γ_{opt}, $0.53 \angle +36°$, is found in the table of Typical Noise Parameters for a bias current of 2.5 mA. (Alternatively, a slightly more accurate Γ_{opt} could also have been calculated using the CAD circuit file in Figure 15, which includes the RF ground parasitics and stabilizing resistor.) The conjugate of Γ_{opt}, $0.53 \angle -36°$, is plotted on the Smith chart as Point A in Figure 17. Since Point A is not sufficiently close to the R = 1 or G = 1 circles on the Smith chart, a single series or shunt element will not provide an exact match. (For less critical NF performance, a simple series inductor would be adequate for the input match.) A two-element matching network will therefore be required.

Impedances in this region of the Smith chart can be matched to 50 Ω by either of two possible L-C combinations, either a shunt C-series L or a shunt L-series C. Normally, the shunt L-series C would be a good choice since its high pass filter characteristic would help roll off excess low end gain. However, a DC blocking capacitor would be required between the INA-12063 and the matching network. Placing extraneous components within matching network is usually not recommended. The shunt C-series L network is therefore chosen as the input matching topology.

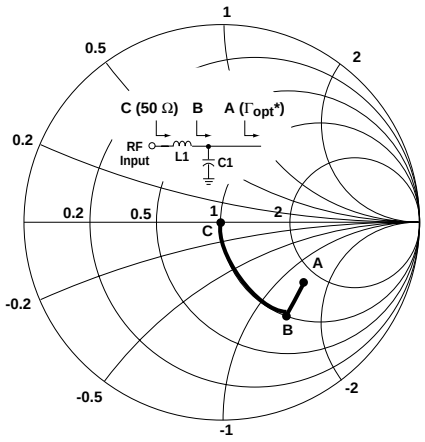


Figure 17. Input Impedance Match.

As shown in Figure 17, a shunt capacitor of 0.59 pF will move Γ_{opt} * at Point A to a position on the unit conductance circle (G=1) at Point B. A 11.2 nH series inductor then completes the match to 50 Ω by moving the impedance at Point B to the center of the chart.

The value of the shunt capacitor is small enough that a short length of open-circuit transmission line could be used in place of the lumped element capacitor. This saves the expense of a chip component with the tradeoff of a small amount of additional circuit board space. A 0.20-inch length of open-circuit 50 Ω line is one choice that would be equivalent to the 0.59 pF shunt capacitor. The input matching circuit is shown in Figure 19.

Results of this step:

The input circuit is:

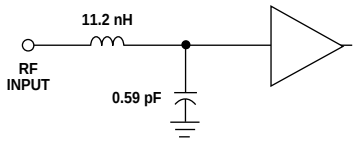


Figure 18. Input Circuit.

7. Design of the output impedance matching network. Using the circuit file from step 4 (Figure 15), *Touchstone* was used to calculate the load impedance Γ_{ml} (0.62 ∠+35°) of the INA-12063 to achieve maximum power transfer. The conjugate of Γ_{ml}, Γ_{ml}* (0.62 ∠-35°), is plotted as Point A on the Smith chart in Figure 19.

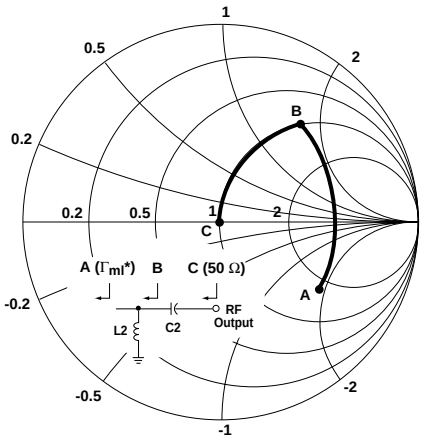


Figure 19. Output Impedance Match.

The two possible L-C networks that can be used to match Γ_{ml}* to 50 Ω are either a shunt C-series L or a shunt L-series C circuit. By choosing the shunt L-series C circuit, two of the DC considerations from Step 5 can be satisfied: the shunt L can be bypassed and used to apply the +3 volt supply to the RF output terminal, and the series C will serve double duty as the DC blocking capacitor.

Referring again to Figure 19, a shunt inductance of 10.8 nH moves Γ_{ml}* at Point A to Point B which is on the G1 circle of the Smith chart. The addition of 1.9 pF of series capacitance completes the impedance transformation to Point C at the center of the chart. The output matching circuit is shown in Figure 20.

Results of this step:

The output circuit is:

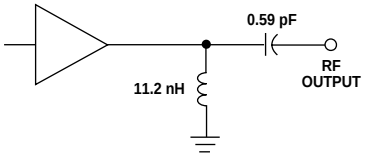


Figure 20. Output Circuit.

The circuit values from this step and from Step 6 will be used as a starting point to be refined in Step 9 when the circuit is expanded to take practical interconnections and parasitics into account.

8. PCB Layout. The results of the preceding steps and the PCB layout guidelines in design Step 8 were used to draft the circuit board layout shown in Figure 21. Since parasitic effects are minimal, the current source resistor, R2, can be conveniently placed directly from the RF output to the I_{bias} connection. A bypass capacitor is added to the shunt stabilizing resistor, R1 and matching inductor, L2, on the output. A DC blocking capacitor, C1, is included at the input to complete the amplifier.

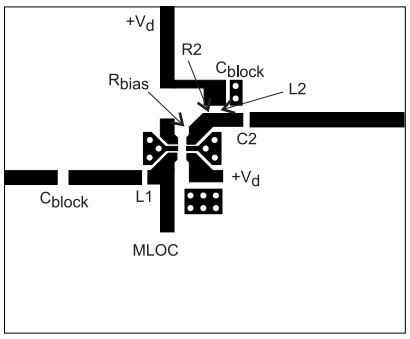


Figure 21. PCB Layout of 900 MHz LNA.

Results of this step:

PCB layout completed.

9. Final CAD simulation and optimization. With reference to Figure 21 the CAD circuit file from step 4 is embellished to include the effects of component mounting pads, lengths of transmission lines used to interconnect components, ground vias, bypass and blocking capacitors, etc. (Since 900 MHz is a fairly moderate frequency, extremely fine detail is not required.)

Using the previous element values for the matching circuits as a starting point, *Touchstone* was used to optimize the circuit for noise figure and output match, which were the primary design goals from Step 1. The input and output matching elements were used as variables for the optimization. Following the optimization, the value of the stabilizing resistor, R1, was also reviewed and it was found that an increase to 330 Ω was sufficient to make K>1 over the entire frequency range of the S-parameters. The *Touchstone* circuit file for the complete amplifier is shown in Appendix A and the simulation results in Appendix B.

The schematic for the complete INA-12063 amplifier circuit is shown in Figure 22.

A final simulation using optimized component values predicted performance of the amplifier at 900 MHz to be:

NF = 1.6 dB
Gain = 13.4 dB
MAG = 14.1 dB
Input RL = 8.4 dB
Output RL = 31 dB

Results of this step:

Optimization of circuit and verification of performance goals.

10. Assemble and test. A circuit based on the PCB layout was assembled using components with standard values that were closest to those resulting from the circuit optimization.

The test results compared well with the computer simulations from the previous step. For this particular circuit, it was determined experimentally that less shunt capacitance was required at the input than predicted by the CAD analysis. As a result, the shunt, open circuit stub near Pin 3 was shortened to tune the circuit for minimum noise figure. The final LNA is shown in Figure 23.

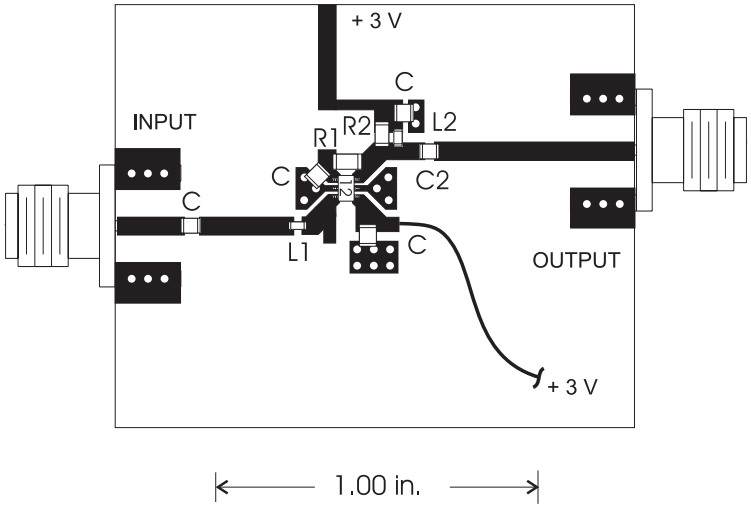


Figure 23. Completed 900 MHz LNA.

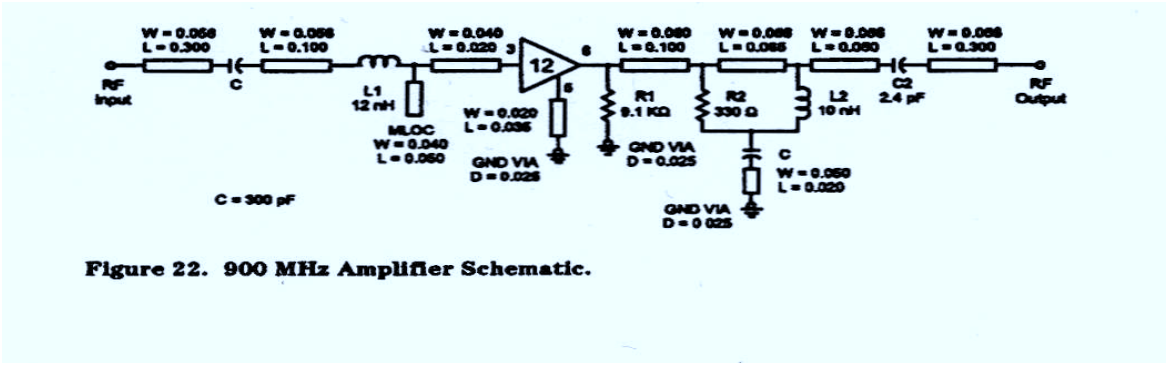


Figure 22. 900 MHz Amplifier Schematic.

Actual, measured test results are shown in Figures 24 through 28. Output power for 1 dB of gain compression (P_{1dB}) at 900 MHz was measured as -4.6 dBm.

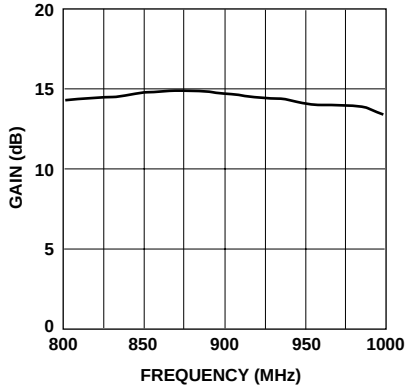


Figure 24. Measured Gain of Example 900 MHz LNA.

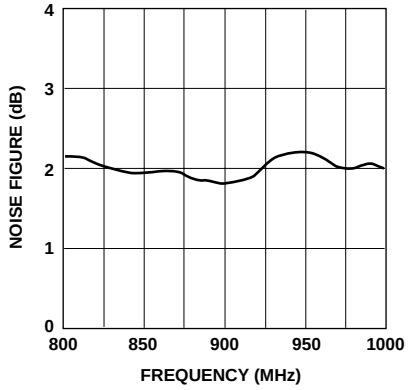


Figure 25. Measured Noise Figure of Example 900 MHz LNA.

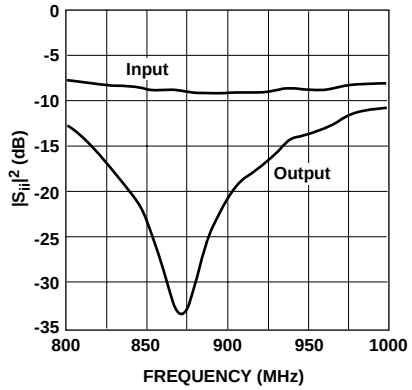


Figure 26. Measured Input and Output Return Loss of Example 900 MHz LNA.

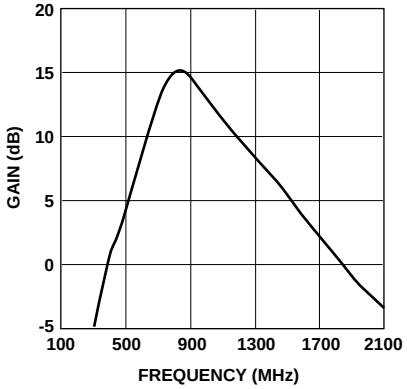


Figure 27. Measured Gain of Example 900 MHz LNA for Extended Frequency.

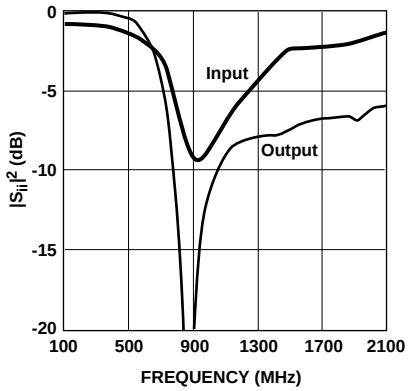


Figure 28. Measured Input and Output Return Loss of Example 900 MHz LNA for Extended Frequency.

Results of this step:
A prototype circuit was built and performance goals verified by measurement. The following 900 MHz data was measured on the example LNA:

NF = 1.9 dB
Gain = 14.7 dB
P_{1dB} (output) = -4.6 dBm
Input Return Loss = 9.6 dB
(Input VSWR = 2.0 : 1)
Output Return Loss = 20.4 dB
(Output VSWR = 1.2 : 1)
DC Power = 8 mW
(3 volts, 2.55 mA)

Hints and Troubleshooting

• Oscillation

Even though a design may be unconditionally stable (K > 1 and B1 > 0) over its full frequency range, other possibilities exist that may cause an amplifier circuit to oscillate. One thing to look for, is oscillation in bias circuits. It is important to capacitively bypass the connections to active bias circuits to ensure stable operation. In multistage circuits, feedback through bias lines can also lead to oscillation.

Components of insufficient quality for the frequency range of the amplifier can sometimes lead to instability. Also, component values that are chosen to be much higher in value than is appropriate for the application can present a problem. In both of these cases, the components may have reactive parasitics that make their impedances very different than expected. Chip capacitors may have excessive inductance, or chip inductors can exhibit resonances at unexpected frequencies.

In systems with high gain cascades, another possible feedback path that could lead to oscillation is radiation. Feedback via radiation is most frequently encountered in situations where a large cavity housing is used in combination with multiple gain stages. One solution to minimizing radiation feedback is to design the housing so that it is well below its equivalent waveguide cutoff frequency. Another solution is to use shielding to partition the gain.

• A Note on Supply Line Bypassing

When multiple bypass capacitors are used throughout the power supply lines in a wireless system, consideration should be given to potential resonances. It is important to ensure that the capacitors, when combined with additional parasitic L's and C's on the circuit board, do not form resonant circuits. The addition of a small value resistor in the bias supply line between bypass capacitors will often "de-Q" the bias circuit and eliminate resonance effects.

SMT Assembly

Reliable assembly of surface mount components is a complex process that involves many material, process, and equipment factors, including: method of heating (e.g., IR or vapor phase reflow, wave soldering, etc.) circuit board material, conductor thickness and pattern, type of solder alloy, and the thermal conductivity and thermal mass of components. Components with a low mass, such as the SOT-363 package, will reach solder reflow temperatures faster than those with a greater mass.

The INA-12063 is has been qualified to the time-temperature profile shown in Figure 29. This profile is representative of an IR reflow type of surface mount assembly process.

After ramping up from room temperature, the circuit board with components attached to it (held in place with solder paste) passes through one or more preheat zones. The preheat zones increase the temperature of the board and components to prevent thermal shock and begin evaporating solvents from the solder paste. The reflow zone briefly elevates the temperature sufficiently to produce a reflow of the solder.

The rates of change of temperature for the ramp-up and cool-down zones are chosen to be low enough to not cause deformation of the board or damage to components due to thermal shock. The maximum temperature in the reflow zone (T_{MAX}) should not exceed 235°C.

These parameters are typical for a surface mount assembly process for the INA-12063. As a general guideline, the circuit board and components should be exposed only to the minimum temperatures and times necessary to achieve a uniform reflow of solder.

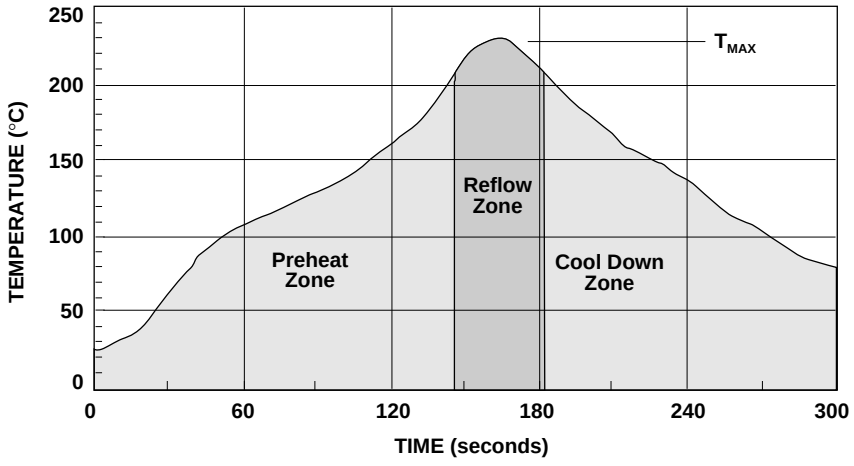


Figure 29. Surface Mount Assembly Profile.

Statistical Parameters

Several categories of parameters appear within this data sheet. Parameters may be described with values that are either minimum or maximum, "typical," or standard deviations.

The values for parameters are based on comprehensive product characterization data, in which automated measurements are made on of a minimum of 500 parts taken from 3 non-consecutive process lots of semiconductor wafers. The data derived from product characterization tends to be normally distributed, e.g., fits the standard bell curve.

Parameters considered to be the most important to system performance are bounded by *minimum* or *maximum* values. For the INA-12063, these parameters are: Power Gain ($|S_{21}|^2$), Noise Figure (NF), and Device Current. Each of these guaranteed parameters is 100% tested.

Values for most of the parameters in the table of Electrical Specifications that are described by *typical* data are the mathematical mean (μ), of the normal distribution taken from the characterization data. For parameters where measurements or mathematical averaging may not be practical, such as S-parameters or Noise Parameters and the performance curves, the data represents a nominal part taken from the center of the characterization distribution. Typical values are intended to be used as a basis for electrical design.

To assist designers in optimizing not only the immediate circuit using the INA-12063, but to also optimize and evaluate trade-offs that affect a complete wireless system, the *standard deviation* (σ) is provided for many of the Electrical Specifications parameters (at 25°C) in addition to the mean. The standard deviation is a measure of the variability about the mean. It will be recalled that a normal distribution is completely described by the mean and standard deviation.

Standard statistics tables or calculations provide the probability of a parameter falling between any two values, usually symmetrically located about the mean. Referring to Figure 30 for example, the probability of a parameter being between $\pm 1\sigma$ is 68.3%; between $\pm 2\sigma$ is 95.4%; and between $\pm 3\sigma$ is 99.7%.

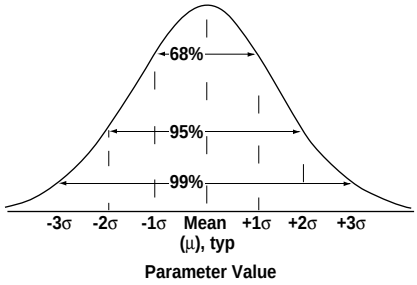


Figure 30. Normal Distribution.

Phase Reference Planes

The positions of the reference planes used to specify S-parameters and Noise Parameters for the INA-12063 are shown in Figure 31. As seen in the illustration, the reference planes are located at the point where the package leads contact the test circuit.

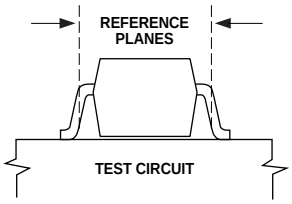


Figure 31. Phase Reference Planes.

Test Circuits

The test circuit shown in Figure 32 is used for 100% testing of the guaranteed RF and DC parameters that are shown in the Table of Electrical Specifications.

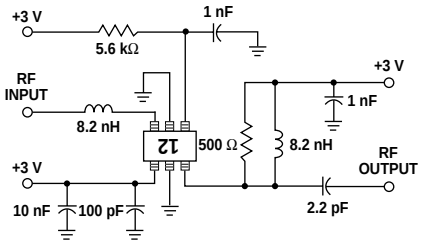


Figure 32. 900 MHz Test Circuit.

The test circuits in Figures 32 and 33 were used to generate the characterization data and performance curves for 900 MHz and 250 MHz.

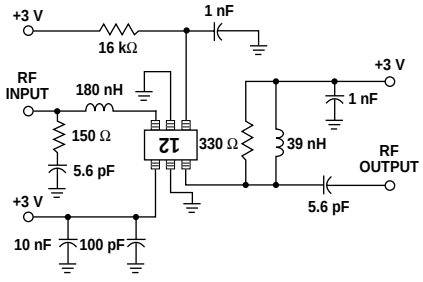


Figure 33. 250 MHz Test Circuit.

Electrostatic Sensitivity

RFICs are electrostatic discharge (ESD) sensitive devices. Although the INA-12063 is robust in design, permanent damage may occur to these devices if they are subjected to high energy electrostatic discharges. Electrostatic charges as high as several thousand volts (which readily accumulate on the human body and on test equipment) can discharge without detection and may result in degradation in performance, reliability, or failure.

Electronic devices may be subjected to ESD damage in any of the following areas:

- Storage and handling
- Inspection and testing
- Assembly
- In-circuit use

The INA-12063 is a ESD Class 1 device. Therefore, proper ESD precautions are recommended when handling, inspecting, testing, assembling, and using these devices to avoid damage.

The in-use aspect of potential ESD damage is sometimes overlooked. One such example of possible damage is in the use of an ESD sensitive device as the front-end LNA stage in personal communication equipment, such as cellular telephones, PCS, or RF modems.

The input to receiver LNAs are frequently connected to external antennas that are subject to human contact and exposure to other potentially damaging levels of ESD. If this type of condition exists, some type of circuit protection may be needed. One simple method of preventing ESD damage is to add a DC return path (e.g., a shunt inductor) to the input of the receiver. This type of protection may be integrated into other parts of the receiver front end, such as in a T/R switch, filter, or the input matching network to the LNA.

Appendix A - *Touchstone* Circuit File.

```
! Hewlett-Packard CMCD
!  Bob Myers      20 Sept 1996
!
! HP Touchstone circuit file
! INA-12063 Single Stage LNA
!    fc = 900 MHz, Vc = 3.0 V, Ic = 2.5 mA
!    Input Matched for NF

DIM
   FREQ GHZ
   RES  OH
   CAP  PF
   IND  NH
   LNG  IN
   ANG  DEG

VAR
! Input match
   L1#  0   12.6477     20
   A1#  0    0.201808     0.4             ! Length of MLOC
!  C1#  0    0.636904    10
! Output match
   L2#  0    9.25249     20
   C2#  0    2.56665     10

CKT
   MSUB   ER=4.8  H=0.031  T=0.001  RHO=1  RGH=0
   MLIN    1    2    W=0.056  L=0.300
   CAP     2    3    C=300           ! Input DC block
   MLIN    3    4    W=0.056  L=0.100
   IND     4    5    L^L1            ! L1 in Input match
   MLOC    5       W=0.04  L^A1      ! Z1 in Input match
!  CAP     5    0    C^C1            ! Alternate shunt C
   MLIN    5    6    W=0.04   L=0.020
   S2P     6    7    8     C:\SPARA\A120633B.S2P
   RES     7    0    R=9100          ! R1 bias resistor
   MLIN    8    9    W=0.020  L=0.035       ! Z2 in RF ground
   VIA     9    0    D1=0.025  D2=0.025  H=0.031  T=0.0015  W=0.04
   MLIN    7    10   W=0.06   L=0.100
   RES     10   12   R=330           ! R2 Stabilizing R
   MLIN    10   11   W=0.056  L=0.065
   IND     11   12   L^L2            ! L2 in Output match
   MLIN    11   15   W=0.056  L=0.050
   CAP     12   13   C=300           ! Bypass C
   MLIN    13   14   W=0.050  L=0.020
   VIA     14   0    D1=0.025  D2=0.025  H=0.031  T=0.001  W=0.04
   CAP     15   16   C^C2            ! C2 in Output match
   MLIN    16   17   W=0.056  L=0.300
   DEF2P   1    17   INA12

TERM
   Z0 = 50

OUT
   INA12   NF         GR3
   INA12   DB[S21]    GR1
   INA12   DB[S11]    GR2
   INA12   DB[S22]    GR2
   INA12   DB[GMAX]   GR1
```

```
   INA12   K                ! Stability factor (K > 1)
   INA12   B1               ! Stability Measure (B1 > 0)

FREQ
   SWEEP  0.1  3.1   0.02

GRID
   FREQ  0.8   1.0   0.05
!  FREQ  0.1   3.1   0.1
   GR1   0    20     5              ! Gain
   GR2   0   -40     10             ! Return loss
   GR3   0     4     1              ! NF

OPT
   FREQ   0.85   0.95
   INA12  NF<1.6      5
  INA12  DB[S22]<-20 1
```

Appendix B – *Touchstone* Output File.

FREQ GHZ	NF INA12	DB[S21] INA12	DB[S11] INA12	DB[S22] INA12	DB[GMAX] INA12	K INA12	B1 INA12
0.1	11.178	-43.253	-0.913	0.000	5.717	109.193	0.000
0.2	9.706	-13.998	-1.070	-0.005	22.248	1.404	0.002
0.3	8.725	-4.922	-1.429	-0.027	22.535	1.094	0.010
0.4	7.627	1.602	-1.843	-0.111	21.559	1.071	0.036
0.5	6.366	6.760	-2.947	-0.418	18.878	1.295	0.108
0.6	4.929	11.048	-4.674	-1.404	17.490	1.414	0.287
0.7	3.388	13.713	-7.101	-4.424	16.155	1.569	0.634
0.8	2.048	14.210	-8.450	-11.782	15.081	1.656	0.957
0.9	1.588	13.289	-7.910	-35.279	14.143	1.813	1.104
1.0	2.490	11.823	-6.677	-14.634	13.285	1.926	1.161
1.1	4.284	10.309	-5.483	-11.002	12.521	2.018	1.198
1.2	6.292	8.776	-4.459	-8.998	11.836	2.122	1.223
1.3	8.193	7.440	-3.727	-7.952	11.221	2.230	1.237
1.4	9.918	6.113	-3.076	-7.141	10.708	2.259	1.248
1.5	11.469	4.870	-2.611	-6.578	10.169	2.287	1.249
1.6	12.868	3.720	-2.221	-6.221	9.663	2.369	1.256
1.7	14.146	2.647	-1.900	-5.875	9.243	2.416	1.254
1.8	15.317	1.637	-1.646	-5.602	8.885	2.370	1.252
1.9	16.402	0.728	-1.440	-5.414	8.558	2.317	1.252
2.0	17.415	-0.174	-1.265	-5.222	8.233	2.288	1.247
2.1	18.367	-1.007	-1.124	-5.024	7.924	2.279	1.236
2.2	19.264	-1.850	-1.011	-4.905	7.498	2.344	1.231
2.3	20.112	-2.453	-0.912	-4.871	7.307	2.285	1.237
2.4	20.927	-3.275	-0.815	-4.736	7.002	2.299	1.229
2.5	21.700	-3.842	-0.737	-4.665	6.926	2.116	1.228
2.6	22.446	-4.446	-0.672	-4.546	6.747	2.039	1.217
2.7	23.162	-5.015	-0.615	-4.528	6.521	1.978	1.220
2.8	23.861	-5.656	-0.566	-4.345	6.252	1.975	1.195
2.9	24.530	-6.216	-0.523	-4.338	5.870	2.103	1.198
3.0	25.179	-6.619	-0.475	-4.171	6.107	1.889	1.177
3.1	25.811	-7.041	-0.442	-4.077	6.024	1.760	1.164

Results of computer simulation of optimized 900 MHz LNA.

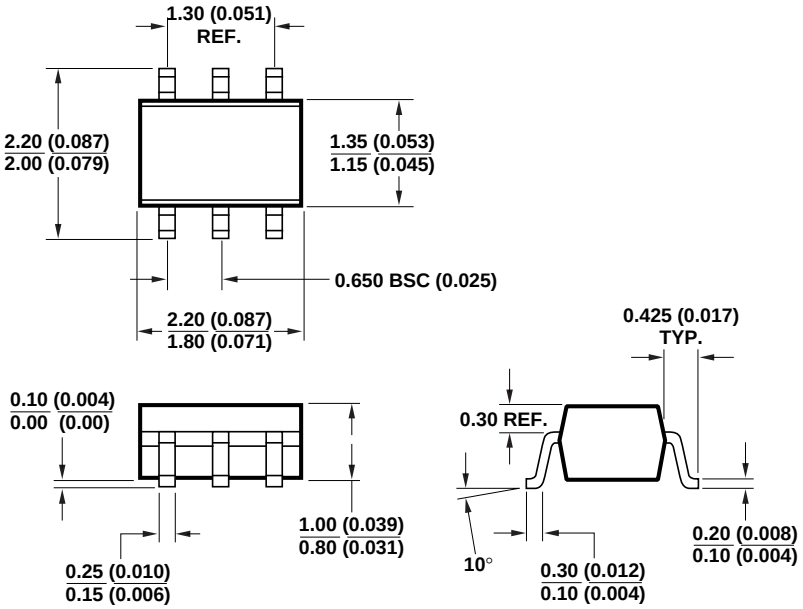
[1] U.S. Patent Number 5436595

INA-12063 Part Number Ordering Information

Part Number	Devices per Container	Container
INA-12063-TR1	3000	7" reel
INA-12063-BLK	100	tape strip in antistatic bag

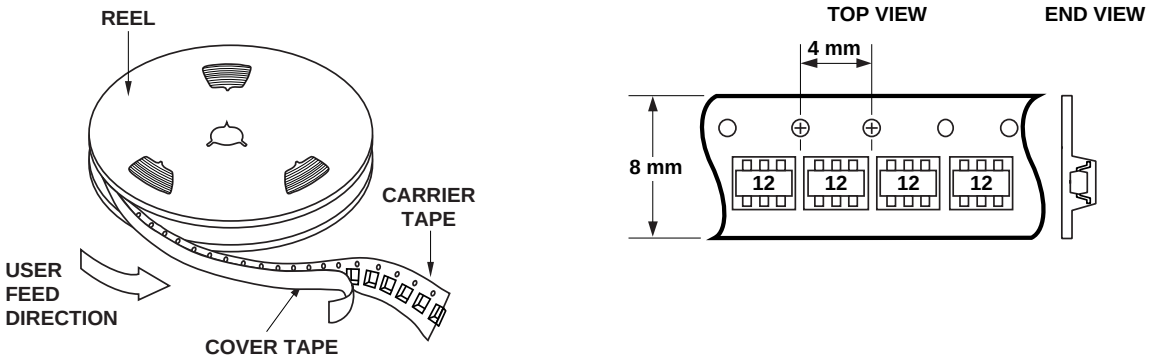
Package Dimensions

Outline 63 (SOT-363/SC-70)



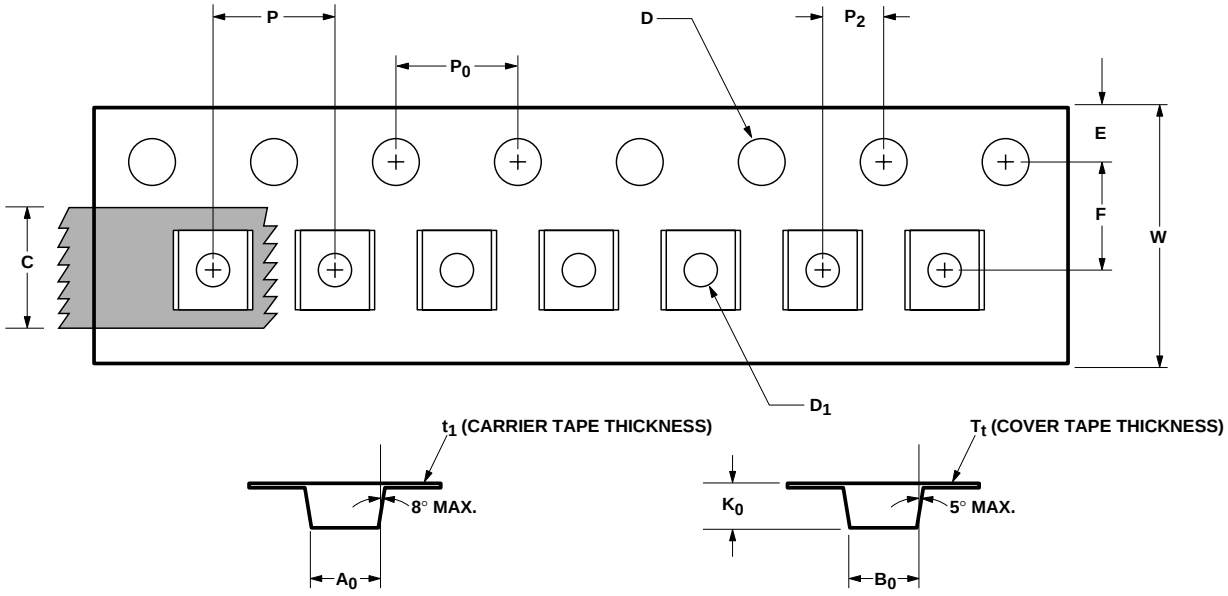
DIMENSIONS ARE IN MILLIMETERS (INCHES)

Device Orientation



Tape Dimensions and Product Orientation

For Outline 63



DESCRIPTION		SYMBOL	SIZE (mm)	SIZE (INCHES)
CAVITY	LENGTH	A_0	2.24 ± 0.10	0.088 ± 0.004
	WIDTH	B_0	2.34 ± 0.10	0.092 ± 0.004
	DEPTH	K_0	1.22 ± 0.10	0.048 ± 0.004
	PITCH	P	4.00 ± 0.10	0.157 ± 0.004
	BOTTOM HOLE DIAMETER	D_1	1.00 + 0.25	0.039 + 0.010
PERFORATION	DIAMETER	D	1.55 ± 0.05	0.061 ± 0.002
	PITCH	P_0	4.00 ± 0.10	0.157 ± 0.004
	POSITION	E	1.75 ± 0.10	0.069 ± 0.004
CARRIER TAPE	WIDTH	W	8.00 ± 0.30	0.315 ± 0.012
	THICKNESS	t_1	0.255 ± 0.013	0.010 ± 0.0005
COVER TAPE	WIDTH	C	5.4 ± 0.10	0.205 ± 0.004
	TAPE THICKNESS	T_t	0.062 ± 0.001	0.0025 ± 0.00004
DISTANCE	CAVITY TO PERFORATION (WIDTH DIRECTION)	F	3.50 ± 0.05	0.138 ± 0.002
	CAVITY TO PERFORATION (LENGTH DIRECTION)	P_2	2.00 ± 0.05	0.079 ± 0.002