



3.0 GHz Wideband Silicon RFIC Amplifier

Technical Data

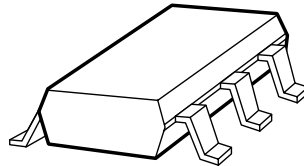
Features

- 17 dB Gain at 1.9 GHz
- +3 dBm $P_{1\text{dB}}$ at 1.9 GHz
- Single +3V Supply
- Unconditionally Stable

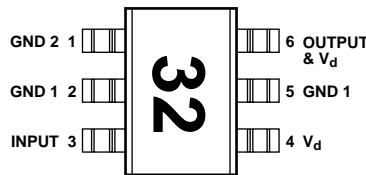
Applications

- LO Buffer and Driver Amplifier for Cellular, Cordless, Special Mobile Radio, PCS, ISM, Wireless LAN, DBS, TVRO, and TV Tuner

Surface Mount SOT-363 (SC-70) Package



Pin Connections and Package Marking



Note: Package marking provides orientation and identification.

INA-32063

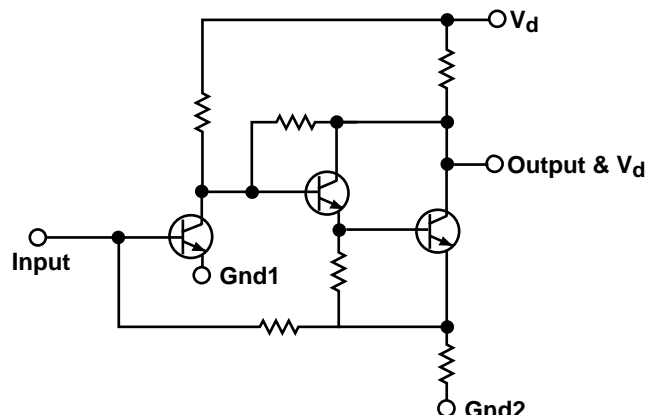
Description

Agilent's INA-32063 is a Silicon RFIC amplifier that offers excellent gain and output power for applications to 3.0 GHz. Packaged in an ultraminiature SOT-363 package, it requires half of the board space of a SOT-143 package.

The INA-32063 offers wide bandwidth and good linearity and 17 dB gain with a modest supply current. With its input and output matched internally to 50 Ω , the INA-32063 is a simple to use gain block that is suitable for numerous applications.

The INA-32063 is fabricated using Agilent's 30 GHz-fmax, ISOSAT™ Silicon-bipolar process that uses nitride, self-alignment, submicrometer lithography, trench isolation, ion implantation, and polyimide intermetal dielectric and scratch protection to achieve superior performance, uniformity and reliability.

Simplified Schematic



Absolute Maximum Ratings

Symbol	Parameter	Units	Absolute Maximum ^[1]
V_d	Device Voltage, RF output to ground	V	6.0
P_{in}	CW RF Input Power	dBm	+7.0
T_j	Junction Temperature	°C	150
T_{STG}	Storage Temperature	°C	-65 to 150

Thermal Resistance^[2]:

$$\theta_{jc} = 170^\circ\text{C/W}$$

Notes:

1. Operation of this device above any one of these limits may cause permanent damage.
2. $T_C = 25^\circ\text{C}$ (T_C is defined to be the temperature at the package pins where contact is made to the circuit board)

INA-32063 Electrical Specifications, $T_C = 25^\circ\text{C}$, $Z_0 = 50 \Omega$, $V_d = 3 \text{ V}$

Symbol	Parameters and Test Conditions	Units	Min.	Typ.	Max.	Std. Dev. ^[4]
$ S_{21} ^2$	Gain in 50 Ω system $f = 0.9 \text{ GHz}$ $f = 1.9 \text{ GHz}$ $f = 2.4 \text{ GHz}$	dB	15.5 ^[3]	16.8 17.8 18.2		0.39
NF_{50}	Noise Figure $f = 1.9 \text{ GHz}$	dB		4.4		0.21
P_{1dB}	Output Power at 1 dB Gain Compression $f = 0.9 \text{ GHz}$ $f = 1.9 \text{ GHz}$ $f = 2.4 \text{ GHz}$	dBm		3.6 4.8 4.0		
IP_3	Output Third Order Intercept Point $f = 0.9 \text{ GHz}$ $f = 1.9 \text{ GHz}$ $f = 2.4 \text{ GHz}$	dBm		15.3 14.4 11.5		
$VSWR_{in}$	Input VSWR $f = 0.1 - 2.4 \text{ GHz}$			1.1:1		
$VSWR_{out}$	Output VSWR $f = 0.1 - 2.4 \text{ GHz}$			1.6:1		
I_d	Device Current	mA		20	25 ^[3]	1.1

Notes:

3. Guaranteed specifications are 100% tested in production.
4. Standard deviation number is based on measurement of a large number of parts from three non-consecutive wafer lots during the initial characterization of this product, and is intended to be used as an estimate for distribution of the typical specification.

INA-32063 Typical Performance, $T_C = 25^\circ\text{C}$, $Z_O = 50\ \Omega$, $V_d = 3\ \text{V}$

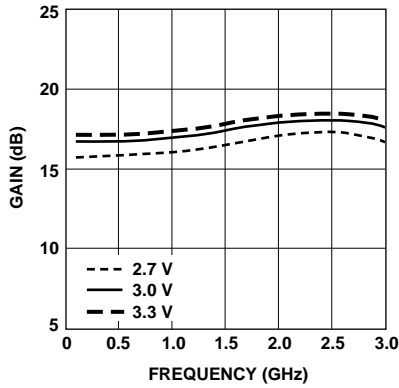


Figure 1. Gain vs. Frequency and Voltage.

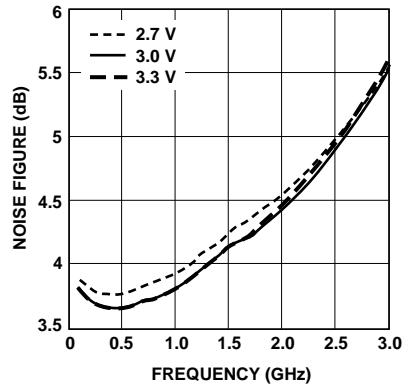


Figure 2. Noise Figure vs. Frequency and Voltage.

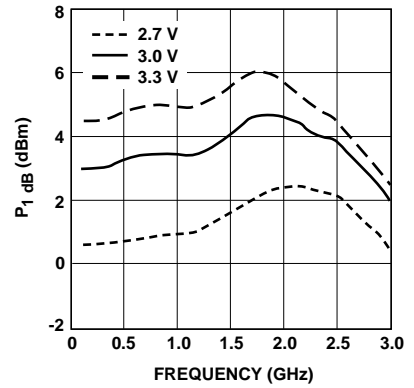


Figure 3. Output Power for 1 dB Gain Compression vs. Frequency and Voltage.

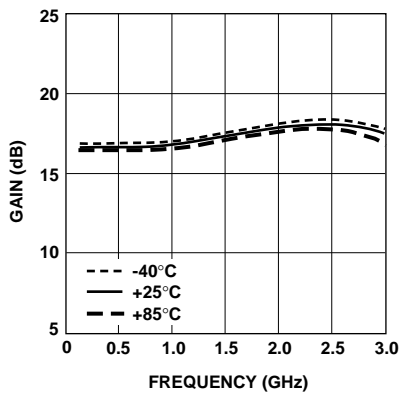


Figure 4. Gain vs. Frequency and Temperature.

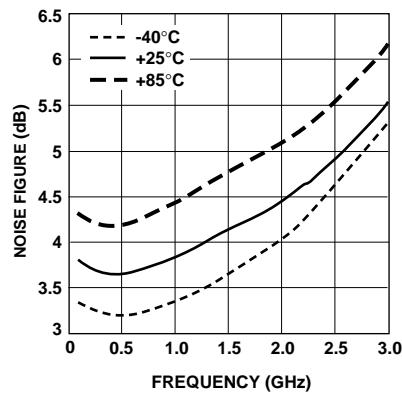


Figure 5. Noise Figure vs. Frequency and Temperature.

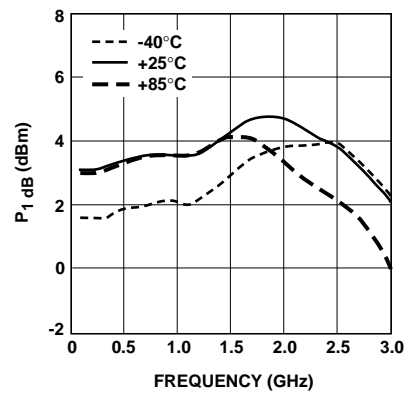


Figure 6. Output Power for 1 dB Gain Compression vs. Frequency and Temperature.

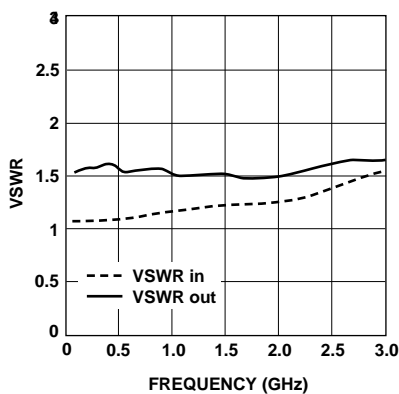


Figure 7. Input and Output VSWR vs. Frequency.

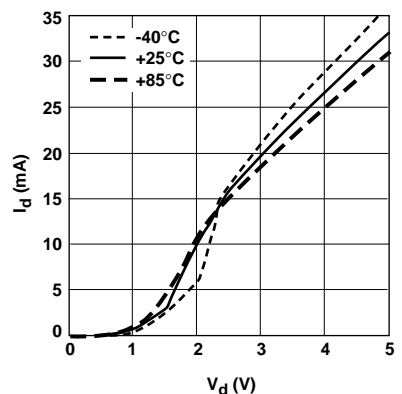


Figure 8. Supply Current vs. Voltage and Temperature.

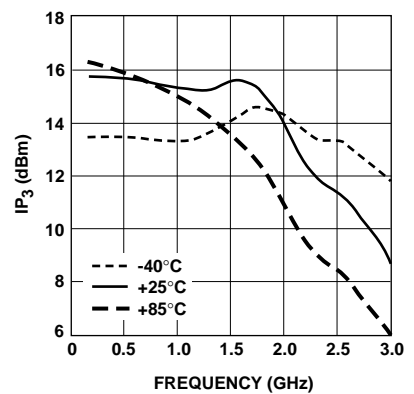


Figure 9. Third Order Intercept Point, IP_3 vs. Frequency and Temperature.

INA-32063 Typical Scattering Parameters^[5], $T_C = 25^\circ\text{C}$, $Z_0 = 50\ \Omega$, $V_d = 3.0\ \text{V}$

Freq. GHz	S_{11}		dB	S_{21}		dB	S_{12}		S_{22}		K Factor
	Mag	Ang		Mag	Ang		Mag	Ang	Mag	Ang	
0.1	0.034	19	16.5	6.72	-4	-26.8	0.046	3	0.215	-5	1.68
0.2	0.034	30	16.5	6.71	-9	-27.9	0.040	0	0.230	-6	1.89
0.3	0.039	35	16.6	6.73	-13	-27.7	0.041	-3	0.227	-7	1.84
0.4	0.043	41	16.6	6.75	-17	-28.3	0.039	-10	0.238	-8	1.91
0.5	0.053	53	16.6	6.78	-22	-28.3	0.038	-7	0.226	-8	1.96
0.6	0.054	49	16.7	6.80	-26	-28.0	0.040	-10	0.218	-9	1.87
0.7	0.059	49	16.7	6.85	-30	-28.5	0.038	-12	0.223	-12	1.94
0.8	0.065	50	16.8	6.90	-35	-28.9	0.036	-13	0.224	-16	2.02
0.9	0.072	49	16.8	6.94	-39	-29.1	0.035	-12	0.220	-21	2.05
1.0	0.080	47	16.9	7.00	-44	-29.2	0.035	-11	0.215	-25	2.03
1.1	0.084	48	17.0	7.09	-48	-29.1	0.035	-13	0.211	-29	2.06
1.2	0.090	46	17.1	7.16	-53	-29.3	0.034	-15	0.211	-33	2.10
1.3	0.096	45	17.2	7.23	-58	-29.5	0.033	-15	0.206	-40	2.07
1.4	0.101	46	17.3	7.32	-62	-29.8	0.033	-15	0.205	-47	2.10
1.5	0.107	45	17.4	7.40	-67	-29.9	0.032	-14	0.204	-55	2.11
1.6	0.109	43	17.5	7.48	-72	-29.6	0.033	-16	0.194	-63	2.04
1.7	0.108	41	17.6	7.59	-77	-29.9	0.032	-19	0.193	-68	2.07
1.8	0.110	38	17.7	7.69	-83	-30.1	0.031	-20	0.194	-77	2.10
1.9	0.113	36	17.8	7.79	-88	-30.5	0.030	-22	0.197	-85	2.13
2.0	0.118	32	17.9	7.88	-94	-30.6	0.029	-23	0.198	-94	2.17
2.1	0.121	26	18.0	7.98	-100	-30.8	0.029	-25	0.206	-101	2.13
2.2	0.129	20	18.1	8.03	-106	-31.1	0.028	-27	0.214	-111	2.17
2.3	0.138	13	18.1	8.06	-112	-31.3	0.027	-29	0.220	-120	2.22
2.4	0.151	6	18.2	8.09	-119	-31.5	0.027	-31	0.225	-128	2.20
2.5	0.163	-1	18.2	8.09	-125	-31.6	0.026	-34	0.232	-135	2.26
2.6	0.175	-7	18.1	8.04	-132	-32.0	0.025	-37	0.242	-143	2.33
2.7	0.189	-13	18.0	7.96	-138	-32.3	0.024	-42	0.247	-151	2.42
2.8	0.199	-19	17.9	7.84	-145	-32.8	0.023	-46	0.250	-160	2.53
2.9	0.208	-26	17.8	7.73	-152	-33.3	0.022	-51	0.250	-166	2.67
3.0	0.216	-33	17.6	7.56	-158	-33.6	0.021	-56	0.249	-173	2.84
3.1	0.224	-40	17.3	7.36	-165	-34.2	0.019	-63	0.246	180	3.20
3.2	0.234	-48	17.1	7.16	-171	-35.1	0.018	-70	0.239	173	3.46
3.3	0.243	-57	16.8	6.92	-177	-35.8	0.016	-78	0.229	168	4.02
3.4	0.254	-64	16.5	6.67	176	-36.7	0.015	-86	0.220	163	4.44
3.5	0.266	-71	16.1	6.39	170	-37.1	0.014	-97	0.212	157	4.95
3.6	0.280	-77	15.8	6.13	165	-38.3	0.012	-110	0.196	151	6.00
3.7	0.292	-83	15.4	5.86	159	-38.8	0.011	-121	0.182	146	6.84
3.8	0.301	-88	14.9	5.58	154	-39.0	0.011	-130	0.170	142	7.18
3.9	0.309	-92	14.5	5.32	149	-38.3	0.012	-142	0.156	136	6.90
4.0	0.317	-97	14.1	5.07	144	-37.6	0.013	-152	0.139	131	6.69
4.1	0.323	-101	13.7	4.84	139	-36.5	0.015	-160	0.124	125	6.08
4.2	0.327	-105	13.3	4.61	134	-35.3	0.017	-166	0.110	120	5.64
4.3	0.328	-109	12.9	4.39	130	-34.0	0.020	-173	0.095	112	5.05
4.4	0.331	-113	12.4	4.19	126	-32.8	0.023	-178	0.079	101	4.61
4.5	0.333	-117	12.0	3.99	122	-31.7	0.026	177	0.065	88	4.30
4.6	0.334	-122	11.6	3.81	118	-30.7	0.029	172	0.052	68	4.04
4.7	0.337	-126	11.2	3.63	114	-29.8	0.032	168	0.041	42	3.85
4.8	0.338	-130	10.8	3.47	110	-29.0	0.036	165	0.031	15	3.59
4.9	0.342	-134	10.4	3.31	106	-28.0	0.040	162	0.022	-5	3.39
5.0	0.347	-137	10.0	3.17	103	-27.2	0.044	159	0.013	-17	3.22

Note:

5. Reference plane per Figure 15 in Applications Information section.

INA-32063 Applications Information

Introduction

The INA-32063 is a +3 volt silicon RFIC amplifier that is designed with a two stage internal network to provide a broadband gain and 50 Ω input and output impedance. With a typical +4.8 dBm P-1 dB compressed output power at 1900 MHz, for only 20 mA supply current. The broad bandwidth, INA-32063, is well suited for amplifier applications in mobile communication systems.

A feature of the INA-32063 is a positive gain slope over the 1–2.5 GHz range that is useful in many satellite-based TV and datacom systems.

In addition to use in buffer and driver amplifier applications in the cellular market, the INA-32063 will find many applications in battery operated wireless communication systems.

Operating Details

The INA-32063 is a voltage-biased device that operates from a +3 volt power supply with a typical current drain of 20 mA. All bias regulation circuitry is integrated into the RFIC.

Figure 10 shows a typical implementation of the INA-32063. The supply voltage for the INA-32063 must be applied to two terminals, the V_d pin and the RF Output pin.

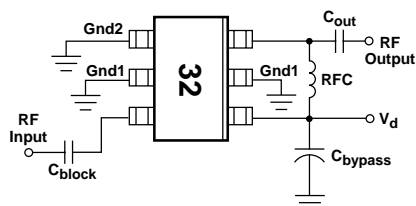


Figure 10. Basic Amplifier Application.

The V_d connection to the amplifier is RF bypassed by placing a capacitor to ground near the V_d pin of the amplifier package.

The power supply connection to the RF Output pin is achieved by means of a RF choke (inductor). The value of the RF choke must be large relative to 50 Ω in order to prevent loading of the RF Output. The supply voltage end of the RF choke is bypassed to ground with a capacitor. If the physical layout permits, this can be the same bypass capacitor that is used at the V_d terminal of the amplifier.

Blocking capacitors are normally placed in series with the RF Input and the RF Output to isolate the DC voltages on these pins from circuits adjacent to the amplifier. The values for the blocking and bypass capacitors are selected to provide a reactance at the lowest frequency of operation that is small relative to 50 Ω .

Example Layout for 50 Ω Output Amplifier

An example layout for an amplifier using the INA-32063 with 50 Ω input and 50 Ω output is shown in Figure 11.

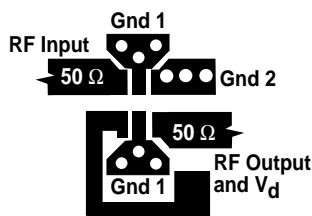


Figure 11. RF Layout.

This example uses a microstripline design (solid groundplane on the backside of the circuit board). The circuit board material is 0.031-inch thick FR-4. Plated through holes (vias)

are used to bring the ground to the topside of the circuit where needed. The performance of INA-32063 is sensitive to ground path inductance. The two-stage design creates the possibility of a feedback loop being formed through the ground returns of the stages, Gnd 1 and Gnd 2.

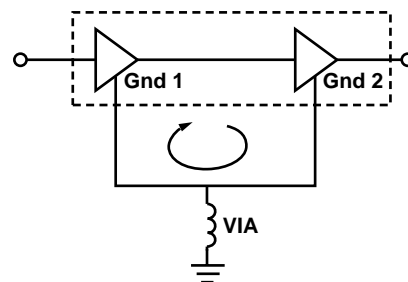


Figure 12. INA-32063 Potential Ground Loop.

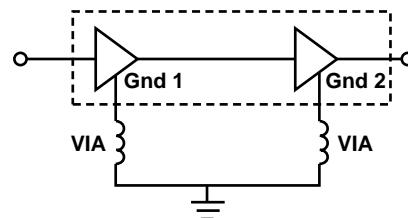


Figure 13. INA-32063 Suggested Layout.

At least one ground via should be placed adjacent to each ground pin to assure good RF grounding. Multiple vias are used to reduce the inductance of the path to ground and should be placed as close to the package terminals as practical.

The effects of the potential ground loop shown in Figure 12 may be observed as a “peaking” in the gain versus frequency response, an increase in input VSWR, or even as return gain at the input of the INA-32063.

Figure 14 shows an assembled amplifier. The +3 volt supply is fed directly into the V_d pin of the

INA-32063 and into the RF Output pin through the RF choke (RFC). Capacitor C3 provides RF bypassing for both the V_d pin and the power supply end of the RFC. Capacitor C4 is optional and may be used to add additional bypassing for the V_d line. A well-bypassed V_d line is especially necessary in cascades of amplifier stages to prevent oscillation that may occur as a result of RF feedback through the power supply lines.

For this demonstration circuit, the value chosen for the RF choke was 120 nH (Coilcraft 1008CS-221, TOKO LL2012 -F or equivalent). All of the blocking and bypass capacitors are 100 pF. The gap in the output transmission line was bridged using copper foil cut to size. These values provide excellent amplifier performance from under 50 MHz through 2.4 GHz. Larger values for the choke and capacitors can be used to extend the lower end of the bandwidth. Since the gain of the INA-32063 extends down to DC, the frequency response of the amplifier is limited only by the values of the capacitors and choke.

A convenient method for making RF connection to the demonstration board is to use a PCB mounting type of SMA connector (Johnson 142-0701-881, or equivalent). These connectors can be slipped over the edge of the PCB and the center conductor soldered to the input and output lines. The ground pins of the connectors can be soldered to the ground plane on the backside of board.

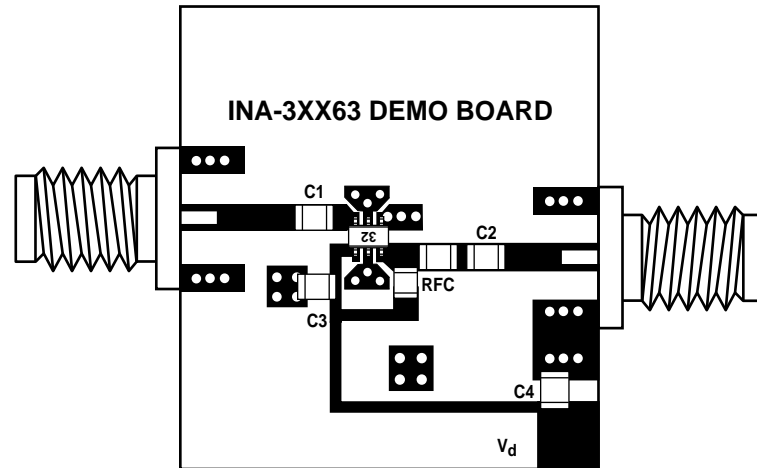


Figure 14. Assembled Amplifier.

PCB Materials

Typical choices for PCB material for low cost wireless applications are FR-4 or G-10 with a thickness of 0.025 (0.635 mm) or 0.031 inches (0.787 mm). A thickness of 0.062 inches (1.574 mm) is the maximum that is recommended for use with this particular device. The use of a thicker board material increases the inductance of the plated through vias used for RF grounding and may deteriorate circuit performance. Adequate grounding is needed not only to obtain maximum amplifier performance but also to reduce any possibility of instability.

Phase Reference Planes

The positions of the reference planes used to measure S-Parameters for this device are shown in Figure 15. As seen in the illustration, the reference planes are located at the point where the package leads contact the test circuit.

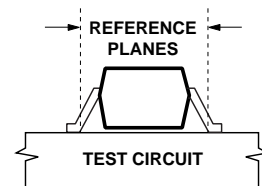


Figure 15. Phase Reference Planes.

SOT-363 PCB Layout

The INA-32063 is packaged in the miniature SOT-363 (SC-70) surface mount package. A PCB pad layout for the SOT-363 package is shown in Figure 16 (dimensions are in inches). This layout provides ample allowance for package placement by automated assembly equipment without adding pad parasitics that could impair the high frequency performance of the INA-32063. The layout that is shown with a nominal SOT-363 package footprint superimposed on the PCB pads for reference.

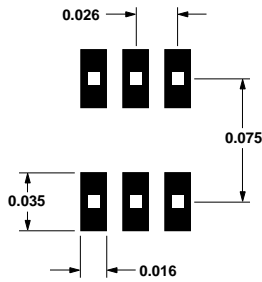


Figure 16. PCB Pad Layout for INA-32063 (dimensions in inches).

Statistical Parameters

Several categories of parameters appear within this data sheet. Parameters may be described with values that are either “minimum or maximum,” “typical,” or “standard deviations.” The values for parameters are based on comprehensive product characterization data, in which automated measurements are made on a large number of parts taken from 3 non-consecutive process lots of semiconductor wafers. The data derived from product characterization tends to be normally distributed, e.g., fits the standard “bell curve.”

Parameters considered to be the most important to system performance are bounded by minimum or maximum values. For the INA-32063, these parameters are: Power Gain ($|S_{21}|^2$) and the Device Current (I_d). Each of these guaranteed parameters is 100% tested. Values for most of the parameters in the table of Electrical Specifications that are described by typical data are the mathematical mean (μ), of the normal distribution taken from the characterization data. For parameters where measurements

or mathematical averaging may not be practical, such as S-parameters or Noise Parameters and the performance curves, the data represents a nominal part taken from the “center” of the characterization distribution. Typical values are intended to be used as a basis for electrical design.

To assist designers in optimizing not only the immediate circuit using the INA-32063, but to also optimize and evaluate trade-off that affect a complete wireless system, the standard deviation (σ) is provided for many of the Electrical Specifications parameters (at 25°C) in addition to the mean. The standard deviation is a measure of the variability about the mean. It will be recalled that a normal distribution is completely described by the mean and standard deviation.

Standard statistics tables or calculations provide the probability of a parameter falling between any two values, usually symmetrically located about the mean. Referring to Figure 17 for example, the probability of a parameter being between $\pm 1\sigma$ is 68.3%; between $\pm 2\sigma$ is 95.4%; and between $\pm 3\sigma$ is 99.7%.

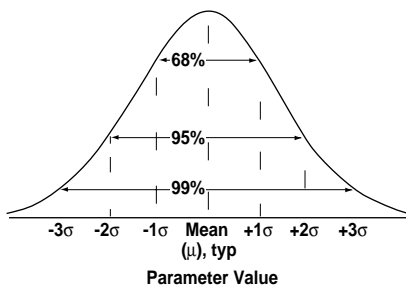


Figure 17. Normal Distribution.

SMT Assembly

Reliable assembly of surface mount components is a complex process that involves many material, process, and equipment factors, including: method of heating (e.g., IR or vapor phase reflow, wave soldering, etc.) circuit board material, conductor thickness and pattern, type of solder alloy, and the thermal conductivity and thermal mass of components. Components with a low mass, such as the SOT-363 package, will reach solder reflow temperatures faster than those with a greater mass.

The INA-32063 has been qualified to the time-temperature profile shown in Figure 18. This profile is representative of an IR reflow type of surface mount assembly process.

After ramping up from room temperature, the circuit board with components attached to it (held in place with solder paste) passes through one or more preheat zones. The preheat zones increase the temperature of the board and components to prevent thermal shock and begin evaporating solvents from the solder paste. The reflow zone briefly elevates the temperature sufficiently to produce a reflow of the solder. The rates of change of temperature for the ramp-up and cool down zones are chosen to be low enough to not cause deformation of the board or damage to components due to thermal shock.

For more information on mounting considerations for packaged microwave semiconductors

please refer to Agilent application note AN-A006.

These parameters are typical for a surface mount assembly process for the INA-32063. As a general guideline, the circuit board and components should only be exposed to the minimum temperatures and times necessary to achieve a uniform reflow of solder.

Electrostatic Sensitivity



RFICs are electrostatic discharge (ESD) sensitive devices.

Although the INA-32063 is robust in design, permanent damage may occur to these devices if they are subjected to high-energy electrostatic discharges. Electrostatic charges as high as several thousand volts (which readily accumulate on the

human body and on test equipment) can discharge without detection and may result in degradation in performance or failure. Electronic devices may be subjected to ESD damage in any of the following areas:

- Storage & handling
- Inspection & testing
- Assembly
- In-circuit use

The INA-32063 is an ESD Class 1 device. Therefore, proper ESD precautions are recommended when handling, inspecting, and assembling these devices to avoid damage.

For more information on Electrostatic Discharge and Control refer to Agilent application note AN-A004R.

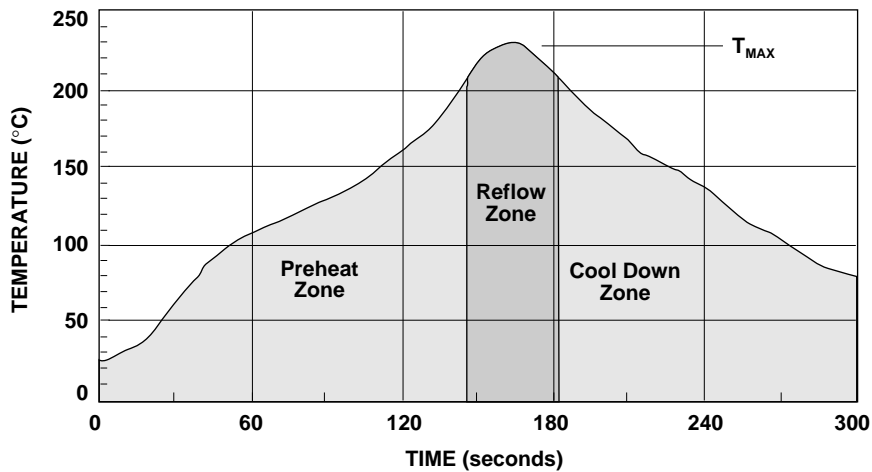
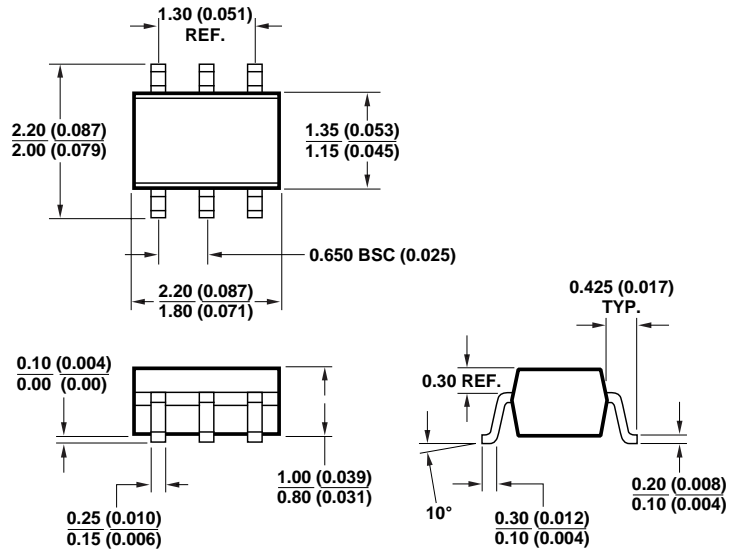


Figure 18. Surface Mount Assembly Profile.

Package Dimensions

Outline 63 (SOT-363/SC-70)



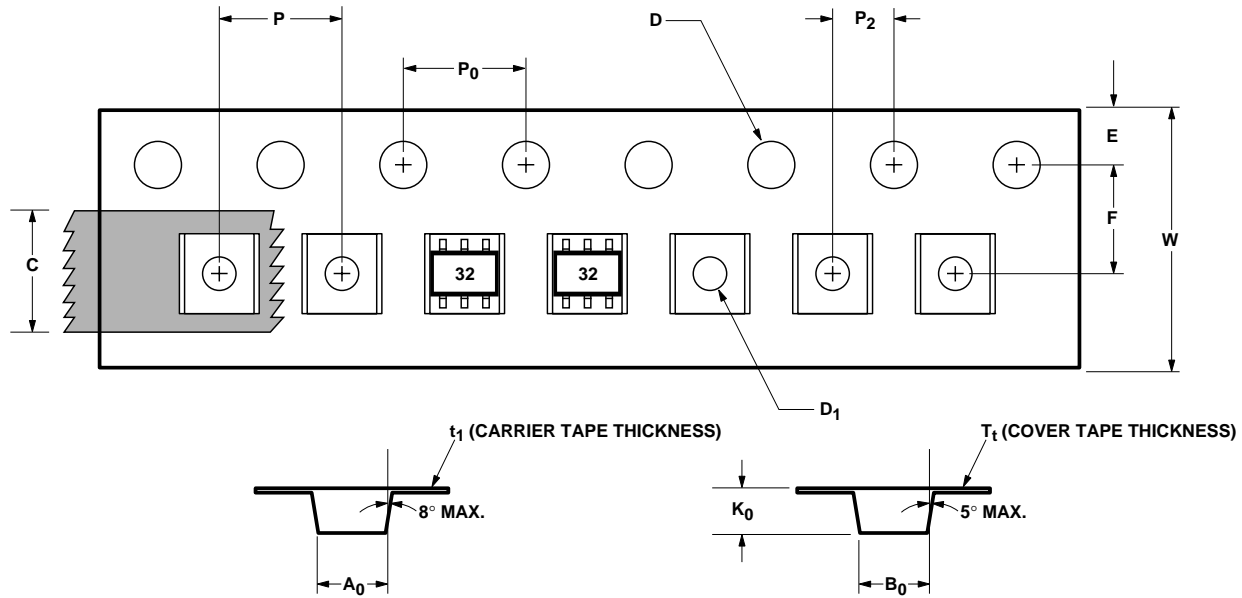
DIMENSIONS ARE IN MILLIMETERS (INCHES)

INA-32063 Part Number Ordering Information

Part Number	Devices per Container	Container
INA-32063-BLK	100	tape strip in antistatic bag
INA-32063-TR1	3,000	7" reel
INA-32063-TR2	10,000	13" reel

Tape Dimensions and Product Orientation

For Outline 63



DESCRIPTION		SYMBOL	SIZE (mm)	SIZE (INCHES)
CAVITY	LENGTH	A_0	2.24 ± 0.10	0.088 ± 0.004
	WIDTH	B_0	2.34 ± 0.10	0.092 ± 0.004
	DEPTH	K_0	1.22 ± 0.10	0.048 ± 0.004
	PITCH	P	4.00 ± 0.10	0.157 ± 0.004
	BOTTOM HOLE DIAMETER	D_1	$1.00 + 0.25$	$0.039 + 0.010$
PERFORATION	DIAMETER	D	1.55 ± 0.05	0.061 ± 0.002
	PITCH	P_0	4.00 ± 0.10	0.157 ± 0.004
	POSITION	E	1.75 ± 0.10	0.069 ± 0.004
CARRIER TAPE	WIDTH	W	8.00 ± 0.30	0.315 ± 0.012
	THICKNESS	t_1	0.255 ± 0.013	0.010 ± 0.0005
COVER TAPE	WIDTH	C	5.4 ± 0.10	0.205 ± 0.004
	TAPE THICKNESS	T_t	0.062 ± 0.001	0.0025 ± 0.00004
DISTANCE	CAVITY TO PERFORATION (WIDTH DIRECTION)	F	3.50 ± 0.05	0.138 ± 0.002
	CAVITY TO PERFORATION (LENGTH DIRECTION)	P_2	2.00 ± 0.05	0.079 ± 0.002



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Obsoletes 5965-8921E

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