

IECQ-CECC

QC 88000-C002

COMPONENT

ISSUE 1

SPECIFICATION

March 2007

**Component Specification
For
Ceramic Hermetically Sealed
High Speed Optocouplers**



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FOREWORD

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The object of the System is to facilitate international trade by the harmonization of the specifications and quality assessment procedures for electronic components, and by the grant of an internationally recognised Mark, or Certificate of Conformity. The components produced or services provided under the system are thereby acceptable in all member countries without further testing.

This Component Specification is based upon the requirements of IEC Publication QC 001002-2, and has been prepared by:

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AMENDMENT RECORD

No previous issue.

REQUIREMENTS

The requirements for IECQ-CECC Component Specifications as detailed in QC 001002-2 Amendment 1 clause 5.4 are satisfied by the following data sheet.

It should note that IECQ-CECC are not responsible for manufacturers declarations made in data sheets which fall outside the limits of approved detailed in IECQ-CECC certificates.

This Component Specification is intended for use with applicable IECQ-CECC Assessment Specifications. Eg: QC 88000-A0001

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Ceramic Hermetically Sealed High Speed Optocouplers

- | | |
|-------------|------------|
| ■ 4N55 | ■ CSM168-4 |
| ■ CD850 | ■ CSM1801 |
| ■ CH380 | ■ CSM1800 |
| ■ CS800/801 | ■ MC800 |
| ■ CSM168-2 | |

Features

- Release to IECQ-CECC
- Hermetically Sealed
- High Density Packaging
- 1500V DC withstand Test Voltage
- Low Input Requirements
- High Current Transfer Ratio

Applications

- Military, high reliability system
- Medical instruments
- Mos, Cmos Applications
- Logic Interfacing
- Data Transmission
- Power Supply

Description

These devices are single, dual and quad, hermetically sealed optocouplers. Each channel is composed of a Gallium Arsenide infra-red emitting diode and a silicon phototransistor. Package styles for these devices include 6 pin, 8 pin, 16 pin flat pack, and hybrid 4 pin, with surface mount, butt cut and gull wing options available.

The same electrical die, assembly processes and materials are used for each channel of each device shown below. Therefore absolute maximum ratings, recommended operating conditions, electrical specifications and performance characteristics are identical for all units. Any exceptions, due to packaging variations and limitations, are as noted.

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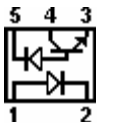
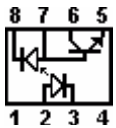
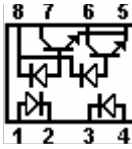
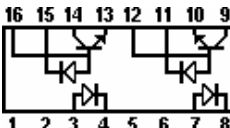

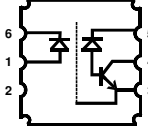
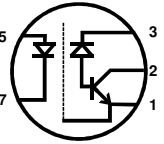
Selection Guide Package Styles and Configuration Options

Package	16 pin DIP	8 pin DIP	6 pin Hybrid	16 pin Flat Pack	6 Pad LCC	6pin metal Can TO-5
Lead Style						
Channels	2	1/2	1	4	1	1
Common Channel Wiring						

Isocom Part Numbers and Options

Commercial	4N55	CS800/801 CD850	CH380	CSM168-2/4	CSM1800/01	MC800
Defense Level	4N55/L2	CS800/801/L2 CD850/L2	CH380/L2	CSM168-2/4/L2	CSM1800/01	MC800/L2
Space Level	4N55/L2S	CS800/801/L2S CD850/L2S	CH380/L2S	CSM168-2/4/L2S	CSM1800/01	MC800/L2S
Standard Gold Plate Finish	Gold Plate	Gold Plate	Gold Plate	Gold Plate	Gold Plate	Gold Plate
Solder Dipped	Option 20	Option 20	Option 20			
Butt Cut/Gold Plate	Option 10	Option 10	Option 10			
Gull Wing/Soldered	Option 30	Option 30	Option 30			
Crew Cut/Gold Plate	Option 60	Option 60	Option 60			

Functional Diagrams

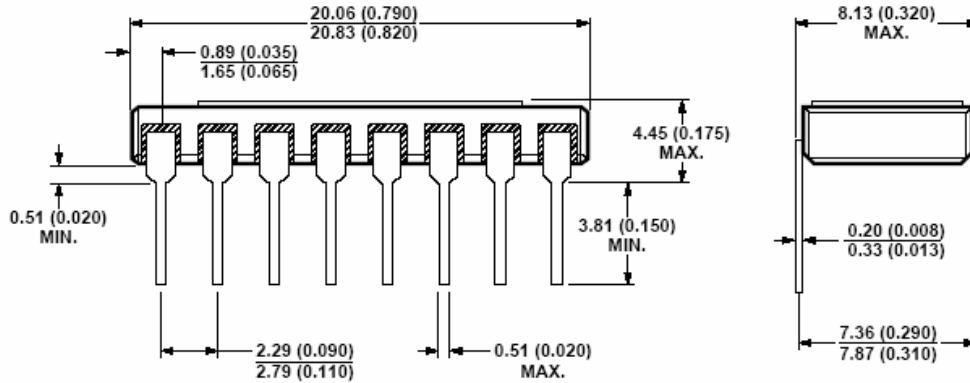
CH380	CS800/801	CD850	4N55	CSM168-4 CSM168-2	CSM1800/01
1 Channel	1 Channel	2 Channel	2 Channel	2-4 Channel	1 Channel
					
MC800					
1 Channel					
					

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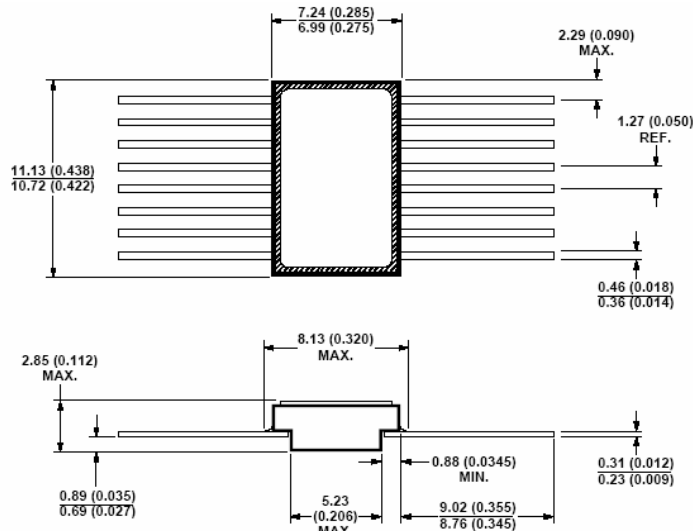
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Outline Drawings

16 pin DIP, 4 Channel



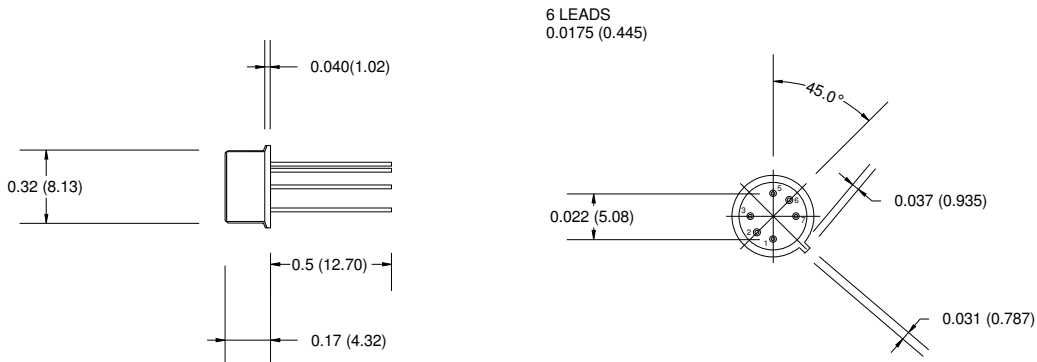
16 pin Flat Pack, 4 Channel



MILLIMETERS

NOTE: DIMENSIONS IN

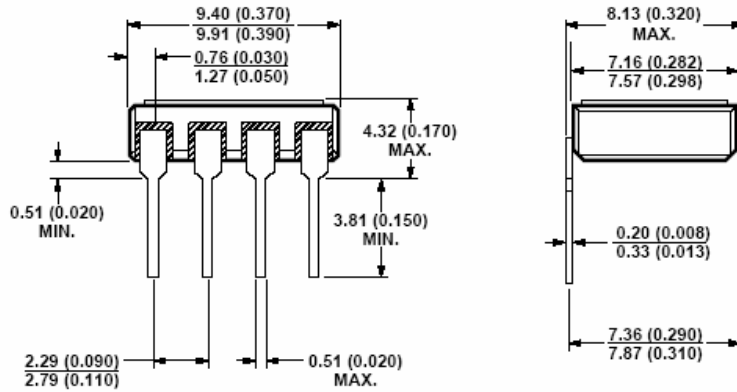
6 pin TO-5, 1 Channel



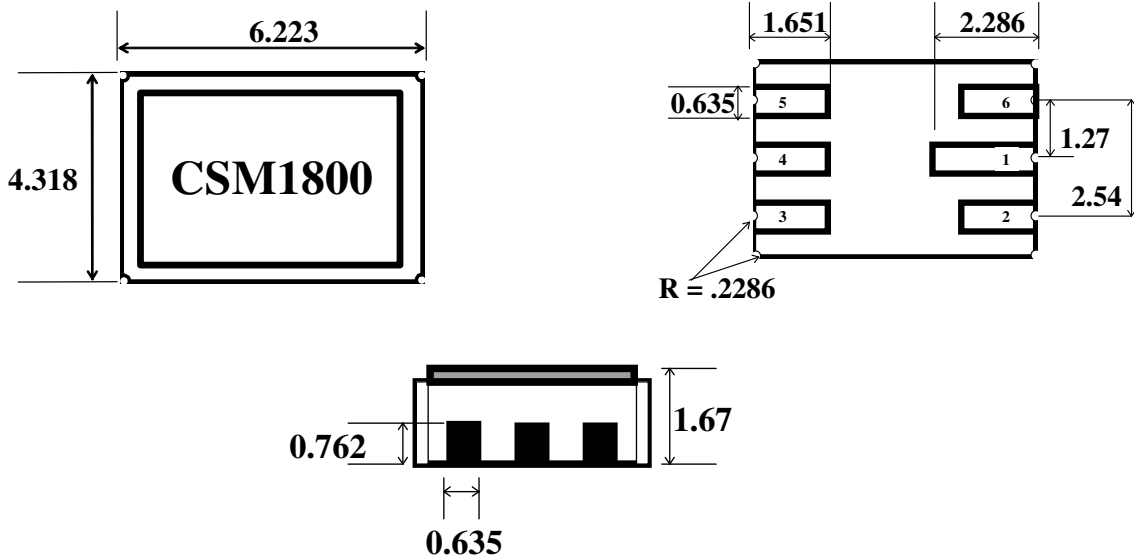
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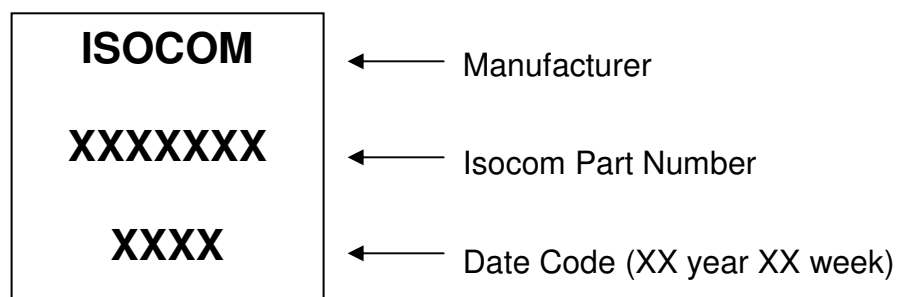
8 pin DIP 1 and 2 Channel



6 Terminal LCC Surface Mount, 1 Channel



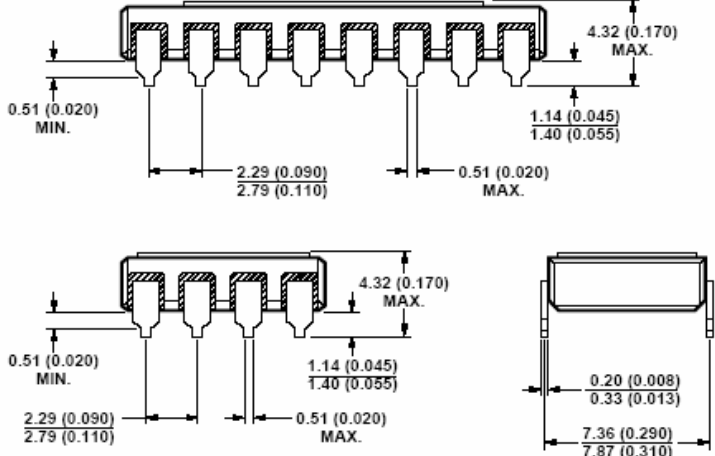
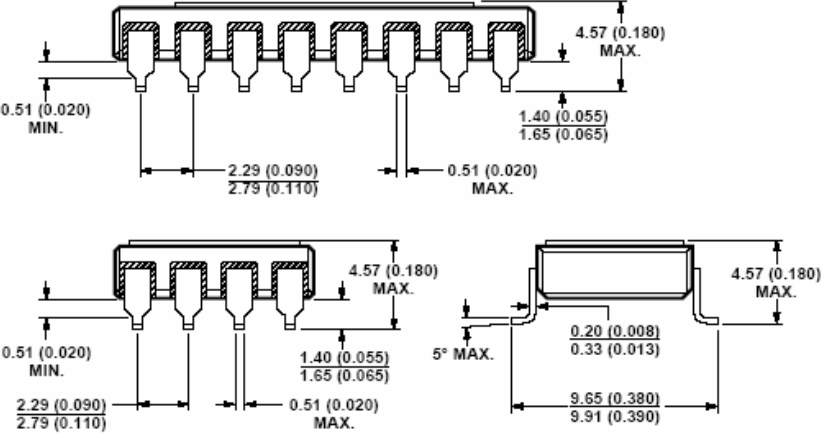
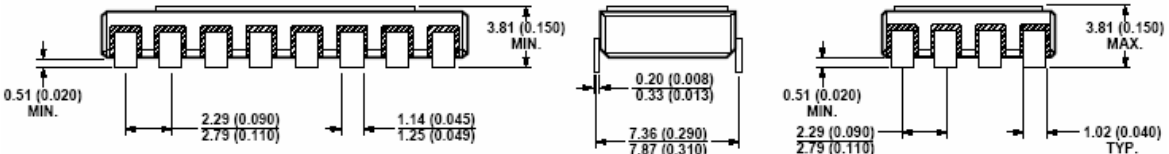
Device Marking



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Hermetic Optocoupler Options

Option	Description
10	<p>Surface mountable hermetic optocoupler with leads trimmed for butt joint assembly. This option is available on commercial hi-rel product in 8 and 16 pin DIP</p> 
20	
30	<p>Surface mountable hermetic optocoupler with leads cut and bent for gull wing assembly. This option is available on commercial and hi-rel product in 8 and 16 pin DIP.</p> 
60	<p>Surface mountable hermetic optocoupler with leads trimmed for butt joint assembly. This option is available on commercial hi-rel product in 8 and 16 pin DIP</p> 

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Absolute Maximum Ratings

Storage Temperature	-65°C to +150°C
Operating Temperature	-55°C to +125°C

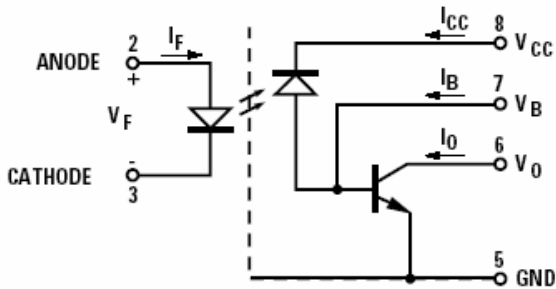
Input Diode

Peak Forward Current	40mA	≤ 1 mS duration
Average Forward Current	20mA	
Reverse Voltage	5V	
Power Dissipation	36mW	Derate linearly above 100°C at 1.4W/°C for CH380 and CS800/801

Output Detector

Supply Voltage	-0.5 to 20V	V _{CC}
Average Current	8mA	I _O
Peak Current	16mA	I _O
Voltage	-0.5 to 20V	V _O
Power Dissipation	40mW	For CH380 and CS800/801
	50mW	Derate linearly above 100°C at 1.4W/°C for CD850, CSM6530 and 4N55
Emitter-Base Reverse Voltage	3V	BV _{EBO}
Base Current	5mA	I _B

Single Channel Schematic



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Electrical Characteristics

$T_A = -55^{\circ}\text{C}$ to $+125^{\circ}\text{C}$ U.O.S.

All typical values at $V_{CC} = 5\text{V}$, $T_A = 25^{\circ}\text{C}$ (each channel where appropriate).

Parameter	Symbol	Test Conditions	Device	Min	Type	Max	Units
Current Transfer Ratio (See notes 1 & 2)	$h_{f(\text{CTR})}$	$V_{CC} = 4.5\text{V}$, $V_O = 0.4\text{V}$, $I_F = 16\text{mA}$,		9	20	-	%
			CS801	15	-		
		$V_{CC} = 4.5\text{V}$, $V_O = 0.5\text{V}$, $I_F = 16\text{mA}$	CD850	9	17	-	
Logic Low Output Voltage	V_{OL}	$V_{CC} = 4.5\text{V}$, $I_F = 16\text{mA}$ $I_O = 1.44\text{mA}$		-	0.3	0.4	V
			CD850	-	0.3	0.5	
Logic High Output Current (See note 1)	I_{OH}	$I_{F1} = 0$, $I_{F2} = 20\text{mA}$ $V_O = V_{CC} = 18\text{V}$		-	30	250	μA
			$I_{F1} = I_{F2} = 20\text{mA}$, $V_O = V_{CC} = 15$	CD850 CSM1800			
Logic Low Supply Current (See note 1)	I_{OCL}	$V_{CC} = 18\text{V}$, $I_{F1} = I_{F2} = 20\text{mA}$		-	30	200	μA
		$V_{CC} = 18\text{V}$, $I_{F1} = 20\text{mA}$	CS800/1				
		$V_{CC} = 15\text{V}$ $I_{F1} = 16\text{mA}$ $I_{F2} = 0$	CH380 CSM1800				
		$V_{CC} = 16\text{V}$ $I_{F1} = I_{F2} = 16\text{mA}$	CD850			400	
Logic High Supply Current (See note 1)	I_{OCH}	$V_{CC} = 18\text{V}$, $I_F = 0\text{mA}$, I_F (other channel) = 20mA		-	0.4	10	μA
Input Forward Voltage (See note 1)	V_F	$I_F = 20\text{mA}$		-	1.45	1.9	V
Input Reverse Breakdown (See note 1)	V_{BR}	$I_R = 10\mu\text{A}$		3	-	-	V
Input-Output Insulation Leakage Current (See notes 3 & 9)	I_{IO}	$RH = 45\%$, $T_A = 25^{\circ}\text{C}$, $t = 5\text{S}$ $V_{IO} = 1500\text{VDC}$		-	-	1.0	μA
		$RH = 45\%$, $T_A = 25^{\circ}\text{C}$, $t = 5\text{S}$ $V_{IO} = 500\text{VDC}$	CH380				
Propagation Delay Time to Logic Low at Output (See note 1)	t_{PHL}	$R_L = 8.2\text{K}\Omega$, $I_F = 16\text{mA}$, $V_{CC} = 5\text{V}$ $C_L = 50\text{pF}$		-	0.4	2.0	μS
			$R_L = 1.9\text{K}$, $I_F = 16\text{mA}$, $V_{CC} = 5\text{V}$	CD850 CSM1800			
Propagation Delay Time to Logic High at Output (See note 1)	t_{PLH}	$R_L = 8.2\text{K}\Omega$, $I_F = 16\text{mA}$, $V_{CC} = 5\text{V}$ $C_L = 50\text{pF}$		-	2.0	6.0	μS
			$R_L = 1.9\text{K}$, $I_F = 16\text{mA}$, $V_{CC} = 5\text{V}$	CD850 CSM1800			

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Typical Characteristics

$T_A = 25^\circ\text{C}$

Parameter	Symbol	Test Conditions	Notes	Min	Type	Max	Units
Temperature Coefficient of Forward Voltage	$\frac{\Delta V_F}{\Delta T_A}$	$I_F = 20\text{mA}$	1	-	-1.9	-	mV/°C
Input Capacitance	C_{IN}	$f = 1\text{MHz}, V_F = 0$	1	-	125	-	pF
Resistance (Input-Output)	R_{I-O}	$V_{I-O} = 500\text{Vdc}$	1	-	10^{12}	-	Ω
Capacitance (Input-Output)	C_{I-O}	$f = 1\text{MHz}$	1 & 4	-	1.0	-	pF
Input-Input Insulation Leakage Current	I_{I-I}	45% Relative Humidity $V_H = 500\text{Vdc}, t = 5\text{S}$	5	-	1	-	pA
Capacitance (Input-Input)	C_{I-I}	$f = 1\text{MHz}$	5	-	0.6	-	pF
Transistor DC Current Gain	hFE	$V_O = 5\text{V}, I_O = 3\text{mA}$	1	-	130	-	-
Small Signal Current Transfer Ratio	$\frac{\Delta I_O}{\Delta I_F}$	$V_{CC} = 5\text{V}, V_O = 2\text{V}$	1	-	20	-	%
Common Mode Transient Immunity at Logic Low Level Output	CM_L	$I_F = 16\text{mA}, R_L = 8.2\text{K}\Omega$ $V_{CM} = 10\text{V}_{P-P}$ $V_O (\text{max}) = 0.8\text{V}$	1 & 7	-	-1000	-	V/ μS
Common Mode Transient Immunity at Logic High Level Output	CM_H	$I_F = 0\text{mA}, R_L = 8.2\text{K}\Omega$ $V_{CM} = 10\text{V}_{P-P}$ $V_O (\text{max}) = 2.0\text{V}$	1 & 6	-	1000	-	V/ μS
Bandwidth	BW	$R_L = 100\Omega$	8	-	2	-	MHz

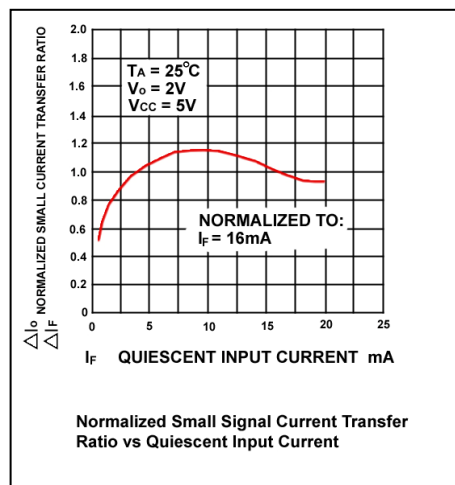
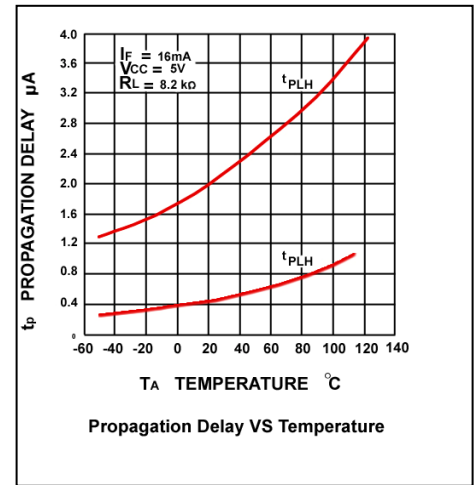
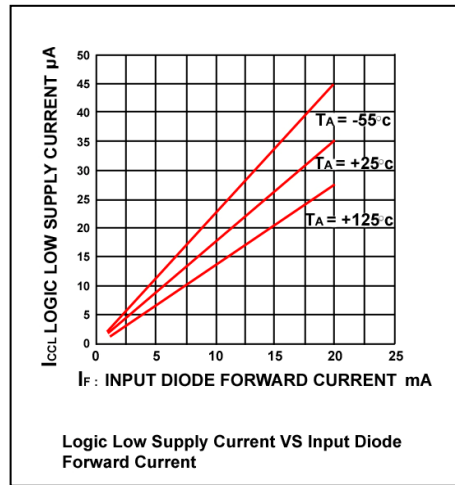
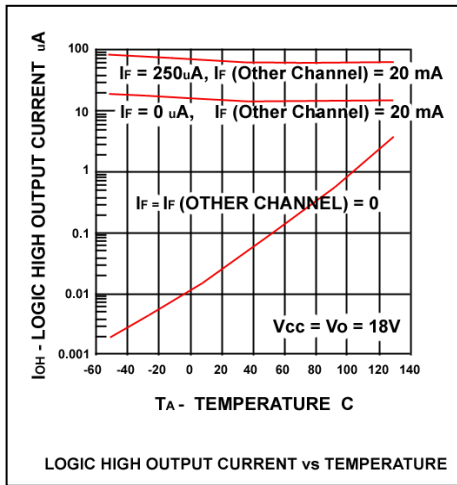
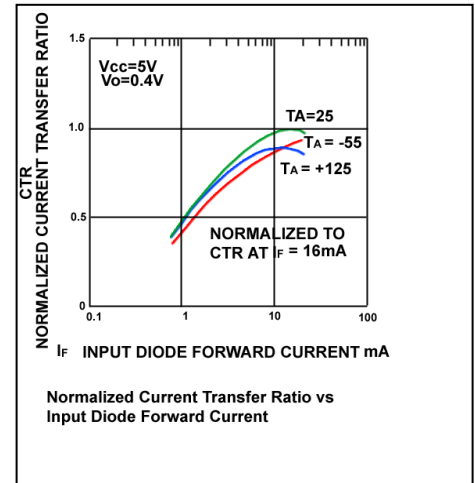
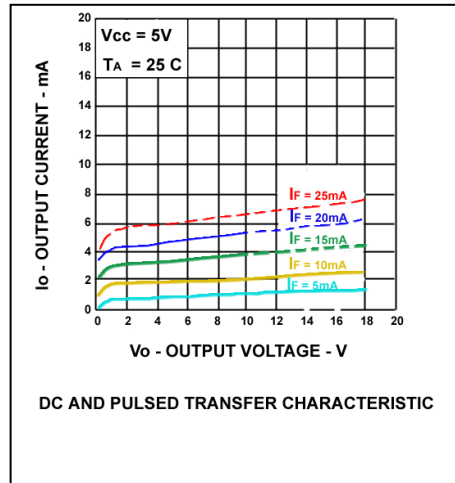
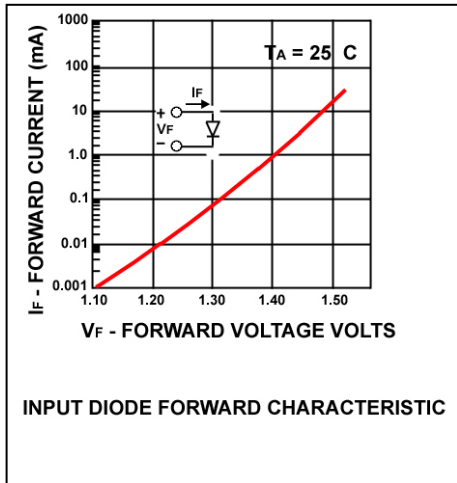
Notes (Apply typically to 16 pin package)

1. Each channel, where appropriate.
2. Current Transfer ratio is defined as the ratio of output collector current, I_O , to the forward LED input current, I_F , times 100%. CTR is known to degrade slightly over the unit's lifetime as a function of input current, temperature, signal duty cycle and system on time. It is recommended that designers allow at least 20-25% guard band for CTR degradation.
3. Measured between pins 1 through 8 shorted together, and pins 9 through 16 shorted together.
4. Measured between each input pair shorted together, and the output pins for that channel shorted together.
5. Measured between pins 3 and 4 shorted together, and pins 7 and 8 shorted together.
6. CM_H is the steepest slope (dV/dt) on the leading edge of the common mode pulse, V_{CM} , for which the output will remain in the logic high state (i.e., $V_O > 2.0\text{V}$).
7. CM_L is the steepest slope (dV/dt) on the trailing edge of the common mode pulse, V_{CM} , for which the output will remain in the logic low state (i.e., $V_O < 0.8\text{V}$).
8. Bandwidth is the frequency at which the AC output voltage is 3dB below the low frequency asymptote.
9. This is a momentary withstand test, not an operating condition.

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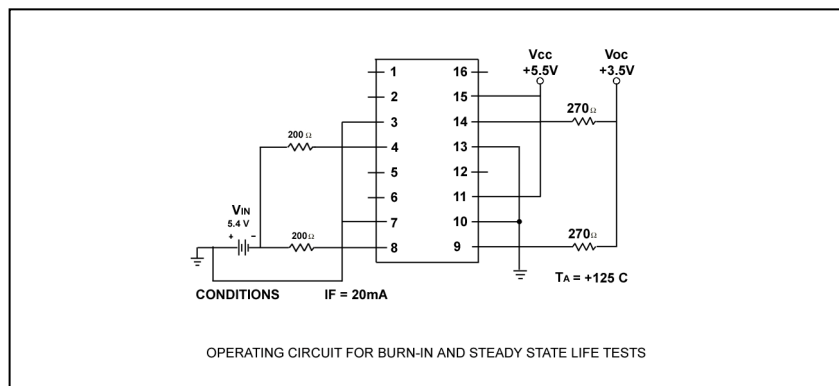
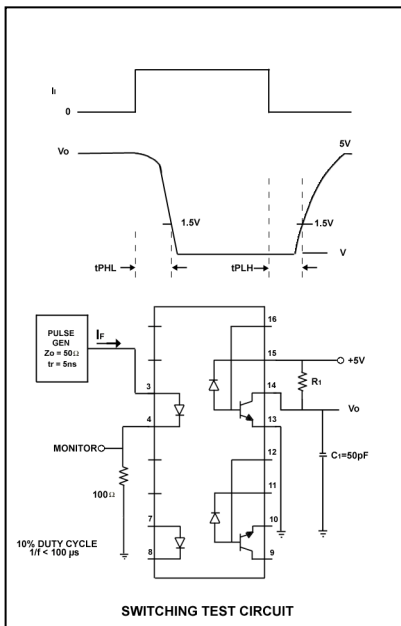
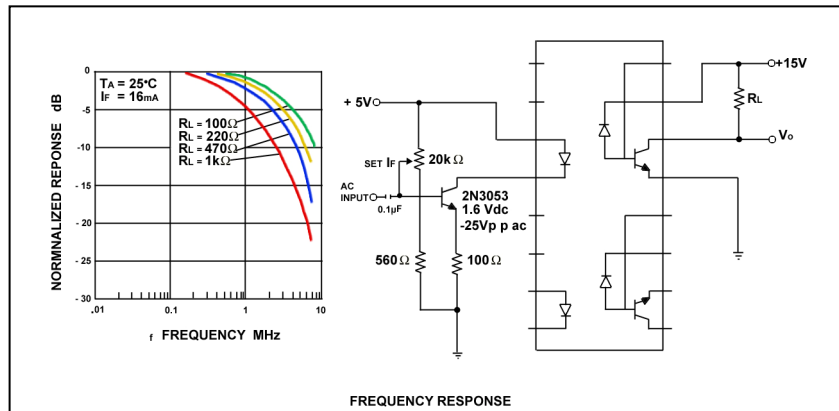
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Electrical Characteristics



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