SED1330

CMOS GRAPHIC LCD CONTROLLER

This part is replaced by SED1335. Some pin differences between SED1330 and SED1335 exist. Please check SED1335 data sheet. S-MOS Systems, Inc., will continue to support existing designs which use SED1330.

■ DESCRIPTION

The SED1330 is a CMOS low-power dot matrix liquid crystal graphic display controller. The device stores in external RAM display data sent by an 8-bit microcomputer, and generates all the signals required by the LCD drivers. The LSI incorporates an internal character generator ROM which supports user-defined characters (also an external CGROM can be supported).

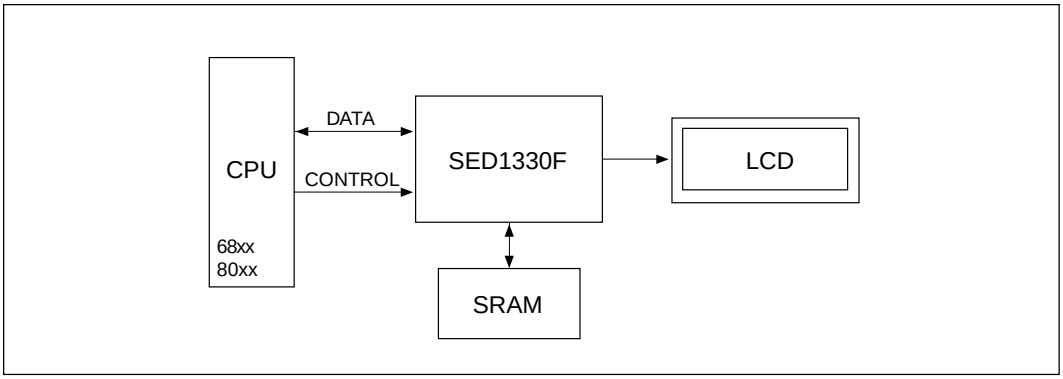
The SED1330 can be interfaced to high-speed microprocessors such as the Intel family or Motorola family. The controller supports a set of rich commands that will allow the user to create a layered display of characters and graphics.

Also, the controller functions as a pipeline buffer between the MPU and display memory so that low-cost, medium-speed SRAM can be used.

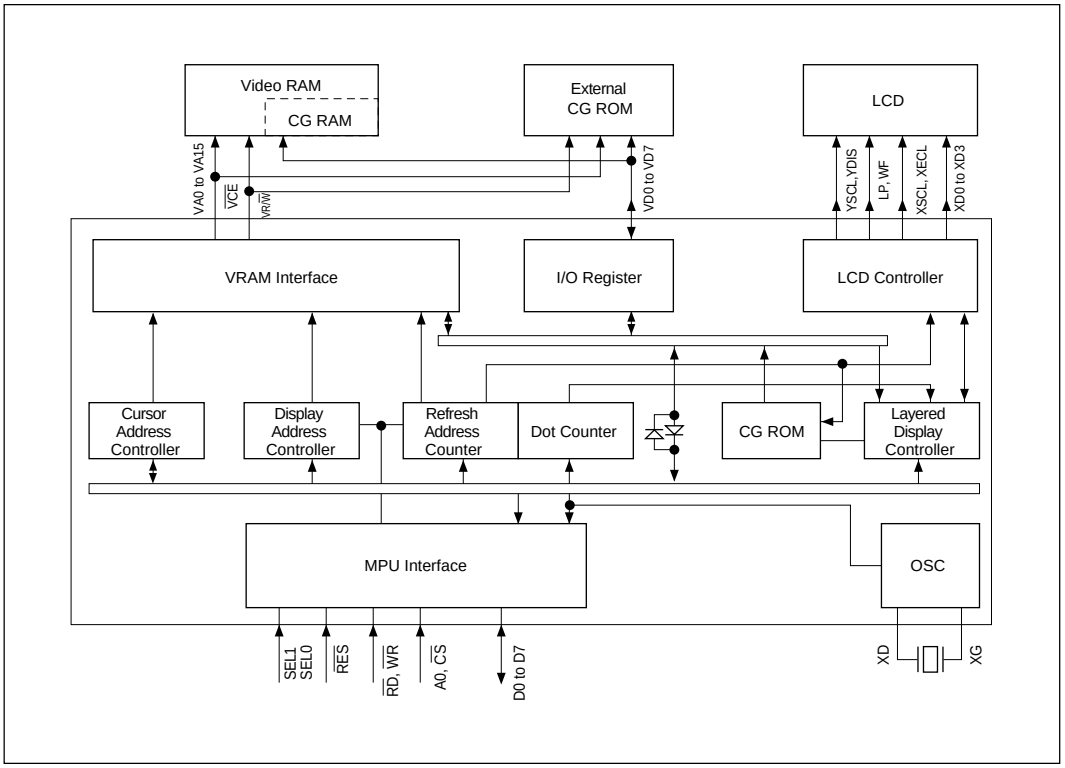
■ FEATURES

- CMOS low-power graphic and character display controller
- Selectable MPU interface is compatible with both the Intel family and the Motorola family
- Smooth scrolling support:
  Horizontal and vertical scroll
  Scrolling of selected areas of the display
- Multimode display:
  2 layers of overlapping character and graphics
  3 layers of overlapping graphics
- Selectable display synthesis:
  Inverse video
  Flashing display, cursor on/off/blink
  Under and bar cursor, block cursor
  Simple animation
- Programmable cursor
- Internal character generator ROM
- Supports external character generator ROM:
  8 × 8 or 8 × 16 pixel characters
  Allows mixing of ROM and RAM character sets
- Supports 64K bytes of memory:
  2 of 32K × 8 100ns SRAM
  or 8 of 8K × 8 100ns SRAM
- Display duty ..... 1/2 to 1/256
- Low power dissipation ..... 5mA (typical)
  0.05µA (typical), standby
- Logic power supply ..... 4.5 to 5.5V
- Package ..... Plastic QFP5-60 pin (FBA)
  Plastic QFP6-60 pin (FBB)

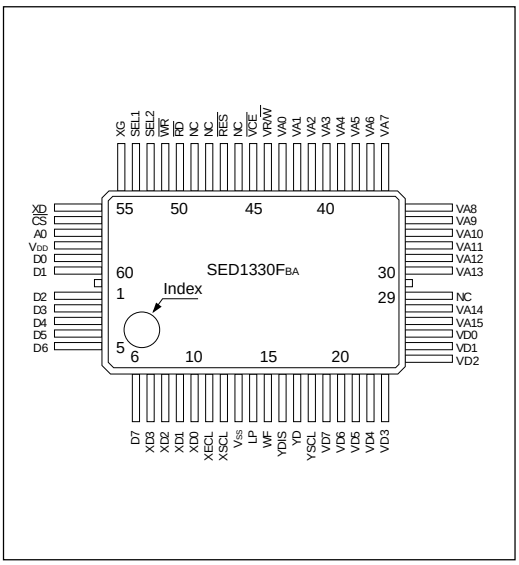
■ SYSTEM BLOCK DIAGRAM

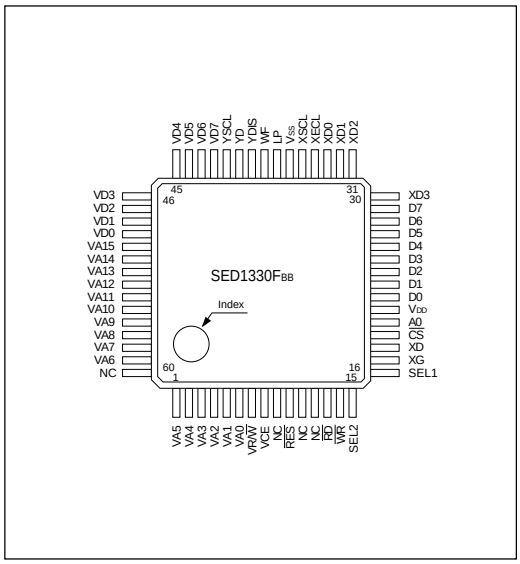


■ BLOCK DIAGRAM



■ PINOUT





■ PIN DESCRIPTIONS

Pin Name	Pin No.		I/O	Functions
	SED1330F$_{BA}$	SED1330F$_{BB}$		
XG	54	17	I	Oscillator terminal
XD	55	18	O	Oscillator terminal
V_{DD}	58	21	+5V	Power supply
V_{SS}	13	36	GND (0V)	Power supply
SEL1, 2	53 • 52	16 • 15	I	MPU interface format selection
D0 to D7	59 to 60 1 to 6	22 to 29	I/O	Data bus
A0	57	20	I	Data type selection
$\overline{RD}$	50	13	I	80 series Read strobe signal 68 series “E” clock
$\overline{WR}$	51	14	I	80 series Write strobe signal 68 series R/$\overline{W}$ signal
$\overline{CS}$	56	19	I	Chip select
$\overline{RES}$	47	10	I	Reset
VA0 to VA15	43 to 30 28 to 27	6 to 1 59 to 50	O	VRAM address bus
VD0 to VD7	26 to 19	49 to 42	I/O	VRAM data bus
VR/$\overline{W}$	44	7	O	VRAM R/$\overline{W}$ signal
$\overline{VCE}$	45	8	O	Memory control signal
XD0 to XD3	10 to 7	33 to 30	O	Dot data output bus to X driver
XSCL	12	35	O	Dot data shift clock for X driver
XECL	11	34	O	Chip enable shift clock for Y driver
LP	14	37	O	Dot data latch pulse
WF	15	38	O	Frame signal
YSCL	18	41	O	Scan data shift clock for Y driver
YD	17	40	O	Scan data output
YDIS	16	39	O	Power down signal when display OFF

NC: No Connection

■ ELECTRICAL CHARACTERISTICS

● Absolute Maximum Ratings

(V_{SS} = 0V)

Parameter	Symbol	Ratings	Unit
Supply voltage	V_{DD}	–0.3 to 7.0	V
Input voltage	V_I	–0.5 to V_{DD}+0.5	V
Power dissipation	P_D	300	mW
Operating temperature	T_{opr}	–20 to 75	°C
Storage temperature	T_{stg}	–60 to 150	°C
Soldering temperature and time	T_{sol}	260°C, 10s (at lead)	—

● DC ELECTRICAL CHARACTERISTICS

(V_{DD} = 5V±10%, V_{SS} = 0V, T_a = –20 to 75°C)

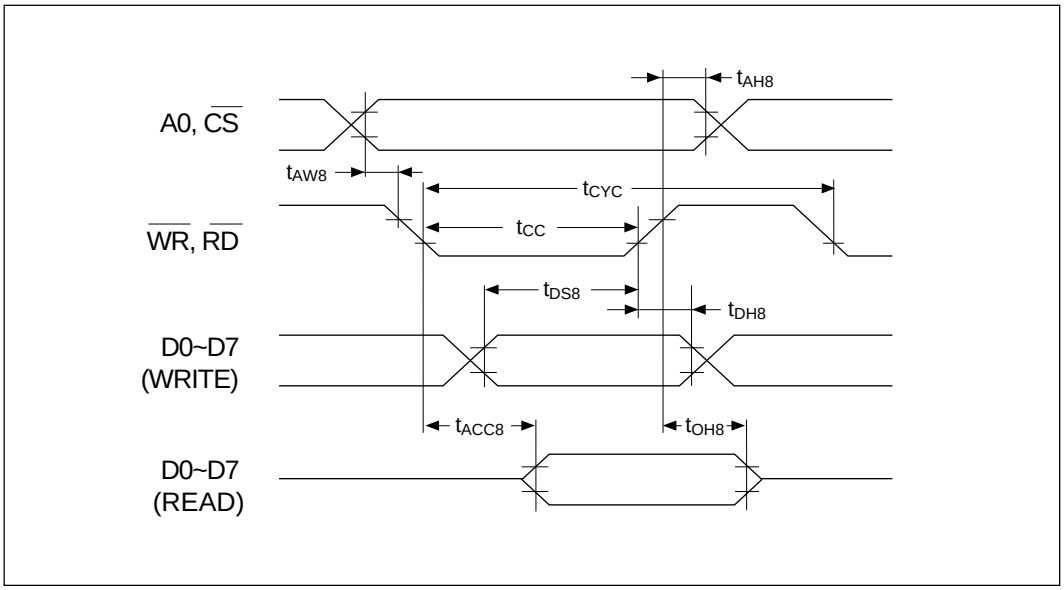
Parameter		Symbol	Condition	Min	Typ	Max	Unit
Operating voltage		V_{DD}		4.5	5.0	5.5	V
Register data retention voltage		V_{OH}		2.0	—	6.0	V
TTL	High level input voltage	V_{IHT}	D0 to D7, A0, $\overline{CS}$, $\overline{RD}$, $\overline{WR}$,	2.2	—	V_{DD}+0.3	V
	Low level input voltage	V_{ILT}	VD0 to VD7, I_{OH}= –5.0mA,	–0.3	—	0.8	V
	High level output voltage	V_{OHT}	I_{OL}=5.0mA, VR/$\overline{W}$, $\overline{VCE}$,	2.4	—	—	V
	Low level output voltage	V_{OLT}	$\overline{REF}$	—	—	0.4	V
CMOS	High level input voltage	V_{IHC}	I_{OH}=1.6mA, I_{OL}= –1.6mA,	0.8V_{DD}	—	—	V
	Low level input voltage	V_{ILC}	SEL1, 2, SYNC, YD, XD0 to	—	—	0.2V_{DD}	V
	High level output voltage	V_{OHC}	XD3, XSCL, XECL, LP, FR,	V_{DD}–0.4	—	—	V
	Low level output voltage	V_{OLC}	YSCL, YDIS, OSC1, OSC2	—	—	0.4	V
SCHMITT	Positive trigger threshold voltage	V_{T+}	$\overline{RES}$ *	0.5V_{DD}	0.7V_{DD}	0.8V_{DD}	V
	Negative trigger threshold voltage	V_{T-}		0.2V_{DD}	0.3V_{DD}	0.5V_{DD}	V
Input leakage current		I_{LI}	V_I=V_{DD} or V_{SS}	—	0.05	2.0	µA
Output leakage current		I_{LO}		—	0.10	5.0	µA
Average operating current		I_{DDA}	f_{OSC}=10MHz, No load (No external V-RAM) XG=$\overline{CS}$=V_{DD}	—	8	12	mA
Standby current		I_{DDS}		—	0.05	20	µA
Oscillation frequency		f_{OSC}	AT X'tal XG, XD	1.0	—	10.0	MHz
External clock frequency		f_{CLK}		—	—	10.0	MHz
Feed back resistance		R_f		0.5	1.0	5.0	MΩ

* $\overline{RES}$ input pulse should be longer than 1.0ms.

VL5 should be OFF when $\overline{RES}$ is "L".

● **AC CHARACTERISTICS**

○ **System Bus READ/WRITE Timing I (8080)**

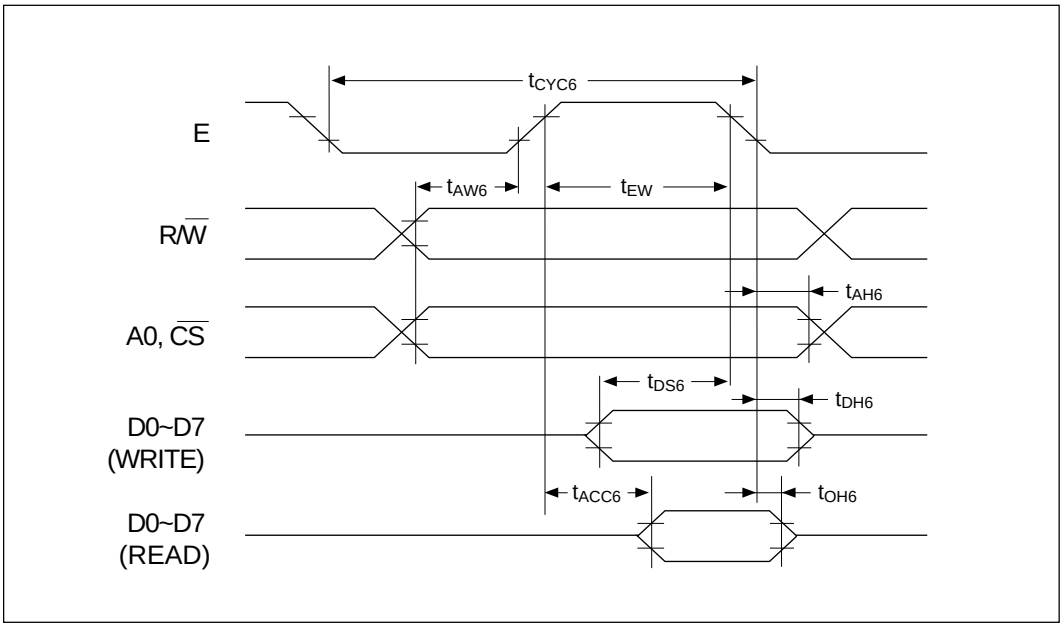


Signal	Parameter	Symbol	Rating		Unit	Remark
			Min	Max		
A0, $\overline{CS}$	Address hold time	t_{AH8}	10	—	ns	CL = 100 pF + 1TTL
	Address setup time	t_{AW8}	30	—	ns	
$\overline{WR}$, $\overline{RD}$	System cycle time	t_{CYC}	*1	—	ns	
	Control pulse width	t_{CC}	220	—	ns	
D0 to D7	Data setup time	t_{DS8}	120	—	ns	
	Data hold time	t_{DH8}	10	—	ns	
	$\overline{RD}$ access time	t_{ACC8}	—	120	ns	
	Output disable time	t_{OH8}	10	50	ns	

*1. $t_{CYC} = 2t_c + t_{CC} + t_{CEA} + 75 > t_{ACV} + 245$ ..... Memory control/movement control commands.

$= 4t_C + t_{CC} + 30$ ..... All other commands.

○ **System Bus READ/WRITE Timing II (6800)**



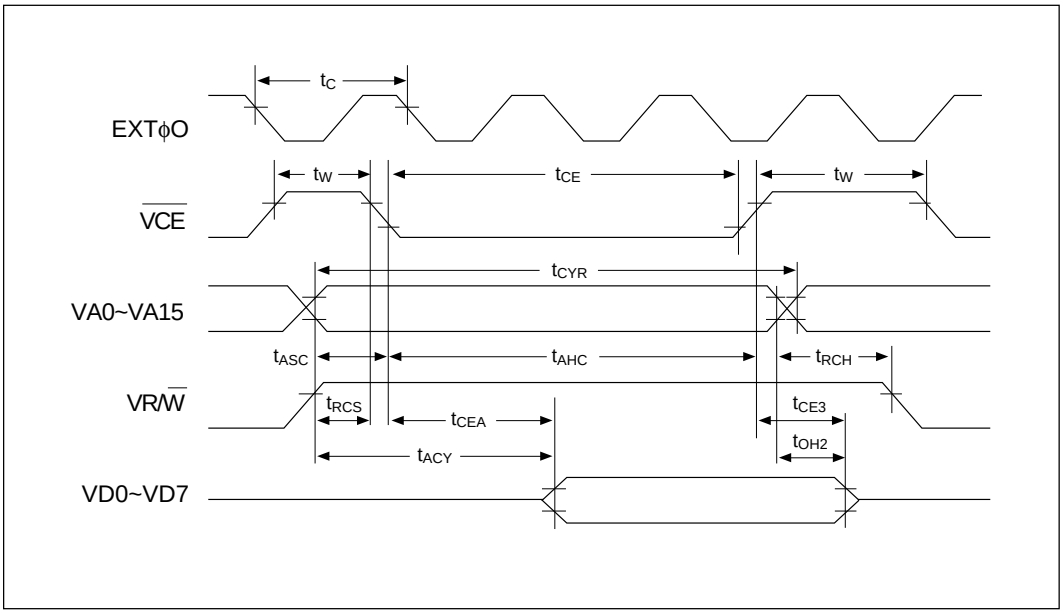
Signal	Parameter	Symbol	Rating		Unit	Remark
			Min	Max		
A0, $\overline{CS}$, R/$\overline{W}$	System cycle time	t_{CYC6}*1	*2	—	ns	CL = 100 pF + 1 TTL
	Address setup time	t_{AW6}	30	—	ns	
	Address hold time	t_{AH6}	10	—	ns	
D0 to D7	Data setup time	t_{DS6}	120	—	ns	
	Data hold time	t_{DH6}	10	—	ns	
	Output disable time	t_{OH6}	10	50	ns	
	Access time	t_{ACC6}	—	120	ns	
E	Enable pulse width	t_{EW}	220	—	ns	

*1. t_{CYC6} means a cycle of ($\overline{CS}$.E) not E alone.

*2. $t_{CYC6} = 2t_c + t_{EW} + t_{CEA} + 75 > t_{ACV} + 245$ ..... Memory control/movement control commands.

$= 4t_C + t_{EW} + 30$ ..... All other commands.

○ **Display Memory READ Timing**



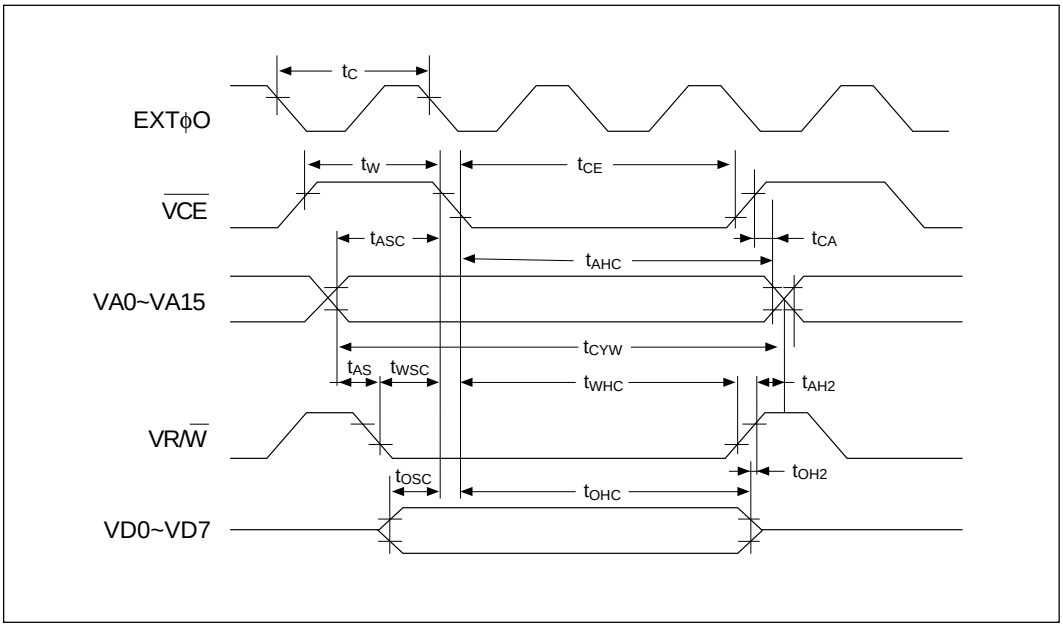
Signal	Parameter	Symbol	Rating		Unit	Remark
			Min	Max		
EXT ϕ0	Clock cycle	tC	100	—	ns	CL = 100 pF + 1TTL
$\overline{VCE}$	$\overline{VCE}$ high-level pulse width	tW	tC – 40	—	ns	
	$\overline{VCE}$ low-level pulse width	tCE	2tC – 40	—	ns	
VA0 to VA15	Read cycle time	tCYR	*1	—	ns	
	$\overline{VCE}$ address setup time (fall)	tASC	tC – 45	—	ns	
	$\overline{VCE}$ address hold time (fall)	tAHC	2tC – 40	—	ns	
VR/$\overline{W}$	$\overline{VCE}$ read cycle setup time (fall)	tRCS	tC – 45	—	ns	
	$\overline{VCE}$ read cycle hold time (fall)	tRCH	tc/2 – 35	—	ns	
VD0 to VD7	Address access time	tACV	—	*2	ns	
	$\overline{VCE}$ access time	tCEA	—	*3	ns	
	Output data hold time	tOH2	0	—	ns	
	$\overline{VCE}$ data off time	tCE3	0	—	ns	

*1. tCYR = 3tC

*2. tACV = 3tC – 120

*3. tCEA = 2tC – 120

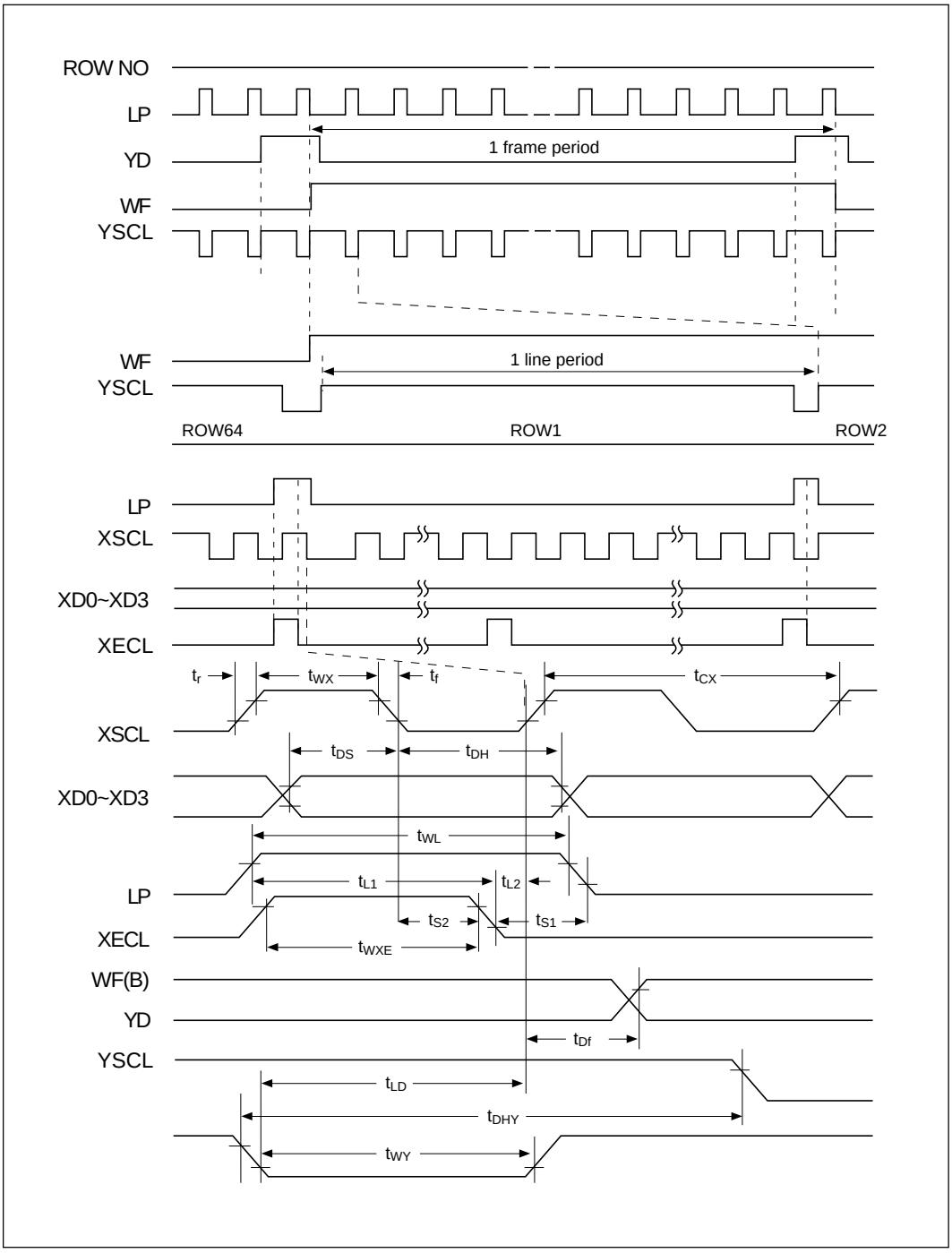
○ **Display Memory WRITE Timing**



Signal	Parameter	Symbol	Rating		Unit	Remark
			Min	Max		
EXT ϕ0	Clock cycle	tC	100	—	ns	CL = 100 pF + 1TTL
VCE	VCE HIGH-level pulse width	tW	tC – 40	—	ns	
	VCE LOW-level pulse width	tCE	2tC – 40	—	ns	
VA0 to VA15	Write cycle time	tCYW	3tC	—	ns	
	VCE address hold time (fall)	tAHC	2tC – 40	—	ns	
	VCE address setup time (fall)	tASC	tC – 55	—	ns	
	VCE address hold time (rise)	tCA	5	—	ns	
	VR/W address setup time (fall)	tAS	0	—	ns	
	VR/W address hold time (rise)	tAH2	15	—	ns	
VR/W	VCE write setup time (fall)	tWSC	tC – 55	—	ns	
	VCE write hold time (fall)	tWHC	2tC – 40	—	ns	
VD0 to VD7	VCE data input setup time (fall)	tDSC	tWSC – 10	—	ns	
	VCE data input hold time (fall)	tDHC	2tC – 30	—	ns	
	VR/W data hold time (rise)	tDH2	10*	50	ns	

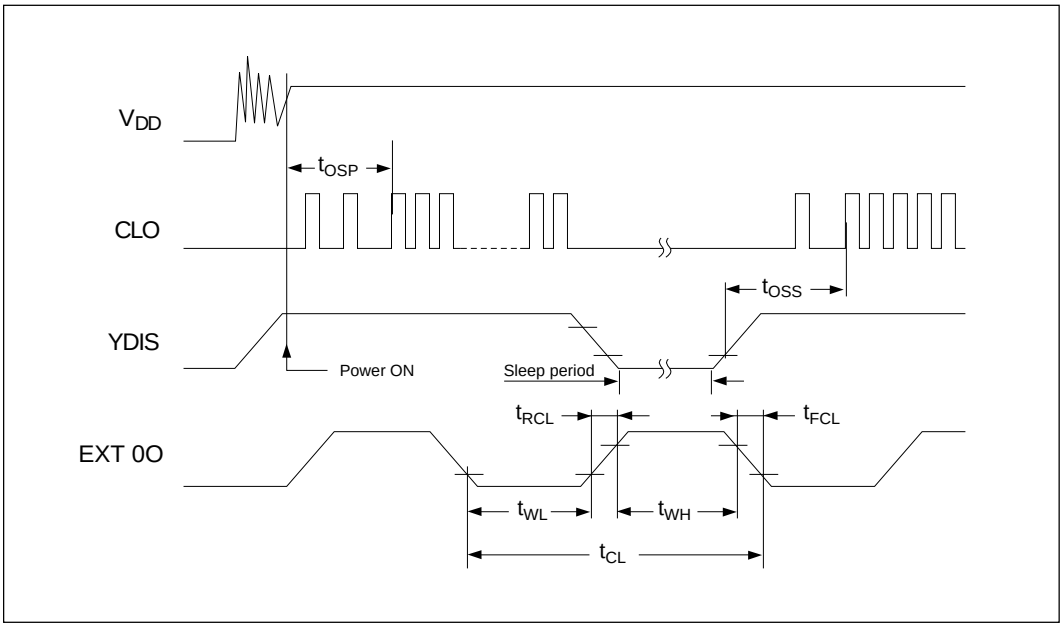
* Lines VD0 to VD7 are latched.

○ **LCD Control Timing**



Signal	Parameter	Symbol	Rating		Unit	Remark
			Min	Max		
EXT ϕ0	Clock cycle	t_C	100	—	ns	V_{DD} = 5.0V ± 10% CL = 150F
	Rising time	t_r	—	35	ns	
	Falling time	t_f	—	35	ns	
XSCL	Shift clock cycle time	t_{CX}	4t_C	—	ns	
	XSCL clock pulse width	t_{WX}	t_{CX2} – 80	—	ns	
XD0 to XD3	X-data hold time	t_{DH}	t_{CX2} – 100	—	ns	
	X-data setup time	t_{DS}	t_{CX2} – 100	—	ns	
LP	Latch data setup time	t_{LS}	t_{CX2} – 100	—	ns	
	LP signal pulse width	t_{WL}	t_{CX4} – 80	—	ns	
XECL	XECL setup time	t_{L1}	t_{CX3} – 100	—	ns	
	XECL data hold time	t_{L2}	t_C – 30	—	ns	
	Enable setup time	t_{S1}	t_C – 30	—	ns	
	Enable delay time	t_{S1}	t_C – 30	—	ns	
	XECL clock pulse width	t_{WXE}	t_{CX3} – 80	—	ns	
WF	Time allowance of WF delay	t_{DF}	—	100	ns	
YSCL	LP delay time against YSCL	t_{LD}	t_{CX4} – 100	—	ns	
	YSCL clock pulse width	t_{WY}	t_{CX4} – 80	—	ns	
YD	Y-data hold time	t_{DHY}	t_{CX6} – 100	—	ns	

○ **Oscillator Timing**

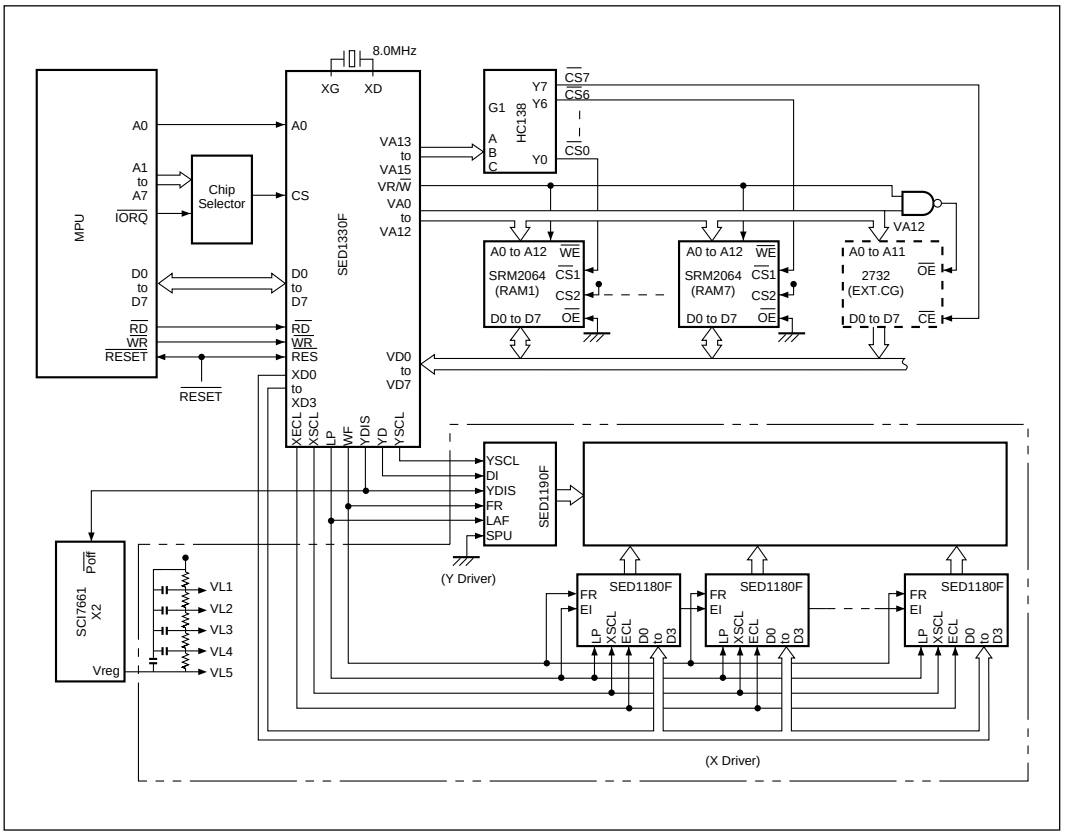


Signal	Parameter	Symbol	Rating		Unit	Remark
			Min	Max		
CLO	Time to stable CLO output after power-ON	t_{OSP}	—	3	ms	$\overline{RES}$ = H 20 pF
	Time to stable CLO after sleep OFF	t_{OSS}	—	1	ms	
EXT ϕ0	External clock rise time	t_{RCL}	—	15	ns	
	External clock fall time	t_{FCL}	—	15	ns	
	External clock high-pulse width	t_{WH}	*1	*2	ns	
	External clock low-pulse width	t_{WL}	*1	*2	ns	
	External clock cycle	t_{CL}	100	—	ns	

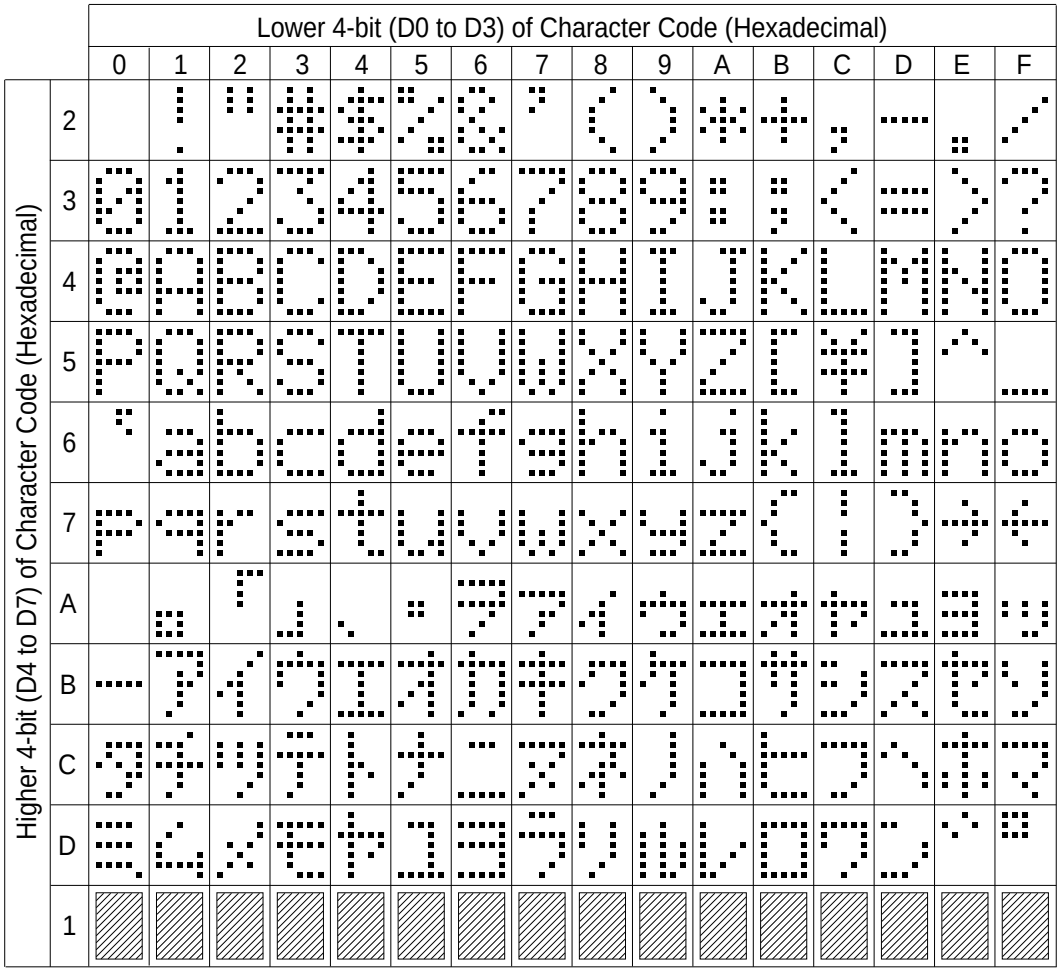
*1. $(t_C - t_{RCL} - t_{FCL}) \times 475/1000 < t_{WH}, t_{WL}$

*2. $(t_C - t_{RCL} - t_{FCL}) \times 525/1000 > t_{WH}, t_{WL}$

■ EXAMPLE OF APPLICATION



■ CHARACTER CODE TABLE (BUILT-IN CHARACTER GENERATOR)



Note: ▨ means all dots of 6 × 8 matrix are on.

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