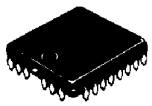
HD61945MP

PLL Synthesizer IC

The HD61945MP for PLL synthesizer Ic has been developed for cellular radio applications.

Features

- Incorporates an 11-bit counter for standard frequency, a 10-bit main counter for the comparative frequency and a 7-bit swallow counter.
- Low power dissipation in intermittent operation mode.



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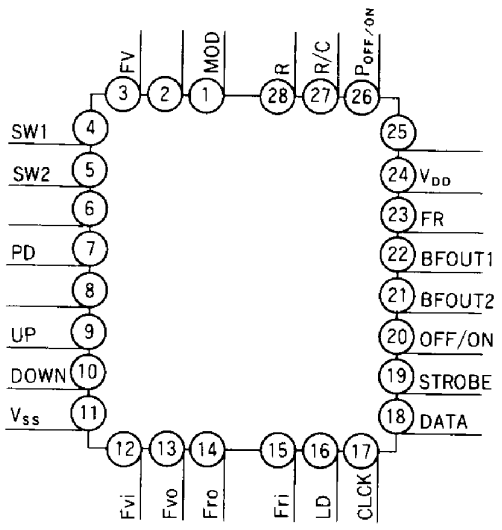
Pin Arrangement

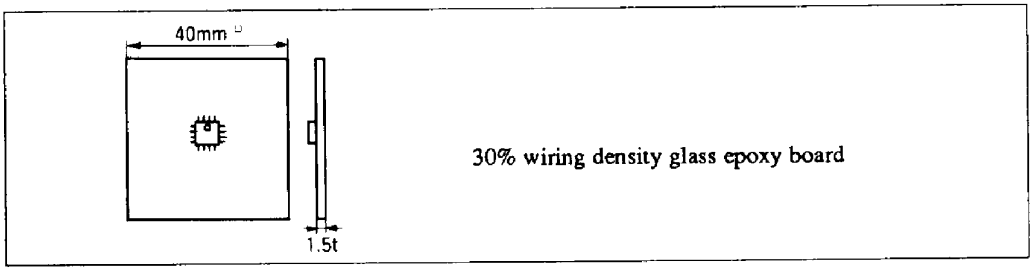


(Top View)

Absolute Maximum Ratings (Published specifications) (Ta = 25°C, Vss = 0 V)

Item	Symbols	HD61945MP	Unit	Notes
Supply voltage	$V_{DD\ max}$	7.0	V	*2
Input terminal voltage range	V_{IN}	–0.3 to V_{DD} + 0.3	V	
Power dissipation	Pd	500	mW	*1
Operating ambient temperature range	Topr	–30 to +75	°C	
Storage temperature range	Tstg	–55 to +125	°C	

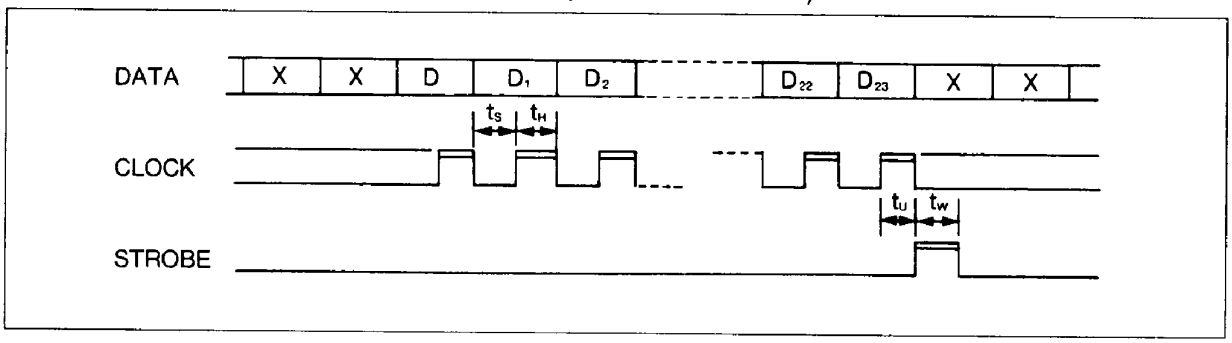
Notes: *1. For Ta = 75°C when mounted on a glass epoxy board.



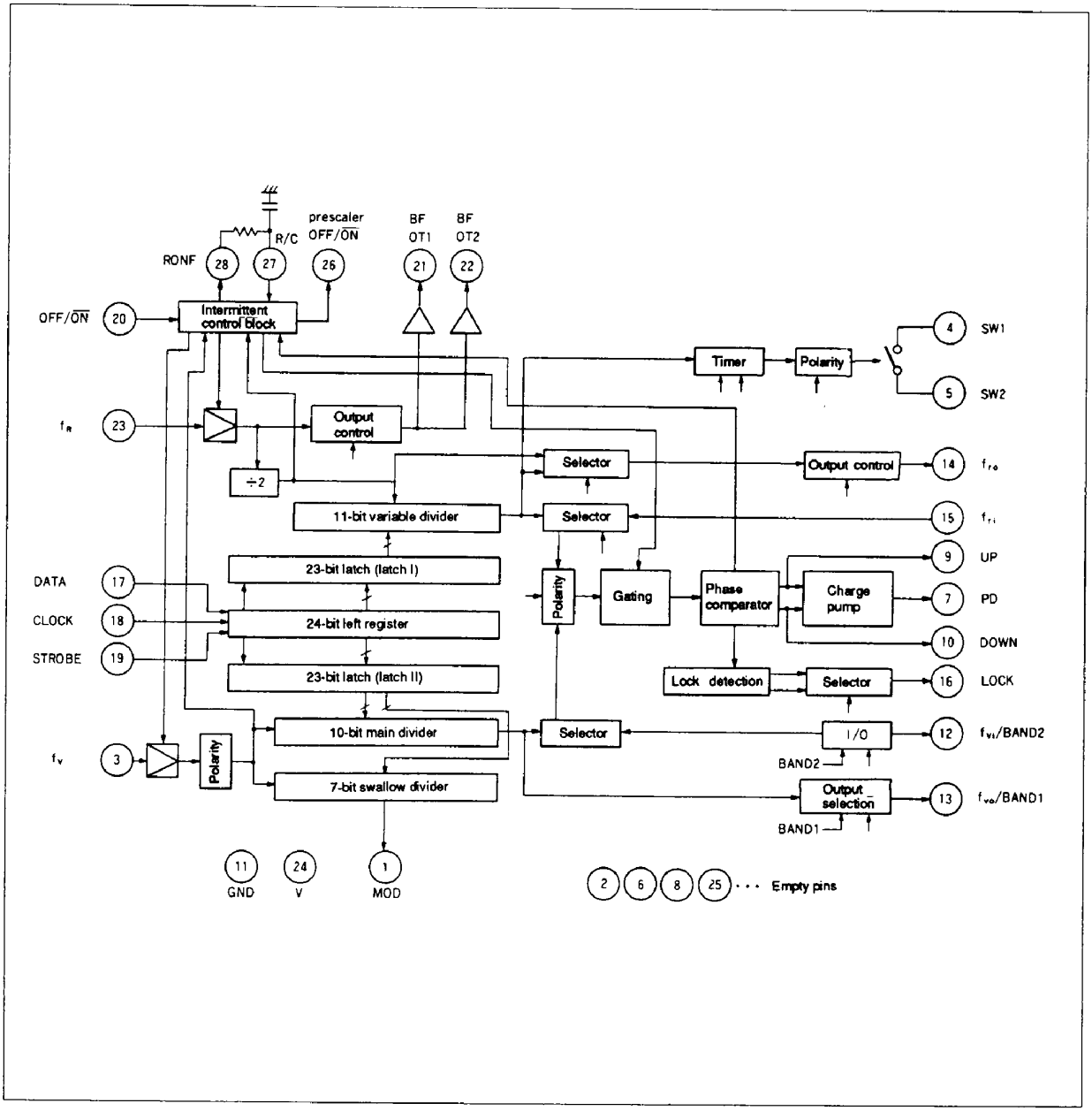
*2. Standard operating voltage should be 5.0 ± 0.25 V.

Data, Clock, Strobe Timing Chart

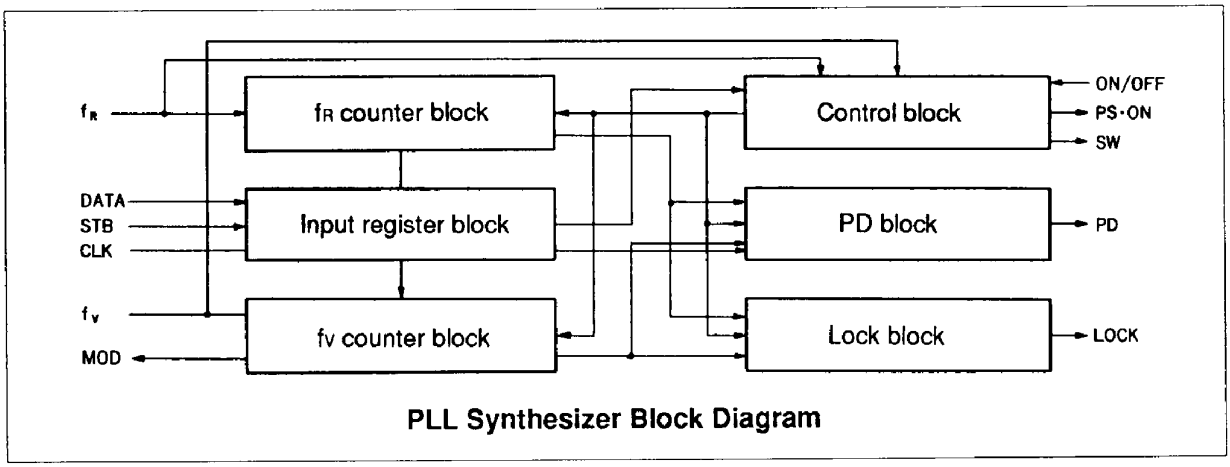
(ts, tH ≅ 500 ns or > 400 ns, tw ≅ 500 ns or > 400 ns, tv ≅ 500 ns or > 0 ns)



Block Diagram



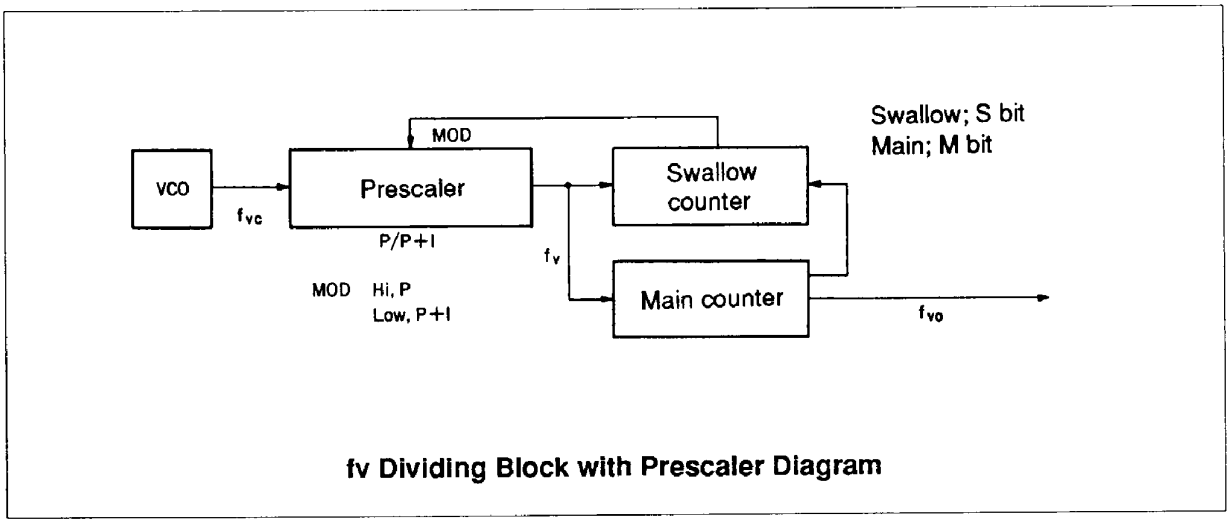
Block Functions



PLL Synthesizer Block Diagram

f_R counter block: The f_R consists of an 11-bit counter and a half divider. Reference frequency f_R is divided by the dividend at the input register pins.

fv counter block: The fv counter block consists of a 10-bit main counter 7-bit swallow counter. It determines the dividend with an external prescaler.



fv Dividing Block with Prescaler Diagram

Input register block: The input register block has two 24-bit registers and determines block setting values. It converts serial input signals to parallel format for input register.

PD block: The PD block sends acceleration or deceleration signals to VCO with a phase detector. It can reverse external inputs and signals, depending on values set at the input register.

Lock block: The lock block detects PLL lock status.

Control block: The control block controls block timing operations.

Pin Functions

Pin No.	Pin Name	I/O	Description	Remarks
1	MOD	O	Control signal output pin for the dual-modulus prescaler connected externally.	Set to "L" when pin 20 is "H."
2	NC	—		
3	FV	I	Input pin for the comparison divider. To connect to the prescaler, ac connection should be used because the amplifier incorporates a bias circuit.	
4	SW1	—	An analog switch is incorporated between pins 4 and 5. It switches on or off according to the strobe signals (pin 19) for the serial-data latch or the synchronous signals from the intermittent control block. Polarity is determined by D20 of the control register II. Switching time can be set to four modes by D21 and D22. Therefore, the switches can be used to change the VCOLPF characteristic.	Refer to Control register I and II.
5	SW2	—		
6	NC	—		
7	PD	O	Built-in charge pump output pin. Output polarity is set by D21 of control register I. PD output determined by the relation between reference divider output phase ϕr and comparison divider output phase ϕ is shown in the chart below.	Refer to Control register I.
8	NC	—		
9	UP	O	External charge pump output pin. Output polarity can be changed by D21 of control register I. Output determined by the relation between reference divider output phase ϕr and comparison divider output phase ϕv is shown in the chart below.	Refer to Control register I.
10	DOWN	O		
11	Vss	—		
12	Fvi/BAND2	I/O	When D18 of control register I is "0," pin 12 is in output mode and outputs the state of D19 of control register II to switch VCO band over. When D18 is "1," pin 12 is in input mode and external fv can be input to the phase comparator instead of the internal fv from the comparison divider.	Refer to Control register I and II.
13	Fvo/BAND1	O	When D19 of the control register is "0," pin 13 outputs the state of the control register II to switch VCO band over. When D19 is "1," the output from the comparison divider can be output from this pin.	Refer to Control register I and II.
14	FR0	O	When D_0 of the control register is "0," fr from the reference divider is output from pin 14. When D_0 is "1," the reference frequency input from pin 23 is reduced by half and is output from pin 14.	Refer to Control register I.

D_{21} set value	$\phi r > \phi v$	$\phi r = \phi v$	$\phi r < \phi v$
"0"	"H"	HiZ	"L"
"1"	"L"	HiZ	"H"

Pin Name	D_{21} set value	$\phi r > \phi v$	$\phi r = \phi v$	$\phi r < \phi v$
UP	"0"	"L"	"H"	"H"
	"1"	"H"	"H"	"L"
DOWN	"0"	"H"	"H"	"L"
	"1"	"H"	"H"	"H"

Pin Functions (continued)

Pin No.	Pin Name	I/O	Description	Remarks
15	FR1	I	External fr input pin. When D20 of control register I is "1," input signals from this pin are input to the phase comparator instead of the fr output signals from the reference divider.	Refer to Control register I.
16	LOCK	O	phase comparator lock detection pin. Outputs "H" when synchronizing. For output mode, either level output or pulse output can be chosen by D22 of control register I.	Refer to Control register I.
17	CLOCK	I	Reference clock input pin for serial data input to control registers I and II.	Pull down
18	DATA	I	Input pin for serial data to be input to control registers I and II. The last data D23 determines whether the data is latched into control register I or II.	Refer to Control register I and II. Pull down
19	STROB	I	Strobe signal input pin to latch the data into the control register. (Data is fetched when "H" signal is input.)	Pull down
20	OFF/ON	I	Phase synchronous dividing control signal input pin. When "L" is input, phase synchronous dividing is started and the state becomes operation mode. When "H" is input, the state becomes receive waiting mode.	Pull down
21 22	BFOUT2 BFOUT1	O O	Pin 23 fR inputs are output through the buffer. When D12 = "1," output is prohibited ("L" is fixed). Whe D12 = "0," signals are output through the butter.	Refer to Control register I and II.
23	FR	I	Reference signal(12 MHz) input pin. AC connection should be done with TCXO because the amplifier incorporates a bias circuit.	
24	V_{DD}	—		
25	NC	—		
26	D OFF/ON	O	Prescaler power on/off signal input pin. Input P off/on = "L" signal	
27	R/C	I	to turn on the prescaler power.	
28	RONF	O	Connect a register between pins 27 and 28 and ground a capacitor at pin 27. Then, set operation timing between the prescaler and this IC with a constant.	

HD61945 How to Use Latch

Bit	Latch I (Standard divider: $f_R \rightarrow fr0$) Name	Latch input data "0"	Latch input data "1"	Remarks	Name	Latch I (Variable divider: $fv \rightarrow fv\,0$) Latch input data "0"	Latch input data "1"	Remarks
D1	2N/+2	Output fr = f_R + 2N	Output fr = f_R + 2		LSB			
D2	LSB	$N_{TR} = 2 \times N$		When 2N/ + 2 = "1"		Total dividing frequency Ntv		
D3		N is specified as a binary number.		and f_REXT = "1,"		is specified as a binary		
D4				D1 to D11 are		number when the latch is		
D5		When 2N/ + 2 = "0,"		disregarded.		combined with the prescaler		
D6		N_{TR} can be specified as binary number.				128/129.		
D7				When 2N/ + 2 = "1"		(Ntv max = $2^{17} - 1$)		
D8				and fEXT = "0,"				
D9				f = f + 2N is				
D10				provided to PD.				
D11	MSB				MSB			
D12	f_R Buffer OUT	Output f_R to outside	Not output f_R to outside	f_R: Output buffer				
D13 D14 D15	for testing	O	Prohibited					
D16	for POLARITY	Falling clock	Rising clock	In combination with prescaler				
D17	fv OUTPUT	Not output fv to outside	Output fv to outside	fv0 outputting	(Reserve)			
D18	fv EXTERNAL	Internal fv	External fv	fv PD input selection	BAND1	VCO band switch data		fv OUTPUT = "0"
D19	fr OUTPUT	Not output fr to outside	Output fr to outside	fr 0 outputting	BAND 2			fv EXTERNAL = "0"
D20	fr EXTERNAL	Internal fr	External fr	fr PD input selection	SWITCH POLA	Switch is "ON" when timer is on.	Switch is "OFF" when timer is on.	Analog switch
D21	PD POLARITY	$\phi r \geq \phi v$: "H"	$\phi r > \phi v$: "L"	PD polarity (UP/DN) selection	Timer LSB	"0": T = 16 τ	"2": T = 64 τ	τ = 1/fr
D22	LOCK DETECT	Level output	Pulse output	"H" outputs during synchronizing.	Timer MSB	"1": T = 32 τ	"3": T = 128 τ	
D23	LATCH SELECT	—	O	Latch I selection	LATCH SELECT	O	—	Latch II selection

Electrical Characteristics (Ta = 25°C, V_{DD} = 5.0 V, V_{SS} = 0 V)

Item	Symbol	Test Conditions	Min	Typ	Max	Unit	Applicable pins	Notes
Supply voltage	V_{DD}		4.75	5.00	5.25	V	24	
Input voltage (1)	V_{IH1}		0.7 × V_{DD}	—	—	V	3, 15, 17, 18,	
Input voltage (2)	V_{IL1}		—	—	0.3 × V_{DD}	V	19, 20, 23	
Output voltage (1)	V_{OH}	–I_{OH} = 0.4 mA	V_{DD} - 0.4	—	—	V	1, 7, 9, 10, 12,	
Output voltage (2)	V_{OL}	I_{OL} = 0.4 mA	—	—	0.4	V	13, 14, 16, 21, 22, 26, 28	
Input leakage current (1)	$I_{IH(1)}$	V_{IN} = 5.0 V	—	—	1	µA	4, 5, 12	
Input leakage current (2)	$I_{IL(2)}$	V_{IN} = 0 V	–1	—	—	µA	4, 5, 12, 15, 17, 18, 19, 20, 27	
Operating current	I_{CC}	V_{DD} = 5.0 V	—	7.5	12.0	µA	30	*1
Three-state leakage current (1)	I_{ZH}	V_7 = 5.0 V	—	—	1	µA	7	
Three-state leakage current (2)	I_{ZL}	V_7 = 0 V	–1	—	—	µA	7	
Switch-on voltage	I_{4ON}		—	—	1	V	4	*2
Switch-off voltage	I_{4OFF}		4.2	4.5	—	V	4	*2
Input voltage (3)	V_{IH2}		4.1	—	—	V	12	
Input voltage (4)	V_{IL2}		—	—	0.8	V	12	

Notes: *1. Value when CH1 is locked (Rx = 915.03 MHz)

*2. Test with the measurement circuit in figure 1.

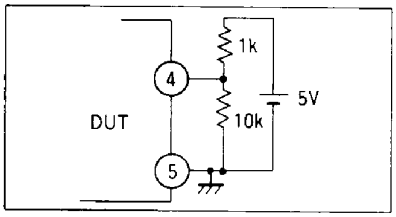


Figure 1

Pin No.	Signal Names		
	Clock Power Source	Input	Output
1			MOD
2		(N.C)	
3		FV	
4			SW1
5			SW2
6		(N.C)	
7			PD
8		(N.C)	
9			UP
10			DOWN
11	Vss		
12		Fvi	BAND2
13			Fvo
14			Fro
15		Fri	
16			LD
17	Clock	CLOCK	
18		DATA	
19		STROBE	
20		OFF/ON	
21			BF OUT2
22			BF OUT1
23		FR	
24	V_{DD}		
25		(N.C)	
26			P OFF/ON
27		R/C	
28			R

Notes on denotation: Terminals are denoted by tij, and non-used terminals are denoted by NC.

System Block Diagram