MITEL

SEMICONDUCTOR

SA866AE/AM
3-Phase Pulse Width Modulation Engine
Advance Information

The SA866AE/AM Motor Control IC has been designed specifically for Pulse-Width Modulation (PWM) control of induction motors used in appliances such as washing machines, HVAC equipment and in light industrial machinery such as machine tools.

The IC allows continuously variable speed via its 10-bit analog to digital converter and external direction pin.

Smooth acceleration and deceleration rates are defined using external resistors and capacitors and controlled by a patented algorithm, to prevent damage to the power electronics and/or load.

The IC controls both voltage and frequency via its PWM kernel ensuring that the motor flux is accurately controlled irrespective of the running frequency.

All parameters, including carrier frequency, waveform type, minimum pulse length, pulse underlap and voltage/frequency characteristics are programmed into the device at power up from a low cost EEPROM. Alternatively for very high volume applications, these may be mask programmed.

Comprehensive analog protection circuitry is provided to ensure reliable operation. All PWM outputs have a high current capability to allow direct drive of optocoupler isolation stages.

This IC may be used in a variety of cost-sensitive applications - particularly in domestic appliances. Since the PWM engine is capable of generating outputs much higher than the normal line frequency, this device is also suitable for high speed machine tools such as cutting and polishing equipment.

FEATURES

- Stand Alone Operation - No Micro Required.
- Analog Speed Input via 10-Bit ADC.
- All User Defined Parameters Held in External EEPROM.
- Factory Mask Programmed ROM for High Volume Applications.
- Specifically Designed for Control of Domestic Appliances and Light Industrial Equipment.
- Three Selectable Power Waveforms including Deadbanded Triplen for Reduced Losses.
- Linear and Fan Law V/f Characteristics.
- Acceleration and Deceleration Times Controlled by External RC.
- Variable Amplitude / Fixed Frequency Mode For Static Inverter Applications.
- Built-in High Current Output Drivers.
- Carrier Frequency Selectable up to 24KHz for Silent Operation.
- Wide Power Frequency Range 0 to 4KHz.
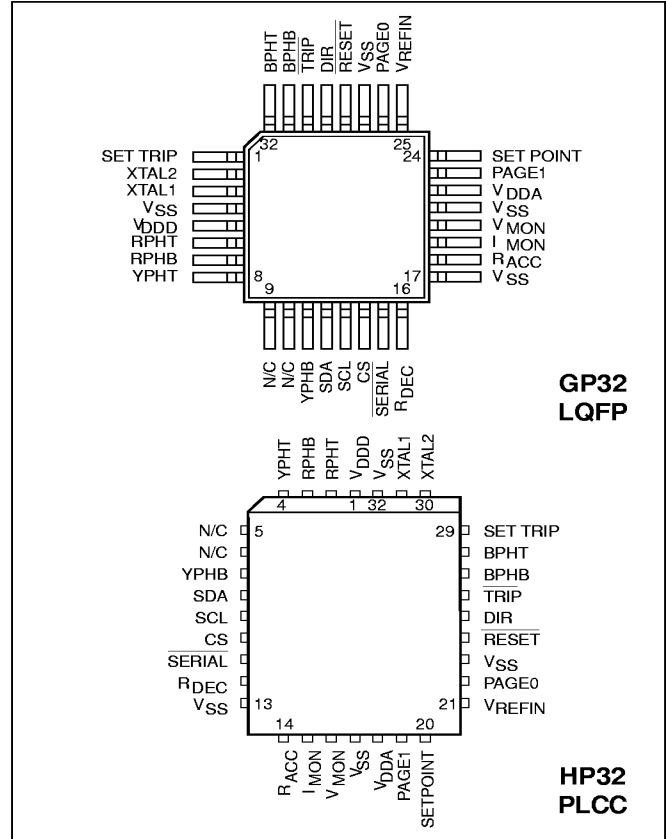- Selectable Minimum Pulse Width and Underlap Times.

Fig.1 Pin connections - top view

- Double Edged Regular Sampling.
- Serial Interface Mode.
- Boot-strapped Driver Precharge.

ORDERING INFORMATION
SA866AE/IG/GP1N
    32-Lead LQFP. EEPROM version.
SA866AE/IG/HP1N
    32-Lead PLCC. EEPROM version.
SA866AMXXX/IG/GP1N
    32-Lead LQFP. Mask Programmed version.
SA866AMXXX/IG/HP1N
    32-Lead PLCC. Mask Programmed version.

(Note: XXX = Customer specific variant number)

SA866AE/AM

ABSOLUTE MAXIMUM RATINGS

Supply voltage, V_{DD} 7V
Voltage on any pin V_{SS} −0·5V to V_{DD} +0·5V
Storage temperature   −55°C to +150°C
Operating temperature range   −40°C to +85°C

The temperature ranges quoted apply to all package types. Many package types are available. Further information is available on request.

Stresses above those listed in the Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions, or at any other condition above those indicated in the operations section of this specification, is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated) V_{DD} = 5V ±10%, T_{amb} = 25°C

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
Input High Voltage	V_{IH}	2	-	-	V	
Input Low Voltage	V_{IL}	-	-	0.8	V	
Input Low Current SET TRIP Input Page0, PAGE1, SERIAL Input All other Inputs	I_{IL}	 −1.0 −20 -	 - - -	 1.0 −115 10	 µA µA µA	V_{IN} = 0V, V_{DD} = 5.5V
Input High Current SET TRIP Input Page0, PAGE1, SERIAL Input All other Inputs	I_{IH}	 20 −1.0 -	 - -	 135 1.0 10	 µA µA µA	V_{IN} = V_{DD} = 5.5V
Output High Voltage	V_{OH}	4·0	4.5	-	V	I_{OH} = − 12mA
Output Low Voltage	V_{OL}	-	0.2	0.4	V	I_{OL} = +12mA
Static Supply Current	I_{DDS}	-	-	8	mA	O/Ps open cct.
Dynamic Supply Current	I_{DDD}	-	(TBD)	(TBD)	mA	XTAL = 25MHz
Supply Voltage	V_{DD}	4·5	5.0	5.5	V	
V_{MON} / I_{MON} Thresholds $(V_{thr} + V_{thf})/2$ $V_{thr} - V_{thf}$		 2.44 140	 $V_{DDA}/2$ 200	 2.56 320	 V mV	V_{DD} = 5·0V
Clock Frequency	f_{CLK}	15	-	25	MHz	
External Clock Duty Cycle	D_{CLK}	40	-	60	%	
SET TRIP = 1 to outputs tripped and $\overline{TRIP}$ = 0	f_{TRIP}	$3/f_{CLK}$	-	$4/f_{CLK}$	s	
Minimum Reset Period at power on	t_{RST}	-	$2CR_{ACC}$	-	s	
R_{ACC}/R_{DEC} Freq. range	t_{AD}	0.5	-	100	KHz	
ACC/DEC Defeat Threshold	V_{DTF}	-	$0.125V_{DDA}$	-	V	
DIR Debounce Period	I_{DBNCE}	-	$1/2f_{CARR}$	$3/4f_{CARR}$	s	

ADC CHARACTERISTICS

Parameter	Min.	Typ.	Max.	Unit.
Resolution	-	10	-	bits
Reference Voltage, Vref	$0.4V_{DD}$	$0.5V_{DD}$	$0.6V_{DD}$	V
Input Voltage Range	0	-	Vref	V
Differential Linearity	-	-	±0.5	lsb
Integral Linearity	-	-	±2	lsb
Zero Offset	-	-	±2	lsb
Input Impedance	1	-	-	MΩ
Conversion Rate	-	4	-	Samples/carrier cycle
Conversion Time		$27/1000f_{CLK}$		

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PIN DESCRIPTIONS

Package Type		Name	Type	Function
GP32	HP32			
1	29	SET TRIP	I	Set Output Trip. Active High. Internal pulldown
2	30	XTAL2	I/O	Clock Crystal connection
3	31	XTAL1	I	Clock Crystal connection
4	32	V_{SS}	P	Ground
5	1	V_{DDD}	P	Positive supply – Digital
6	2	RPHT	O	Red Phase Top
7	3	RPHB	O	Red Phase Bottom
8	4	YPHT	O	Yellow Phase Top
9	5	NC	-	Not connected
10	6	NC	-	Not connected
11	7	YPHB	O	Yellow Phase Bottom
12	8	SDA	I/O	EEPROM / Serial Data
13	9	SCL	I/O	EEPROM / Serial Clock
14	10	CS	I/O	EEPROM / Serial Chip Select
15	11	$\overline{SERIAL}$	I	EEPROM / Serial Mode Select. Internal pullup
16	12	R_{DEC}	I	External RC – Sets deceleration Osc. Rate
17	13	V_{SS}	P	Ground
18	14	R_{ACC}	I	External RC – Sets acceleration Osc. Rate
19	15	I_{MON}	I	Overcurrent - Forces deceleration. Active High
20	16	V_{MON}	I	Overvoltage - Inhibits Accel / Decel. Active High
21	17	V_{SS}	P	Ground
22	18	V_{DDA}	P	Positive Supply – Analog
23	19	PAGE1	I	EEPROM Page Select-1. Internal pullup
24	20	SETPOINT	I	Analog Power Freq. / Amplitude input
25	21	V_{REFIN}	I	ADC Voltage Reference
26	22	PAGE0	I	EEPROM Page Select-0. Internal pullup
27	23	V_{SS}	P	Ground
28	24	$\overline{RESET}$	I	External Reset – Active Low
29	25	DIR	I	External Direction
30	26	$\overline{TRIP}$	O	Trip Latch Status – Active Low
31	27	BPHB	O	Blue Phase Bottom
32	28	BPHT	O	Blue Phase Top

NOTES: (i) V_{DDA} and V_{DDD} pins must be connected together externally, and also all V_{SS} pins must be connected together externally.

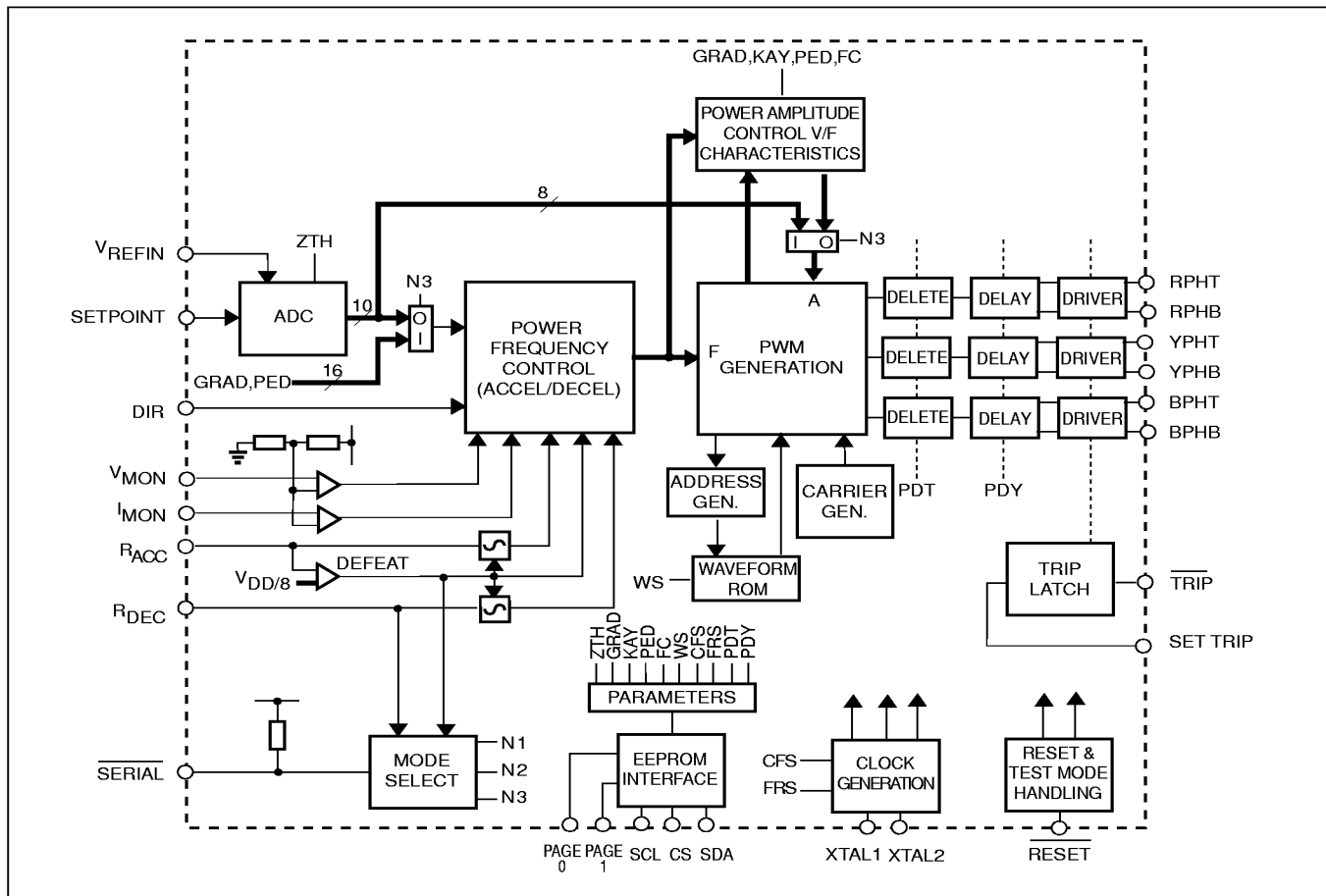(ii) PAGE0 and PAGE1 inputs are not used on the SA866AM variant.

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SA866AE/AM

Fig.2a SA866 block diagram - normal mode

FUNCTIONAL DESCRIPTION

The SA866AE/AM is a digital pulse width modulation (PWM) generation core with peripheral blocks to allow control of parameters which affect the PWM data stream and to enable the pulse train to be optimised for driving power switch inverter circuits.

The device may be operated in a number of modes which generally fall into 2 areas: normal and serial. Fig.2a shows a block diagram for the device operating in normal mode; serial mode is dealt with later.

A PWM data stream arises from the comparison of a reference waveform and a carrier waveform, the PWM output changing state whenever the two are equal. For power control applications, the reference is known as the power waveform. Three power waveform shapes are available to the user, stored in digital form in on-chip waveform ROM. These are then scaled in the frequency and amplitude domains before comparison with the carrier. Sinusoid, Triplen and Deadbanded Triplen waveforms are available, the last two offering the potential for increased drive efficiency and reduced losses in the power switches compared to the use of a sinusoid power waveform.

Power frequency is normally controlled by an analog control voltage level applied to the SETPOINT input. This voltage is converted to a digital value by a fast 10 bit ADC; this value becomes the new target (setpoint) power frequency for the ACCEL/DECEL block. The ACCEL/DECEL block allows smooth changes between power frequencies controlled by on-chip oscillators. The frequency of these oscillators is controlled by external resistors and capacitors attached to the R_{ACC} and R_{DEC} pins, allowing independent control of acceleration and deceleration respectively. Internally, the power frequency is represented by 16 bit values allowing smoother acceleration and deceleration than the 10 bit setpoint frequency might suggest.

Two further inputs, V_{MON} and I_{MON} may be used to control acceleration and deceleration in the ACCEL/DECEL block. These override the normal frequency changing function by limiting deceleration or forcing deceleration to zero respectively. This mechanism may be used to provide over-voltage and over-current protection for the power switches.

In normal operation the amplitude of the power waveform is controlled by the device using either a linear or quadratic (Fan-law) dependence on the power frequency. Three parameters are available to the user to define the shape of the characteristic: gradient and pedestal for the linear characteristic, and a third factor for defining the shape of
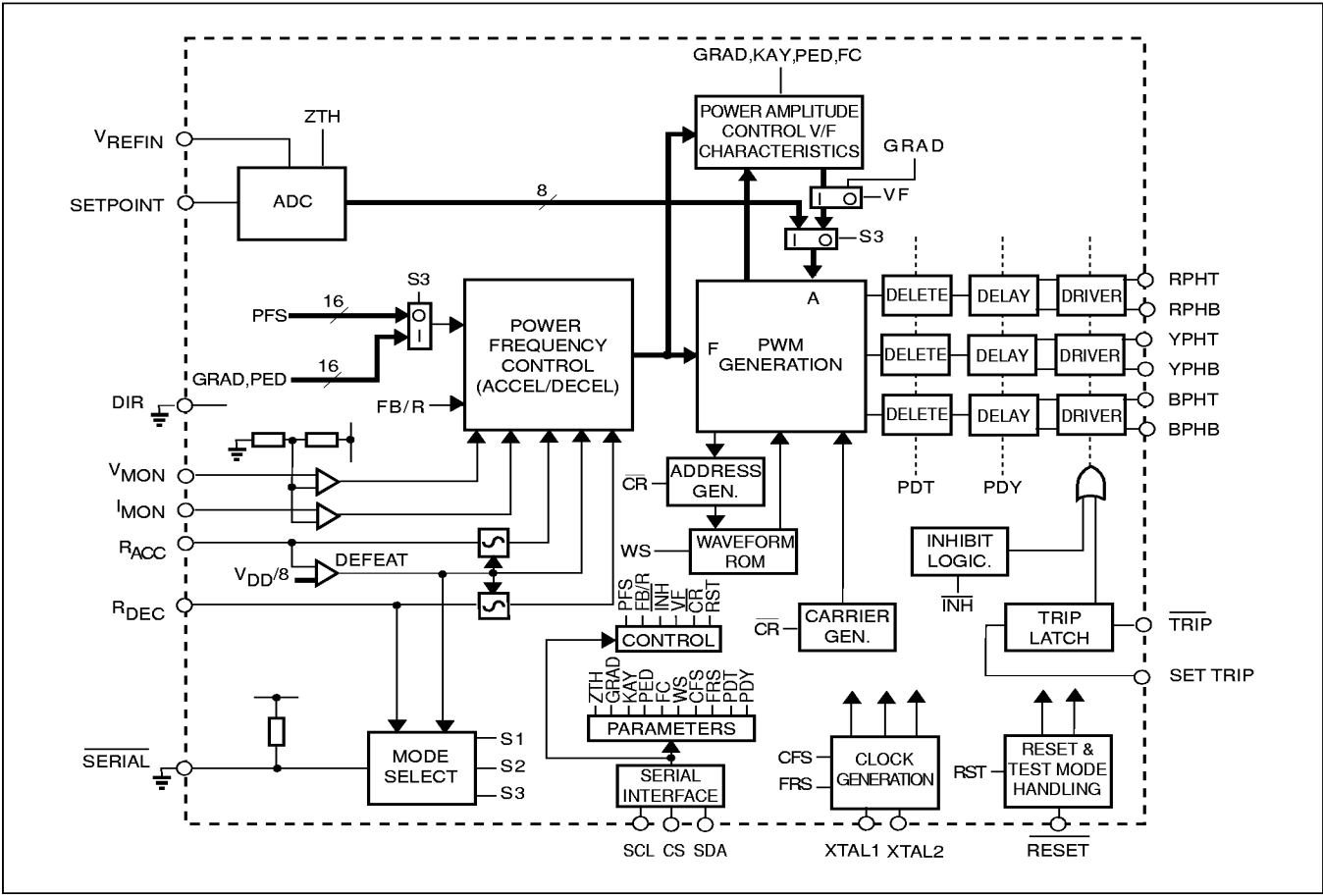
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Fig.2b SA866 block diagram - serial interface mode

the Fan-law curve.

A mode is available where the power frequency is fixed (using the amplitude parameters) and the amplitude is varied using a control voltage at the SETPOINT input.

The raw output from the PWM generation block is processed by pulse deletion and pulse delay blocks before being output as complementary pairs of signals for driving top and bottom switches for each of red, yellow and blue phases. The pulse deletion block allows the definition of the minimum length pulse to appear on the PWM outputs using a user-specified parameter. The pulse delay block introduces a user specifiable period during which top and bottom phase outputs are both switched off, thus avoiding shoot-through problems.

To facilitate the use of bootstrap driver circuits for the power switches, whenever the phase outputs are restarted after they have all been shut down, the bottom phase outputs are all pulsed high for a whole carrier cycle before normal operation is resumed. This gives a time during which the bootstrap capacitors may be charged before any top switch is driven.

An input, SET TRIP, is provided to enable rapid shutdown of all phase outputs in the event of an emergency.

The phase outputs are driven by fast, high-current output drivers so that they may drive opto-isolators and gate driver ICs directly.

All user defined parameters are digital. In normal operation, the values are down-loaded from an external serial EEPROM chip following reset using a MICROWIRE type 3-wire serial interface (the SA866AE acts as bus master). One of four pages of data may be downloaded from the EEPROM, the page being defined by the start address transmitted from the SA866AE and the number of data bits to be downloaded.

On SA866AMXXX devices, the user defined parameters are mask programmed avoiding the need for the serial EEPROM. No automatic download is initiated after reset.

An on-chip clock oscillator allows the use of an external crystal or ceramic resonator to provide a stable, accurate clock.

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MODE SELECTION

	MODE	RACCEL	RDECEL	SERIAL	Use Serial PROM
N1	NORMAL MODE ADC CONTROLLED FREQUENCY ACC/DEC ENABLED	Ext.RC	Ext.RC	1	Y
N2	NORMAL MODE ADC CONTROLLED FREQUENCY ACC/DEC DEFEATED	$<0.125V_{DD}$	$<0.5\ V_{DD}$	1	Y
N3	NORMAL MODE ADC CONTROLLED AMPLITUDE ACC/DEC DEFEATED	$<0.125V_{DD}$	$>0.5\ V_{DD}$	1	Y
S1	SERIAL INTERFACE MODE ADC DISABLED ACC/DEC ENABLED	Ext.RC	Ext.RC	0	N
S2	SERIAL INTERFACE MODE ADC DISABLED ACC/DEC DEFEATED	$<0.125V_{DD}$	$<0.5\ V_{DD}$	0	N
S3	SERIAL INTERFACE MODE ADC CONTROLLED AMPLITUDE ACCEL/DECEL DEFEATED	$<0.125V_{DD}$	$>0.5\ V_{DD}$	0	N

Table 1: Mode selection

The SA866AE/AM offers various modes of operation as shown in Table 1.

Modes N1 – N3 are selected by setting the $\overline{\text{SERIAL}}$ pin to a logic '1' or leaving it open circuit. (The $\overline{\text{SERIAL}}$ input has an internal pull-up resistor to V_{DD}). *These are the normal (stand-alone) operating modes and are described below.*

Modes S1 – S3 are selected by setting the $\overline{\text{SERIAL}}$ pin to a logic '0'. These are the serial modes of operation, which instead of using an EEPROM, use a microprocessor / microcontroller to serially load the initialisation parameters. *These modes are described in detail under the Serial Interface section.*

Mode N1

This is the standard operating mode. The power frequency is set by an external analog voltage applied to the ADC input SETPOINT. External RC networks connected to the R_{ACC} and R_{DEC} pins control the rate of change of Power Frequency as defined by the formula in the Acceleration/Deceleration Logic section. The power waveform output amplitude is controlled by the V/f characteristic defined by the GRAD, PED and KAY parameters.

Mode N2

This mode is selected by applying fixed voltage levels to the R_{ACC} and R_{DEC} pins. Under these conditions the acceleration / deceleration feature is defeated and the power waveform frequency follows changes made to the SETPOINT input voltage instantaneously. The output amplitude is still controlled by the V/f characteristic as defined by the GRAD, PED and KAY parameters, as in Mode N1.

Mode N3

In this mode the ADC input controls the power waveform amplitude, (to 8-bit resolution). The Power Frequency is fixed to a 16-Bit value defined by the GRAD and PED values loaded from the serial EEPROM. GRAD Bit-7 is the MSB and PED Bit-0 the LSB. The DIR pin is used to control the phase order (rotational direction).

When R_{ACC} is $<0.125V_{DD}$ i.e. acceleration and deceleration oscillators defeated, the internal capacitor discharge transistor for the deceleration oscillator is disabled to prevent contention when using the R_{DEC} pin for mode selection.

The use of R_{ACC} and R_{DEC} pins to select modes imposes a requirement that when acceleration / deceleration oscillators are used, the $\overline{\text{RESET}}$ input must be held low long enough to guarantee that the 0.125 V_{DD} defeat threshold is crossed. Failure to do this may result in an incorrect mode being selected.

The $\overline{\text{SERIAL}}$ pin has an internal pull-up to V_{DD}, (nominally 40µA), so it can be left open-circuit in Normal (Stand-alone) mode.
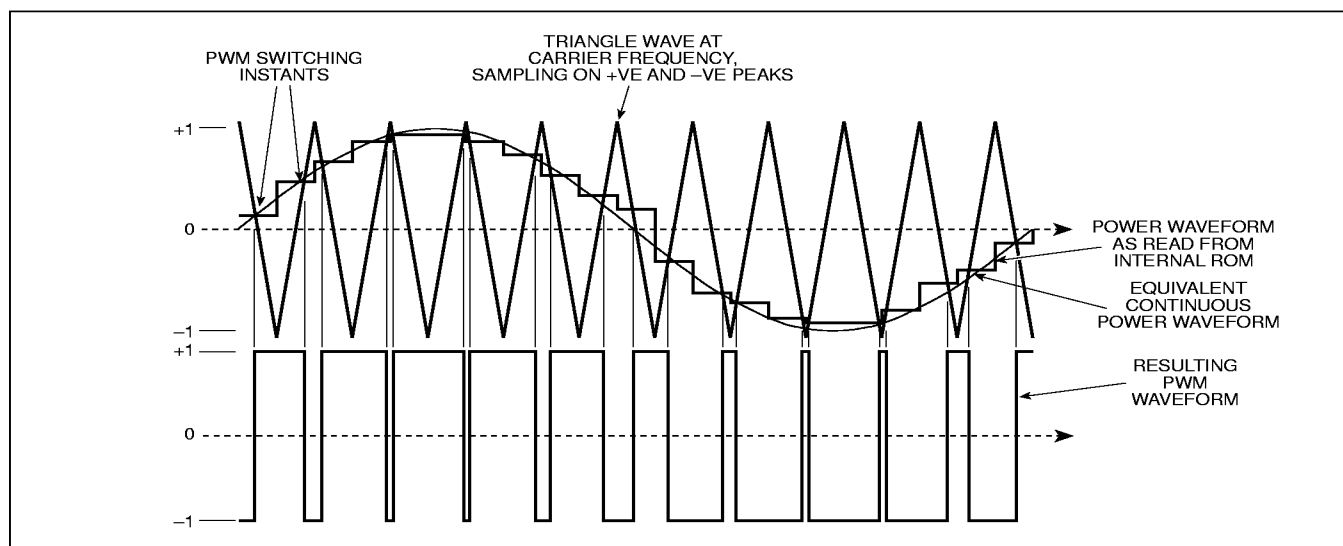
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Fig.3 Asynchronous PWM generation with double-edged regular sampling as used by the SA866

PWM GENERATION LOGIC

An asynchronous method of PWM generation is used in uniform or 'double-edged' regular sampling of the waveform(s) stored in the internal ROM as illustrated in Fig.3.

In general, a pulse width modulation signal is derived by comparing a signal waveform, (in this case the power waveform), with a saw-tooth or triangular carrier waveform of significantly higher frequency. The intersections between the two waveforms, in the time domain, define the locations of transitions in the digital output train, and hence the width of the output pulses. The width of the pulses are directly proportional to the magnitude of the power waveform, thus the larger the magnitude, the longer the 'ON' pulse.

The SA866AE/AM uses a digital implementation of this technique which avoids drift problems associated with the use of analog circuitry. A triangular waveform is synthesised using an up/down counter and a digital comparator is used to compare this with the power waveform. The power waveform is sampled regularly at every peak and trough of the carrier waveform allowing both edges of the PWM output pulse to move in time, hence the term 'double-edged' regular sampling. (A saw-tooth carrier waveform would result in one fixed edge and one moving edge for each PWM pulse.)

The power waveform(s) are stored digitally in on-chip ROM (1536 samples per 360°). The power frequency is controlled by the rate at which the ROM is addressed – a rate which is not related to the carrier frequency on the SA866AE/AM, hence the term 'asynchronous method of PWM generation'. The waveform values obtained from the ROM may also be scaled to produce a variable voltage amplitude.

Fig.3 shows the triangular carrier waveform together with the stepped waveform which results from sampling the outputs of the ROM at the peaks and troughs of the carrier. (A continuous power waveform is also shown for reference.) It can be seen that the PWM edges of the waveform below are obtained at the points where the carrier and the sampled power waveform intersect. The carrier frequency is selectable to over 24KHz (assuming the maximum clock frequency of 25MHz is used), enabling ultrasonic operation for noise critical applications. With a 25MHz clock, power frequency ranges to over 4KHz are possible. Using the ADC input, the resolution of the setpoint frequency is reduced to 10-bits, but during acceleration and deceleration, or when the power frequency is set from other sources, the resolution used is 16 bits. The output phase sequence of the PWM outputs can also be changed to allow both forward and reverse motor operation. (Phase order convention for "forward" is Red-Yellow-Blue, and "reverse" is Red-Blue-Yellow.)

PWM output pulses can be 'tailored' to the inverter characteristics by defining the minimum allowable pulse width, (the SA866AE/AM will delete all shorter pulse from the 'pure' PWM pulse train), and the pulse delay (underlap) time, without the need for external circuitry. This gives cost advantages in both component savings and in allowing the same PWM circuitry to be used for the control of different motor drive circuits simply by changing the defined parameters stored in external EEPROM.
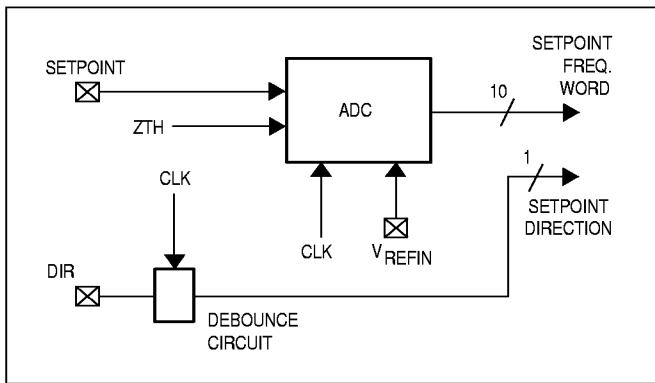
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SA866AE/AM

Fig.4 Speed selection block

SPEED SELECTION

The speed selection block contains a 10-Bit Analog to Digital Converter with Sample and Hold circuit, plus a Zero Threshold Offset circuit.

The ADC performs a single ended conversion to 10-Bit resolution of the voltage applied to the SETPOINT input. Full scale input range is zero to V_{REFIN}. The ADC has two states: sampling/autozeroing and converting. The voltage sample from the SETPOINT input is frozen at the beginning of every quarter carrier cycle and a unipolar conversion of this value made. Conversion time is approx. $27/1000*f_{CARR}$ after which the input returns to the sampling/autozeroing state. Both the sample and hold circuit and the ADC are controlled by internal logic.

An adjustable zero threshold feature is provided for the ADC allowing the selection of 4 different zero levels on the SETPOINT input. The purpose of this is to 'de-sensitise' the zero input level so that, even when the control input voltage has a small offset, the output Power Frequency can be set to zero Hertz. (For example, when driving a motor, this will ensure that when the control input is set to minimum the motor is brought to rest.)

The threshold value is set according to a 2 bit value (ZTH) programmed from the serial EEPROM. The threshold is set on the binary output from the ADC, which means that the setpoint speed will jump from 0 to threshold value in binary terms as the threshold is reached. This only represents an instantaneous jump in Power Frequency if the acceleration and deceleration oscillators are not used.

A small amount of hysteresis is built into the thresholds to prevent the outputs being rapidly enabled/disabled due to noise at the ADC input.

Table 2 shows the effect of programming ZTH. Note that an input range of 0 to 2.5V is assumed for the ADC, corresponding to a 10 bit binary output of all 0s to all 1s.

The location of the ZTH bits in the EEPROM and Serial memory maps are shown in Tables 6 and 13. Zero Thresholds are also applicable in the ADC Controlled Amplitude mode (N3 and S3).

Direction (determined by the order of the three output phases RYB - forward, RBY - reverse) is set using the DIR input. This input is debounced such that the input must remain stable for $3/4f_{CARR}$.

It should be noted that both the DIR and SETPOINT inputs provide target values rather than instantaneous values (unless the acceleration and deceleration oscillators are defeated). Changes of speed occur 1 bit (of a 16 bit internal power frequency word) at a time, at the rate(s) determined by the frequency of the acceleration and deceleration oscillators.

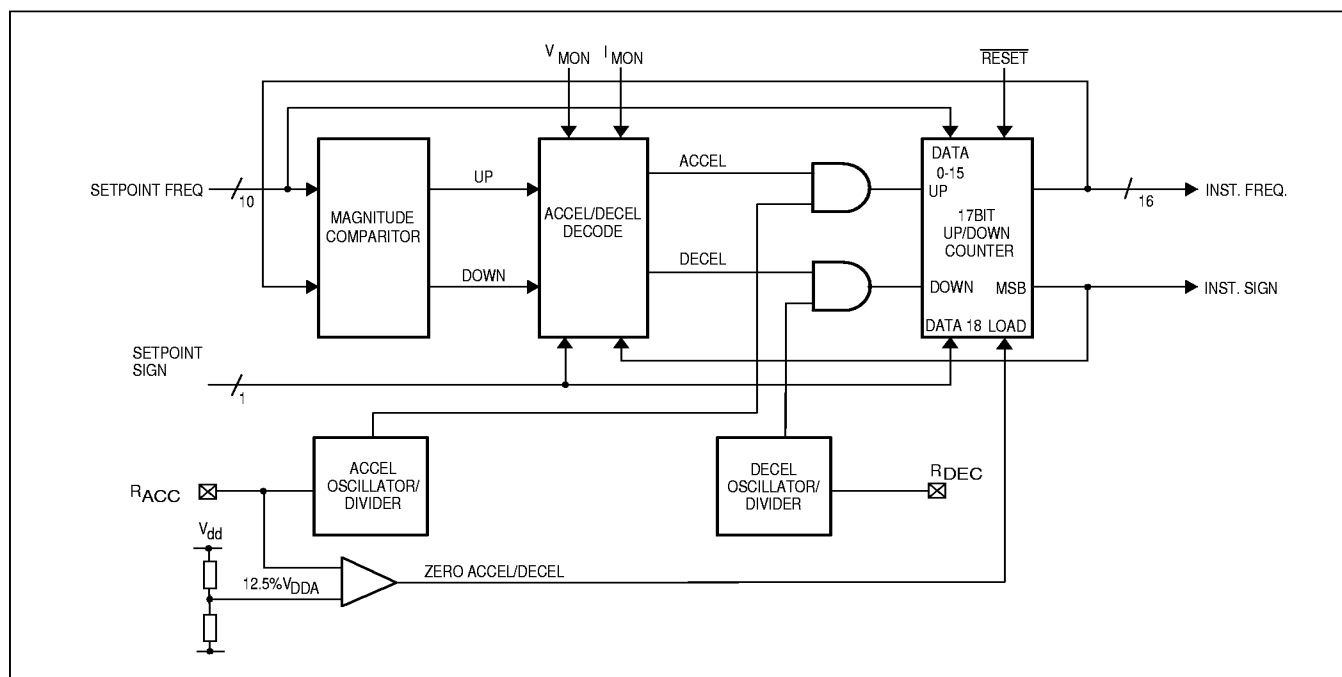| ZTH <1:0>	RISING THRESHOLD (mV)	FALLING THRESHOLD (mV)	RISING THRESHOLD (Binary)	FALLING THRESHOLD (Binary)
00	0	0	0	0
01	50	39	10100	10000
10	100	78	101000	100000
11	200	156	1010001	100000)

Table 2: Zero threshold values

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Fig.5 Acceleration/deceleration logic

ACCELERATION / DECELERATION LOGIC

The acceleration/deceleration block consists of a 16-bit magnitude comparator and an 17-bit up/down counter clocked by the output from the Accel or Decel oscillators. The acceleration and deceleration rates are seperately selectable using external timing components. A resistor (R) is connected from the R_{ACC} pin to V_{DD} and a capacitor (C) from the R_{ACC} pin to V_{SS}. Similary a separate RC network is connected to the R_{DEC} pin. The values of the resistors and capacitors may be the same or different to produce equal or unequal acceleration and deceleration times.

The time taken to accelerate from zero to the maximum speed value determined by the selected Power Frequency range (f_{RANGE}), or to decelerate from this value to zero is given by the expression:

$$t_{ACC/DEC} = 65536 \times R.C \times \ln 3$$

$$\cong \mathbf{72.10^3 \times R.C}$$

where $\mathbf{5K\Omega \leq R \leq 100K\Omega}$
$\mathbf{1nF \leq C \leq 25nF}$

If the R_{ACC} pin is connected to a level <$0.125V_{DD}$, the Accel/Decel function is defeated and any changes in Power Frequency demand are instantaneous. This makes the device suitable for waveform generation applications such as UPS or Static Inverters.

It is possible to drive the R_{ACC} and R_{DEC} inputs directly with an external clock signal(s), instead of using the RC oscillators. Typical input levels are $V_{IL} = 0.3V_{DD}$ and $V_{IH} = 0.6V_{DD}$ but care must be taken to ensure that the low level does not go below $0.125V_{DD}$ and the high level above $0.75V_{DD}$.

The former may cause the device operating mode to be changed inadvertently; the latter may cause contention on the pin as the internal oscillator pull-down transistor switches on.

The magnitude comparator compares the scalar frequency demand from the ADC with the instantaneous scalar frequency output from the up/down counter. The result is a 2-bit output as follows:-

UP	DOWN	Result
0	0	Same, No ACCEL or DECEL
0	1	LOWER
1	0	HIGHER
1	1	ILLEGAL STATE

Table 3 Acceleration/deceleration decoder

These 2 bits are used in conjunction with the V_{MON} and I_{MON} pins and the sign bits to obtain an absolute indication of the required acceleration/deceleration, according to the following rules:-

1) If the V_{MON} condition is invoked ($V_{MON} \geq 0.5V_{DD}$), any acceleration/deceleration will be prevented until V_{MON} falls below $0.5V_{DD}$. This condition has highest priority.

Normal acceleration/deceleration will continue when V_{MON} falls below $0.5V_{DD}$, as dictated by the rest of the algorithm.

This input is used to prevent excessive deceleration rates from regenerating too much power into the external power switching circuitry and causing an overvoltage condition.

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CONDITION	UP	DOWN	REQD. DIRECTION	INSTANT- ANEOUS DIRECTION	ACCEL	DECEL
					Active High	
1.	X	X	0	1	0	1
2.	X	X	1	0	0	1
3.	0	0	0	0	0	0
4.	0	0	1	1	0	0
5.	0	1	0	0	0	1
6.	0	1	1	1	0	1
7.	1	0	0	0	1	0
8.	1	0	1	1	1	0
9.	1	1	X	X	ILLEGAL STATE	

Table 4: Acceleration/deceleration logic conditions

2) If I_{MON} is invoked (i.e. $\geq 0.5V_{DD}$) the scalar value of the instantaneous frequency is reduced at the predetermined deceleration rate irrespective of the states of UP and DOWN. If the instantaneous frequency attains the value zero whilst I_{MON} is $\geq 0.5V_{DD}$ the PWM outputs are turned off (logic 0) for the duration of this condition (this prevents undue motor heating whilst at rest). No acceleration or deceleration is allowed once the frequency has attained the value zero. When I_{MON} is released normal acceleration/deceleration resumes as required by the prevailing conditions. In addition, the PWM outputs are re-enabled.

This condition has lower priority than V_{MON} since the act of decelerating due to I_{MON} being taken high may itself invoke the V_{MON} condition.

This input is intended to prevent too high an acceleration rate from causing an overcurrent/overheat situation at the switching devices.

3) If I_{MON} and V_{MON} are inactive, the algorithm takes the UP and DOWN outputs from the magnitude comparator, together with the required sign from the DIR pin and the instantaneous sign from the up/down counter to compute whether acceleration or deceleration is required:-

(a) If the required and instantaneous signs are different, the first requirement is to decelerate to rest since no change of direction is possible until this has occurred. Therefore, so long as this condition holds, decelerate (see 1 and 2 in Table 4).

(b) If the signs are the same and UP and DOWN are both zero then the required and instantaneous frequencies are matched both in terms of direction and magnitude, therefore neither acceleration or deceleration is required (see 3 and 4 in Table 4).

(c) If the signs are the same but either UP or DOWN is high then the phase order (direction of rotation), does not need to change, but the magnitude does. Therefore, if UP is high, accelerate or if DOWN is high, decelerate (see 5,6,7 and 8 in Table 4).

(d) UP and DOWN both high is an illegal state since both conditions cannot exist concurrently.

The ACCEL and DECEL signals are gated with the Accel or Decel oscillator output to increment or decrement the frequency.

This algorithm is shown below as a flow diagram , Fig.6.

The counter is a synchronous up/down counter, the most significant bit being the instantaneous sign or direction bit. The reset condition of this block is to force the instantaneous sign and frequency to be forward and zero respectively. Whenever the setpoint frequency is equal to zero and the instantaneous frequency reaches zero the phase outputs are inhibited (forced to zero). When starting from this state, (which is also the state immediately following power-up), the top phase outputs are temporarily disabled and the bottom phase outputs pulsed high for a whole carrier cycle before normal PWM operation is resumed. This is to allow a time for charging the top side capacitors in a bootstrapped driver circuit. This sequence is achieved without generating pulses shorter than the pulse deletion time.
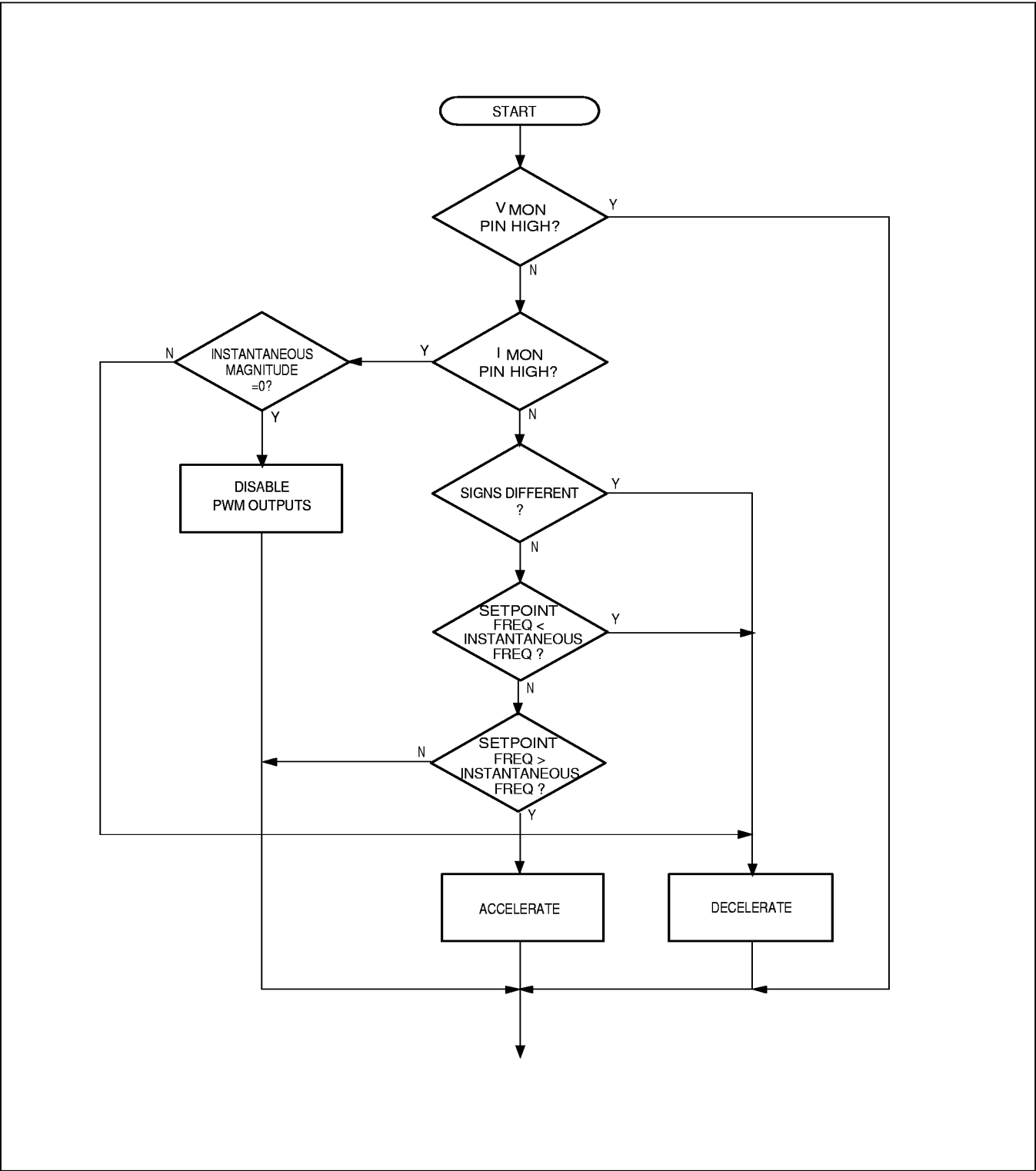
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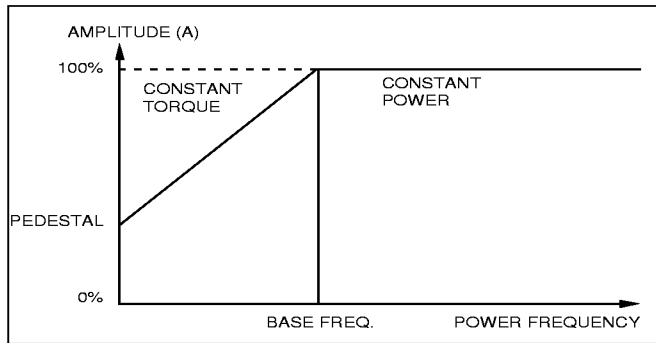Fig.6 Acceleration/deceleration logic flow diagram
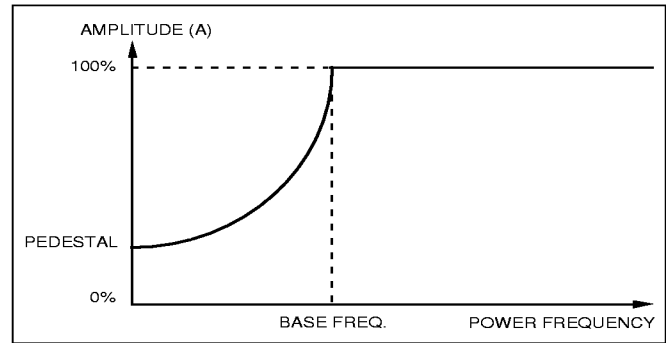
Fig.7 Linear characteristic

Fig.8 Fan-law characteristic

VOLTAGE/FREQUENCY CONTROL

In order to ensure adequate control of motor flux, the SA866AE/AM controls the motor voltage at all frequencies. Two different voltage/frequency control characteristics are provided, a Linear control law and a quadratic 'Fan-law' for fan/blower applications. These V/f characteristics are shown in Figs.7 and 8.

A variable 'pedestal' voltage may be applied at zero frequency in order to overcome copper losses. The voltage then increases either in direct proportion to the frequency (Linear characteristic selected), or as a quadratic function of the frequency (Fan-law selected), up to the required 'Base (or baseplate) frequency'. This is often 50Hz or 60Hz, but may be selected to be anywhere in the frequency range. Frequencies up to the Base frequency are said to be in the Constant Torque region with Linear V/f operation.

Beyond the Base frequency, the amplitude is held at its maximum value. This inevitably leads to a fall in the generated torque with increasing frequency, hence this is termed the Constant Power region.

The scheme by which this control is applied is shown in Fig.9. The shape of the V/f characteristic is governed by the programmable parameters GRAD, KAY and PED. GRAD and PED are positive 8 bit values, KAY is only used if the Fan-law characteristic is selected and is 7 bits magnitude with MSB providing a sign bit (0 - positive, 1 - negative). Note: KAY is <u>not</u> a 2's complement number. The parameter FC is used to select the characteristic (FC = 0: Linear, FC = 1: Fan-law)
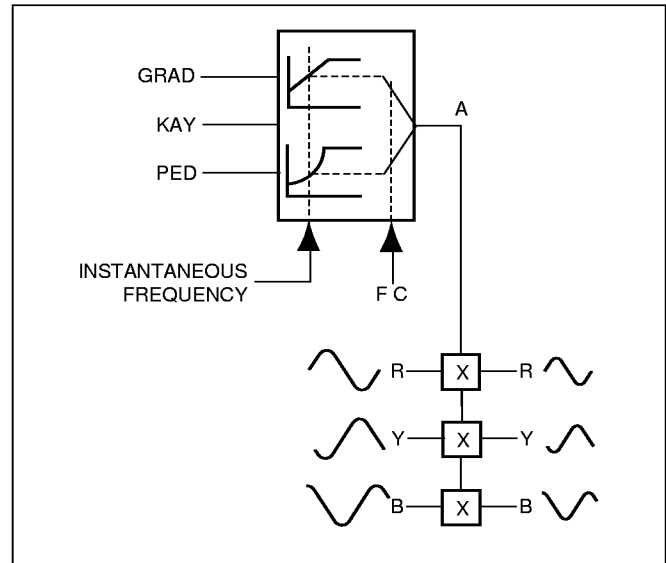

Fig.9 Voltage/frequency control diagram

The equations governing the V/f characteristics are:
LINEAR:

$$A(\%) = \left[\frac{(GRAD \cdot F)}{16} + PED \right] \times \frac{100}{255}$$

and FAN-LAW:

$$A\% = \left\{ \frac{1}{8192} \cdot GRAD \cdot F^2 + \frac{1}{512} \cdot KAY \cdot F + PED \right\} \times \frac{100}{255}$$

where F is the top 8 bits of the instantaneous frequency

i.e. $f(Hz) = \frac{F}{255} \times f_{RANGE} (Hz)$

and if A > 100% then A = 100%
Also for the Fan-law,

If $GRAD \cdot F + 16 \cdot KAY < 0$ then $A = PED \times \frac{100}{255}$

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EEPROM INTERFACE

The SA866AE has a MICROWIRE type, three-wire serial interface to allow it to be connected to a 256-Bit or 1024-Bit Serial Microwire Bus type EEPROM such as a 93C06 or 93C46. All programmable parameters are stored in the EEPROM and downloaded automatically via the serial interface immediately after a RESET input.

Three signals are provided - SDA (Serial Data In/Out), CS (Chip Select) and SCL (Serial Clock). These should be linked directly to the equivalent pins on the EPROM, as shown in Fig.10. The Data In and Data Out pins, (DI and DO outputs on the EEPROM) are linked together. Note that the possible I/O contention error that can occur on these pins, between when the last instruction address bit is input, to the start of the leading zero of the data output, is avoided because the LSB (A0) of the address bit is always a zero.

It is important that the EEPROM used supports auto-increment of the address during a READ instruction - some manufacturers parts do not have this feature, and will not download correctly to the SA866AE. The EEPROM should be configured to operate in the 16-Bit word mode, normally by leaving the ORG input unconnected, or connecting it to V_{DD}.

The memory map for the EEPROM is shown in Table 6. This is divided into 4 pages, each page is 4 Words X 16-Bits. A page contains one full set of Initialisation Parameters, and is defined by the start address sent by the SA866AE to the EEPROM on start-up and the number of bits to be read. This feature allows four different sets of parameters to be selected in a single product, by means of switches or wire links etc. The page is selected by the logic state of the two page inputs, PAGE0 and PAGE1 after a reset condition, as shown below:

PAGE1	PAGE0	Start Address
0	0	XX0000
0	1	XX0100
1	0	XX1000
1	1	XX1100

Table 5 EEPROM page addressing

PAGE0 and PAGE1 both have internal resistive pull-ups. If these inputs are left floating, the last page of the memory map will be selected.

The two leading bits XX form the two LSB's of the op-code for a 93C06 device, or the two MSB's of the 6-bit address for a 93C46 device. These bits are always 00.
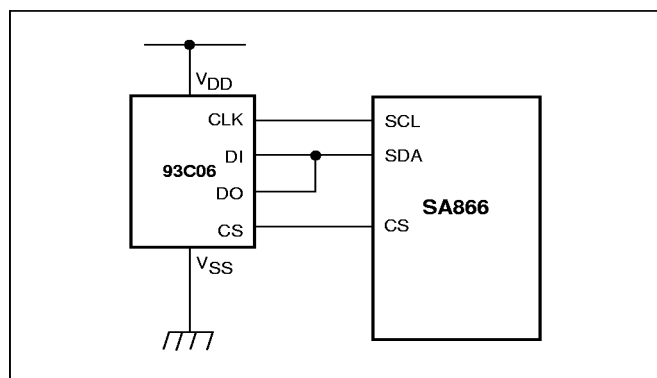

Fig.10 Serial EEPROM interface

Note - If a 1024-Bit 93C46 is used, only the lower 256-Bit locations will be accessed. The remainder of the EEPROM need not be programmed

Fig.11 illustrates the timing of the CS, SCL and SDA signals. Following the rising edge of RESET the CS signal is driven high to select the EEPROM. The SA866AE drives the clock signal, SCL, to control the clocking of data in and out of both the EEPROM and itself. Data for controlling the EEPROM is clocked out of the SA866AE on the falling edges of SCL (to be clocked into the EEPROM on subsequent rising edges). Each bit of parameter data is clocked out of the EEPROM on a rising edge of SCL to be clocked into the SA866AE on the following falling edge.

SDA idles low following reset. On the first falling edge of SCL following CS going high, a high start bit is output on SDA. This is followed by the 'READ' instruction (10) to the EEPROM (this is a read only interface so there is no variation in instruction sent out). Two further zeros are sent out, interpreted by a 93C46 as address MSB's or ignored by a 93C06. These are followed by a 4 bit start address dependant on the state of the PAGE0 and PAGE1 inputs as defined in Table 5.

On the same rising edge of SCL on which the last address is clocked into the EEPROM, the EEPROM outputs a dummy data bit, value 0. On subsequent rising edges of SCL, the EEPROM sends the parameter data back to the SA866AE. The data is sent in 16 bit words, MSB first. Note that there is no separator between 16 bit words (no further dummy bits or toggling of CS is required). When 51 data bits have been clocked into the SA866AE, CS is forced low to terminate the data transfer.

During the READ operation, an accumulator keeps a count of the number of 1's in the incoming data, excepting any in the CHECKSUM word itself. The 3 least significant bits of this count (modulo 8) are compared against the CHECKSUM word after the read operation. The CHECKSUM word, CHKSUM<2:0> are the last 3 bits of data read from the EEPROM. If the two numbers do not agree the device enters a TRIP condition. This state can only be cleared and a new READ cycle initiated by applying a RESET pulse.

Note that the PWM outputs are inhibited (held low), while the serial EEPROM data is downloaded.

MASK PROGRAMMING (SA866AM)

For high volume applications, the Initialisation Parameters may be mask programmed into the SA866AM at manufacture to the user's specific requirements.

The following parameters are mask programmable: CFS, WS, FRS, PDT, PDY, GRAD, PED, KAY, ZTH, FC.

The serial EEPROM interface is disabled for all mask programmed variants, and the page selection feature is not available.

The serial interface remains available but would normally only be used for factory testing. The mask programmed parameters have no effect on the operation of the serial interface.

Please consult your local Customer Service Centre for further information.

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SA866AE/AM

ADDRESS	MSB															LSB
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CHKSUM 2:0			don't care												
	CFS 2:0			WS 1:0		FRS 2:0			KAY 7:0							
	PDY 5:0						ZTH 1:0		PDT 6:0							FC
(00)1100	GRAD 7:0								PED 7:0							
	CHKSUM 2:0			don't care												
	CFS 2:0			WS 1:0		FRS 2:0			KAY 7:0							
	PDY 5:0						ZTH 1:0		PDT 6:0							FC
(00)1000	GRAD 7:0								PED 7:0							
	CHKSUM 2:0			don't care												
	CFS 2:0			WS 1:0		FRS 2:0			KAY 7:0							
	PDY 5:0						ZTH 1:0		PDT 6:0							FC
(00)0100	GRAD 7:0								PED 7:0							
	CHKSUM 2:0			don't care												
	CFS 2:0			WS 1:0		FRS 2:0			KAY 7:0							
	PDY 5:0						ZTH 1:0		PDT 6:0							FC
(00)0000	GRAD 7:0								PED 7:0							

Table 6 EEPROM memory map
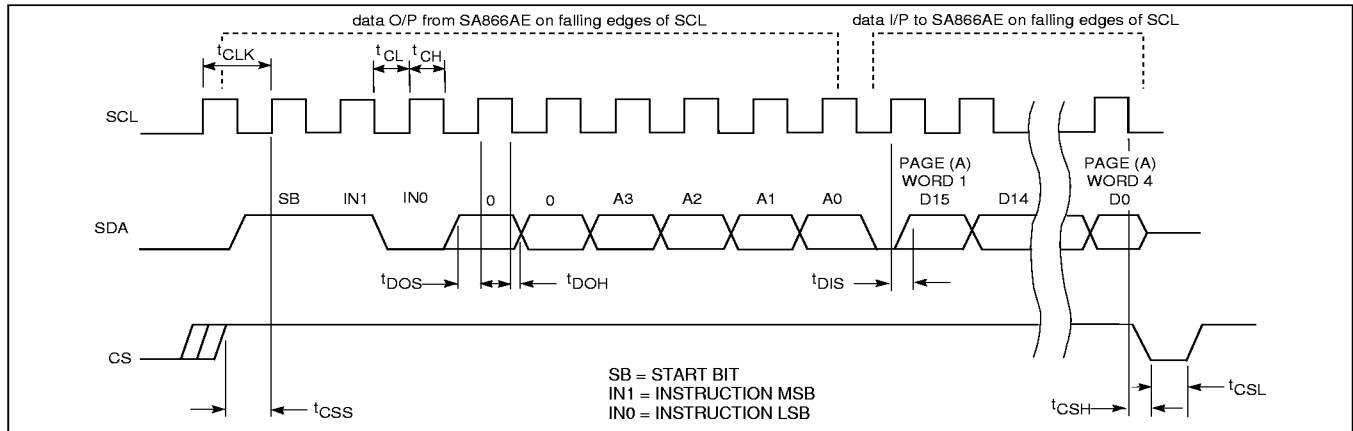
Parameter	Symbol	Min.	Typ.	Max.	Units
Chip select setup time	t_{CSS}	100	-	-	ns
Chip select hold time	t_{CSH}	100	-	-	ns
Clock high time	t_{CH}	-	$0.5t_{CLK}$	-	s
Clock low time	t_{CL}	-	$0.5t_{CLK}$	-	s
Data out setup time	t_{DOS}	200	-	-	ns
Data out hold time	t_{DOH}	200	-	-	ns
Data in setup time	t_{DIS}	200	-	-	ns
Chip select low time	t_{CSL}	-	$0.5t_{CLK}$	-	s
Clock period	t_{CLK}	-	$256/f_{xtal}$	-	s

Fig.11 EEPROM timing (93C06)

INITIALISATION PARAMETERS

This section describes the programmable parameters which may be downloaded from the serial EEPROM or mask programmed.

Carrier Frequency (CFS)

The carrier frequency is a function of the externally applied clock frequency and a division ratio n, determined by the 3-bit CFS word set during initialisation. The values of n are selected as shown in Table 7.

CFS word	111	110	101	100	011	010	001	000
Value of n	7	6	5	4	3	2	1	0

Table 7 Values of clock division ratio n

The carrier frequency, f_{CARR}, is then given by:

$$f_{CARR} = \frac{f_{CLK}}{512 \times 2^{n+1}}$$

where f_{CLK} = clock input frequency.

Power Frequency Range (FRS)

In order to optimise the resolution of the SA866AE/AM the required range of power frequencies may be selected using this parameter. Within the selected range the frequency may be set with 16-bit resolution. It is recommended to use the next higher power frequency range than the maximum required motor frequency. The power frequency range defines the maximum limit of the power frequency. The operating

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power frequency is controlled by the 16-bit Frequency word from the Accel/Decel logic. The power frequency range is a function of the carrier waveform frequency (f_{CARR}) and a multiplication factor m, determined by the 3-bit FRS word. The value of m is determined as shown in Table 8.

FRS word	110	101	100	011	010	001	000
Value of m	6	5	4	3	2	1	0

Table 8 Values of clock division ratio m

The power frequency range, f_{RANGE}, is then given by:

$$f_{RANGE} = \frac{f_{CARR} \times 2^m}{384}$$

where f_{CARR} = carrier frequency.

Pulse Delay Time (Underlap) (PDY)

For each output phase there are two PWM control signals controlling the upper and lower switches in the inverter. In theory these two control signals are always complementary. However, due to the finite and non-equal turn-on and turn-off times of power semiconductors, it is necessary to provide a short delay time during which both outputs are off in order to avoid a transient short through the two devices. This period is known as 'underlap'.

The pulse delay affects all six PWM outputs by delaying the rising edge of each output by an equal amount. The pulse delay time is a function of the carrier waveform frequency and the PDY value, defined by the 6-bit pulse delay time word. The value of PDY is selected as shown in Table 9.

PDY word	111111	111110	...etc...	000000
Value of *PDY*	63	62	...etc...	0

Table 9 Values of PDY

The pulse delay time, t_{pdy}, is then given by:

$$t_{pdy} = \frac{63 - PDY}{f_{CARR} \times 512}$$

where f_{CARR} = carrier frequency.

Fig.12 shows the effect of pulse delay on a pure PWM waveform.

It should be noted that as the pulse delay circuit follows the pulse deletion circuit (see Fig.2), the minimum pulse width seen at the PWM outputs will be shorter than the pulse deletion time set set using the PDT parameter. The actual shortest pulse generated is given by: $t_{pd} - t_{pdy}$.
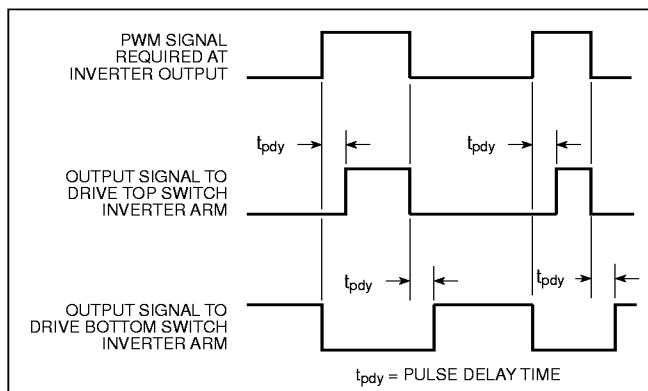

Fig.12 Effect of pulse delay

Pulse Deletion Time (PDT)

Pure PWM pulse trains contain pulses which vary in duty cycle from 0% to 100%. Therefore pulse widths may become very small indeed. In practice short pulses have no useful purpose since the power semiconductors cannot fully turn on/off within their active period. Such pulses only increase the power dissipation in the power devices. Therefore a minimum pulse width may be defined. All pulses shorter in duration than this are eliminated from the PWM train, whether they are low-going or high-going.

To eliminate short pulses the true PWM pulse train is passed through a pulse deletion circuit. The pulse deletion circuit compares pulse widths with the pulse deletion time set in the register. If a pulse (either positive or negative) is greater than the pulse deletion time, it is passed through unaltered, otherwise the pulse is deleted.

The pulse deletion time, t_{pd}, is a function of the carrier wave frequency and PDT, defined by the 7-bit pulse deletion time word. The value of PDT is selected as shown in Table 10.

PDT word	1111111	1111110	...etc...	0000000
Value of *PDT*	127	126	...etc...	0

Table 10 Values of PDT

The pulse deletion time, t_{pd}, is then given by:

$$t_{pd} = \frac{127 - PDT}{f_{CARR} \times 512}$$

where f_{CARR} = carrier frequency.

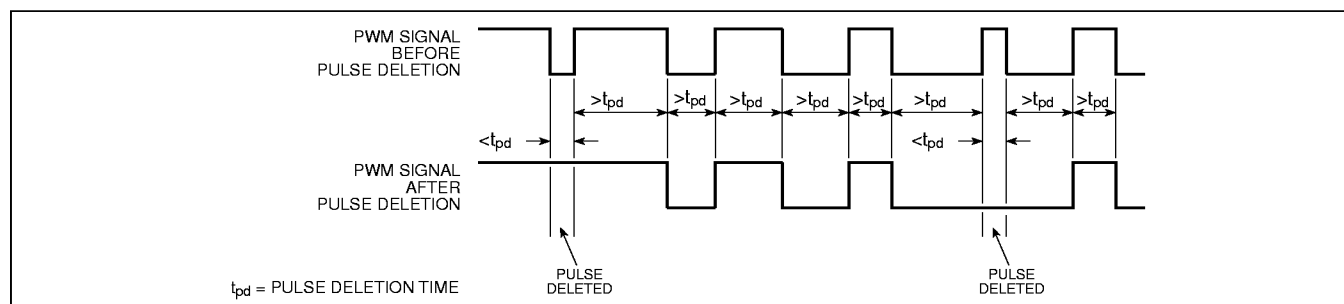Fig.13 shows the effect of pulse deletion on a pure PWM waveform.

Fig.13 Effect of pulse deletion

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WAVEFORM SELECTION

Three waveforms are included as standard with the SA866AE/AM. A pure sinewave is available for applications where waveform purity is important such as static inverter power supplies and uninterruptible power supplies. For three phase induction motor control a Triplen waveform is included which provides maximum utilisation of the inverter DC link voltage using an harmonic injection technique. Also for motor control, a Deadbanded Triplen waveform may be selected which, in addition to providing DC link voltage boost, also acts to reduce the number of switching events in the power semiconductors to reduce the switching loss. A symmetrical technique is used to ensure that each power semiconductor benefits to the same degree.

Two bits, WS0 and WS1, are used to define the power waveform, according to Table 11:

WS1	WS0	Waveform
0	0	Sinusoid (default)
0	1	Triplen (harmonic injection)
1	0	Deadbanded Triplen (switching loss reduction)
1	1	Reserved

Table 11 Waveform selection

The waveforms may be described by the following mathematical relationships and are shown graphically in Fig.14
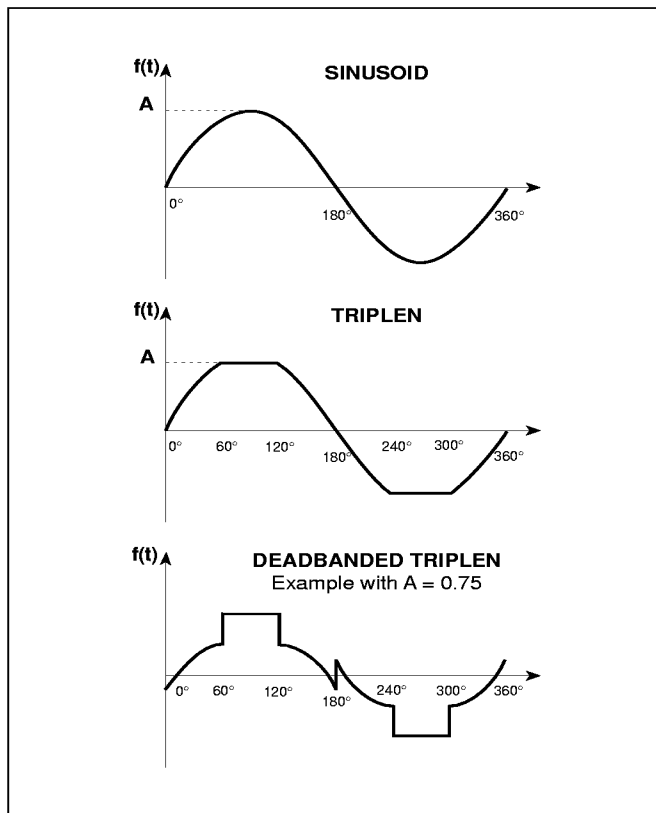

Fig.14 Power waveforms

Sinusoid:

$$f(t) = A \sin (\omega t)$$

where A = amplitude
ω = angular displacement

Triplen:

f(t)	Valid
$f(t) = A(2. \sin (\omega t + 30°) -1)$	$0° \le \omega t < 60°$
$f(t) = A$	$60° \le \omega t \le 120°$
$f(t) = A(2. \sin (\omega t - 30°) -1)$	$120° \le \omega t < 180°$
$f(t) = A(2. \sin (\omega t + 30°) +1)$	$180° \le \omega t < 240°$
$f(t) = -A$	$240° \le \omega t \le 300°$
$f(t) = A(2. \sin (\omega t - 30°) +1)$	$300° \le \omega t < 360°$

Deadbanding:

Below are the modulating functions for the Deadbanded Triplen waveform. These have been normalised and scaled to give a peak line voltage (phase to phase) of 2A. All the 3 phases are shown for clarity, f(t), g(t) and h(t).

Function	Valid
$f(t) = 2A.\sin(\omega t + 30°) -1$ $g(t) = -1$ $h(t) = 2A.\sin(\omega t + 90°) -1$	$0° < \omega t \le 60°$
$f(t) = 1$ $g(t) = 1 + 2A.\sin(\omega t - 150°)$ $h(t) = 1 + 2A.\sin(\omega t + 150°)$	$60° < \omega t \le 120°$
$f(t) = 2A.\sin(\omega t - 30°) -1$ $g(t) = 2A.\sin(\omega t - 90°) -1$ $h(t) = -1$	$120° < \omega t \le 180°$
$f(t) = 1 + 2A.\sin(\omega t + 30°)$ $g(t) = 1$ $h(t) = 1 + 2A.\sin(\omega t + 90°)$	$180° < \omega t \le 240°$
$f(t) = -1$ $g(t) = 2A.\sin(\omega t - 150°) -1$ $h(t) = 2A.\sin(\omega t + 150°) -1$	$240° < \omega t \le 300°$
$f(t) = 1 + 2A.\sin(\omega t - 30°)$ $g(t) = 1 + 2A.\sin(\omega t - 90°)$ $h(t) = 1$	$300° < \omega t \le 360°$

Line output voltages appearing across the load are:
$V_{fg} = f(t) - g(t)$
$V_{gh} = g(t) - h(t)$
$V_{hf} = h(t) - f(t)$
The line voltage waveforms are sinusoidal.

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Voltage/Frequency Control Parameters (GRAD, KAY, PED, FC)

These parameters are used to define either a linear or quadratic (Fan-law) relationship between the frequency and the amplitude of the power waveform. GRAD and PED may also be used to define a fixed power frequency when the amplitude is to be controlled by the ADC (mode N3).

Characteristic Selection (FC)

Table 1 shows how the various modes of operation are selected. When modes N1 or N2 are selected, the FC bit is used to select either the Linear or the Fan-law characteristic as shown in Table 12. In mode N3, FC has no effect.

FC bit	V/f Characteristic
0	Linear
1	Fan-law

Table 12 FC value

Linear V/f (GRAD, PED)

Fig.7 shows the linear characteristic implemented in the SA866AE/AM.

PED is an 8 bit parameter which is used to define the voltage present on the motor coils at zero frequency. This voltage is used to counteract the effects of copper loss which tends to dominate the overall losses at low speeds. The value should be chosen carefully so that the power dissipation in the motor at low frequencies is not excessive. It is possible to defeat the V/f profile by setting PED=255.

$$Pedestal(\%) = \frac{PED \times 100}{255}$$

GRAD is also an 8 bit parameter which defines the slope of the V/f characteristic in the constant torque region of motor operation. This is usually calculated in terms of the motor baseplate frequency and the pedestal value as follows:

$$GRAD = \frac{(255 - PED) \times f_{RANGE}}{16 \times f_{base}}$$ where GRAD $\leq$ 255.

At any instantaneous frequency,

$$A(\%) = \left[\frac{(GRAD \cdot F)}{16} + PED \right] \times \frac{100}{255}$$

where F is the top 8 bits of the instantaneous frequency

i.e. $f(Hz) = \frac{F}{255} \times f_{RANGE}$ (Hz)

and if A > 100% then A = 100%

The parameter, KAY is not used when the linear characteristic is selected.

Fan-law V/f (GRAD, KAY, PED)

Fig.8 shows the Fan-law characteristic implemented in the SA866AE/AM.

The PED parameter has exactly the same function as defined in the linear V/f section. In the variable power region for fan-law, the amplitude is related to the instantaneous frequency by the equation:

$$A\% = \left\{ \frac{1}{8192} \cdot GRAD \cdot F^2 + \frac{1}{512} \cdot KAY \cdot F + PED \right\} x \ \frac{100}{255}$$

where F is the top 8 bits of the instantaneous frequency

i.e. $f(Hz) = \frac{F}{255} \times f_{RANGE}$ (Hz)

and if A > 100% then A = 100%
and if $GRAD \cdot F + 16 \cdot KAY < 0$ then $A = PED \ x \ \frac{100}{255}$

GRAD is an 8 bit value. KAY is of 7 bits magnitude, with the MSB providing a sign bit, (0 - positive, 1 - negative).

ADC Controlled Amplitude (GRAD, PED)

In mode N3, the GRAD and PED parameters are used to define a 16 bit power frequency value, GRAD<7> forms the MSB and PED<0> forms the LSB. This power frequency word (PFW) is related to the actual power frequency by the equation:

$$f_{POWER} = \frac{f_{RANGE}}{65535} \ x \ PFW$$

Zero Threshold Selection

These two bits ZTH<1> and ZTH<0> select the four zero threshold offset for the ADC input, as shown in Table 2.

Checksum

The checksum CHKSUM<2:0> is the last 3-Bits of data read from the EEPROM. These should be set to be equal to the binary value of the 3 least significant bits of the binary sum of all the 1's on the page, not including the checksum itself. There is a checksum for each page of EEPROM memory.

HARDWARE INPUT/OUTPUT FUNCTIONS

SET TRIP Input

The SET TRIP allows an external, active high event to provide a rapid shutdown of the PWM signals. When the SET TRIP input is taken to a logic 1, a delay of 2-3 master clock cycles is triggered internally. If, during this time, the SET TRIP input has remained high, then the PWM outputs will be inhibited and the $\overline{TRIP}$ acknowledge output will become active.

This condition can only be cleared by applying a $\overline{RESET}$ pulse. The SET TRIP input has an internal pulldown. However it is recommended that this input is tied low if it is not used.

Output Trip Status

The $\overline{TRIP}$ output indicates the status of the trip latch and is active low. It does not become active until the end of the SET TRIP delay time (assuming that the SET TRIP input stays high for this period).

This output is capable of directly driving a LED through a current limiting resistor for display purposes.

$\overline{RESET}$ Input

When $\overline{RESET}$ input is taken low it performs the following functions:

i)   All PWM outputs are forced low.

ii) All internal counters are reset to zero.

iii) The instantaneous frequency word is set to zero and the direction bit to 1 (forward).

When $\overline{RESET}$ is taken high:

iv) Test mode can be entered by application of a special code sequence. (Factory test use only).

v)   Initialisation parameter data is downloaded from the selected page of the serial EEPROM.

vi) The inhibit is removed from the PWM outputs and the trip latch set to inactive, provided that the SET TRIP input is inactive. The removal of the inhibit forces the phase bottom outputs to be driven high for a whole carrier cycle before the phase top outputs are enabled.

As a consequence of (iii) to (vi) the device will be re-enabled and will re-accelerate from zero to the set frequency when reset after a TRIP event.

$\overline{RESET}$ input should be held low at power up for a short period, to allow the internal counters etc. to be reset. (minimum one f_{CLK} cycle). However when using the Accel/Decel oscillators, the $\overline{RESET}$ input must be kept low long enough, to ensure that the 0.125V_{DD} defeat threshold is crossed on the R_{ACC} input. This is determined by the charge rate of the external RC time constant, (**NOTE - Failure to do this can result in an incorrect mode being selected.)**

XTAL1/XTAL2

These pins are for the crystal or ceramic resonator, if used. Alternatively, XTAL1 may be used as an input for an externally generated clock signal. Any external input is constrained to having a mark/space ratio of 1:1 $\pm$ 20% to ensure correct device operation.

A small capacitor should be connected from each of these pins to the V_{SS} supply rail when using a crystal or ceramic resonator. The capacitor value is dependant on the crystal characteristics. A suitable value for common crystal types is 56pF.

V_{MON} Input

Analog input which prevents any acceleration/deceleration events when $\geq V_{DD}/2$. This input has higher priority than the I_{MON} pin, and the V_{MON} condition therefore prevails if both V_{MON} and I_{MON} are active simultaneously.

DIR Input

Logical input which allows the phase sequence of the PWM outputs to be reversed. A high input causes forward rotation (R-Y-B), and low causes reverse rotation (R-B-Y).

The DIR pin is not used in modes S1, S2 and S3 but must be connected to either supply to avoid excessive current consumption.

I_{MON} Input

Analog input which causes the instantaneous output frequency to reduce at the predetermined deceleration rate when $\geq V_{DD}/2$. If the frequency is reduced to zero whilst this input is $\geq V_{DD}/2$, the PWM outputs are temporarily turned off and the deceleration inhibited. Normal acceleration may resume when I_{MON} is below $\geq V_{DD}/2$. In addition, the PWM outputs are re-enabled in the event that the frequency had fallen to zero.

V_{REFIN}

Nominal 2.5V external reference input, for the ADC.

PAGE Inputs

The PAGE1 and PAGE0 inputs select one of the four pages containing initialisation parameter data, that are read from the serial EEPROM following $\overline{RESET}$. Internal pullups ensure that Page 4 is selected by default if they are left unconnected. See the EEPROM INTERFACE section for more information.

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SERIAL INTERFACE OPERATION

The SA866AE/AM serial interface can be used to interface the device to a microprocessor / microcontroller by means of a simple 3-wire connection. It uses a write-only MICROWIRE protocol at a rate of up to 750kbits/s.

The serial interface mode of operation is enabled by taking the $\overline{\text{SERIAL}}$ input low. See table 1 for a summary of the different modes of operation. The pins used for the serial EEPROM become inputs for use with the Serial Interface. CS, SCL and SDA are used as chip-select, serial clock and serial data inputs for the serial interface respectively. All of these inputs are debounced, requiring data to remain in a stable state for 15 f_{CLK} clock cycles before a change is registered inside the device. Data is latched in by the interface on the rising edge of SCL. The serial interface register address map is shown in Table 13 and an explanation of the control bits is given in Table 14. It is important to note that the register addressing is not the same as when reading data from the EEPROM, and the serial interface pins operate in a different manner than in the Normal operating mode. The FB/R bit in the serial Control register is used to control the phase order, the external DIR pin is disabled.

MODE S1.

In this mode the ADC is disabled and all parameters are set via the serial interface. The Accel/Decel oscillators are enabled and if VF bit is set to a logic '1', the V/f characteristic will operate as defined by the GRAD, KAY, PED and FC parameters. The amplitude is calculated internally according to the instantaneous power frequency. If VF is set to logic '0' the Amplitude scaling factor (0% to 100%), is taken directly from the serial Gradient register and not calculated.

MODE S2.

This mode is similar to mode S1 above, except that the Accel/Decel oscillators are disabled. The Power Frequency follows any changes made to the serial SpeedTop and SpeedBot registers immediately a write operation is made to the SpeedBot register. (Operation of the VF bit is the same as mode S1.)

MODE S3.

In this mode the Amplitude is controlled via the ADC input, to 8-Bit resolution. The Power Frequency value is loaded to the serial Gradient and Pedestal registers, (the Gradient register holds the top most significant 8-Bits). The SpeedTop and SpeedBot registers are not used in this mode.

(Note - VF bit has no effect in this mode.)

Address	7	6	5	4	3	2	1	0	Register
0000	RST	$\overline{\text{CR}}$	TM3	VF	TM2	TM1	$\overline{\text{INH}}$	FB/R	Control
0001	CFS2	CFS1	CFS0	WS1	WS0	FRS2	FRS1	FRS0	Setup1
0010	PDT6	PDT5	PDT4	PDT3	PDT2	PDT1	PDT0	FC	Setup2
0011	PDY5	PDY4	PDY3	PDY2	PDY1	PDY0	ZTH1	ZTH0	Setup3
0100	PFS15	PFS14	PFS13	PFS12	PFS11	PFS10	PFS9	PFS8	SpeedTop
0101	PFS7	PFS6	PFS5	PFS4	PFS3	PFS2	PFS1	PFS0	SpeedBot
0110	GRAD7	GRAD6	GRAD5	GRAD4	GRAD3	GRAD2	GRAD1	GRAD0	Gradient
0111	PED7	PED6	PED5	PED4	PED3	PED2	PED1	PED0	Pedestal
1000	KAY7	KAY6	KAY5	KAY4	KAY3	KAY2	KAY1	KAY0	Kay

Table 13 Serial interface register map

REGISTER BIT	Function
RST	Software reset, active high - may be cleared by over-writing with 0 or by asserting $\overline{RESET}$ input low.
$\overline{CR}$	Counter reset, active low - resets internal counters so that output holds zero phase red condition (red phase outputs have duty cycle of 50%, yellow and blue phases have duty cycles corresponding to phases of +120° and −120° respectively).
VF	If low, the serial interface may be used to supply amplitude values directly rather than using internal calculation. Gradient value provides 8 bit amplitude scaling factor, 0 -> 100%. Any relationship between power frequency and amplitude is calculated by external processor. If high, enables use of either Linear or Fan-Law V/F characteristic dependent on the value of the FC bit. Amplitude is calculated internally according to instantaneous power frequency. See Voltage/Frequency Characteristic.
$\overline{INH}$	All PWM outputs become low while $\overline{INH}$ is asserted low. When $\overline{INH}$ is deasserted (high) the top phase outputs are temporarily disabled and the bottom phase outputs pulsed high for a whole carrier period, before normal PWM operation is resumed. Both assertion and deassertion of the inhibit condition are achieved without generating pulses shorter than the pulse deletion time.
FB/R	FB/R low, forward direction (R-Y-B). FB/R high, reverse direction (R-B-Y), In Serial mode the DIR pin is disabled
TM1 TM2 TM3	Selects test mode (Factory use only). Default value = 000 (Will only have an effect if the correct procedure is followed for entering test mode.)
FC	When V/f characteristic enabled (V/f = 1), Fan-Law selected when FC = 1, otherwise Linear V/f characteristic selected.

Table 14 Serial interface register bits

All other register bits are parameters described under the Normal operating modes except for PFS. PFS is a 16 bit power frequency word - the output power frequency being given by the equation:

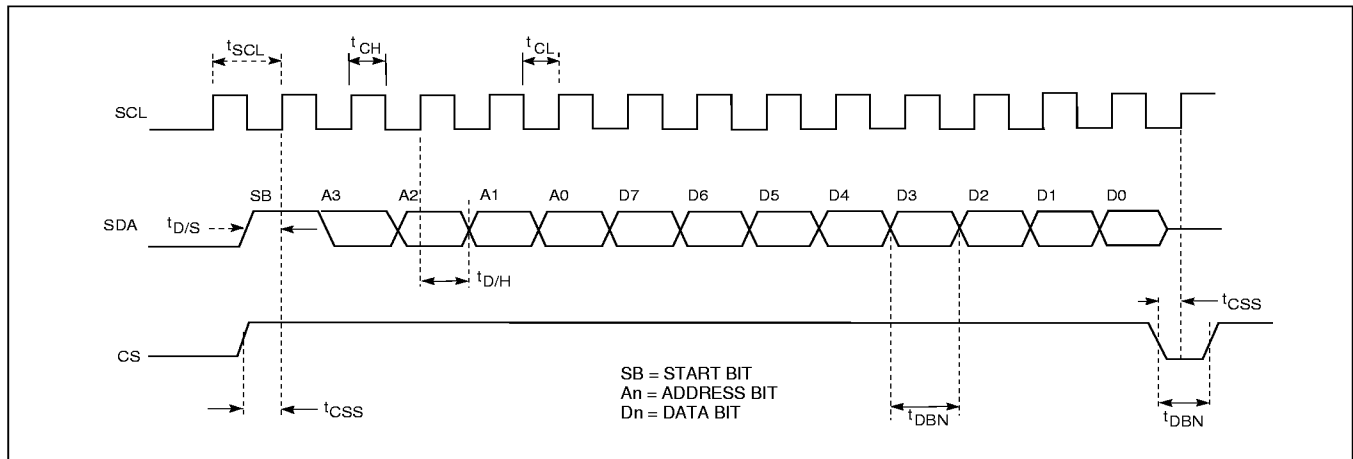$$f_{POWER} = \frac{f_{POWER}}{65535} \times PFS$$

Fig.15 Serial interface timing diagram

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Parameter	Symbol	Min.	Typ.	Max.	Units
Chip select setup time	t_{CSS}	$2/f_{CLK}$	-	-	s
Chip select hold time	t_{CSH}	$8/f_{CLK}$	-	-	s
Clock high time	t_{CH}	$20/f_{CLK}$	-	-	s
Clock low time	t_{CL}	$20/f_{CLK}$	-	-	s
Data in setup time	$t_{D/S}$	$2/f_{CLK}$	-	-	s
Data in hold time	$t_{D/H}$	$2/f_{CLK}$	-	-	s
Data valid (debounce) time	t_{DBN}	$16/f_{CLK}$	-	-	s
Clock period	t_{SCL}	$50/f_{CLK}$	-	-	s

Note: All timings in terms of crystal clock f_{CLK}

Table 15 - Serial interface timing characteristics

Serial Interface Protocol

A write-only MICROWIRE style serial interface protocol is used - this is very similar to that used to access the serial EEPROM but there are differences between the two modes of operation which should be noted.

The SDA input idles at a low level. With the chip selected (CS = 1), the SA866AE/AM reads data from SDA on successive rising edges at the SCL input (assuming that both inputs have been stable for 15 master clock cycles). The chip must be de-selected (CS = 0) for the next rising edge on SCL after a data word has been transmitted in order for the data to be latched inside the SA866AE/AM. Providing that the data input remains low after the data word has been sent, the de-selection pulse need not follow the data word immediately. However, any new high value detected on the data input will be regarded as a new start bit and the first word will be overwritten. If the chip is de-selected at any time during a transmission, any data transmitted from the start bit to that point will be ignored.

A data word consists of a single high start bit, followed by a 4-Bit register address, MSB first (the instruction), followed by 8-Bits of data (also MSB first). See Table 13 for valid register addresses. Attempts to write to an invalid register address result in no action.

The action taken upon receiving a data word depends upon the register written. It is initiated by the rising edge of the crystal clock following the chip-select input (CS) going low and is detailed in Table 16. The complexity of this table arises from the use of 8-Bit serial data words to program 16 or 24-Bit values simultaneously.

Frequency values programmed from the serial interface use either the 16-Bit PFS word or in Mode S3, a combination of the 8-Bit Gradient and Pedestal values. In both cases, the lower byte of the speed value may be updated without requiring other values to be set up. If the data for the upper frequency byte is sent, it is stored temporarily and only takes effect when data for a new lower byte is written.

If direct control of the amplitude of the waveform is required, new values must be transferred at the same time as the corresponding power frequency information. The amplitude value is written to the Gradient register address and held until the lower PFS byte is written or until both upper and lower PFS bytes have been written. In this mode, new frequency (low byte or both high and low bytes) may be written without updating the amplitude value, but a new frequency must be written in order to update the amplitude (the frequency value need not change, but the process of writing a new value must be executed).

Note that no provision is made for a time-out or for checking or acknowledging incoming data.

Reset Operation

The state of the control register bits following the assertion of the external $\overline{RESET}$ input depends on the state of the $\overline{SERIAL}$ input, as follows:

If $\overline{SERIAL}$ = 1 then,
$\overline{RST}$ = 0, $\overline{CR}$ = 1, TM3 = 0, VF = 1, TM2 = 0, TM1 = 0, $\overline{INH}$ = 1, FB/R = 0

If $\overline{SERIAL}$ = 0 then,
$\overline{RST}$ = 0, $\overline{CR}$ = 0, TM3 = 0, VF = 1, TM2 = 0, TM1 = 0, $\overline{INH}$ = 0, FB/R = 0

On assertion of the RST bit, the state as for $\overline{SERIAL}$ = 0 is adopted except that the RST bit itself is not reset.

The Serial interface remains operational when RST = 1 if $\overline{SERIAL}$ = 0.

SA866AE/AM

REGISTER	ACTION
Control Setup1 Setup2 Setup3 Kay	Load incoming data to the appropriate internal register.
SpeedTop	Hold incoming data in a temporary register until data is written into the SpeedBot register.
SpeedBot	If VF = 0: (amplitude data is taken from Gradient register and not calculated) • If the Gradient temporary register contains unused data, make it the new amplitude value. • If the SpeedTop temporary register contains unused data, write it to the top 8 bits of the frequency demand register. • Load the incoming data into the bottom 8 bits of the frequency demand register. If VF = 1: (amplitude data is calculated using linear or fan-law characteristic) • If the SpeedTop temporary register contains unused data, write it to the top 8 bits of the frequency demand register. • Load the incoming data into the bottom 8 bits of the frequency demand register.
Gradient	If VF = 0: (amplitude data is taken from Gradient register and not calculated) • Hold incoming data in a temporary register until data is written into the SpeedBot register. If VF = 1: (using linear or fan-law characteristic) • Load incoming data to the appropriate internal register If using ADC controlled amplitude, mode S3: • Hold data in a temporary register until data is written to the Pedestal register.
Pedestal	If using ADC controlled amplitude, mode S3: • If the Gradient temporary register contains unused data, write it to the top 8 bits of the frequency demand register. • Load the incoming data to the bottom 8 bits of the frequency demand register. Otherwise: • Load incoming data to the appropriate register
Register addresses 9 to 15	No action

Table 16 - Serial interface register operation

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APPLICATIONS

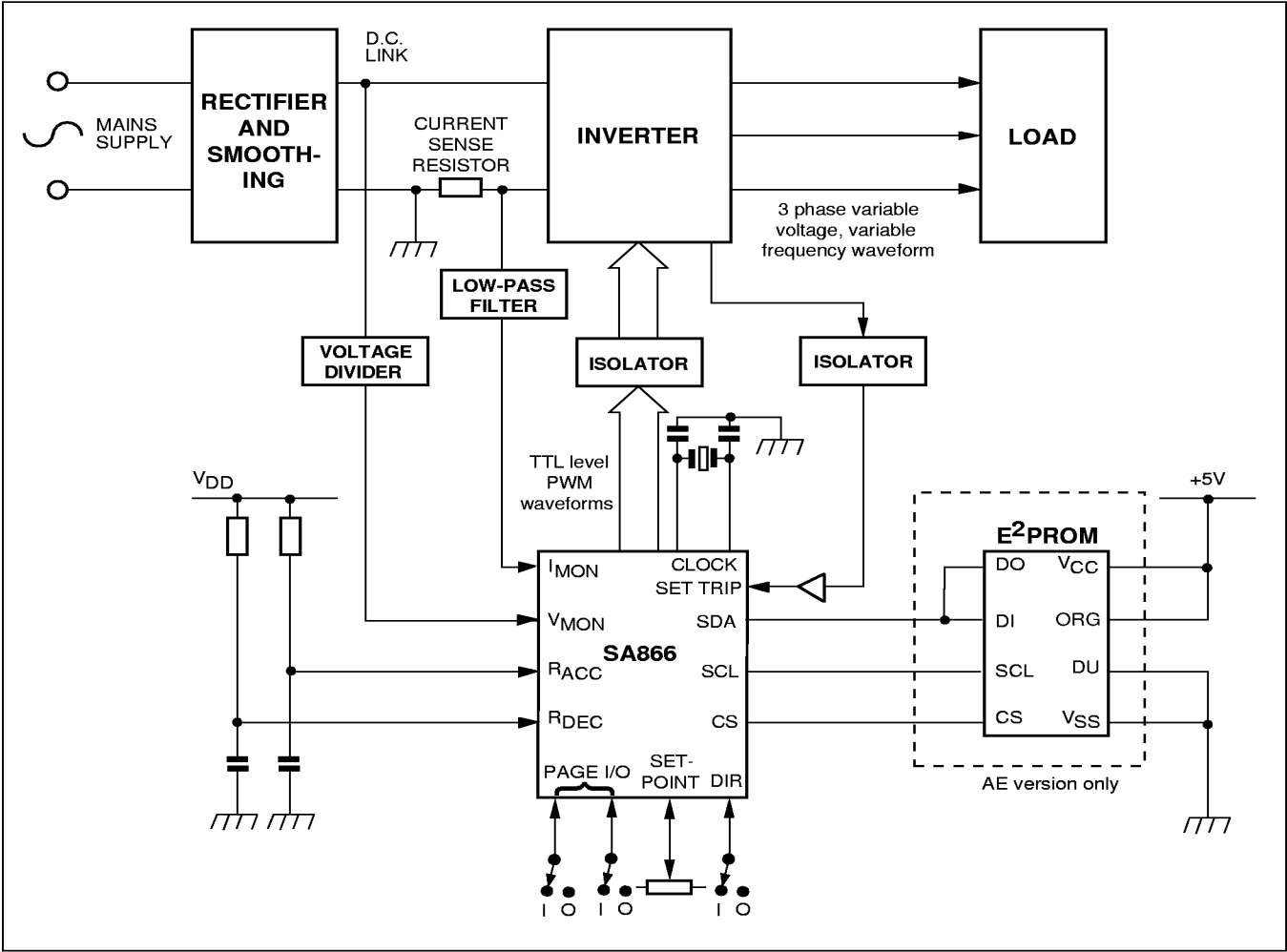*Fig.16 Typical applications circuit*

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PACKAGE DETAILS

Dimensions are shown thus: mm (in). For further package information, please contact your local Customer Service Centre.

PIN 1

PIN 32

PIN 1 IDENT

7·00 (0·276)
NOM. SQ.

5·60 (0·22)
NOM.

9·00/9·39
(0·354/0·369)

0° - 7°

0·13/0·20
(0·005/0·008)

1·00/1·05
(0·039/0·041)

1·20 (0·047)
MAX.

0·65/0·95
(0·026/0·037)

0·30/0·45
(0·012/0·018)

32 LEADS AT
0·80 (0·031)
NOM. SPACING

0·05/0·15
(0·002/0·006)

NOTES
1. Controlling dimensions are millimetres.
2. This package outline diagram is for guidance only. Please contact your Mitel Semiconductor Customer Service Centre for further information.

32-LEAD PLASTIC QUAD FLATPACK – GP32

0·66/0·81
(0·026/0·032)

PIN 1 PIN 32

PIN 1
REF. SIDE

0·38 (0·15)
MIN.

PIN 1 REF. CORNER
1·14 (0·045)
NOM. χ 45°

OPTIONAL
PIN 1
REFERENCE

1·14 (0·045)
NOM. χ 45°

0·33/0·53
(0·013/0·021)

12.1/13.86
(0·476/0·546)

14.86/15.11
(0·585/0·595)

13.9/14.04
(0·547/0·553)

11·36/11·5
(0·447/0·453)

12·32/12·57
(0·485/0·495)

3.18/3.55
(0·125/0·14)

32 LEADS AT
1·27 (0·050)
NOM. SPACING

1.53/2.41
(0.06/0.095)

9·56/11.32
(0·376/0·44)

NOTES
1. Controlling dimensions are inches.
2. This package outline diagram is for guidance only. Please contact your Mitel Semiconductor Customer Service Centre for further information.

32-LEAD QUAD PLASTIC J-LEAD – HP32

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