

# EMIF04-VID01C2

## 4 LINES LOW CAPACITANCE EMI FILTER AND ESD PROTECTION

#### MAIN APPLICATION

IPAD™

Where EMI filtering in ESD sensitive equipment is required:

- LCD and camera for mobile phones
- Computers and printers
- Communication systems
- MCU board

#### DESCRIPTION

The EMIF04-VID01C2 is a 4 lines highly integrated array designed to suppress EMI / RFI noise in all systems subjected to electromagnetic interferences.

The EMIF04-VID01C2 Flip-Chip packaging means the package size is equal to the die size. Additionally, this filter includes an ESD protection circuitry which prevents the protected device from destruction when subjected to ESD surges up to 15 kV.

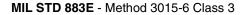
#### BENEFITS

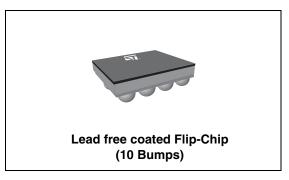
- High efficiency EMI filtering (-40db @ 900MHz)
- Low line capacitance suitable for high speed data bus
- Low serial resistance for camera impedance adaptation
- Optimized PCB space consuming: 1.92mm x 1.29mm
- Very thin package: 0.69 mm
- High efficiency in ESD suppression on inputs pins (IEC61000-4-2 level 4)
- High reliability offered by monolithic integration
   High reducing of parasitic elements through
- integration & wafer level packaging
- Lead free package

# COMPLIES WITH THE FOLLOWING STANDARDS: IEC61000-4-2

Level 4 on input pins

15kV (air discharge) 8kV (contact discharge)

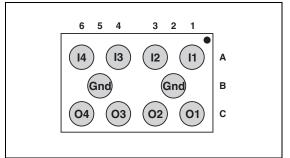




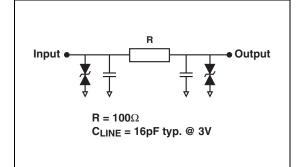
#### Table 1: Order Code

Part Number	Marking
EMIF04-VID01C2	GU

#### Figure 1: Pin Configuration (bump side)



#### **Figure 2: Configuration**



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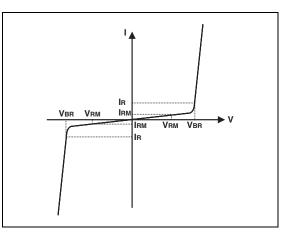
### EMIF04-VID01C2

Symbol	Parameter and test conditions	Value	Unit	
Тj	Maximum junction temperature	125	°C	
T <sub>op</sub>	Operating temperature range	- 40 to + 85	°C	
T <sub>stg</sub>	Storage temperature range	- 55 to + 150	°C	

### Table 2: Absolute Ratings (limiting values)

## Table 3: Electrical Characteristics (T<sub>amb</sub> = $25^{\circ}$ C)

Symbol	Parameter	
V <sub>BR</sub>	Breakdown voltage	
I <sub>RM</sub>	Leakage current @ V <sub>RM</sub>	
V <sub>RM</sub>	Stand-off voltage	
R	Series resistance between Input & Output	
C <sub>line</sub>	Input capacitance per line	



Symbol	Test conditions	Min.	Тур.	Max.	Unit
V <sub>BR</sub>	I <sub>R</sub> = 1mA	6	8	10	V
I <sub>RM</sub>	V <sub>RM</sub> = 3V per line			500	nA
R	I = 10mA	80	100	120	Ω
C <sub>line</sub>	$V_R = 3V DC 1 MHz V_{OSC} = 30 mV$		16	19	pF

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Figure 3: S21 (dB) attenuation measurement dB -10 -20 -30 -40 -50 -60 100k 10M 100M 1M 1G f/Hz

Figure 5: ESD response to IEC61000-4-2 (+15kV air discharge) on one input V(in) and on one output (Vout)

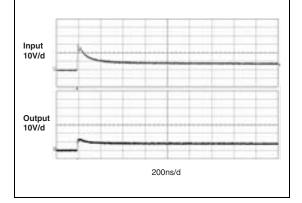
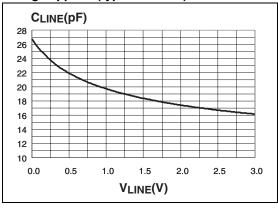


Figure 7: Junction capacitance versus reverse voltage applied (typical values)







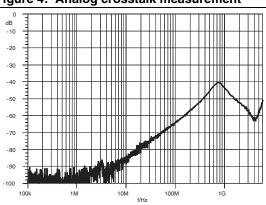
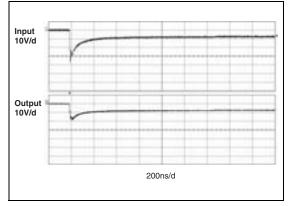


Figure 6: ESD response to IEC61000-4-2 (-15kV air discharge) on one input V(in) and on one output (Vout)





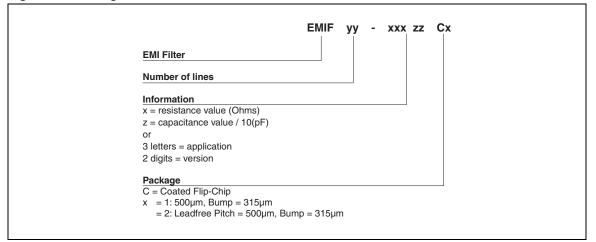
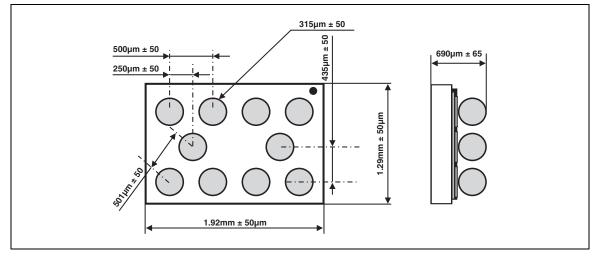
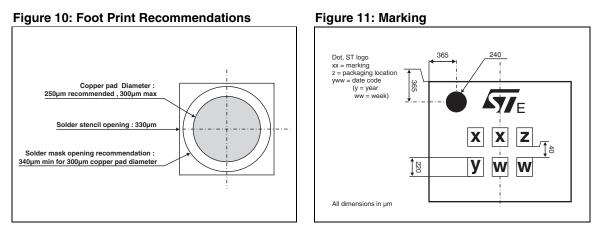


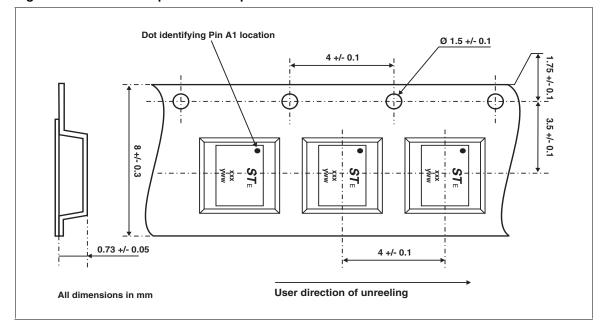
Figure 9: FLIP-CHIP Package Mechanical Data





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#### Figure 12: FLIP-CHIP Tape and Reel Specification

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

#### **Table 4: Ordering Information**

Ordering code	Marking	Package	Weight	Base qty	Delivery mode
EMIF04-VID01C2	GU	Flip-Chip	3.9 mg	5000	Tape & reel 7"

**Note:** More packing informations are available in the application note AN1235: "Flip-Chip: Package description and recommendations for use" AN1751: "EMI Filters: Recommendations and measurements"

#### Table 5: Revision History

Date	Revision	Description of Changes
12-Aug-2005	1	First issue.

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