EMIF04-EAR01F2

IPAD™

4 line EMI filter and ESD protection

Main applications

Where EMI filtering in ESD sensitive equipment is required:

- Earpiece & Headset for Mobile phones
- PDAs
- MP3 players

Description

The **EMIF04-EAR01F2** is a 4 lines highly integrated devices designed to suppress EMI/RFI noise in all systems subjected to electromagnetic interferences. The EMIF04 flip chip packaging means the package size is equal to the die size.

This filter includes an ESD protection circuitry, which prevents the device from destruction when subjected to ESD surges up 15 kV.

Benefits

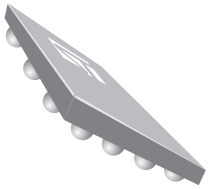
- EMI (I/O) low-pass filter
- High efficiency in EMI filtering
- High density capacitor
- Very low PCB space consuming: 1.92 x 1.42 mm²
- Very thin package: 0.65 mm
- High efficiency in ESD suppression on external pins (IEC 61000-4-2 level 4).
- High reliability offered by monolithic integration
- High reducing of parasitic elements through integration & wafer level packaging.

Complies with the following standards:

IEC 61000-4-2

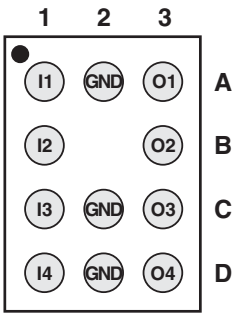
Level 4 15 kV (air discharge) on output pins

Level 1 2 kV (air discharge) on input pins

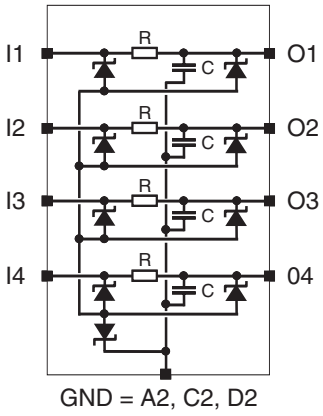


Flip-Chip (11 Bumps)

Pin configuration (Bump side view)



Schematic



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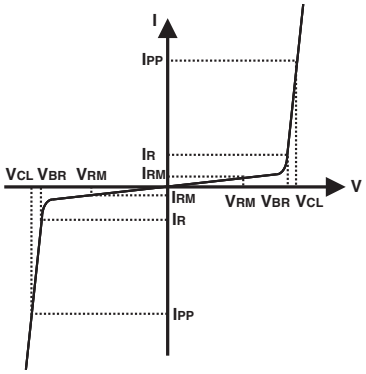
1 Characteristics

Table 1. Absolute maximum ratings (T_{amb} = 25° C)

Symbol	Parameter and test conditions	Value	Unit
V_{PP}	Output pins (A3, B3, C3, D3) ESD discharge IEC61000-4-2, air discharge Input pins (A1, B1, C1, D1) ESD discharge IEC61000-4-2, air discharge	15 2	kV
T_j	Maximum junction temperature	125	°C
T_{op}	Operating temperature range	- 40 to + 85	°C
T_{stg}	Storage temperature range	- 55 to + 150	°C

Table 2. Electrical characteristics (T_{amb} = 25° C)

Symbol	Parameter
V_{BR}	Breakdown voltage
I_{RM}	Leakage current @ V_{RM}
V_{RM}	Stand-off voltage
V_{CL}	Clamping voltage
R_d	Dynamic impedance
I_{PP}	Peak pulse current
R	Series resistance between input and output
C	Capacitance



Symbol	Test conditions	Min.	Typ.	Max.	Unit
V_{BR}	I_R = 1 mA	14		18	V
I_{RM}	V_{RM} = 3 V per line			500	nA
R	Tolerance ± 30%		10		Ω
C	V_{LINE} = 0 V, V_{OSC} = 30 mV, F = 1 MHz Tolerance ± 20%		5.8		nF

Figure 1. S21 (db) all lines attenuation

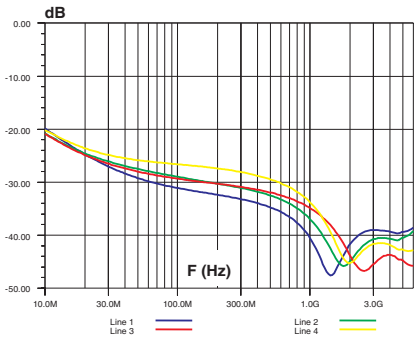


Figure 2. Analog cross talk

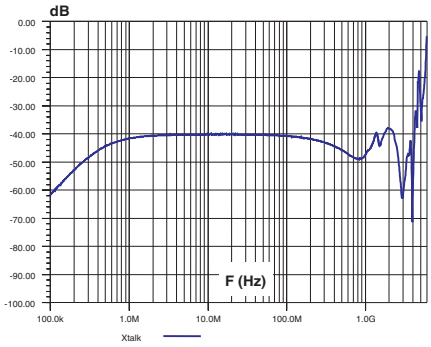


Figure 3. ESD response to IEC61000-4-2 (+15 kV air discharge) on one output

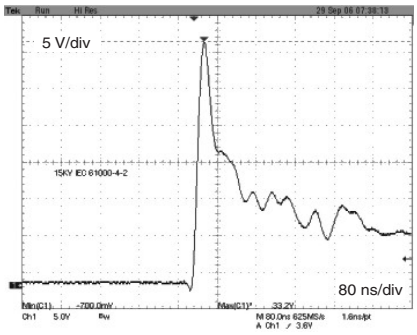


Figure 4. ESD response to IEC61000-4-2 (-15 kV air discharge) on one output

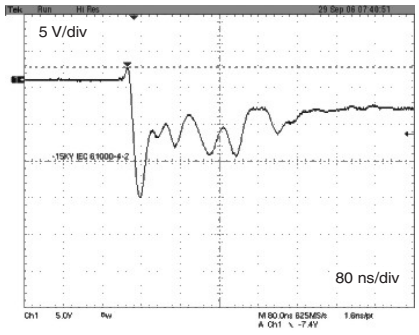
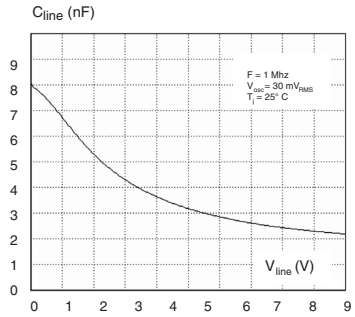


Figure 5. Line capacitance versus reverse applied voltage



2 Ordering information scheme

EMIF yy - xxx zz Fx

EMI Filter

Number of lines

Information
x = resistance value (Ohms)
z = capacitance value / 10(pF)
or
3 letters = application
2 digits = version

Package
F = Flip-Chip
x = 1: 500µm, Bump = 310µm
= 2: Leadfree Pitch = 500µm, Bump = 310µm
= 3: Leadfree Pitch = 400µm, Bump = 255µm

3 Packaging information

Figure 6. Flip-Chip package mechanical data

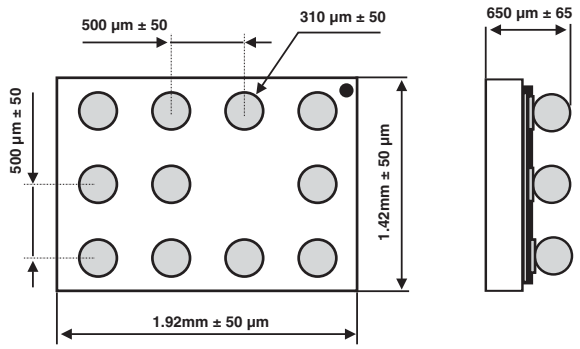


Figure 7. Footprint recommendations

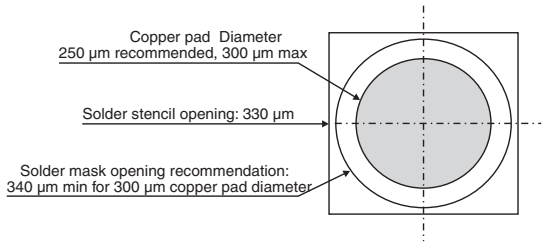


Figure 8. Marking

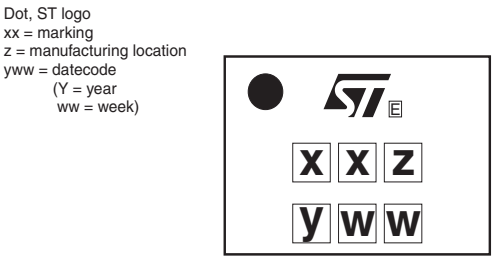
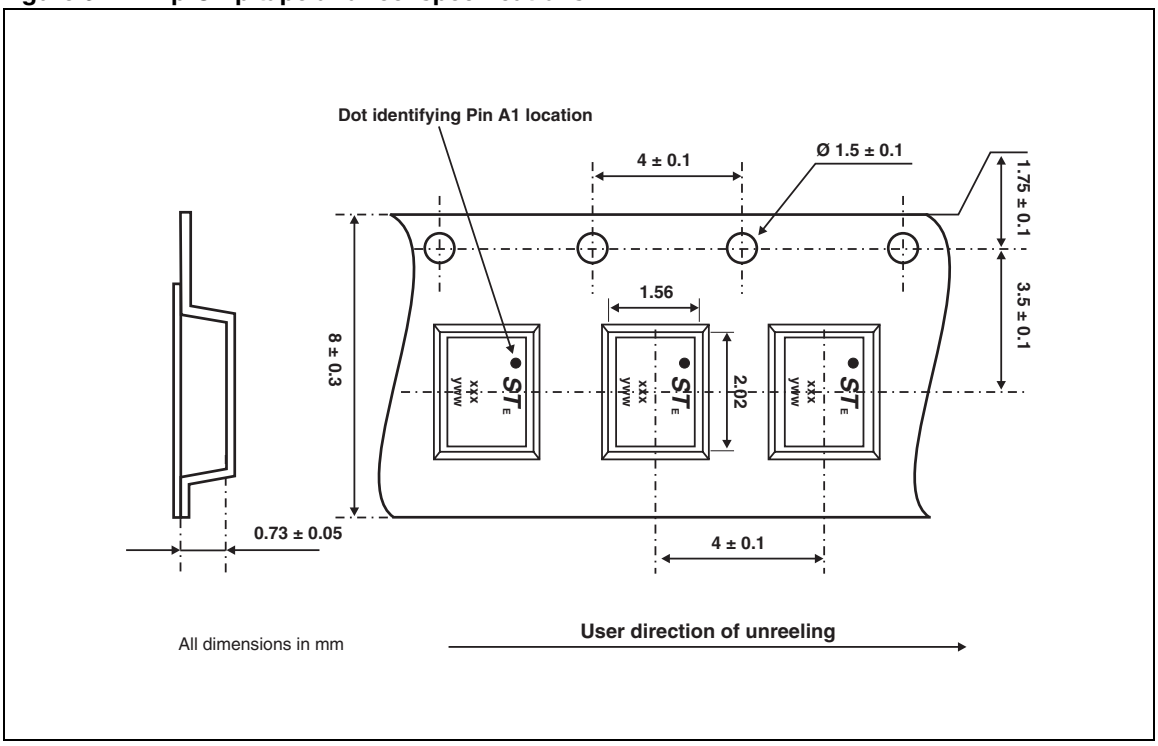


Figure 9. Flip-Chip tape and reel specifications



In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second level interconnect is marked on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

Note: *Note: More information is available in the application note:*
AN2348:"Flip-chip: Package description and recommendations for use"
AN1751: “EMI filters: Recommendations and measurements”

4 Ordering information

Ordering code	Marking	Package	Weight	Base qty	Delivery mode
EMIF04-EAR01F2	GK	Flip-Chip	3.8 mg	5000	Tape & reel 7”

5 Revision history

Date	Revision	Changes
06-Oct-2006	1	Initial release.

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