

# EMIF02-MIC02F2

## **IPAD™**

## 2 LINE EMI FILTER AND ESD PROTECTION

#### MAIN PRODUCT CHARACTERISTICS:

Where EMI filtering in ESD sensitive equipment is required:

- Mobile phones and communication systems
- Computers, printers and MCU Boards

#### **DESCRIPTION**

The EMIF02-MIC02 is a highly integrated devices designed to suppress EMI/RFI noise in all systems subjected to electromagnetic interferences. The EMIF02 flip chip packaging means the package size is equal to the die size.

This filter includes an ESD protection circuitry which prevents the device from destruction when subjected to ESD surges up 15 kV.

### **BENEFITS**

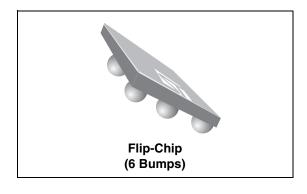
- EMI symmetrical (I/O) low-pass filter High efficiency in EMI filtering
- Lead free package
- Very low PCB space consuming: 1.42 mm x 0.92 mm
- Very thin package: 0.65 mm
- High efficiency in ESD suppression
- High reliability offered by monolithic integration
- High reducing of parasitic elements through integration and wafer level packaging.

### **COMPLIES WITH THE FOLLOWING STANDARDS:** IEC 61000-4-2

Level 4 on input pins 15 kV (air discharge)

(contact discharge) 8 kV

Level 1 on output pins 2 kV (air discharge) 2 kV (contact discharge)



**Table 1: Order Code** 

Part Number	Marking
EMIF02-MIC02F2	FJ

Figure 1: Pin Configuration (Bump side)

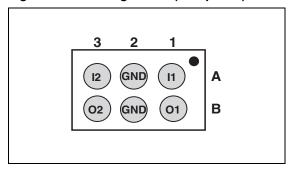
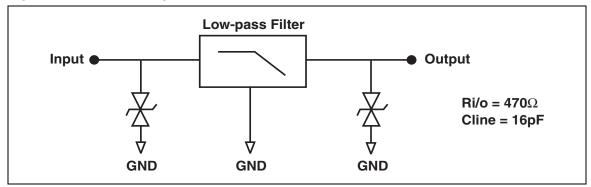


Figure 2: Basic Cell Configuration



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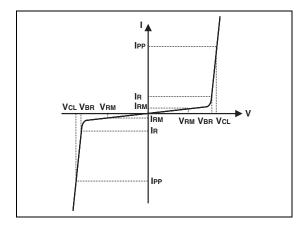
January 2006 REV. 2 1/7

Table 2: Absolute Ratings (limiting values)

Symbol	Parameter and test conditions	Value	Unit
T <sub>j</sub>	Maximum junction temperature	125	°C
T <sub>op</sub>	Operating temperature range	- 40 to + 85	°C
T <sub>stg</sub>	Storage temperature range	- 55 to + 150	°C

**Table 3: Electrical Characteristics**  $(T_{amb} = 25^{\circ}C)$ 

Symbol	Parameter
$V_{BR}$	Breakdown voltage
I <sub>RM</sub>	Leakage current @ V <sub>RM</sub>
V <sub>RM</sub>	Stand-off voltage
V <sub>CL</sub>	Clamping voltage
$R_d$	Dynamic impedance
I <sub>PP</sub>	Peak pulse current
R <sub>I/O</sub>	Series resistance between Input & Output
C <sub>line</sub>	Input capacitance per line



Symbol	Test conditions	Min.	Тур.	Max.	Unit
V <sub>BR</sub>	I <sub>R</sub> = 1 mA	14	16		V
I <sub>RM</sub>	V <sub>RM</sub> = 12 V per line			500	nA
R <sub>I/O</sub>		423	470	517	Ω
C <sub>line</sub>	@ 0 V		16		pF

Figure 3: S21 (dB) attenuation measurement and Aplac simulation

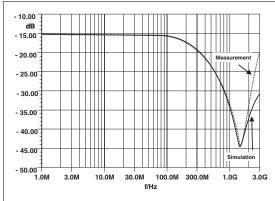


Figure 4: Analog crosstalk measurements

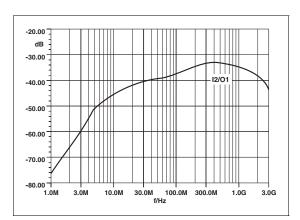


Figure 5: Digital crosstalk measurement

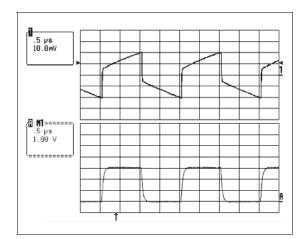


Figure 7: ESD response to IEC 61000-4-2 (+15 kV air discharge) on one input V(in) and on one output (Vout)

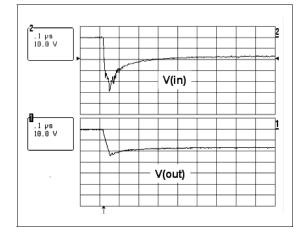


Figure 6: ESD response to IEC 61000-4-2 (+15 kV air discharge) on one input V(in) and on one output (Vout)

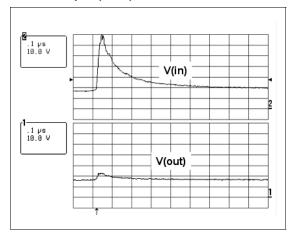
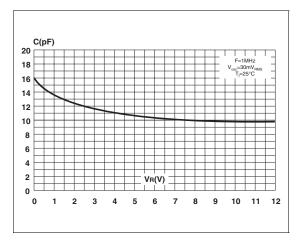


Figure 8: Line capacitance versus applied voltage



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Figure 9: Aplac model

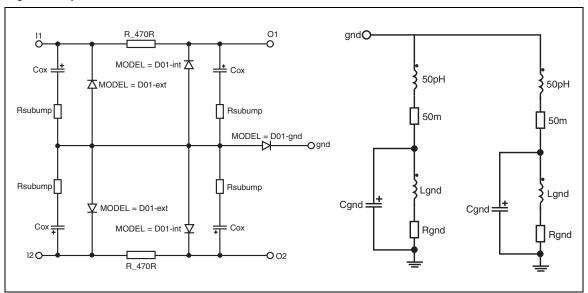


Figure 10: Aplac parameters

IBV = 1u	BV = 7 CJO = Cz_ext IBV = 1u IKF = 1000 IS = 10f ISR = 100p N = 1 M = 0.3333 RS = Rs_ext VJ = 0.6	$CJO = Cz\_int$ IBV = 1u IKF = 1000 IS = 10f ISR = 100p N = 1 M = 0.3333 $RS = Rs\_int$ VJ = 0.6	CJO = Cz_gnd IBV = 1u IKF = 1000 IS = 10f ISR = 100p N = 1 M = 0.3333 RS = Rs_gnd VJ = 0.6	Cz_ext 8.73pF Rs_ext 850m Cz_int 2.9pF Rs_int 850m Cz_gnd 215.61pF Rs_gnd 470m  Rgnd 10m Lgnd 48pH Cgnd 0.15pF
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Figure 11: Ordering Information Scheme

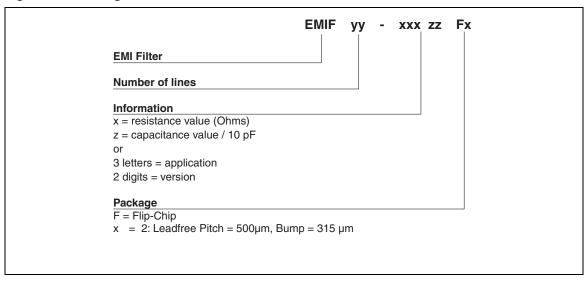


Figure 12: FLIP-CHIP Package Mechanical Data

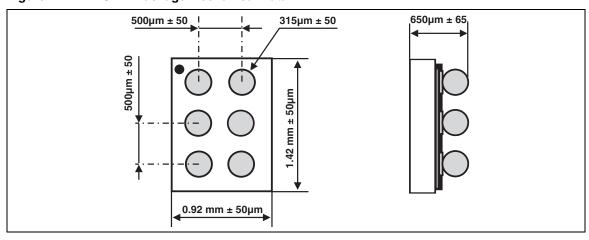


Figure 13: Foot print recommendations

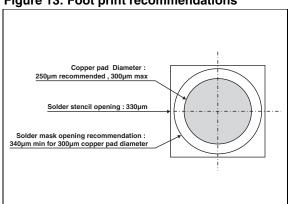
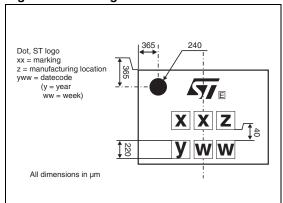


Figure 14: Marking





Dot identifying Pin A1 location

4 +/- 0.1

0 1.5 +/- 0.1

0 1.5 +/- 0.1

All dimensions in mm

User direction of unreeling

Figure 15: FLIP-CHIP Tape and Reel Specification

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second level interconnect is marked on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECO-PACK specifications are available at: www.st.com.

**Table 4: Ordering Information** 

Ordering code	Marking	Package	Weight	Base qty	Delivery mode
EMIF02-MIC02F2	FJ	Flip-Chip	2.3 mg	5000	Tape & reel 7"

**Note:** More informations are available in the application notes: AN1235: "Flip-Chip: Package description and recommendations for use" AN1751: "EMI Filters: Recommendations and measurements"

**Table 5: Revision History** 

Date	Revision	Description of Changes
12-Oct-2004	1	First issue
11-Jan-2006	2	ECOPACK statement added. Die dimensions modified in Figure 12 and first page. Typographical errors corrected.

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