



EMIF02-USB01F2

IPAD™

2 LINES EMI FILTER INCLUDING ESD PROTECTION

PRODUCT CHARACTERISTICS

ESD protection and EMI filtering for:

- USB port

DESCRIPTION

The EMIF02-USB01F2 is a highly integrated array designed to suppress EMI / RFI noise for USB port filtering.

The EMIF02-USB01F2 flip-chip packaging means the package size is equal to the die size.

Additionally, this filter includes an ESD protection circuitry which prevents the protected device from destruction when subjected to ESD surges up to 15 kV.

BENEFITS

- 2 lines low-pass-filter + 2 lines ESD protection
- High efficiency in EMI filtering
- Lead free package
- Very low PCB space consuming: < 2.5 mm²
- Very thin package: 0.65 mm
- High efficiency in ESD suppression (IEC61000-4-2 level 4)
- High reliability offered by monolithic integration
- High reducing of parasitic elements through integration & wafer level packaging.

COMPLIES WITH THE FOLLOWING STANDARDS:

IEC61000-4-2

Level 4

15kV (air discharge)

8kV (contact discharge)

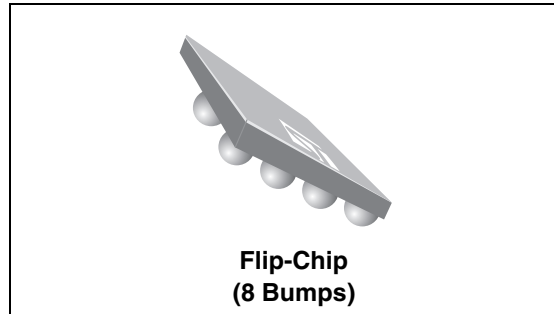


Table 1: Order Code

Part Number	Marking
EMIF02-USB01F2	FF

Figure 1: Pin Configuration (Ball side)

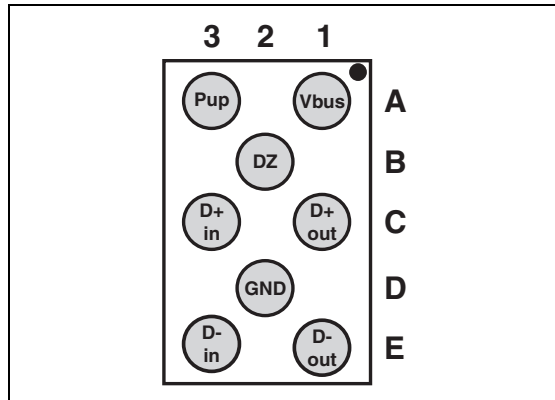
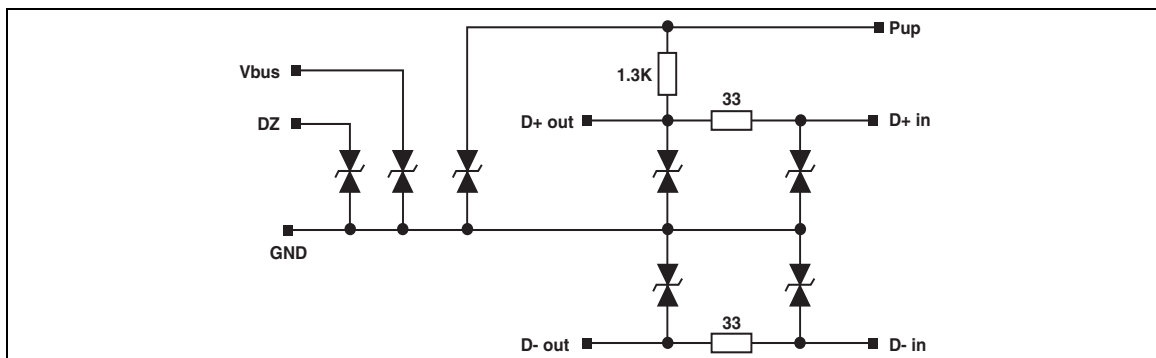


Figure 2: Configuration



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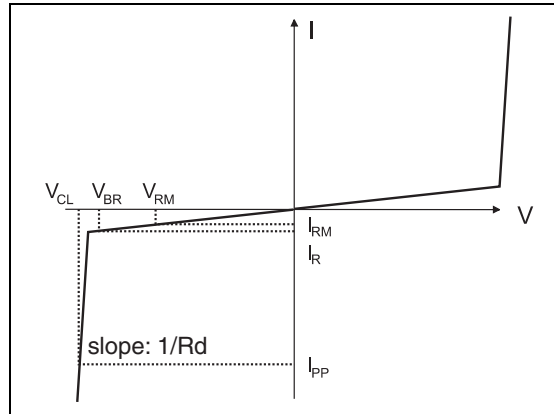
EMIF02-USB01F2

Table 2: Absolute Ratings ($T_{amb} = 25^{\circ}\text{C}$)

Symbol	Parameter and test conditions	Value	Unit
T_j	Junction temperature	125	$^{\circ}\text{C}$
T_{op}	Operating temperature range	- 40 to + 85	$^{\circ}\text{C}$
T_{stg}	Storage temperature range	- 55 to + 150	$^{\circ}\text{C}$

Table 3: Electrical Characteristics ($T_{amb} = 25^{\circ}\text{C}$)

Symbol	Parameter
V_{BR}	Breakdown voltage
I_{RM}	Leakage current @ V_{RM}
V_{RM}	Stand-off voltage
V_{CL}	Clamping voltage
R_d	Dynamic impedance
I_{PP}	Peak pulse current
$R_{I/O}$	Series resistance between Input & Output
C_{line}	Input capacitance per line



Symbol	Test conditions	Min.	Typ.	Max.	Unit
V_{BR}	$I_R = 1 \text{ mA}$	6			V
I_{RM}	$V_{RM} = 3\text{V}$			0.5	μA
C_{line}	@ 0V		40	45	pF
R_1, R_2	Tolerance $\pm 5\%$		33		Ω
R_3	Tolerance $\pm 5\%$		1.30		k Ω

Figure 3: S21 (dB) attenuation measurement

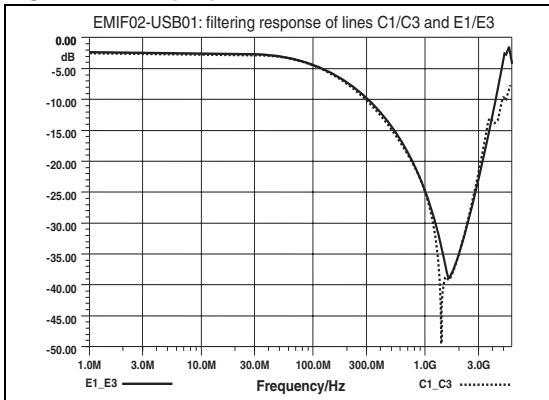


Figure 4: Analog crosstalk measurements

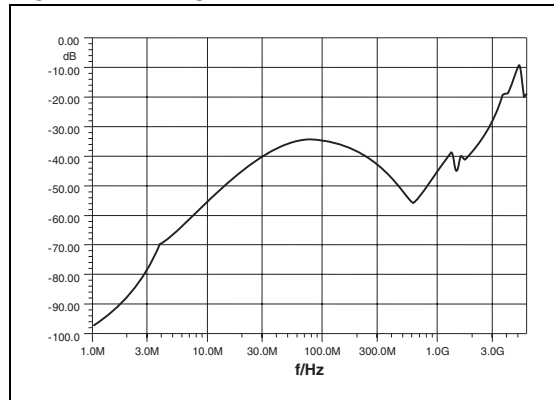


Figure 5: ESD response to IEC61000-4-2 (+15kV air discharge) on one input V(in) and on one output (Vout)

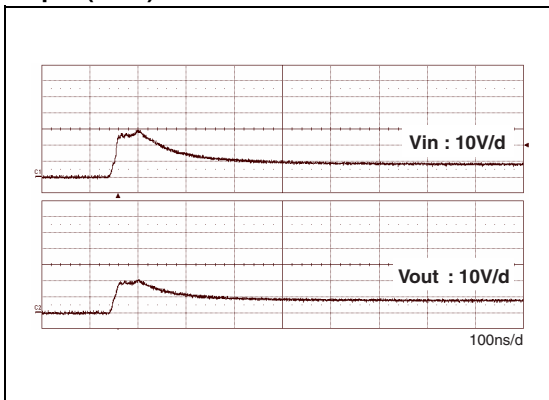


Figure 6: ESD response to IEC61000-4-2 (-15kV air discharge) on one input V(in) and on one output (Vout)

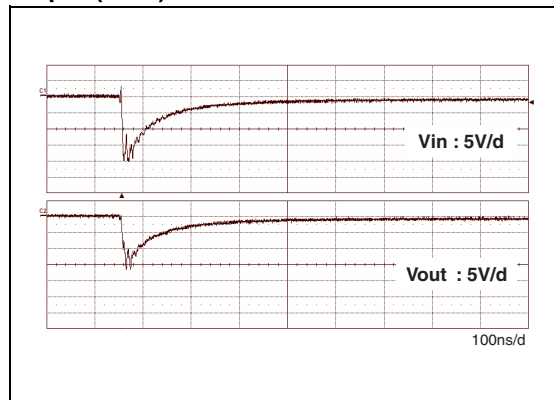


Figure 7: Capacitance versus reverse applied voltage (typical)

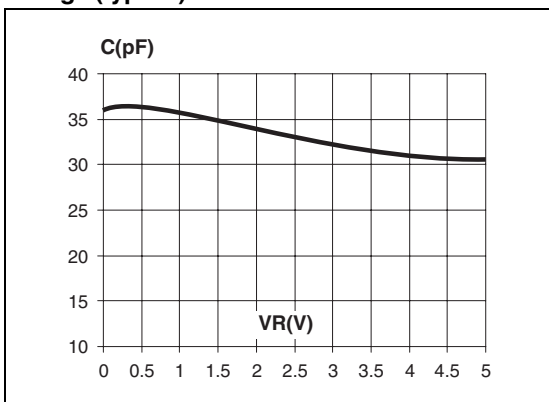


Figure 8: Aplac model (resistors, diodes and bumps and ground connections)

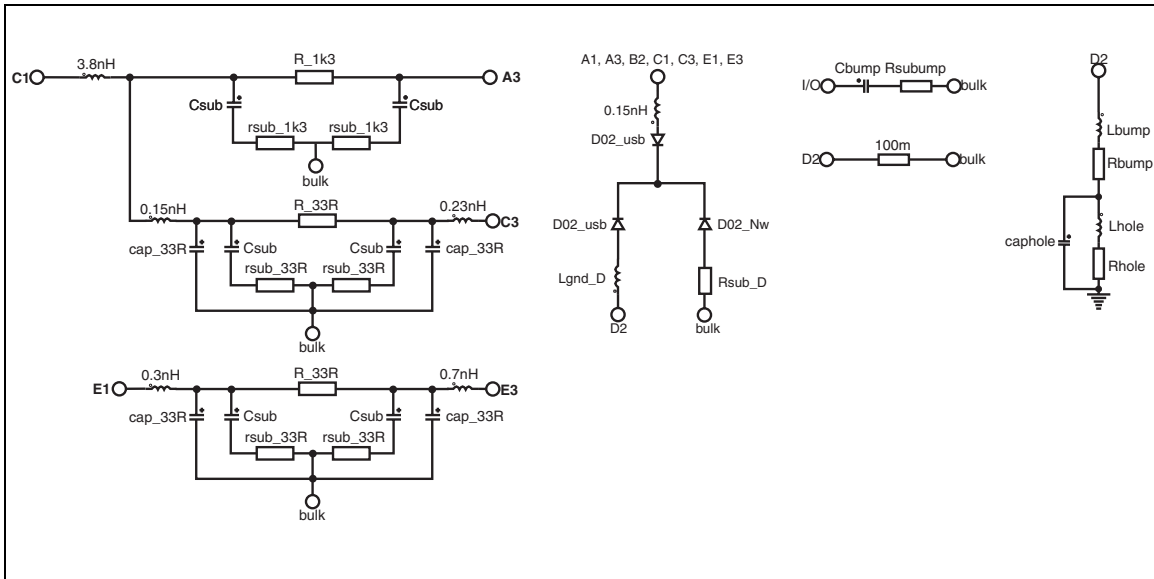


Figure 9: Aplac model parameters

R_33R 33.9	Model D02_Nw	Model D02_usb
cap_33R 1.2pF	BV=100	BV=16
	IBV=1m	IBV=1m
R_1k3 1.3k	CJO=6.8p	CJO=Cz
	M=0.3333	M=0.3333
Cz29pF	RS=2	RS=2
Rsub_D 100	VJ=0.6	VJ=0.6
	TT=100n	TT=100n
Csub0.3pF		
Rsub_33R 15		
Rsub_1k3 50		
lhole10pH		
Rhole400m		
Caphole0.4pF		
Lgnd_D 150pH		
Lbump50pH		
Rbump50m		
Cbump1.5pF		
Rsubump150		

Figure 10: Ordering Information Scheme

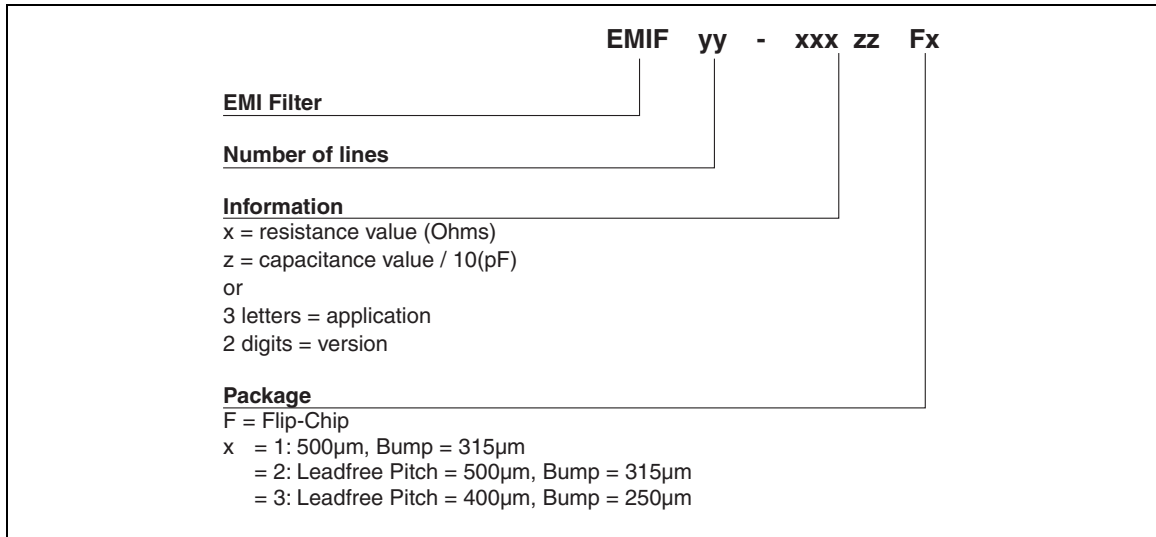


Figure 11: FLIP-CHIP Package Mechanical Data

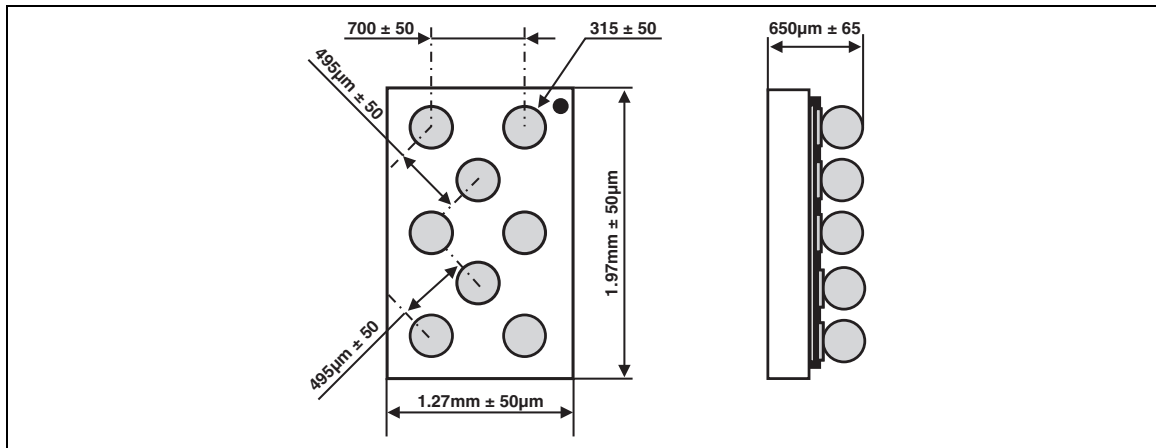


Figure 12: Foot print recommendations

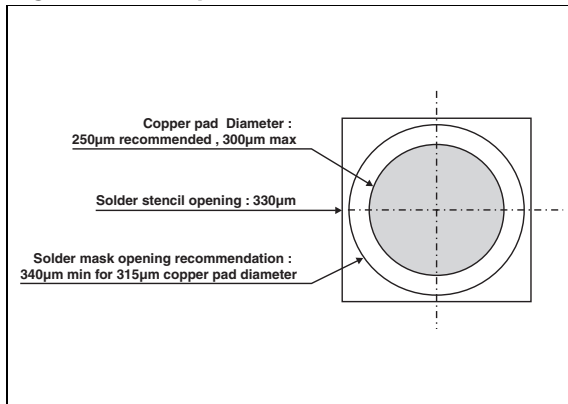


Figure 13: Marking

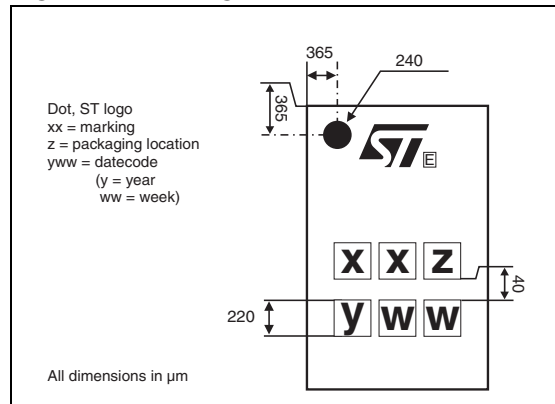


Figure 14: FLIP-CHIP Tape and Reel Specification

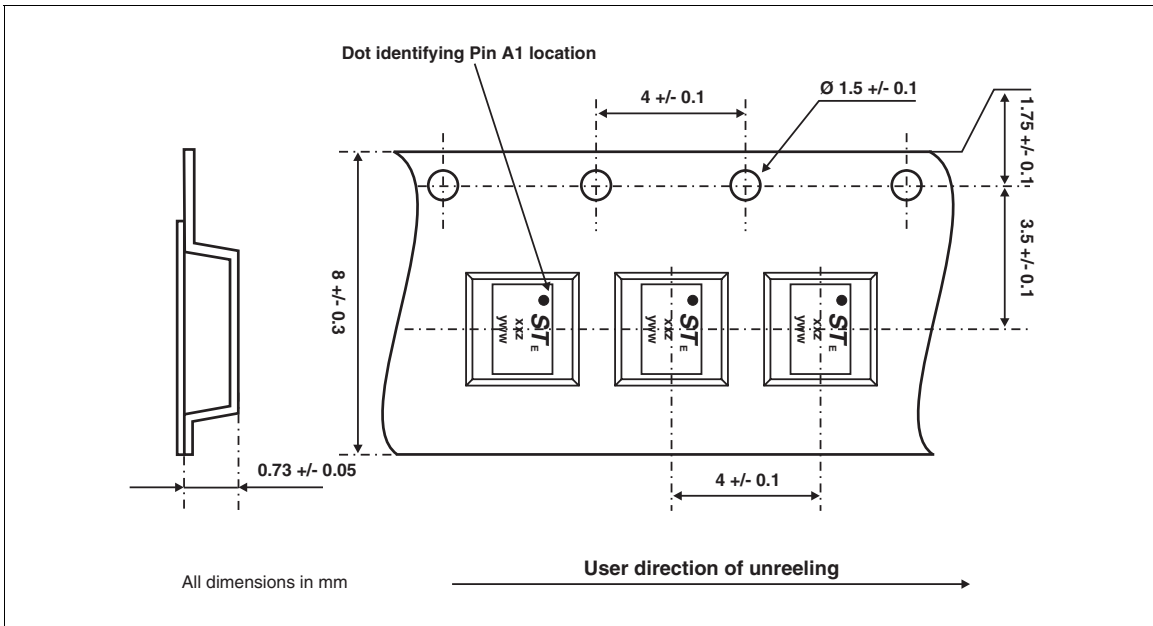


Table 4: Ordering Information

Ordering code	Marking	Package	Weight	Base qty	Delivery mode
EMIF02-USB01F2	FF	Flip-Chip	3.35 mg	5000	Tape & reel 7"

Note: More informations are available in the application notes:
 AN1235: "Flip-Chip: Package description and recommendations for use"
 AN1751: "EMI Filters: Recommendations and measurements"

Table 5: Revision History

Date	Revision	Description of Changes
26-Oct-2004	1	First issue

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