

2-line IPAD™, EMIF filter and ESD protection

Features

- Lead free package
- Very low resistance: 0.35 Ω
- High attenuation: - 45 dB at 900 MHz
- Very low PCB space consumption:
0.89 mm x 1.26 mm
- Very thin package: 0.65 mm
- High efficiency in ESD suppression
IEC6 1000-4-2 level 4
- High reliability offered by monolithic integration
- High reduction of parasitic elements through
integration and wafer level packaging

Complies with the following standards

- IEC 61000-4-2 level 4
 - 15 kV (air discharge)
 - 8 kV (contact discharge)

Application

Mobile phones

Description

The EMIF02-SPK02F2 chip is a highly integrated device designed to suppress EMI/RFI noise for interface line filtering.

The EMIF02-SPK02F2 Flip-Chip packaging means the package size is equal to the die size. That's why the EMIF02-SPK02F2 is a very small device.

Additionally, this filter includes ESD protection circuitry, which prevents damage to the protected device when subjected to ESD surges up 30 kV.

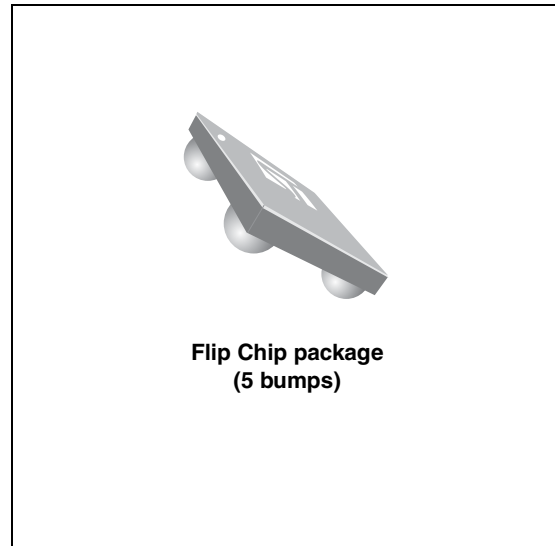


Figure 1. Pin configuration (bump side)

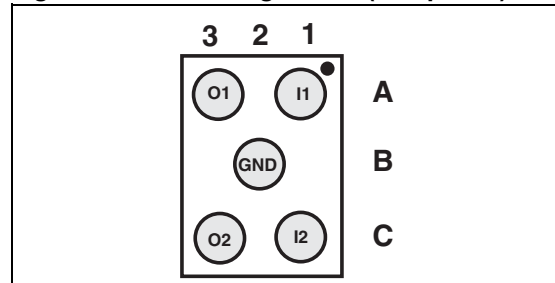
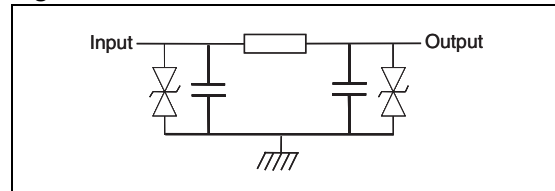


Figure 2. Functional schematic



TM: IPAD is a trademark of STMicroelectronics

1 Characteristics

Table 1. Absolute maximum ratings ($T_{amb} = 25\text{ }^{\circ}\text{C}$)

Symbol	Parameter	Value	Unit
V_{PP}	ESD discharge IEC 61000-4-2		
	Air discharge	30	kV
	Contact discharge	30	
I_{SPK}	Maximum rms current per channel	350	mA
T_j	Junction temperature range	-30 to 125	$^{\circ}\text{C}$
T_{stg}	Storage temperature range	-55 to + 150	$^{\circ}\text{C}$

Table 2. Electrical characteristics ($T_{amb} = 25\text{ }^{\circ}\text{C}$)

Symbol	Parameters				
V_{BR}	Breakdown voltage				
I_{RM}	Leakage current @ V_{RM}				
V_{RM}	Stand-off voltage				
V_{CL}	Clamping voltage				
R_d	Dynamic impedance				
I_{PP}	Peak pulse current				
$R_{I/O}$	Series resistance between input and output				
C_{line}	Input capacitance per line				
Symbol	Test conditions	Min	Typ	Max	Unit
V_{BR}	$I_R = 1\text{ mA}$	6			V
I_{RM}	$V_{RM} = 3\text{ V}$			400	nA
$R_{I/O}$			0.35	0.8	Ω
C_{line}	$V_R = 0\text{ V DC}, 1\text{ MHz}$	185	250	315	pF
f_c	Cut-off frequency: $Z_{SOURCE} = Z_{LOAD} = 50\ \Omega$		20		MHz

Figure 3. S21 attenuation measurement

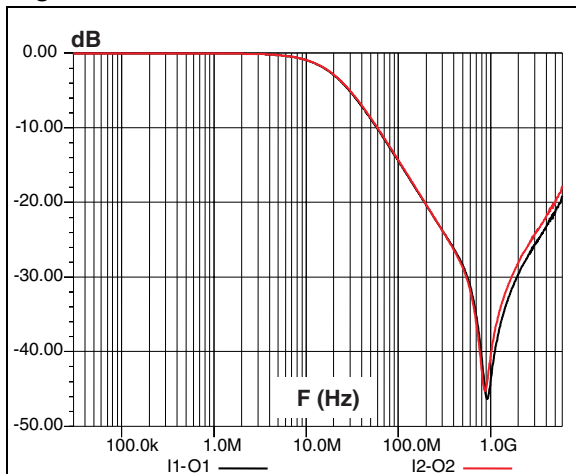


Figure 4. Analog crosstalk measurements

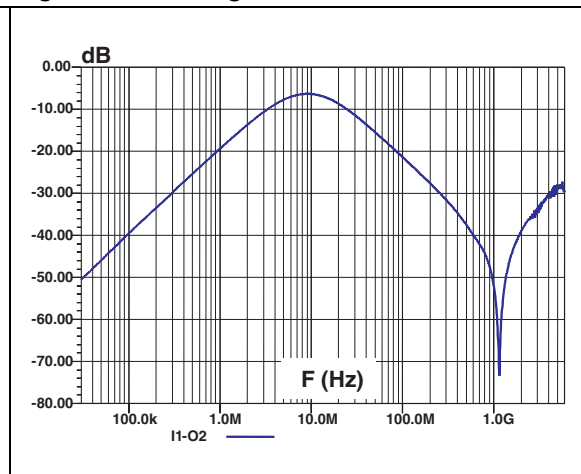


Figure 5. ESD response to IEC 61000-4-2 (+15 kV air discharge) on one input $V_{(in)}$ and on one output $V_{(out)}$

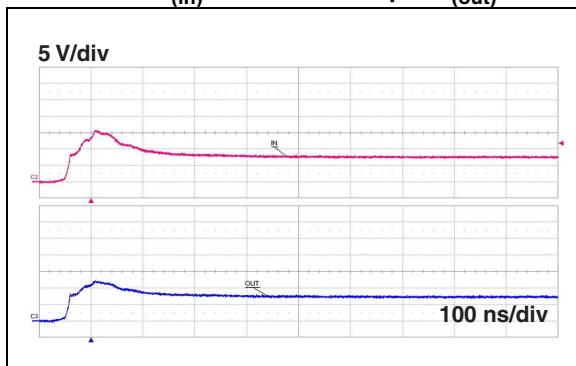


Figure 6. ESD response to IEC 61000-4-2 (-15 kV air discharge) on one input $V_{(in)}$ and on one output $V_{(out)}$

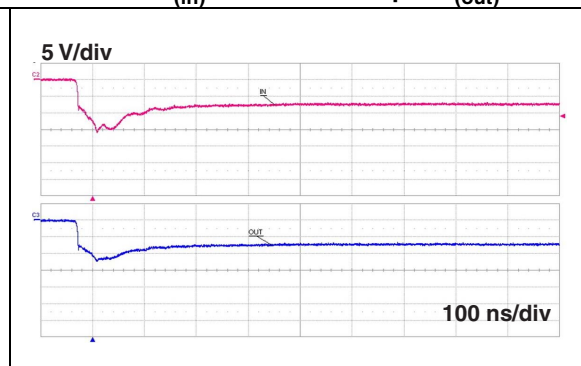
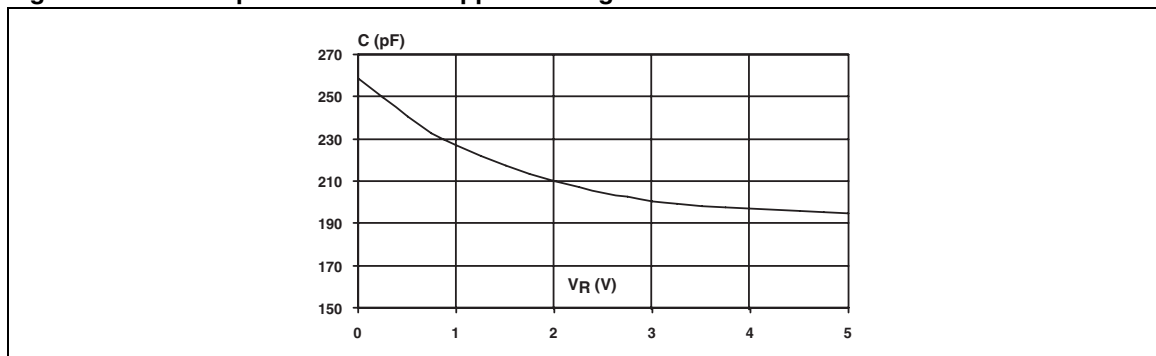
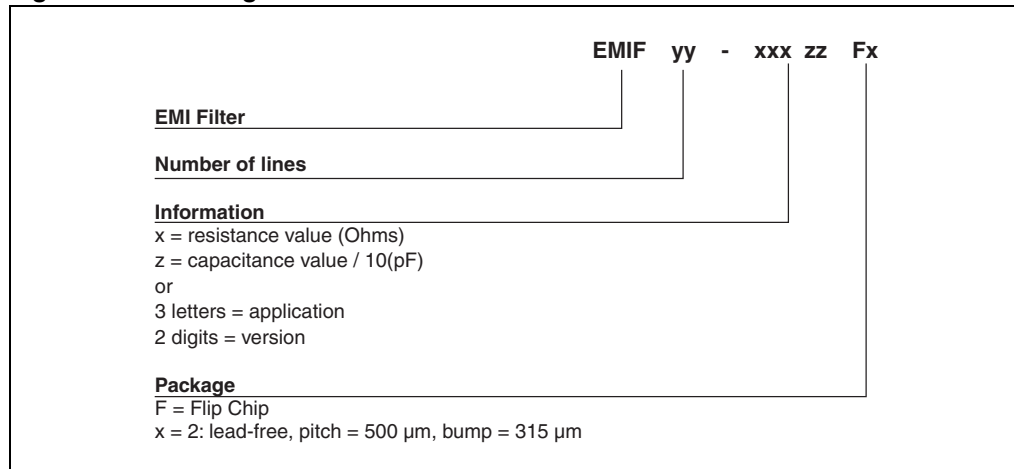


Figure 7. Line capacitance versus applied voltage



2 Ordering information scheme

Figure 8. Ordering information scheme



3 Package information

In order to meet environmental requirements, ST offers these devices in ECOPACK[®] packages. These packages have a lead-free second level interconnect. The category of second level interconnect is marked on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at www.st.com.

Figure 9. Package dimensions

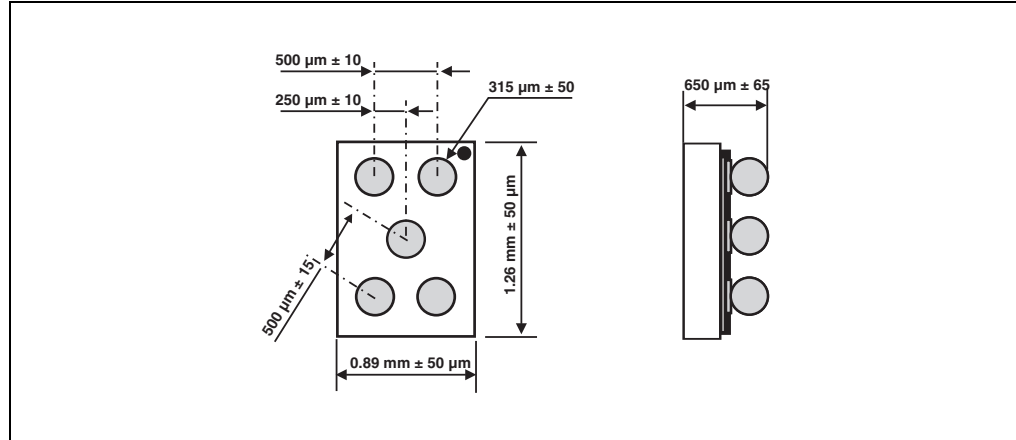


Figure 10. Footprint

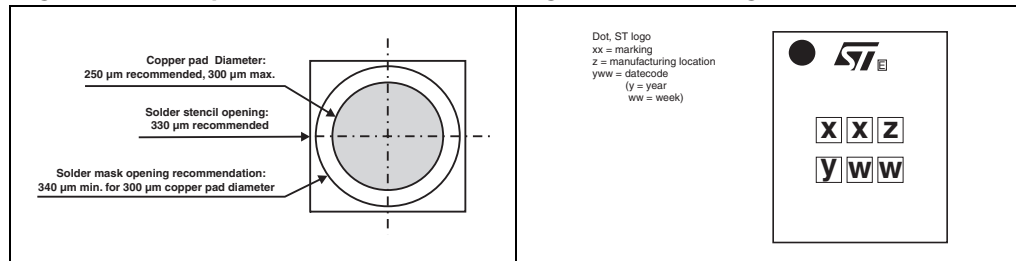


Figure 11. Marking

Dot, ST logo
 xx = marking
 z = manufacturing location
 yww = datecode
 (y = year
 ww = week)

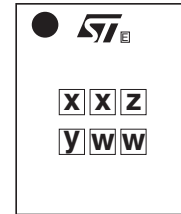
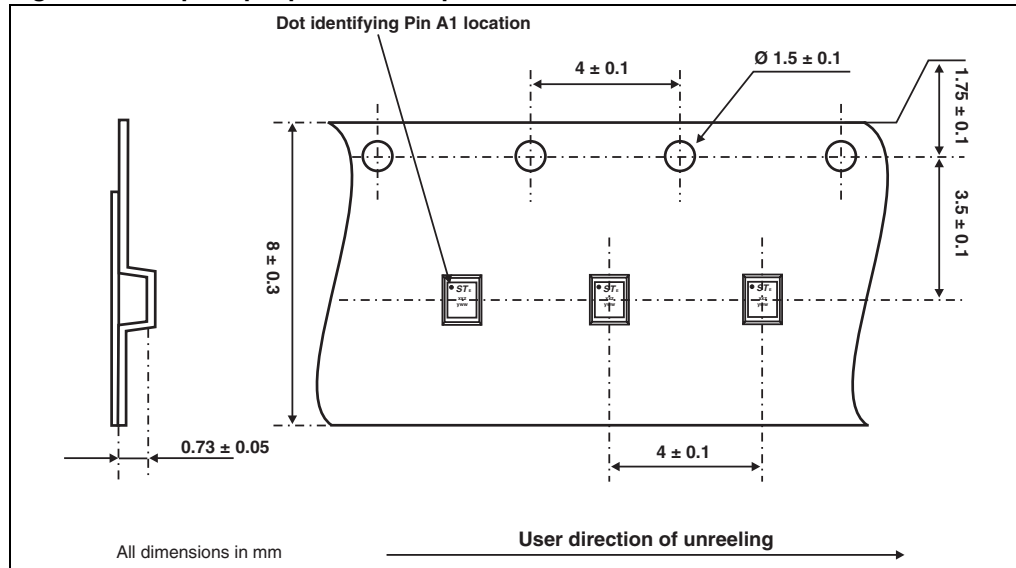


Figure 12. Flip Chip tape and reel specification



Note: More information is available in the application notes:
 AN1235: "Flip Chip: Package description and recommendations for use"
 AN1751: "EMI filters: Recommendations and measurements"

4 Ordering information

Table 3. Ordering information

Order code	Marking	Package	Weight	Base qty	Delivery mode
EMIF02-SPK02F2	JD	Flip Chip	1.8 mg	5000	Tape and reel 7"

5 Revision history

Table 4. Document revision history

Date	Revision	Changes
17-Sep-2008	1	Initial release.

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