



# EMIF02-MIC02F3

IPAD™

2 line EMI filter including ESD protection

## Main product characteristics:

Where EMI filtering in ESD sensitive equipment is required:

- Mobile phones and communication systems
- Computers, printers and MCU Boards

## Description

The EMIF02-MIC02F3 is a highly integrated device designed to suppress EMI/RFI noise in all systems subjected to electromagnetic interference.

This filter includes ESD protection circuitry, which prevents damage to the application when subjected to ESD surges up to 15 kV.

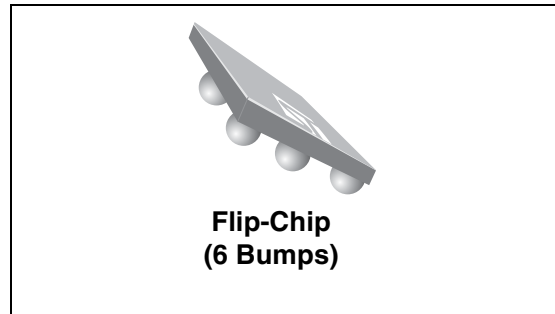
## Benefits

- EMI symmetrical (I/O) low-pass filter
- High efficiency EMI filtering
- Lead-free package
- Very low PCB space consumption: 0.9 mm<sup>2</sup>
- Very thin package: 0.60 mm
- High efficiency ESD suppression
- High reliability offered by monolithic integration
- High reduction of parasitic elements through integration and wafer level packaging

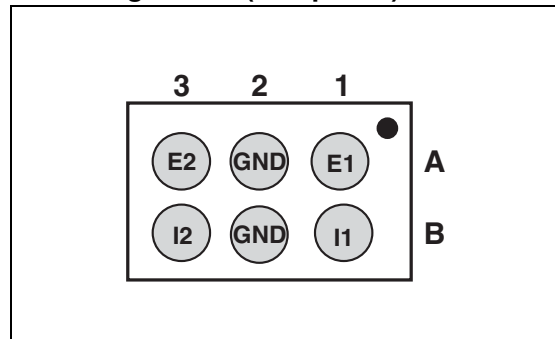
## Complies with the following standards:

### IEC61000-4-2:

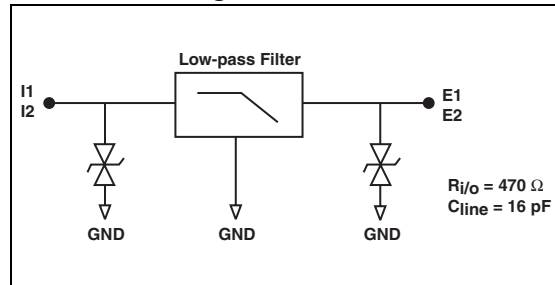
- Level 4 on external pins 15 kV (air discharge)  
8 kV (contact discharge)
- Level 1 on internal pins 2 kV (air discharge)  
2 kV (contact discharge)



## Pin configuration (bump side)



## Basic cell configuration



## Order code

Part Number	Marking
EMIF02-MIC02F3	HB

TM: IPAD id a trademark of STMicroelectronics

January 2006

Rev 1  
1/8

[www.st.com](http://www.st.com)

# 1 Characteristics

## 1.1 Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
$V_{PP}$	<b>External pins (A1, A3):</b>		
	ESD discharge IEC61000-4-2, air discharge	15	kV
	ESD discharge IEC61000-4-2, contact discharge	8	
	<b>Internal pins (B1, B3):</b>		
ESD discharge IEC61000-4-2, air discharge	2		
$T_j$	Junction temperature	125	°C
$T_{op}$	Operating temperature range	-40 to + 85	°C
$T_{stg}$	Storage temperature range	-55 to +150	°C

## 1.2 Electrical characteristics ( $T_{amb} = 25\text{ °C}$ )

Symbol	Parameter
$V_{BR}$	Breakdown voltage
$I_{RM}$	Leakage current @ $V_{RM}$
$V_{RM}$	Stand-off voltage
$V_{CL}$	Clamping voltage
$R_d$	Dynamic impedance
$I_{PP}$	Peak pulse current
$R_{I/O}$	Series resistance between Input & Output
$C_{line}$	Input capacitance per line

Symbol	Test conditions	Min.	Typ.	Max.	Unit
$V_{BR}$	$I_R = 1\text{ mA}$	14	16		V
$I_{RM}$	$V_{RM} = 12\text{ V per line}$			200	nA
$R_{I/O}$	Tolerance $\pm 10\%$		470		$\Omega$
$C_{line}$	$V_{line} = 0\text{V}$ , $V_{OSC} = 30\text{ mV}$ , $F = 1\text{ MHz}$ , (measured under zero light conditions)		16	20	pF

Figure 1. S21 (dB) attenuation measurement (Line 1)

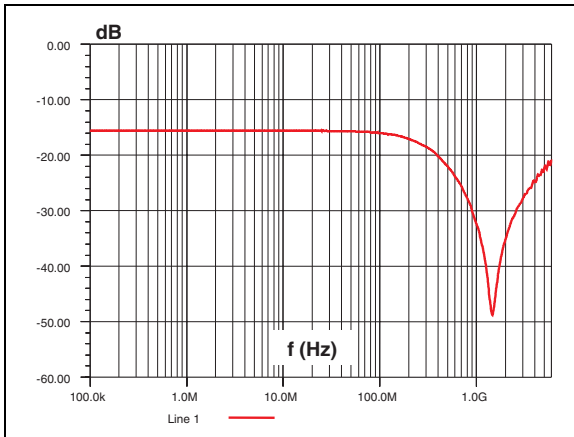


Figure 2. S21 (dB) attenuation measurement (Line 2)

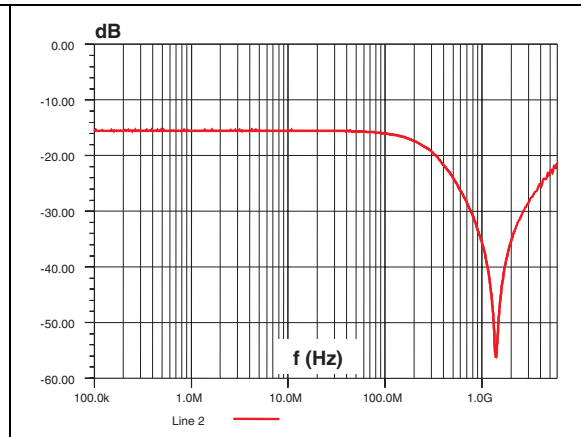


Figure 3. Analog crosstalk measurement

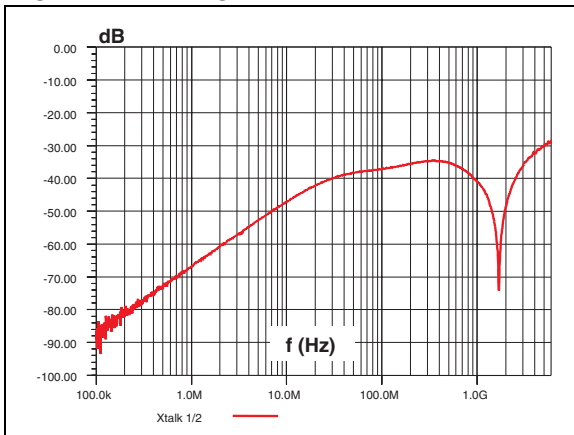


Figure 4. Digital crosstalk measurement

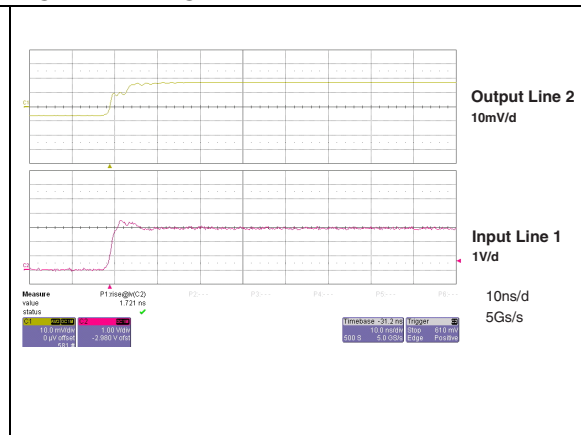


Figure 5. ESD response to IEC61000-4-2 (+15kV air discharge) on one input and on one output

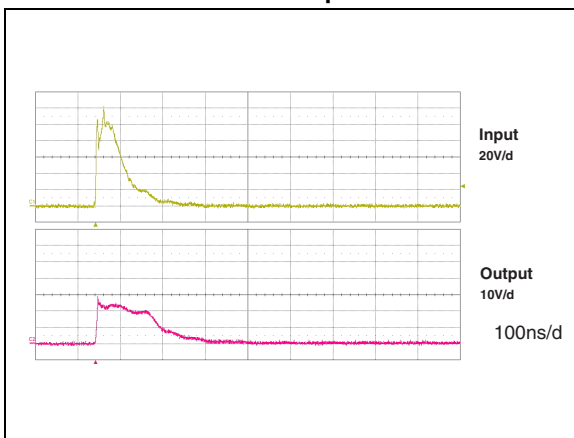
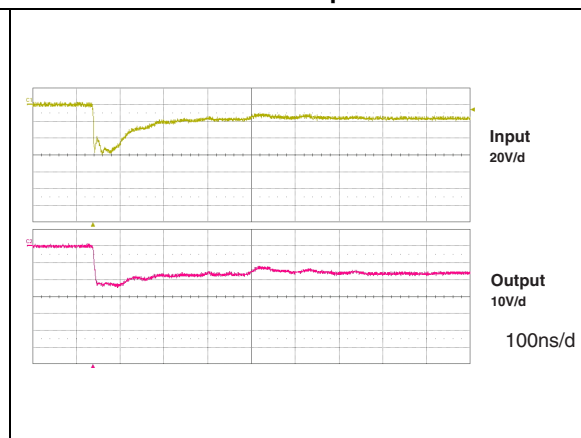
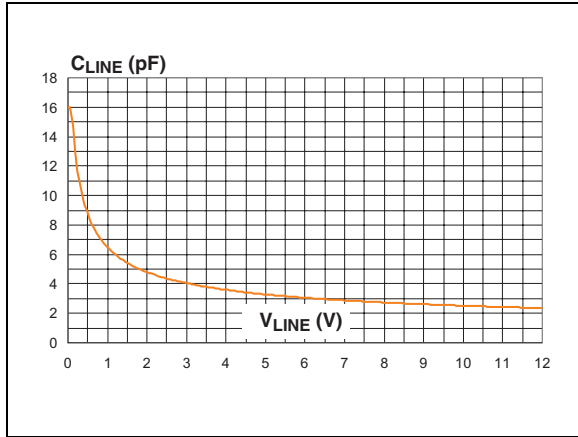


Figure 6. ESD response to IEC61000-4-2 (-15kV air discharge) on one input and on one output



**Figure 7. Line capacitance versus applied voltage**



**Figure 8. Aplac model**

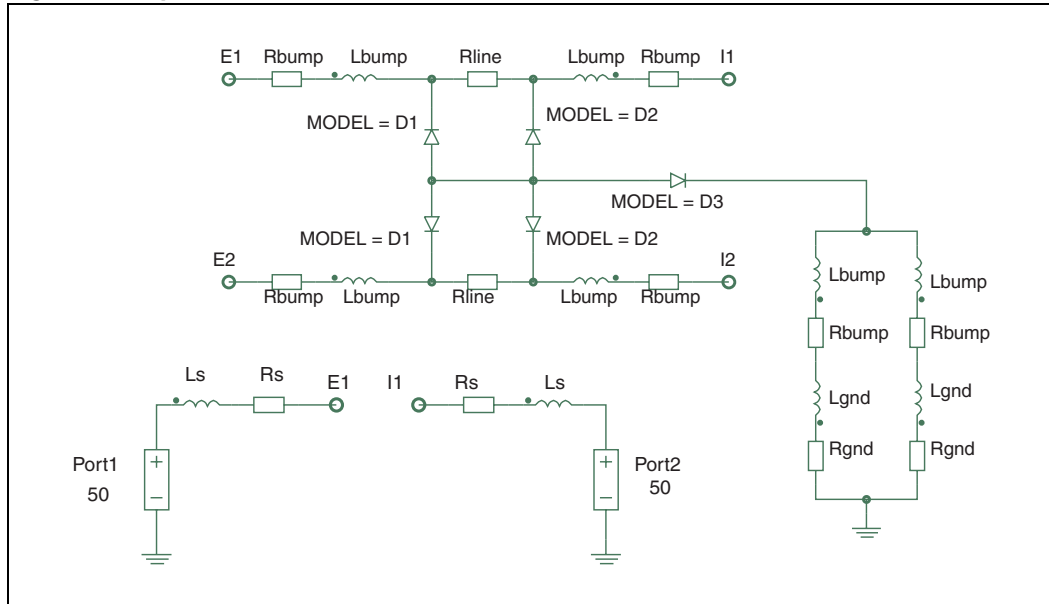


Figure 9. Aplac parameters

Variables	Diode D1	Diode D2	Diode D3
aplacvar Rline 490	BV=7	BV=7	BV=7
aplacvar C_d1 11p	CJO=c_d1	CJO=c_d2	CJO=c_d3
aplacvar C_d2 5p	IBV=1u	IBV=1u	IBV=1u
aplacvar C_d3 240p	IKF=1000	IKF=1000	IKF=1000
aplacvar L 2pH	IS=10f	IS=10f	IS=10f
aplacvar Ls 950pH	ISR=100p	ISR=100p	ISR=100p
aplacvar Rs 150m	N=1	N=1	N=1
aplacvar Lbump 50pH	M=0.3333	M=0.3333	M=0.3333
aplacvar Rbump 20m	RS=0.85	RS=0.85	RS=0.47
aplacvar Lgnd 80pH	VJ=0.6	VJ=0.6	VJ=0.6
aplacvar Rgnd 100m	TT=50n	TT=50n	TT=50n

## 2 Ordering information scheme

EMIF	yy	-	xxx	zz	Fx
<b>EMI Filter</b>					
<b>Number of lines</b>					
<b>Information</b>					
x = resistance value (Ohms)					
z = capacitance value / 10(pF)					
or					
3 letters = application					
2 digits = version					
<b>Package</b>					
F = Flip-Chip					
x = 2: Leadfree Pitch = 500µm, Bump = 315µm					
= 3: Leadfree Pitch = 400µm, Bump = 255µm					

### 3 Package information

Figure 10. Mechanical data

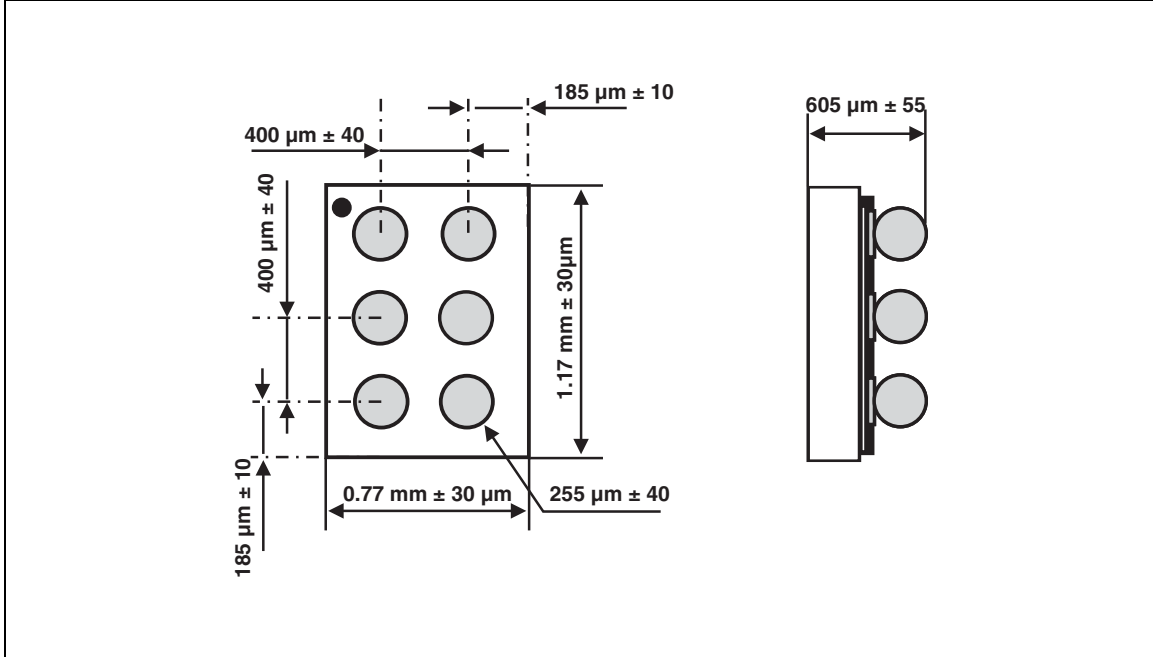


Figure 11. Foot print recommendations

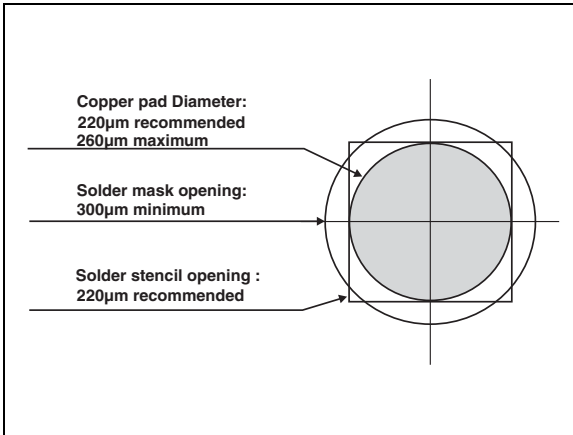


Figure 12. Marking

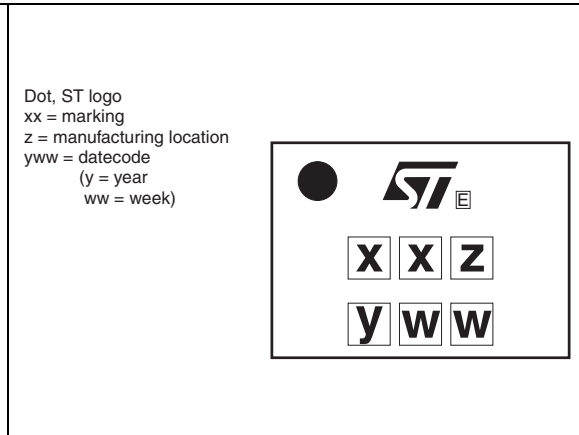
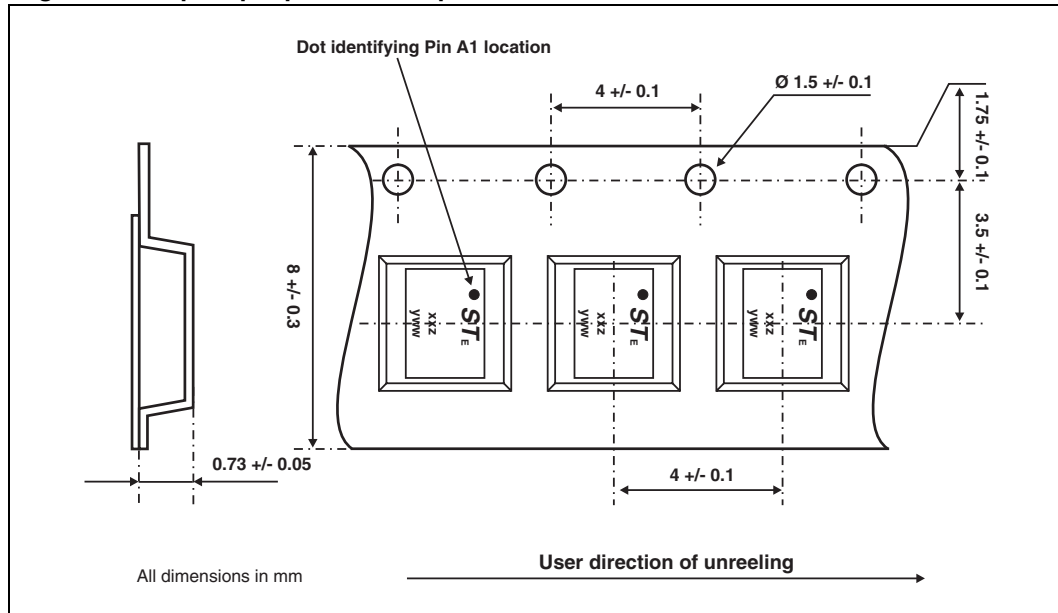


Figure 13. Flip-chip tape and reel specifications



In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second level interconnect is marked on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: [www.st.com](http://www.st.com).

## 4 Ordering information

Part Number	Marking	Package	Base qty	Delivery mode
EMIF02-MIC02F3	HB	Flip-Chip	5000	Tape & reel (7")

Note: More information is available in the application notes:  
 AN1235: "Flip-Chip: Package description and recommendations for use"  
 AN1751: "EMI Filters: Recommendations and measurements"

## 5 Revision history

Date	Revision	Changes
17-Jan-2006	1	Initial release.

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