EMIF02-AV01F3

IPAD

EMI filter and ESD protection

Main application

- Dual audio and video line interface protection and filtering in mobile phones

Description

The EMIF02-AV01F3 is a highly integrated array designed to suppress EMI / RFI noise and provide impedance matching for mobile phones and portable applications.

The EMIF02-AV01F3 is in Flip-chip package to offer space saving and high RF performance.

Additionally, this low-pass filter includes an ESD protection circuitry to prevent damage to the application when subjected to ESD surges up to 15 kV.

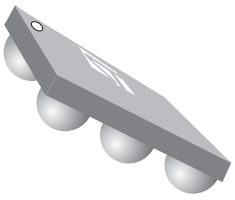
Benefits

- High-density capacitor
- EMI low-pass filter and ESD protection
- High-efficiency in EMI filtering
- Lead-free package
- 400 µm pitch
- Very small PCB footprint: 0.91 mm x 1.31 mm
- Very thin package: 0.605 mm
- High reliability offered by monolithic integration
- Reduction of parasitic elements thanks to CSP integration

Complies with following standards:

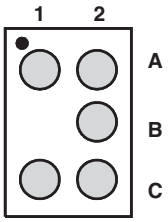
IEC 61000-4-2

level 4 on external pin (A2, C2)	15 kV (air discharge) 8 kV (contact discharge)
level 1 on internal pin (A1, C1)	2 kV (air discharge) 2 kV (contact discharge)

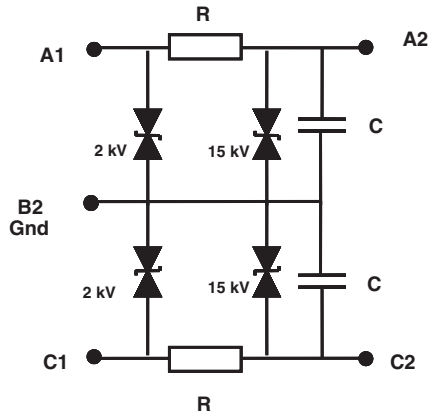


Flip-Chip
5 Bumps

Pin configuration (Bump side view)



Schematic



Order code

Part number	marking
EMIF2-AV01F3	HH

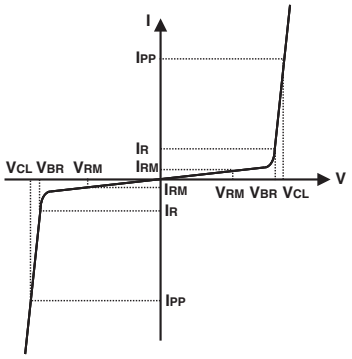
1 Electrical characteristics

Table 1. Absolute maximum ratings (T_{amb} = 25° C)

Symbol	Parameter	Value	Unit
V_{pp}	**Internal pins (A1, C1)** ESD discharge IEC 61000-4-2, air discharge ESD discharge IEC 61000-4-2, contact discharge **External pins (A2, C2)** ESD discharge IEC 61000-4-2, air discharge ESD discharge IEC 61000-4-2, contact discharge	 2 2 15 8	kV
T_j	Maximum junction temperature	125	° C
P_{TOT}	Total Power Dissipation	200	mW
T_{op}	Operating temperature range	-40 to +85	° C
T_{stg}	Storage temperature range	-55 to 150	° C

Table 2. Electrical characteristics (T_{amb} = 25° C)

Symbol	Parameters
V_{BR}	Breakdown voltage
I_{RM}	Leakage current @ V_{RM}
V_{RM}	Stand-off voltage
V_{CL}	Clamping voltage
R_d	Dynamic impedance
I_{PP}	Peak pulse current
$R_{I/O}$	Series resistance between input and output
C_{line}	Input capacitance per line



Symbol	Test conditions	Min	Typ	Max	Unit
V_{BR}	I_R = 1 mA	14		18	V
I_{RM}	V_{RM} = 3 V per line			0.5	µA
$R_{I/O}$		12	15	18	Ω
C_{line}	V_{line} = 0 V, V_{OSC} = 30 mV, F = 100 kHz	2.56	3.2	3.84	nF

Figure 1. S21 (dB) attenuation

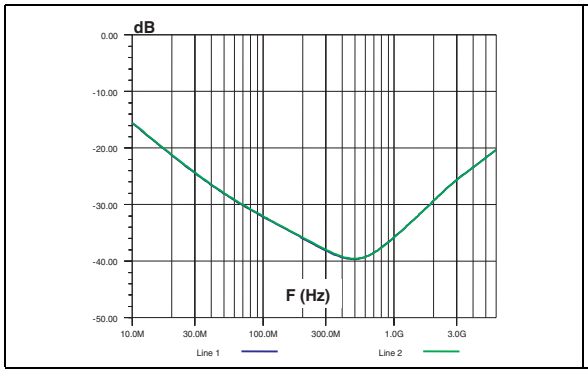


Figure 2. Analog crosstalk

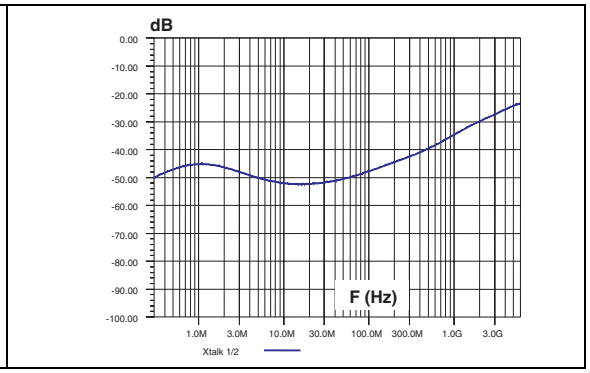


Figure 3. Digital crosstalk

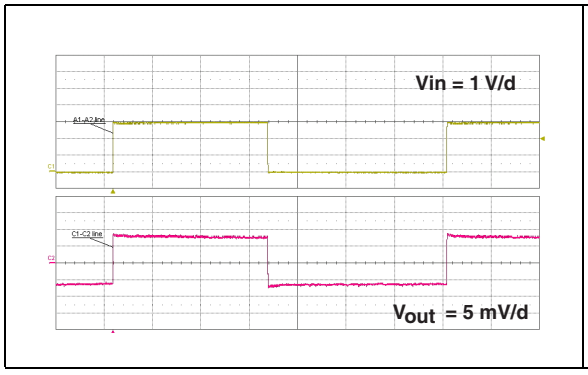


Figure 4. ESD response to IEC 61000-4-2 (+15 kV air discharge) on one input (V_{IN}) and one output (V_{OUT})

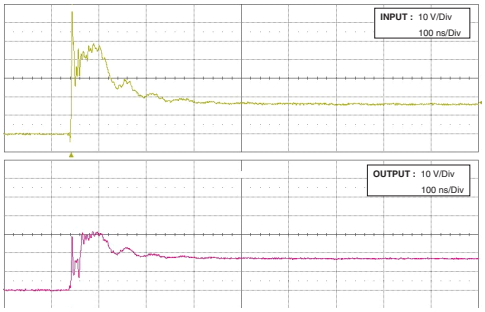


Figure 5. ESD response to IEC 61000-4-2 (-15 kV air discharge) on one input (V_{IN}) and one output (V_{OUT})

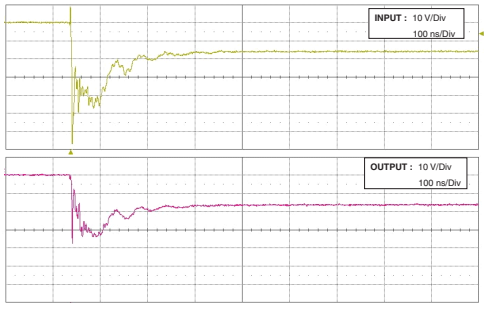
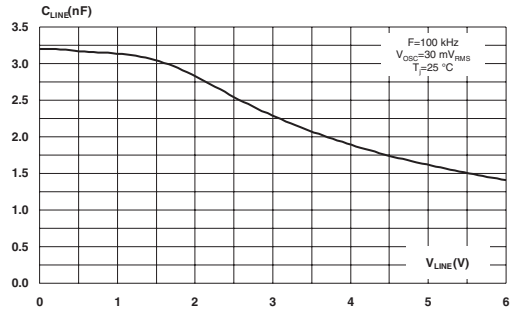


Figure 6. Line capacitance versus applied voltage



2 Ordering information scheme

EMIF yy - xx zz Fx

EMI Filter

Number of lines

Information
x = resistance value (Ohms)
z = capacitance value / 10 (pF)
or
2 letters = application
2 digits = version

Package
F = Flip-Chip
x = 3: Lead free, Pitch = 400 µm, Bump = 255 µm

3 Package information

Figure 7. Package dimensions

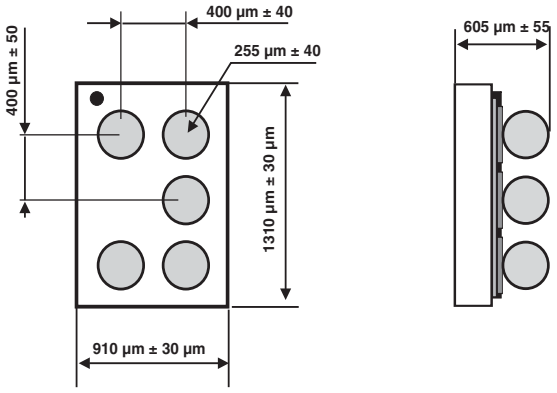


Figure 8. Footprint

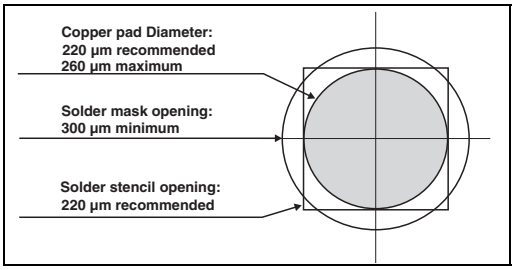


Figure 9. Marking

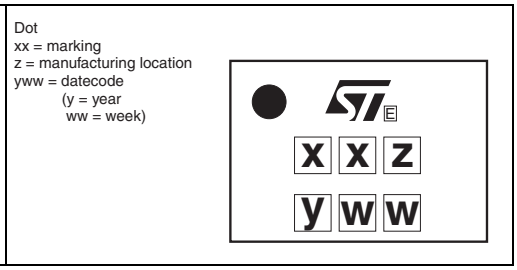
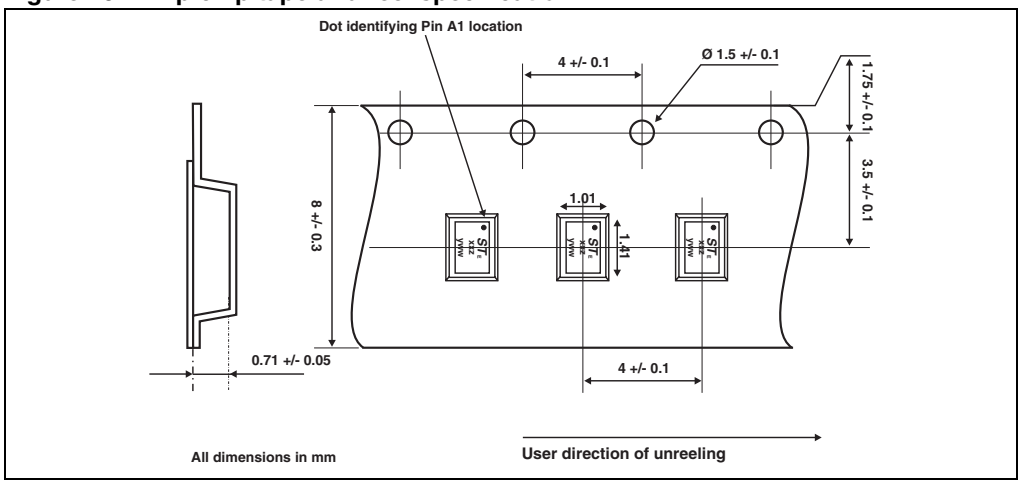


Figure 10. Flip-chip tape and reel specification



In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a lead-free second level interconnect. The category of second level interconnect is marked on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

Note: *Note: More information is available in the application note:*
AN2348:"Flip-chip: Package description and recommendations for use"
AN1751: “EMI filters: Recommendations and measurements”

4 Ordering information

Ordering code	Marking	Package	Weight	Base qty	Delivery mode
EIMF02-AV01F3	HH	Flip-chip	1.4 mg	5000	Tape and reel 7”

5 Revision history

Date	Revision	Changes
06-Oct-2006	1	Initial release
11-Oct-2006	2	Corrected test conditions for C_{line} in Table 2.

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