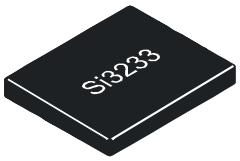
Si3233

ProSLIC® Programmable CMOS SLIC with Ringing/Battery Voltage Generation

Features

- Software Programmable SLIC with codec interface
- Software programmable internal balanced ringing up to 90 V_{PK} (5 REN up to 4 kft, 3 REN up to 8 kft)
- Integrated battery supply with dynamic voltage output
  - On-chip dc-dc converter continuously minimizes power in all operating modes
  - Entire solution can be powered from a single 3.3 V or 5 V supply
  - 3.3 V to 35 V dc input range
  - Dynamic 0 V to –94.5 V output
- Software programmable linefeed parameters:
  - Ringing frequency, amplitude, cadence, and waveshape
  - 2-wire ac impedance
  - constant current feed (20 to 41 mA)
  - Loop closure and ring trip thresholds and filtering
- Software programmable signal generation and audio processing:
  - Phase-continuous FSK (caller ID) generation
  - Dual audio tone generators
  - Smooth and abrupt polarity reversal
- Extensive test and diagnostic features
  - Realtime dc linefeed measurement
  - GR-909 line test capabilities
- SPI control interface
- Extensive programmable interrupts
- 100% software configurable global solution
- Lead-Free and RoHS-compliant

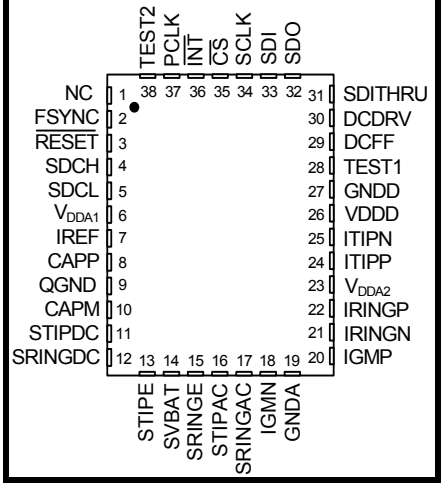


Ordering Information

See page 95.

Pin Assignments

QFN Package



Applications

- Interface to Broadcom devices
  - BCM11xx residential gateway
  - BCM3341 VOIP processor
  - BCM33xx cable modem
- Voice over IP
- Terminal adapters
- Fixed cellular terminal

Description

The Si3233 ProSLIC® is a low-voltage CMOS device that provides a multi-functional subscriber line interface ideal for customer premise equipment (CPE) applications. The ProSLIC integrates subscriber line interface circuit (SLIC) and battery generation functionality into a single CMOS integrated circuit. The integrated battery supply continuously adapts its output voltage to minimize power and enables the entire solution to be powered from a single 3.3 V (Si3233M only) or 5 V supply. The ProSLIC controls the phone line through Silicon Labs' Si3201 Linefeed IC or discrete circuitry. Si3233 features include software-configurable 5 REN internal ringing up to 90 V_{PK}, DTMF generation, and a comprehensive set of telephony signaling capabilities for operation with only one hardware solution. The ProSLIC is packaged in a 38-pin QFN and the Si3201 is packaged in a thermally-enhanced 16-pin SOIC.

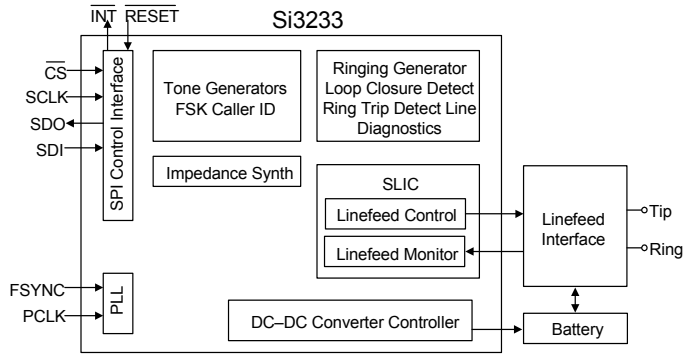
Patents pending

U.S. Patent #6,567,521

U.S. Patent #6,812,744

Other patents pending

Functional Block Diagram



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1. Electrical Specifications

Table 1. Absolute Maximum Ratings and Thermal Information[1]

Parameter	Symbol	Value	Unit
Si3233			
DC Supply Voltage	V_{DDD}, V_{DDA1}, V_{DDA2}	–0.5 to 6.0	V
Input Current, Digital Input Pins	I_{IN}	±10	mA
Digital Input Voltage	V_{IND}	–0.3 to (V_{DDD} + 0.3)	V
Operating Temperature Range[2]	T_A	–40 to 100	ºC
Storage Temperature Range	T_{STG}	–40 to 150	ºC
TSSOP-38 Thermal Resistance, Typical	θ_{JA}	70	ºC/W
QFN-38 Thermal Resistance, Typical	θ_{JA}	35	ºC/W
Continuous Power Dissipation[2]	P_D	0.7	W
Si3201			
DC Supply Voltage	V_{DD}	–0.5 to 6.0	V
Battery Supply Voltage	V_{BAT}	–104	V
Input Voltage: TIP, RING, SRINGE, STIPE pins	V_{INHV}	(V_{BAT} – 0.3) to (V_{DD} + 0.3)	V
Input Voltage: ITIPP, ITIPN, IRINGP, IRINGN pins	V_{IN}	–0.3 to (V_{DD} + 0.3)	V
Operating Temperature Range[2]	T_A	–40 to 100	ºC
Storage Temperature Range	T_{STG}	–40 to 150	ºC
SOIC-16 Thermal Resistance, Typical[3]	θ_{JA}	55	ºC/W
Continuous Power Dissipation[2]	P_D	1.0	W

Notes:
1. Permanent device damage may occur if the above Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions as specified in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. Operation above 125 °C junction temperature may degrade device reliability.
3. Thermal resistance assumes a multi-layer PCB with the exposed pad soldered to a topside PCB pad.

Table 2. Recommended Operating Conditions

Parameter	Symbol	Test Condition	Min*	Typ	Max*	Unit
Ambient Temperature	T_A	F-grade	0	25	70	°C
Ambient Temperature	T_A	G-grade	–40	25	85	°C
Si3233 Supply Voltage	V_{DDD},V_{DDA1} ,V_{DDA2}		3.13	3.3/5.0	5.25	V
Si3201 Supply Voltage	V_{DD}		3.13	3.3/5.0	5.25	V
Si3201 Battery Voltage	V_{BAT}	$V_{BATH} = V_{BAT}$	–96	—	–10	V

***Note:** All minimum and maximum specifications are guaranteed and apply across the recommended operating conditions. Typical values apply at nominal supply voltages and an operating temperature of 25 °C unless otherwise stated. Product specifications are only guaranteed when the typical application circuit (including component tolerances) is used.

Table 3. AC Characteristics

(V_{DDA}, V_{DDD} = 3.13 to 5.25 V, T_A = 0 to 70°C for F-Grade, –40 to 85°C for G-Grade)

Parameter	Test Condition	Min	Typ	Max	Unit
TX/RX Performance					
Overload Level	THD = 1.5%	2.5	—	—	V_{PK}
Audio Tone Generator Signal-to-Distortion Ratio[1]	0 dBm0, Active off-hook, and OHT, any Zac	45	—	—	dB
Intermodulation Distortion		—	—	–45	dB
2-Wire Return Loss	200 Hz to 3.4 kHz	30	35	—	dB
Noise Performance					
Idle Channel Noise[2]	C-Message Weighted	—	—	15	dBrnC
	Psophometric Weighted	—	—	–75	dBmP
	3 kHz flat	—	—	18	dBrn
PSRR from VDDA	RX and TX, DC to 3.4 kHz	40	—	—	dB
PSRR from VDDD	RX and TX, DC to 3.4 kHz	40	—	—	dB
PSRR from VBAT	RX and TX, DC to 3.4 kHz	40	—	—	dB
Longitudinal Performance					
Longitudinal to Metallic Balance	200 Hz to 3.4 kHz, $\beta_{Q1,Q2} \geq$ 150, 1% mismatch	56	60	—	dB
	$\beta_{Q1,Q2}$ = 60 to 240[3]	43	60	—	dB
	$\beta_{Q1,Q2}$ = 300 to 800[3]	53	60	—	dB
	Using Si3201	53	60	—	dB
Metallic to Longitudinal Balance	200 Hz to 3.4 kHz	40	—	—	dB

Notes:
1. Analog signal measured as VTIP – VRING. Assumes ideal line impedance matching.
2. The level of any unwanted tones within the bandwidth of 0 to 4 kHz does not exceed –55 dBm.
3. Assumes normal distribution of betas.

Table 3. AC Characteristics (Continued)

(V_{DDA}, V_{DDD} = 3.13 to 5.25 V, T_A = 0 to 70°C for F-Grade, –40 to 85°C for G-Grade)

Parameter	Test Condition	Min	Typ	Max	Unit
Longitudinal Impedance	200 Hz to 3.4 kHz at TIP or RING Register selectable ETBO/ETBA				
	00	—	33	—	Ω
	01	—	17	—	Ω
	10	—	17	—	Ω
Longitudinal Current per Pin	Active off-hook 200 Hz to 3.4 kHz Register selectable ETBO/ETBA				
	00	—	4	—	mA
	01	—	8	—	mA
	10	—	8	—	mA

Notes:
1. Analog signal measured as VTIP – VRING. Assumes ideal line impedance matching.
2. The level of any unwanted tones within the bandwidth of 0 to 4 kHz does not exceed –55 dBm.
3. Assumes normal distribution of betas.

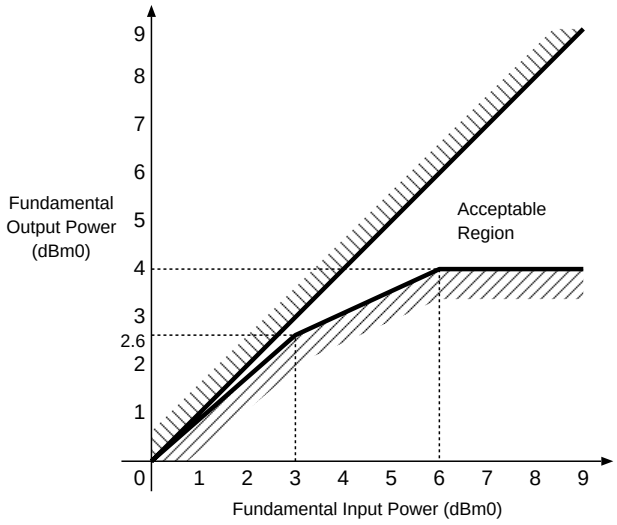


Figure 1. Overload Compression Performance

Table 4. Linefeed Characteristics

(V_{DDA}, V_{DDD} = 3.13 to 5.25 V, T_A = 0 to 70°C for F-Grade, –40 to 85°C for G-Grade)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Loop Resistance Range	R_{LOOP}	See note.*	0	—	160	Ω
DC Loop Current Accuracy		I_{LIM} = 29 mA, ETBA = 4 mA	–10	—	10	%
DC Open Circuit Voltage Accuracy		Active Mode; V_{OC} = 48 V, $V_{TIP} – V_{RING}$	–4	—	4	V
DC Differential Output Resistance	R_{DO}	$I_{LOOP} < I_{LIM}$	—	160	—	Ω
DC Open Circuit Voltage—Ground Start	V_{OCTO}	$I_{RING}<I_{LIM}$; V_{RING} wrt ground V_{OC} = 48 V	–4	—	4	V
DC Output Resistance—Ground Start	R_{ROTO}	$I_{RING}<I_{LIM}$; RING to ground	—	160	—	Ω
DC Output Resistance—Ground Start	R_{TOTO}	TIP to ground	150	—	—	kΩ
Loop Closure/Ring Ground Detect Threshold Accuracy		I_{THR} = 11.43 mA	–20	—	20	%
Ring Trip Threshold Accuracy		I_{THR} = 40.64 mA	–10	—	10	%
Ring Trip Response Time		User Programmable Register 70 and Indirect Register 23	—	—	—	
Ring Amplitude	V_{TR}	5 REN load; sine wave; R_{LOOP} = 160 Ω, V_{BAT} = –75 V	44	—	—	V_{rms}
Ring DC Offset	R_{OS}	Programmable in Indirect Register 6	0	—	—	V
Trapezoidal Ring Crest Factor Accuracy		Crest factor = 1.3	–.05	—	.05	
Sinusoidal Ring Crest Factor	R_{CF}		1.35	—	1.45	
Ringing Frequency Accuracy		f = 20 Hz	–1	—	1	%
Ringing Cadence Accuracy		Accuracy of ON/OFF Times	–50	—	50	ms
Calibration Time		↑CAL to ↓CAL Bit	—	—	600	ms
Power Alarm Threshold Accuracy		At Power Threshold = 300 mW	–25	—	25	%

***Note:** DC resistance round trip; 160 Ω corresponds to 2 kft 26 gauge AWG.

Table 5. Monitor ADC Characteristics

(V_{DDA}, V_{DDD} = 3.13 to 5.25 V, T_A = 0 to 70°C for F-Grade, –40 to 85°C for G-Grade)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Differential Nonlinearity (6-bit resolution)	DNLE		–1/2	—	1/2	LSB
Integral Nonlinearity (6-bit resolution)	INLE		–1	—	1	LSB
Gain Error (voltage)			—	—	10	%
Gain Error (current)			—	—	20	%

Table 6. Si3233 DC Characteristics, V_{DDA} = V_{DDD} = 5.0 V

(V_{DDA},V_{DDD} = 4.75 V to 5.25 V, T_A = 0 to 70°C for F-Grade, –40 to 85°C for G-Grade)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
High Level Input Voltage	V_{IH}		0.7 x V_{DDD}	—	—	V
Low Level Input Voltage	V_{IL}		—	—	0.3 x V_{DDD}	V
High Level Output Voltage	V_{OH}	SDITHRU: I_O = –4 mA SDO: I_O = –8 mA	V_{DDD} – 0.6	—	—	V
Low Level Output Voltage	V_{OL}	SDITHRU: I_O = 4 mA SDO,$\overline{INT}$: I_O = 8 mA	—	—	0.4	V
Input Leakage Current	I_L		–10	—	10	µA

Table 7. Si3233 DC Characteristics, V_{DDA} = V_{DDD} = 3.3 V

(V_{DDA},V_{DDD} = 3.13 V to 3.47 V, T_A = 0 to 70°C for F-Grade, –40 to 85°C for G-Grade)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
High Level Input Voltage	V_{IH}		0.7 x V_{DDD}	—	—	V
Low Level Input Voltage	V_{IL}		—	—	0.3 x V_{DD} D	V
High Level Output Voltage	V_{OH}	SDITHRU: I_O = –2 mA SDO: I_O = –4 mA	V_{DDD} – 0.6	—	—	V
Low Level Output Voltage	V_{OL}	SDITHRU: I_O = 2 mA SDO,$\overline{INT}$: I_O = 4 mA	—	—	0.4	V
Input Leakage Current	I_L		–10	—	10	µA

Table 8. Power Supply Characteristics

(V_{DDA},V_{DDD} = 3.13 V to 5.25 V, T_A = 0 to 70°C for F-Grade, –40 to 85°C for G-Grade)

Parameter	Symbol	Test Condition	Typ[1]	Typ[2]	Max	Unit
Power Supply Current, Analog and Digital	$I_A + I_D$	Sleep ($\overline{RESET}$ = 0)	0.1	0.13	0.2	mA
		Open	33	42.8	49	mA
		Active on-hook ETBO = 4 mA, codec and Gm amplifier powered down	37	53	68	mA
		Active OHT ETBO = 4 mA	57	72	83	mA
		Active off-hook ETBA = 4 mA, I_{LIM} = 20 mA	73	88	99	mA
		Ground-start	36	47	55	mA
		Ringing Sinewave, REN = 1, V_{PK} = 56 V	45	55	65	mA
V_{DD} Supply Current (Si3201)	I_{VDD}	Sleep mode, RESET = 0	110	110	—	µA
		Open (high impedance)	110	110	—	µA
		Active on-hook standby	110	110	—	µA
		Forward/reverse active off-hook, ETBA = 4 mA, V_{BAT} = –24 V	110	110	—	µA
		Forward/reverse OHT, ETBO = 4 mA, V_{BAT} = –70 V	110	110	—	µA
V_{BAT} Supply Current[3]	I_{BAT}	Sleep ($\overline{RESET}$ = 0)	0	0	—	mA
		Open (DCOF = 1)	0	0	—	mA
		Active on-hook V_{OC} = 48 V	—	3	—	mA
		Active OHT ETBO = 4 mA	—	11	—	mA
		Active off-hook ETBA = 4 mA, I_{LIM} = 20 mA	—	30	—	mA
		Ground-start	—	2	—	mA
		Ringing V_{PK_RING} = 56 V_{PK}, sinewave ringing, REN = 1	—	5.5	—	mA

Notes:

1. V_{DDD}, V_{DDA} = 3.3 V.
2. V_{DDD}, V_{DDA} = 5.25 V.
3. I_{BAT} = current from V_{BAT} (the large negative supply). For a switched-mode power supply regulator efficiency of 71%, the user can calculate the regulator current consumption as I_{BAT} x V_{BAT}/(0.71 x V_{DC}).

Table 9. Switching Characteristics—General Inputs

V_{DDA} = V_{DDA} = 3.13 to 5.25 V, T_A = 0 to 70°C for F-Grade, –40 to 85°C for G-Grade, C_L = 20 pF)

Parameter	Symbol	Min	Typ	Max	Unit
Rise Time, $\overline{\text{RESET}}$	t_r	—	—	20	ns
$\overline{\text{RESET}}$ Pulse Width	t_{rl}	100	—	—	ns
Note: All timing (except Rise and Fall time) is referenced to the 50% level of the waveform. Input test levels are V_{IH} = V_D – 0.4 V, V_{IL} = 0.4 V. Rise and Fall times are referenced to the 20% and 80% levels of the waveform.					

Table 10. Switching Characteristics—SPI

V_{DDA} = V_{DDA} = 3.13 to 5.25 V, T_A = 0 to 70°C for F-Grade, –40 to 85°C for G-Grade, C_L = 20 pF

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Cycle Time SCLK	t_c		0.062	—	—	µs
Rise Time, SCLK	t_r		—	—	25	ns
Fall Time, SCLK	t_f		—	—	25	ns
Delay Time, SCLK Fall to SDO Active	t_{d1}		—	—	20	ns
Delay Time, SCLK Fall to SDO Transition	t_{d2}		—	—	20	ns
Delay Time, $\overline{\text{CS}}$ Rise to SDO Tri-state	t_{d3}		—	—	20	ns
Setup Time, $\overline{\text{CS}}$ to SCLK Fall	t_{su1}		25	—	—	ns
Hold Time, $\overline{\text{CS}}$ to SCLK Rise	t_{h1}		20	—	—	ns
Setup Time, SDI to SCLK Rise	t_{su2}		25	—	—	ns
Hold Time, SDI to SCLK Rise	t_{h2}		20	—	—	ns
Delay Time between Chip Selects (Continuous SCLK)	t_{cs}		440	—	—	ns
Delay Time between Chip Selects (Non-continuous SCLK)	t_{cs}		220	—	—	ns
SDI to SDITHRU Propagation Delay	t_{d4}		—	4	10	ns
Note: All timing is referenced to the 50% level of the waveform. Input test levels are V_{IH} = V_{DDD} –0.4 V, V_{IL} = 0.4 V						

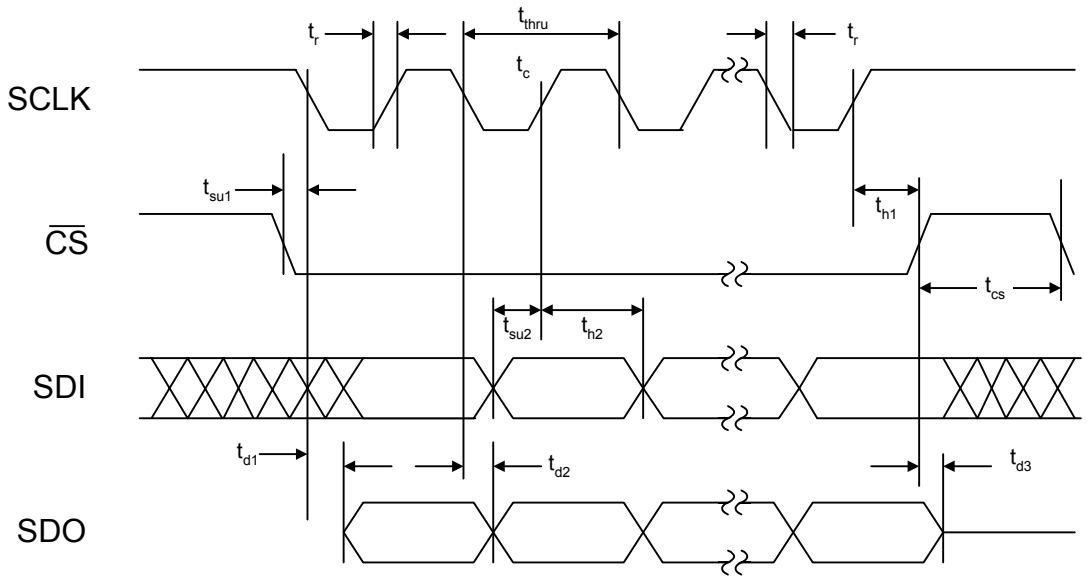


Figure 2. SPI Timing Diagram

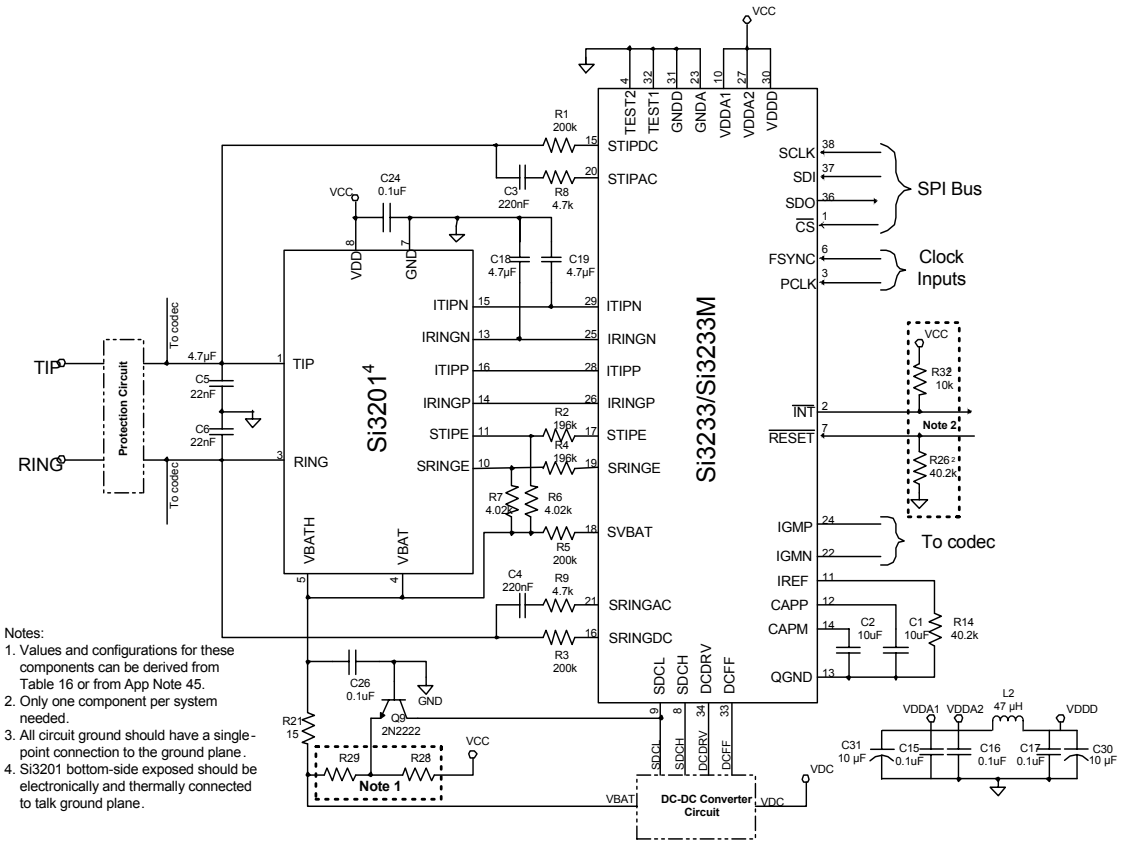
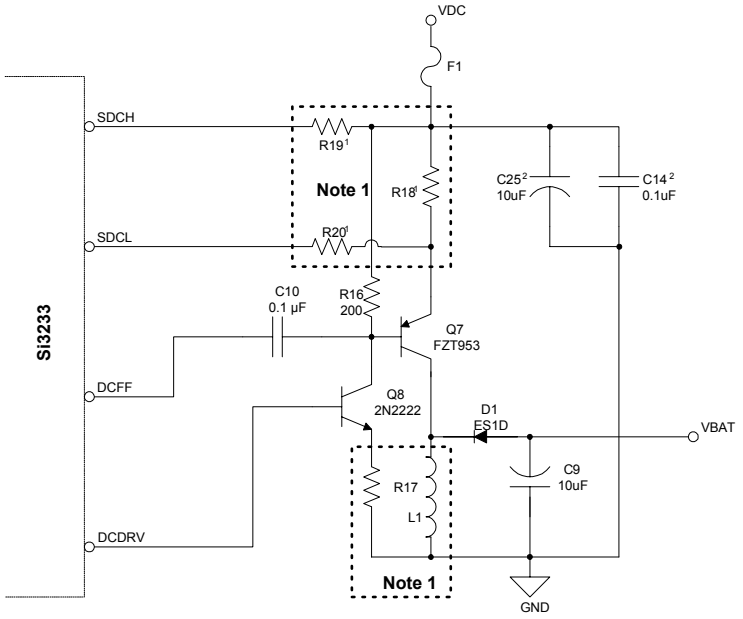


Figure 3. Si3233/Si3233M Application Circuit Using Si3201

Table 11. Si3233/Si3233M + Si3201 External Component Values

Component(s)	Value	Supplier
C1,C2	10 µF, 6 V Ceramic or 16 V Low Leakage Electrolytic, ±20%	Murata, Nichicon URL1C100MD
C3,C4	220 nF, 100 V, X7R, ±20%	Murata, Johanson, Novacap, Venkel
C5,C6	22 nF, 100 V, X7R, ±20%	Murata, Johanson, Novacap, Venkel
C15,C16,C17,C24	0.1 µF, 6 V, Y5V, ±20%	Murata, Johanson, Novacap, Venkel
C18,C19	4.7 µF, Cer. 6 V, X7R, ±20%	Murata, Johanson, Novacap, Venkel
C26	0.1 µF, 100 V, X7R, ±20%	Murata, Johanson, Novacap, Venkel
C30, C31	10 µF, 6 V, Electrolytic, ±20%	Panasonic
L2	47 µH, 150 mA	Coilcraft
R1,R3,R5	200 kΩ, 1/10 W, ±1%	
R2,R4	196 kΩ, 1/10 W, ±1%	
R6,R7	4.02 kΩ, 1/10 W, ±1%	
R8,R9	4.7 kΩ, 1/10 W, ±1%	
R14,R26*	40.2 kΩ, 1/10 W, ±1%	
R15	243 Ω, 1/10 W, ±1%	
R21	15 Ω, 1/4 W, ±5%	
R28,R29	1/10 W, 1% (See AN45 or Table 16 for value selection)	
R32*	10 kΩ, 1/10 W, ±5%	
Q9	60 V, General Purpose Switching NPN	ON Semi MMBT2222ALT1; Central Semi CMPT2222A; Zetex FMMT2222
***Note:** Only one component per system needed.		

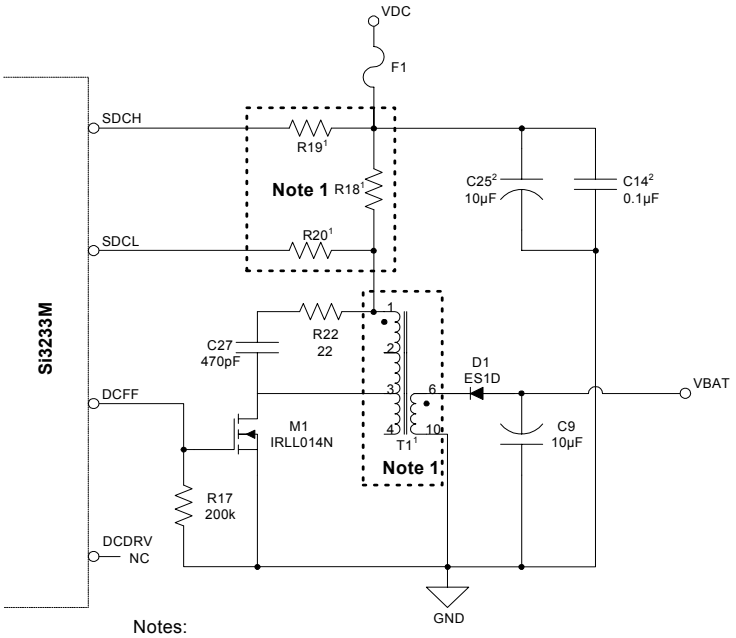


Notes:
1. Values and configurations for these components can be derived from Table 17 or from App Note 45.
2. Voltage rating for C14 and C25 must be greater than VDC.

Figure 4. Si3233 DC-DC Converter Circuit

Table 12. Si3233 DC-DC Converter Component Values

Component(s)	Value	Supplier
C9	10 µF, 100 V, Electrolytic, ±20%, low ESR (tan(δ) ≤ 0.08)	Panasonic
C10	0.1 µF, 50 V, X7R, ±20%	Murata, Johanson, Novacap, Venkel
C14*	0.1 µF, X7R, ±20%, low ESR (tan(δ) ≤ 0.08)	Murata, Johanson, Novacap, Venkel
C25*	10 µF, Electrolytic, ±20%	Panasonic
R16	200 Ω, 1/10 W, ±5%	
R17	1/10 W, ±5% (See AN45 or Table 17 for value selection)	
R18	1/4 W, ±5% (See AN45 or Table 17 for value selection)	
R19,R20	1/10 W, ±1% (See AN45 or Table 17 for value selection)	
F1	Fuse	Belfuse SSQ Series
D1	Ultra Fast Recovery 200 V, 1A Rectifier	General Semi ES1D; Central Semi CMR1U-02
L1	1A, Shielded Inductor (See AN45 or Table 17 for value selection)	API Delevan SPD127 series, Sumida CDRH127 series, Datatronics DR340-1 series, Coilcraft DS5022
Q7	120 V, High Current Switching PNP	Zetex FZT953, FZT955, ZTX953, ZTX955
Q8	60 V, General Purpose Switching NPN	ON Semi MMBT2222ALT1, MPS2222A; Central Semi CMPT2222A; Zetex FMMT2222
***Note:** Voltage rating of this device must be greater than V_{DC}.		



Notes:
1. Values and configurations for these components can be derived from Table 18 or from App Note 45.
2. Voltage rating for C14 and C25 must be greater than VDC.

Figure 5. Si3233M MOSFET/Transformer DC-DC Converter Circuit

Table 13. Si3233M MOSFET/Transformer DC-DC Converter Component Values

Component(s)	Value	Supplier
C9	10 µF, 100 V, Electrolytic, ±20%, low ESR (tan(δ) ≤ 0.08)	Panasonic
C14*	0.1 µF, X7R, ±20%	Murata, Johanson, Novacap, Venkel
C25*	10 µF, Electrolytic, ±20%, low ESR (tan(δ) ≤ 0.08)	Panasonic
C27	470 pF, 100 V, X7R, ±20%	Murata, Johanson, Novacap, Venkel
R17	200 kΩ, 1/10 W, ±5%	
R18	1/4 W, ±5% (See AN45 or Table 21 for value selection)	
R19,R20	1/10 W, ±1% (See AN45 or Table 21 for value selection)	
R22	22 Ω, 1/10 W, ±5%	
F1	Fuse	Belfuse SSQ Series
D1	Ultra Fast Recovery 200 V, 1A Rectifier	General Semi ES1D; Central Semi CMR1U-02
T1	Power Transformer	Coiltronic CTX01-15275; Datatronics SM76315; Midcom 31353R-02
M1	100 V, Logic Level Input MOSFET	Intl Rect. IRLL014N; Intersil HUF76609D3S; ST Micro STD5NE10L, STN2NE10L
***Note:** Voltage rating of this device must be greater than V_{DC}.		

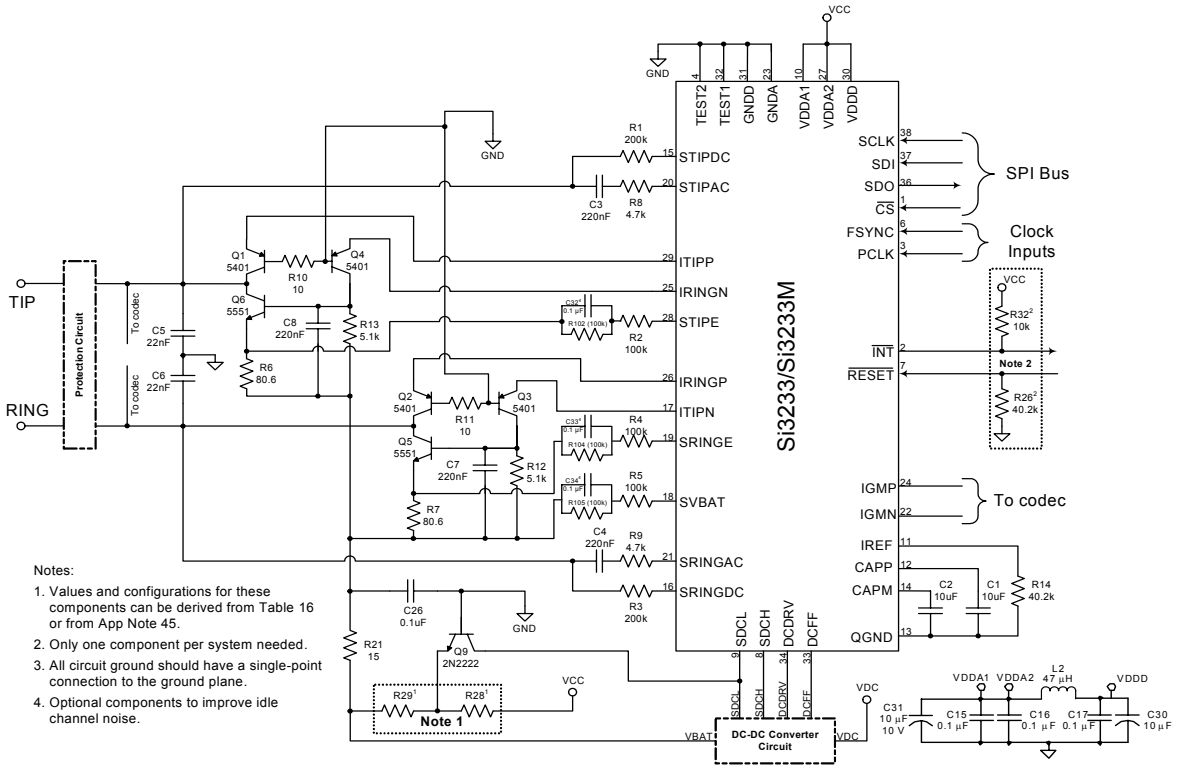


Figure 6. Si3233/Si3233M Typical Application Circuit Using Discrete Components

Table 14. Si3233/Si3233M External Component Values—Discrete Solution

Component(s)	Value	Supplier/Part Number
C1,C2	10 µF, 6 V Ceramic or 16 V Low Leakage Electrolytic, ±20%	Murata, Panasonic, Nichicon URL1C100MD
C3,C4	220 nF, 100 V, X7R, ±20%	Murata, Johanson, Novacap, Venkel
C5,C6	22 nF, 100 V, X7R, ±20%	Murata, Johanson, Novacap, Venkel
C7,C8	220 nF, 50 V, X7R, ±20%	Murata, Johanson, Novacap, Venkel
C15,C16,C17	0.1 µF, 6 V, Y5V, ±20%	Murata, Johanson, Novacap, Venkel
C26	0.1 µF, 100 V, X7R, ±20%	Murata, Johanson, Novacap, Venkel
C30,C31	10 µF, 16 V, Electrolytic, ±20%	Panasonic
C32, C33, C34	0.1 µF, 50 V, ±20%	Venkel
L2	47 µH, 150 mA	Coilcraft
Q1,Q2,Q3,Q4	120 V, PNP, BJT	Central Semi CMPT5401; ON Semi MMBT5401LT1, 2N5401; Zetex FMMT5401
Q5,Q6	120 V, NPN, BJT	Central Semi CZT5551, ON Semi 2N5551
Q9	NPN General Purpose BJT	ON Semi MMBT2222ALT1, MPS2222A; Central Semi CMPT2222A; Zetex FMMT2222
R1,R3	200 kΩ, 1/10 W, ±1%	
R2, R4, R5, R102, R104, R105	100 kΩ, 1/10 W, ±1%	
R6,R7	80.6 Ω, 1/4 W, ±1%	
R8,R9	4.7 kΩ, 1/10 W, ±1%	
R10,R11	10 Ω, 1/10 W, ±5%	
R12,R13	5.1 kΩ, 1/10 W, ±5%	
R14,R26*	40.2 kΩ, 1/10 W, ±1%	

Table 14. Si3233/Si3233M External Component Values—Discrete Solution (Continued)

R15	243 Ω, 1/10 W, ±1%	
R21	15 Ω, 1/4 W, ±1%	
R28,R29	1/10 W, ±1% (See AN45 or Table 16 for value selection)	
R32*	10 kΩ, 1/10 W, ±5%	
***Note:** Only one component per system needed.		

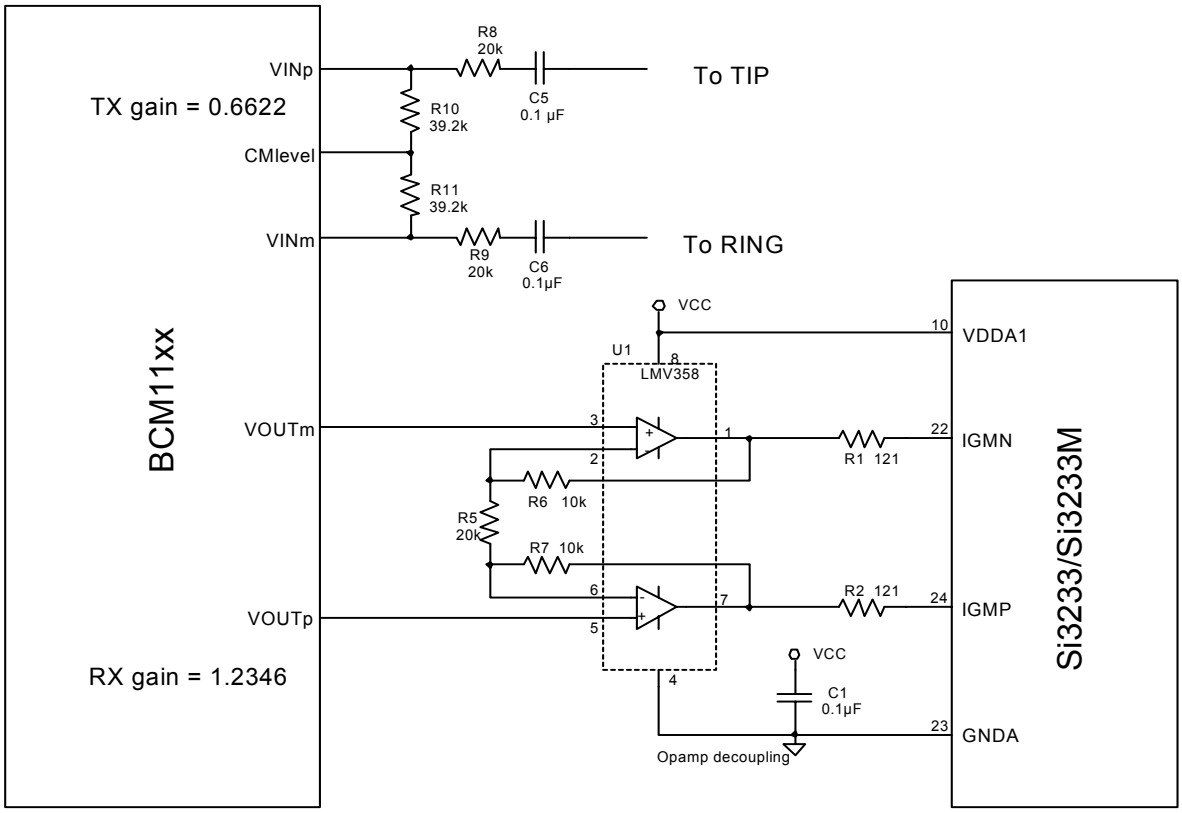


Figure 7. Interface to Broadcom BCM11xx

Table 15. External Component Values—BCM11xx Interface

Component(s)	Value	Comments/Part Number
C1	0.1 µF, 6 V, Y5V, ±20%	Murata, Johnson, Novacap, Venkel
C5, C6	0.1 µF, 100 V, X7R, ±20%	Murata, Johnson, Novacap, Venkel
R1, R2	121 Ω, 1/10 W, ±1%	
R5, R8, R9	20 kΩ, 1/10 W, ±1%	
R6, R7	10 kΩ, 1/10 W, ±1%	
R10, R11	39.2 kΩ, 1/10 W, ±1%	
U1	Dual Rail-to-Rail Op Amp	Texas Instruments LMV358, Micrel MIC7122

Table 16. Component Value Selection for Si3233

Component	Value	Comments
R28	1/10 W, 1% resistor For V_{DD} = 3.3 V: 26.1 kΩ For V_{DD} = 5.0 V: 37.4 kΩ	R28 = (V_{DD} + V_{BE})/148 µA where V_{BE} is the nominal VBE for Q9
R29	1/10 W, 1% resistor For V_{CLAMP} = 80 V: 541 kΩ For V_{CLAMP} = 85 V: 574 kΩ For V_{CLAMP} = 100 V: 676 kΩ	R29 = V_{CLAMP}/148 µA where V_{CLAMP} is the clamping voltage for V_{BAT}

Table 17. Component Value Selection Examples for BJT/Inductor DC-DC Converter

VDC	Maximum Ringing Load/Loop Resistance	L1	R17	R18	R19, R20
5 V	3 REN/117 Ω	67 µH	150 Ω	0.15 Ω	16.5 kΩ
12 V	5 REN/117 Ω	150 µH	162 Ω	0.56 Ω	56.2kΩ
24 V	5 REN/117 Ω	220 µH	175 Ω	2.0 Ω	121 kΩ
Note: There are other system and software conditions that influence component value selection. Please refer to “AN45: “Design Guide for the Si3210/15/16 DC-DC Converter” for detailed guidance.					

Table 18. Component Value Selection Examples for Si3233M MOSFET/Transformer DC-DC Converter

VDC	Maximum Ringing Load/Loop Resistance	Transformer Ratio	R18	R19, R20
3.3 V	3 REN/117 Ω	1:2	0.06 Ω	7.15 Ω
5.0 V	5 REN/117 Ω	1:2	0.10 Ω	16.5 Ω
12 V	5 REN/117 Ω	1:3	0.6 Ω	56.2 Ω
24	5 REN/117 Ω	1:4	2.1 Ω	121 Ω
Note: There are other system and software conditions that influence component value selection. Please refer to “AN45: “Design Guide for the Si3210/15/16 DC-DC Converter” for detailed guidance.				

2. Functional Description

The Si3233 ProSLIC® is a feature-rich low-voltage CMOS device that provides all the SLIC, DTMF, and signal generation functions needed for a complete analog telephone interface when connected to an external codec. The ProSLIC performs all battery, overvoltage, ringing, supervision, and test functions. Unlike most monolithic SLICs, the Si3233 does not require externally supplied high-voltage battery supplies. It generates all necessary battery voltages from a positive dc supply using its own dc-dc converter controller. Two fully programmable tone generators can produce DTMF tones, phase continuous FSK (caller ID) signaling, and call progress tones. The Si3201 linefeed interface IC performs all high voltage functions. The Si3201 can also be replaced with low-cost discrete circuits as shown in the typical application in Figure 6.

The Si3233 is designed to be used with Broadcom devices such as BCM1101, BCM3351/52, and BCM6352. Special directions are required to interface the Si3233 to other devices. Please contact Silicon Laboratories for guidance.

The linefeed provides programmable on-hook voltage, programmable off-hook loop current, reverse battery operation, loop or ground start operation, and on-hook transmission ringing voltage. Loop current and voltage are continuously monitored using an integrated A/D converter. Balanced 5 REN ringing with or without a programmable dc offset is supported. Programmable offset, frequency, waveshape, and cadence allow the Si3233 to ring the widest variety of terminal devices and to reduce external controller requirements.

2.1. Si3230 to Si3233 Differences

The hardware and software differences between the Si3230 and the Si3233 are highlighted below for customers migrating designs from the Si3230 to the Si3233.

2.1.1. Hardware Changes

- The Si3233 adds China and Japan impedances. See "2.6. Two-Wire Impedance Matching" on page 34.
- Pulse metering and DTMF detection are removed from the Si3233.
- External resistors R8 and R9 are changed from 470 Ω to 4.7 kΩ. See the typical application circuits in Figure 3 on page 12 and Figure 6 on page 15.
- The Si3233 adds PLL free-run mode. PLL free-run mode is described in Section "2.8. PLL Free-run Operation" on page 34.

2.1.2. Software Changes

- The sample rate for the two-tone oscillators has changed from 8 kHz to 16 kHz, therefore, the audio tone coefficient equation has changed. See "2.4.2. Oscillator Frequency and Amplitude" on page 27 for a complete description.
- The Si3233 provides an automatic calibration routine for gain mismatch. Manual calibration is not required. Refer to "AN35: Si321x User's Quick Reference Guide".
- The Indirect Registers have been re-mapped. When porting code from the Si3230 to the Si3233, the indirect register access function needs to be modified. See"4. Indirect Registers" on page 85.

2.2. Linefeed Interface

The ProSLIC's linefeed interface offers a rich set of features and programmable flexibility to meet the broadest application requirements. The dc linefeed characteristics are software programmable; key current, voltage, and power measurements are acquired in realtime and provided in software registers.

2.2.1. DC Feed Characteristics

The ProSLIC has programmable constant voltage and constant current zones as depicted in Figure 8. Open circuit TIP-to-RING voltage (V_{OC}) defines the constant voltage zone and is programmable from 0 V to 94.5 V in 1.5 V steps. The loop current limit (I_{LIM}) defines the constant current zone and is programmable from 20 mA to 41 mA in 3 mA steps. The ProSLIC has an inherent dc output resistance (R_O) of 160 Ω.

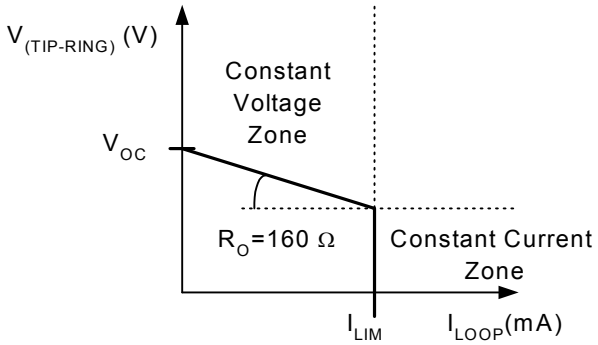


Figure 8. Simplified DC Current/Voltage Linefeed Characteristic

The TIP-to-RING voltage (V_{OC}) is offset from ground by a programmable voltage (V_{CM}) to provide voltage headroom to the positive-most terminal (TIP in forward polarity states and RING in reverse polarity states) for carrying audio signals. Table 19 summarizes the parameters to be initialized before entering an active state.

Table 19. Programmable Ranges of DC Linefeed Characteristics

Parameter	Programmable Range	Default Value	Register Bits	Location*
I_{LIM}	20 to 41 mA	20 mA	ILIM[2:0]	Direct Register 71
V_{OC}	0 to 94.5 V	48 V	VOC[5:0]	Direct Register 72
V_{CM}	0 to 94.5 V	3 V	VCM[5:0]	Direct Register 73

***Note:** The ProSLIC uses registers that are both directly and indirectly mapped. A “direct” register is one that is mapped directly.

2.2.2. Linefeed Architecture

The Si3233 uses either the Si3201 linefeed interface IC or a low-cost external circuit to generate the high voltages required for subscriber line interfaces.

The ProSLIC uses both voltage and current sensing to control TIP and RING. DC and AC line voltages on TIP and RING are measured through sense resistors R1/R3 and R8/R9, respectively.

The ProSLIC measures voltage at various nodes in order to monitor the linefeed current. The sense circuitry is calibrated on-chip to guarantee measurement accuracy with standard external component tolerances. See "2.2.9. Linefeed Calibration" on page 23 for details.

2.2.3. Linefeed Operation States

The ProSLIC linefeed has eight states of operation as shown in Table 20. The state of operation is controlled using the Linefeed Control register (direct Register 64).

The open state turns off all currents into the external bipolar transistors and can be used in the presence of fault conditions on the line and to generate Open Switch Intervals (OSIs). TIP and RING are effectively tri-stated with a dc output impedance of about 150 kΩ. The ProSLIC can also automatically enter the open state if it detects excessive power being consumed in the external bipolar transistors. See "2.2.5. Power Monitoring and Line Fault Detection" on page 21 for more details.

In the forward active and reverse active states, linefeed circuitry is on and the audio signal paths are powered down during an on-hook loop condition.

In the forward and reverse on-hook transmission states audio signal paths are powered up to provide data transmission during an on-hook loop condition.

The TIP Open state turns off all control currents to the line driver devices connected to TIP and provides an active linefeed on RING for ground start operation.

The RING Open state provides similar operation with the RING drivers off and TIP active.

The ringing state drives programmable ringing waveforms onto the line.

2.2.4. Loop Voltage and Current Monitoring

The ProSLIC continuously monitors the TIP and RING voltages and external BJT currents. These values are available in registers 78–89. Table 21 on page 20 lists the values that are measured and their associated registers. An internal A/D converter samples the measured voltages and currents from the analog sense circuitry and translates them into the digital domain. The A/D updates the samples at an 800 Hz rate. Two derived values are also reported—loop voltage and loop current. The loop voltage, $V_{TIP} – V_{RING}$, is reported as a 1-bit sign, 6-bit magnitude format. For ground start operation the reported value is the RING voltage. The loop current, $(I_{Q1} – I_{Q2} + I_{Q5} – I_{Q6})/2$, is reported in a 1-bit sign, 6-bit magnitude format. In RING open and TIP open states the loop current is reported as $(I_{Q1} – I_{Q2}) + (I_{Q5} – I_{Q6})$.

Table 20. ProSLIC Linefeed Operations

LF[2:0]*	Linefeed State	Description
000	Open	TIP and RING tri-stated.
001	Forward Active	$V_{TIP} > V_{RING}$.
010	Forward On-Hook Transmission	$V_{TIP} > V_{RING}$; audio signal paths powered on.
011	TIP Open	TIP tri-stated, RING active; used for ground start.
100	Ringing	Ringing waveform applied to TIP and RING.
101	Reverse Active	$V_{RING} > V_{TIP}$.
110	Reverse On-Hook Transmission	$V_{RING} > V_{TIP}$; audio signal paths powered on.
111	Ring Open	RING tri-stated, TIP active.
Note: The Linefeed register (LF) is located in direct Register 64.		

Table 21. Measured Realtime Linefeed Interface Characteristics

Parameter	Measurement Range	Resolution	Register Bits	Location*
Loop Voltage Sense ($V_{TIP} – V_{RING}$)	–94.5 to +94.5 V	1.5 V	LVSP, LVS[6:0]	Direct Register 78
Loop Current Sense	–78.75 to +78.5 mA	1.25 mA	LCSP, LCS[5:0]	Direct Register 79
TIP Voltage Sense	0 to –95.88 V	0.376 V	VTIP[7:0]	Direct Register 80
RING Voltage Sense	0 to –95.88 V	0.376 V	VRING[7:0]	Direct Register 81
Battery Voltage Sense 1 (V_{BAT})	0 to –95.88 V	0.376 V	VBATS1[7:0]	Direct Register 82
Battery Voltage Sense 2 (V_{BAT})	0 to –95.88 V	0.376 V	VBATS2[7:0]	Direct Register 83
Transistor 1 Current Sense	0 to 81.35 mA	0.319 mA	IQ1[7:0]	Direct Register 84
Transistor 2 Current Sense	0 to 81.35 mA	0.319 mA	IQ2[7:0]	Direct Register 85
Transistor 3 Current Sense	0 to 9.59 mA	37.6 µA	IQ3[7:0]	Direct Register 86
Transistor 4 Current Sense	0 to 9.59 mA	37.6 µA	IQ4[7:0]	Direct Register 87
Transistor 5 Current Sense	0 to 80.58 mA	0.316 mA	IQ5[7:0]	Direct Register 88
Transistor 6 Current Sense	0 to 80.58 mA	0.316 mA	IQ6[7:0]	Direct Register 89
***Note:** The ProSLIC uses registers that are both directly and indirectly mapped. A “direct” register is one that is mapped directly.				

2.2.5. Power Monitoring and Line Fault Detection

In addition to reporting voltages and currents, the ProSLIC continuously monitors the power dissipated in each linefeed transistor. Realtime output power of any one of the six linefeed transistors can be read by setting the Power Monitor Pointer (direct Register 76) to point to the desired transistor and then reading the Line Power Output Monitor (direct Register 77).

The realtime power measurements are low-pass filtered and compared to a maximum power threshold. Maximum power thresholds and filter time constants are software programmable and should be set for each transistor pair based on the characteristics of the transistors used. Table 22 describes the registers associated with this function. If the power in any external transistor exceeds the programmed threshold, a power alarm event is triggered. The ProSLIC sets the Power Alarm register bit, generates an interrupt (if enabled), and automatically enters the Open state (if AOPN = 1). This feature protects the external transistors from fault conditions and, combined with the loop voltage and current monitors, allows diagnosis of the type of fault condition present on the line.

The value of each thermal low-pass filter pole is set according to the equation:

$$\text{Thermal LPF Pole [12:0]} = \frac{4096}{800 \times \tau}$$

where τ is the thermal time constant of the transistor package, 4096 is the full range of the 12-bit register, and 800 is the sample rate in hertz. Generally τ = 3 seconds for SOT223 packages and τ = 0.16 seconds for SOT23, but check with the manufacturer for the package thermal constant of a specific device. For example, the power alarm threshold and low-pass filter values for Q5 and Q6 using a SOT223 package transistor are computed as follows:

$$\text{PT56[7:0]} = \frac{P_{MAX}}{\text{Resolution}} = \frac{1.28}{0.0304} = 42 = 2\text{Ah}$$

Thus, indirect Register 21 should be set to 2Ah x 2^7 = 1500h.

Note: The power monitor resolution for Q3 and Q4 is different from that of Q1, Q2, Q5, and Q6.

Table 22. Associated Power Monitoring and Power Fault Registers

Parameter	Description/ Range	Resolution	Register Bits	Location*
Power Monitor Pointer	0 to 5 points to Q1 to Q6, respectively	N/A	PWRMP[2:0]	Direct Register 76
Line Power Monitor Output	0 to 7.8 W for Q1, Q2, Q5, Q6 0 to 0.9 W for Q3, Q4	30.4 mW 3.62 mW	PWROM[7:0]	Direct Register 77
Power Alarm Threshold, Q1 & Q2	0 to 7.8 W	30.4 mW	PPT12[7:0]	Indirect Register 19
Power Alarm Threshold, Q3 & Q4	0 to 0.9 W	3.62 mW	PPT34[7:0]	Indirect Register 20
Power Alarm Threshold, Q5 & Q6	0 to 7.8 W	30.4 mW	PPT56[7:0]	Indirect Register 21
Thermal LPF Pole, Q1 & Q2	see equation above		NQ12[12:0]	Indirect Register 24
Thermal LPF Pole, Q3 & Q4	see equation above		NQ34[12:0]	Indirect Register 25
Thermal LPF Pole, Q5 & Q6	see equation above		NQ56[12:0]	Indirect Register 26
Power Alarm Interrupt Pending	Bits 2 to 7 correspond to Q1 to Q6, respectively	N/A	QnAP[n+1], where n = 1 to 6	Direct Register 19

Table 22. Associated Power Monitoring and Power Fault Registers (Continued)

Power Alarm Interrupt Enable	Bits 2 to 7 correspond to Q1 to Q6, respectively	N/A	QnAE[n+1], where n = 1 to 6	Direct Register 22
Power Alarm Automatic/Manual Detect	0 = manual mode 1 = enter open state upon power alarm	N/A	AOPN	Direct Register 67

***Note:** The ProSLIC uses registers that are both directly and indirectly mapped. A "direct" register is one that is mapped directly. An "indirect" register is one that is accessed using the indirect access registers (direct registers 28 through 31).

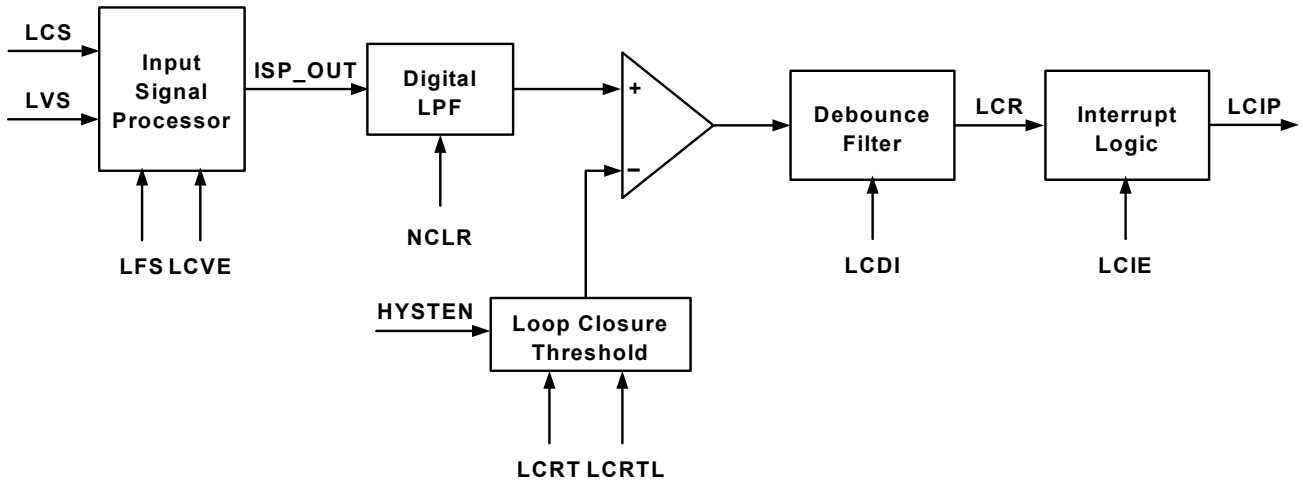


Figure 9. Loop Closure Detection

2.2.6. Loop Closure Detection

A loop closure event signals that the terminal equipment has gone off-hook during on-hook transmission or on-hook active states. The ProSLIC performs loop closure detection digitally using its on-chip monitor A/D converter. The functional blocks required to implement loop closure detection are shown in Figure 9. The primary input to the system is the Loop Current Sense value provided in the LCS register (direct Register 79). The LCS value is processed in the Input Signal Processor when the ProSLIC is in the on-hook transmission or on-hook active linefeed state, as indicated by the Linefeed Shadow register, LFS[2:0] (direct Register 64). The data then feeds into a programmable digital low-pass filter, which removes unwanted ac signal components before threshold detection.

The output of the low-pass filter is compared to a programmable threshold, LCRT (indirect register 15). The threshold comparator output feeds a programmable debouncing filter. The output of the debouncing filter remains in its present state unless the input remains in the opposite state for the entire period of time programmed by the loop closure debounce interval, LCDI (direct Register 69). If the debounce interval has been satisfied, the LCR bit will be set to indicate that a valid loop closure has occurred. A loop closure interrupt is generated if enabled by the LCIE bit (direct Register 22). Table 23 lists the registers that must be written or monitored to correctly detect a loop closure condition.

2.2.7. Loop Closure Threshold Hysteresis

Programmable hysteresis to the loop closure threshold can be enabled by setting HYSTEN = 1 (direct Register 108, bit 0). The hysteresis is defined by LCRT (indirect Register 15) and LCRTL (indirect Register 66), which set the upper and lower bounds, respectively.

2.2.8. Voltage-Based Loop Closure Detection

An optional voltage-based loop closure detection mode is enabled by setting LCVE = 1 (direct Register 108, bit 2). In this mode, the loop voltage is compared to the loop closure threshold register (LCRT), which represents a minimum voltage threshold instead of a maximum current threshold. If hysteresis is also enabled, LCRT represents the upper voltage boundary, and LCRTL represents the lower voltage boundary for hysteresis. Although voltage-based loop closure detection is an option, the default current-based loop closure detection is recommended.

Table 23. Register Set for Loop Closure Detection

Parameter	Register	Location
Loop Closure Interrupt Pending	LCIP	Direct Reg. 19
Loop Closure Interrupt Enable	LCIE	Direct Reg. 22
Loop Closure Threshold	LCRT[5:0]	Indirect Reg. 15
Loop Closure Threshold—Lower	LCRTL[5:0]	Indirect Reg. 66
Loop Closure Filter Coefficient	NCLR[12:0]	Indirect Reg. 22
Loop Closure Detect Status (monitor only)	LCR	Direct Reg. 68
Loop Closure Detect Debounce Interval	LCDI[6:0]	Direct Reg. 69
Hysteresis Enable	HYSTEN	Direct Reg. 108
Voltage-Based Loop Closure	LCVE	Direct Reg. 108

2.2.9. Linefeed Calibration

An internal calibration algorithm corrects for internal and external component errors. The calibration is initiated by setting the CAL bit in direct Register 96. Upon completion of the calibration cycle, this bit is automatically reset.

It is recommended that a calibration be executed following system power-up. Upon release of the chip reset, the Si3233 will be in the open state. After powering up the dc-dc converter and allowing it to settle for time (t_{settle}) the calibration can be initiated. Additional calibrations may be performed, but only one calibration should be necessary as long as the system remains powered up.

During calibration, V_{BAT}, V_{TIP}, and V_{RING} voltages are controlled by the calibration engine to provide the correct external voltage conditions for the algorithm. Calibration should be performed in the on-hook state. RING or TIP must not be connected to ground during the calibration.

2.3. Battery Voltage Generation and Switching

The Si3233 integrates a dc-dc converter controller that dynamically regulates a single output voltage. This eliminates the need to supply large external battery voltages. Instead, it converts a single positive input voltage into the real-time battery voltage needed for any given state according to programmed linefeed parameters.

2.3.1. DC-DC Converter General Description

The dc-dc converter dynamically generates the large negative voltages required to operate the linefeed interface. The Si3233 acts as the controller for a buck-boost dc-dc converter that converts a positive dc voltage into the desired negative battery voltage. In addition to eliminating external power supplies, this allows the Si3233 to dynamically control the battery voltage to the minimum required for any given mode of operation.

Extensive design guidance can be obtained from Application Note 45 (AN45) and from an interactive dc-dc converter design spreadsheet. Both of these documents are available on the Silicon Laboratories website (www.silabs.com).

2.3.2. BJT/Inductor Circuit Using Si3233

The BJT/Inductor circuit, as defined in Figure 4, offers a flexible, low-cost solution. Depending on selected L1 inductance value and the switching frequency, the input voltage (V_{DC}) can range from 5 V to 30 V. By nature of a dc-dc converter's operation, peak and average input currents can become large with small input voltages. Consider this when selecting the appropriate input voltage and power rating for the V_{DC} power supply.

In this circuit, a PNP power BJT (Q7) switches the current flow through low ESR inductor L1. The Si3233 uses the DCDRV and DCFF pins to switch Q7 on and off. DCDRV controls Q7 through NPN BJT Q8. DCFF is ac coupled to Q7 through capacitor C10 to assist R16 in turning off Q7. Therefore, DCFF must have opposite polarity to DCDRV, and the Si3233 (not Si3233M) must be used.

2.3.3. MOSFET/Transformer Circuit Option Using Si3233M

The MOSFET/transformer circuit option, as defined in Figure 5, offers higher power efficiencies across a larger input voltage range. Depending on the transformer's primary inductor value and the switching frequency, the input voltage (V_{DC}) can range from 3.3 V to 35 V. Therefore, it is possible to power the entire ProSLIC

solution from a single 3.3 V or 5 V power supply. By nature of a dc-dc converter's operation, peak and average input currents can become large with small input voltages. Consider this when selecting the appropriate input voltage and power rating for the V_{DC} power supply (number of REN supported).

In this circuit, an n-channel power MOSFET (M1) switches the current flow through a power transformer T1. T1 is specified in Application Note 45 (AN45), and includes several taps on the primary side to facilitate a wide range of input voltages. The Si3233M version of the Si3233 must be used for the application circuit depicted in Figure 5 because the DCFF pin is used to drive M1 directly and therefore must be the same polarity as DCDRV. DCDRV is not used in this circuit option; connecting DCFF and DCDRV together is not recommended.

2.3.4. DC-DC Converter Architecture

The control logic for a pulse width modulated (PWM) dc-dc converter is incorporated in the Si3233. Output pins, DCDRV and DCFF, are used to switch a bipolar transistor or MOSFET. The polarity of DCFF is opposite to that of DCDRV.

The dc-dc converter circuit is powered on when the DCOF bit in the Power Down Register (direct Register 14, bit 4) is cleared to 0. The switching regulator circuit within the Si3233 is a high performance, pulse-width modulation controller. The control pins are driven by the PWM controller logic in the Si3233. The regulated output voltage (V_{BAT}) is sensed by the SVBAT pin and is used to detect whether the output voltage is above or below an internal reference for the desired battery voltage. The dc monitor pins SDCH and SDCL monitor input current and voltage to the dc-dc converter external circuitry. If an overload condition is detected, the PWM controller will turn off the switching transistor for the remainder of a PWM period to prevent damage to external components. It is important that the proper value of R18 be selected to ensure safe operation. Guidance is given in Application Note 45 (AN45).

The PWM controller operates at a frequency set by the dc-dc Converter PWM register (direct Register 92). During a PWM period the outputs of the control pins DCDRV and DCFF are asserted for a time given by the read-only PWM Pulse Width register (direct Register 94).

The dc-dc converter must be off for some time in each cycle to allow the inductor or transformer to transfer its stored energy to the output capacitor, C9. This minimum off time can be set through the dc-dc Converter Switching Delay register, (direct Register 93). The number of 16.384 MHz clock cycles that the controller is off is equal to DCTOF (bits 0 through 4) plus 4. If the dc Monitor pins detect an overload condition, the dc-dc converter interrupts its conversion cycles regardless of the register settings to prevent component damage. These inputs should be calibrated by writing the DCCAL bit (bit 7) of the dc-dc Converter Switching Delay register, direct Register 93, after the dc-dc converter has been turned on.

The most negative terminal (V_{RING} or V_{TIP}) is offset from the battery voltage (V_{BAT}) by a programmable overlead voltage (V_{OV}) to allow sufficient headroom for audio signals.

The dc-dc converter can be made to adjust more quickly to voltage changes by setting DCSU = 1 (Direct Register 108, bit 5). Audio band noise can optionally be reduced using an audio band filter by setting DCFIL = 1 (Direct Register 108, bit 1).

2.3.5. DC-DC Converter During Forward Active

The Si3233 dynamically adjusts V_{BAT} to match the requirements of the loop and line state. The behavior of the tracking dc-dc converter in the active state is shown in Figure 10.

In the active state, the TIP-to-RING open circuit voltage is kept at V_{OC} in the constant voltage region while the regulator output voltage, $V_{BAT} = V_{CM} + V_{OC} + V_{OV}$.

When the loop current attempts to exceed I_{LIM}, the dc line driver circuit enters constant current mode allowing the TIP to RING voltage to track R_{LOOP}. As the TIP terminal is kept at a constant voltage, it is the RING terminal voltage that tracks R_{LOOP} and, as a result, the $|V_{BAT}|$ voltage will also track R_{LOOP}. In this state, $|V_{BAT}| = I_{LIM} \times R_{LOOP} + V_{CM} + V_{OV}$. As R_{LOOP} decreases below the VOC/I_{LIM} mark, the regulator output voltage can continue to track R_{LOOP} (TRACK = 1), or the R_{LOOP} tracking mechanism is stopped when $|V_{BAT}| = |V_{BATL}|$ (TRACK = 0). The former case is the more common application and provides the maximum power dissipation savings. In principle, the regulator output voltage can go as low as $|V_{BAT}| = V_{CM} + V_{OV}$, offering significant power savings.

When TRACK = 0, $|V_{BAT}|$ will not decrease below V_{BATL}. The RING terminal voltage, however, continues to decrease with decreasing R_{LOOP}. The power dissipation on the NPN bipolar transistor driving the RING terminal can become large and may require a higher power rating device. The non-tracking mode of operation is required by specific terminal equipment which, in order to initiate certain data transmission modes, goes briefly on-hook to measure the line voltage to determine whether there is any other off-hook terminal equipment on the same line. TRACK = 0 mode

is desired since the regulator output voltage has long settling time constants (on the order of tens of milliseconds) and cannot change rapidly for TRACK = 1 mode. Therefore, the brief on-hook voltage measurement would yield approximately the same voltage as the off-hook line voltage and would cause the terminal equipment to incorrectly sense another off-hook terminal.

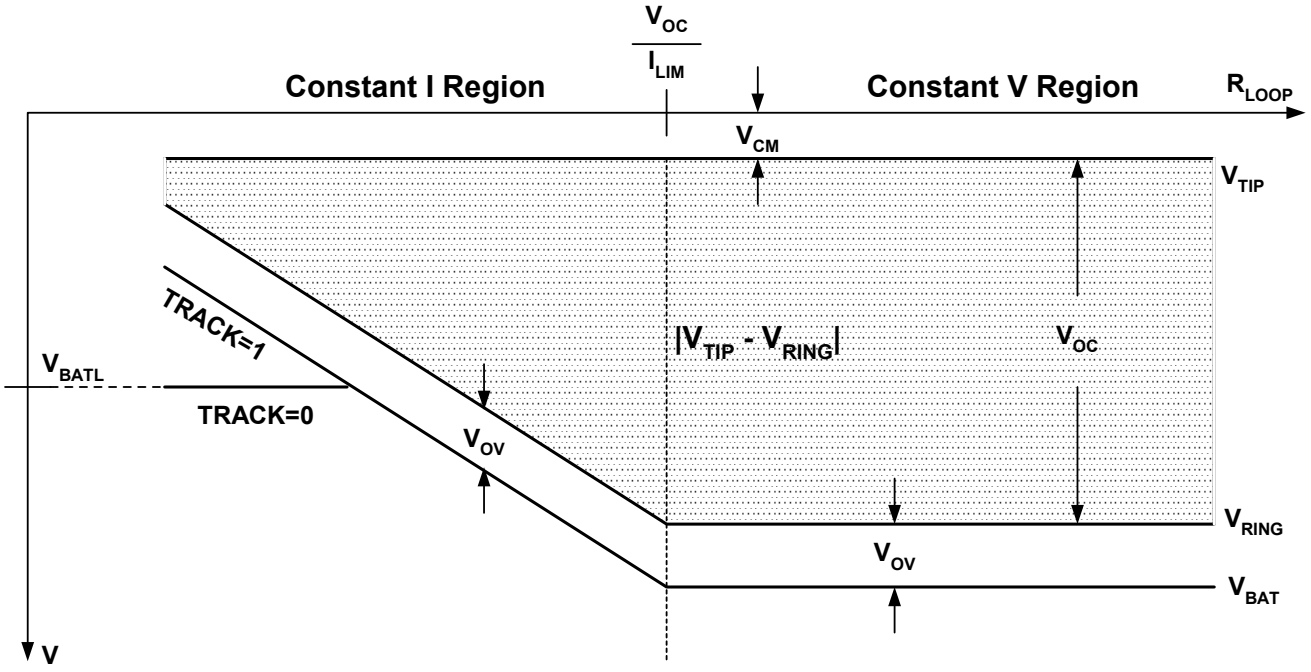


Figure 10. V_{TIP}, V_{RING}, and V_{BAT} in the Forward Active State

Table 24. Associated Relevant DC-DC Converter Registers

Parameter	Range	Resolution	Register Bit	Location
DC-DC Converter Power-off Control	n/a	n/a	DCOF	Direct Register 14
DC-DC Converter Calibration Enable/Status	n/a	n/a	DCCAL	Direct Register 93
DC-DC Converter PWM Period	0 to 15.564 us	61.035 ns	DCN[7:0]	Direct Register 92
DC-DC Converter Min. Off Time	(0 to 1.892 us) + 4 clock cycles	61.035 ns	DCTOF[4:0]	Direct Register 93
High Battery Voltage—V_{BATH}	0 to –94.5 V	1.5 V	VBATH[5:0]	Direct Register 74
Low Battery Voltage—V_{BATL}	0 to –94.5 V	1.5 V	VBATL[5:0]	Direct Register 75
V_{OV}	0 to –9 V or 0 to –13.5 V	1.5 V	VMIND[3:0] VOV	Indirect Register 64 Direct Register 66

Note: The ProSLIC uses registers that are both directly and indirectly mapped. A “direct” register is one that is mapped directly. An “indirect” register is one that is accessed using the indirect access registers (direct registers 28 through 31).

2.3.6. DC-DC Converter During Ringing

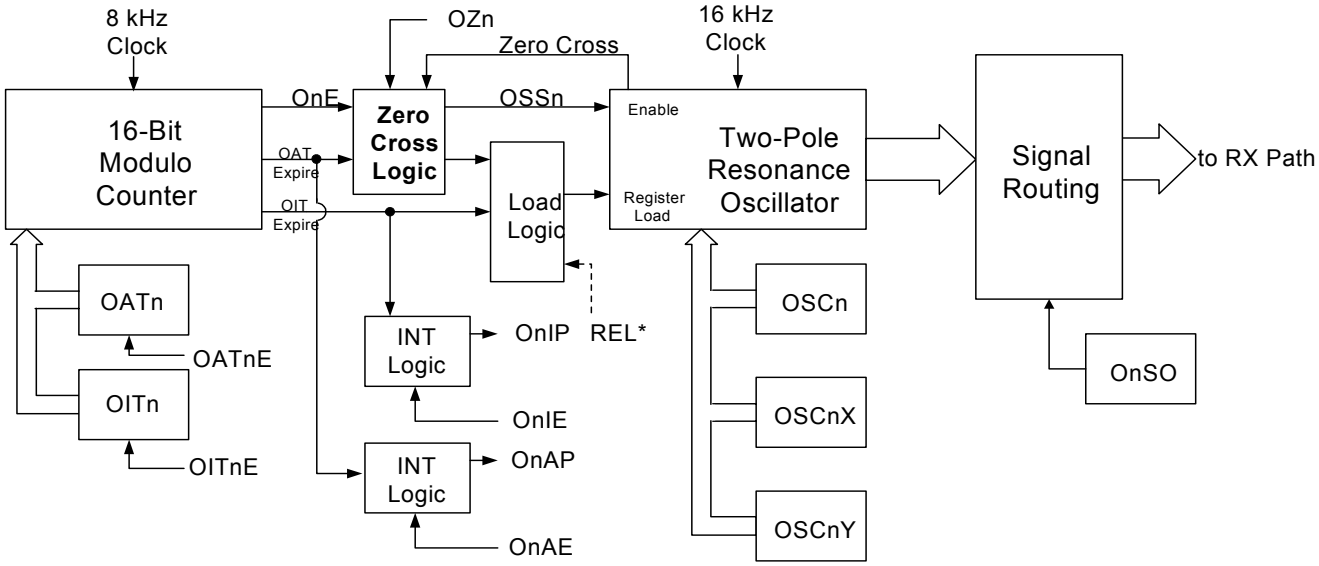
When the ProSLIC enters the ringing state, it requires voltages well above those used in the active mode. The voltage to be generated and regulated by the dc-dc converter during a ringing burst is set using the VBATH register (direct Register 74). VBATH can be set between 0 and –94.5 V in 1.5 V steps. To avoid clipping the ringing signal, VBATH must be set larger than the ringing amplitude. At the end of each ringing burst the dc-dc converter switches back to active state regulation as described above.

2.4. Tone Generation

Two digital tone generators are provided in the ProSLIC. They allow the generation of a wide variety of single or dual tone frequency and amplitude combinations and spare the user the effort of generating the required POTS signaling tones on the PCM highway. DTMF, FSK (caller ID), call progress, and other tones can all be generated on-chip.

2.4.1. Tone Generator Architecture

A simplified diagram of the tone generator architecture is shown in Figure 11. The oscillator, active/inactive timers, interrupt block, and signal routing block are connected to give the user flexibility in creating audio signals. Control and status register bits are placed in the figure to indicate their association with the tone generator architecture. These registers are described in more detail in Table 25.



*Tone Generator 1 Only
n = "1" or "2" for Tone Generator 1 and 2, respectively

Figure 11. Simplified Tone Generator Diagram

2.4.2. Oscillator Frequency and Amplitude

Each of the two tone generators contains a two-pole resonant oscillator circuit with a programmable frequency and amplitude, which are programmed via indirect registers OSC1, OSC1X, OSC1Y, OSC2, OSC2X, and OSC2Y. The sample rate for the two oscillators is 16 kHz. The equations are as follows:

$$coeff_n = \cos(2\pi f_n/16\ kHz),$$

where f_n is the frequency to be generated;

$$OSCn = coeff_n \times (2^{15});$$

$$OSCnX = \frac{1}{4} \times \sqrt{\frac{1-coeff}{1+coeff}} \times (2^{15}-1) \times \frac{Desired\ V_{rms}}{1.11\ V_{rms}}$$

where desired Vrms is the amplitude to be generated;

$$OSCnY = 0,$$

n = 1 or 2 for oscillator 1 or oscillator 2, respectively.

For example, in order to generate a DTMF digit of 8, the two required tones are 852 Hz and 1336 Hz. Assuming the generation of half-scale values (ignoring twist) is desired, the following values are calculated:

$$coeff_1 = \cos\left(\frac{2\pi 852}{16000}\right) = 0.94455$$

$$OSC1 = 0.94455(2^{15}) = 30951 = 78E6h$$

$$OSC1X = \frac{1}{4} \times \sqrt{\frac{0.05545}{1094455}} \times (2^{15}-1) \times 0.5 = 692 = 2B3h$$

$$OSC1Y = 0$$

$$coeff_2 = \cos\left(\frac{2\pi 1336}{16000}\right) = 0.86550$$

$$OSC2 = 0.86550\ (2^{15}) = 28361 = 3EC8h$$

$$OSC2X = \frac{1}{4} \times \sqrt{\frac{0.13450}{1.86550}} \times (2^{15}-1) \times 0.5 = 1098 = 44Bh$$

$$OSC2Y = 0$$

The computed values above would be written to the corresponding registers to initialize the oscillators. Once the oscillators are initialized, the oscillator control registers can be accessed to enable the oscillators and direct their outputs.

2.4.3. Tone Generator Cadence Programming

Each of the two tone generators contains two timers, one for setting the active period and one for setting the inactive period. The oscillator signal is generated during the active period and suspended during the inactive period. Both the active and inactive periods can be programmed from 0 to 8 seconds in 125 µs steps. The active period time interval is set using OAT1 (direct registers 36 and 37) for tone generator 1 and OAT2 (direct registers 40 and 41) for tone generator 2.

To enable automatic cadence for tone generator 1, define the OAT1 and OIT1 registers and then set the O1TAE bit (direct Register 32, bit 4) and O1TIE bit (direct Register 32, bit 3). This enables each of the timers to control the state of the Oscillator Enable bit, O1E (direct Register 32, bit 2). The 16-bit counter will begin counting until the active timer expires, at which time the 16-bit counter will reset to zero and begin counting until the inactive timer expires. The cadence continues until the user clears the O1TAE and O1TIE control bits. The zero crossing detect feature can be implemented by setting the OZ1 bit (direct Register 32, bit 5). This ensures that each oscillator pulse ends without a dc component. The timing diagram in Figure 12 is an example of an output cadence using the zero crossing feature.

One-shot oscillation can be achieved by enabling O1E and O1TAE. Direct control over the cadence can be achieved by controlling the O1E bit (direct Register 32, bit 2) directly if O1TAE and O1TIE are disabled.

The operation of tone generator 2 is identical to that of tone generator 1 using its respective control registers.

Note: Tone Generator 2 should not be enabled simultaneously with the ringing oscillator due to resource sharing within the hardware.

Continuous phase frequency-shift keying (FSK) waveforms may be created using tone generator 1 (not available on tone generator 2) by setting the REL bit (direct Register 32, bit 6), which enables reloading of the OSC1, OSC1X, and OSC1Y registers at the expiration of the active timer (OAT1).

Table 25. Associated Tone Generator Registers

Tone Generator 1			
Parameter	**Description / Range**	**Register Bits**	**Location**
Oscillator 1 Frequency Coefficient	Sets oscillator frequency	OSC1[15:0]	Indirect Register 0
Oscillator 1 Amplitude Coefficient	Sets oscillator amplitude	OSC1X[15:0]	Indirect Register 1
Oscillator 1 initial phase coefficient	Sets initial phase	OSC1Y[15:0]	Indirect Register 2
Oscillator 1 Active Timer	0 to 8 seconds	OAT1[15:0]	Direct Registers 36 & 37
Oscillator 1 Inactive Timer	0 to 8 seconds	OIT1[15:0]	Direct Register 38 & 39
Oscillator 1 Control	Status and control registers	OSS1, REL, OZ1, O1TAE, O1TIE, O1E, O1SO[1:0]	Direct Register 32
Tone Generator 2			
Parameter	**Description/Range**	**Register**	**Location**
Oscillator 2 Frequency Coefficient	Sets oscillator frequency	OSC2[15:0]	Indirect Register 3
Oscillator 2 Amplitude Coefficient	Sets oscillator amplitude	OSC2X[15:0]	Indirect Register 4
Oscillator 2 initial phase coefficient	Sets initial phase	OSC2Y[15:0]	Indirect Register 5
Oscillator 2 Active Timer	0 to 8 seconds	OAT2[15:0]	Direct Registers 40 & 41
Oscillator 2 Inactive Timer	0 to 8 seconds	OIT2[15:0]	Direct Register 42 & 43
Oscillator 2 Control	Status and control registers	OSS2, OZ2, O2TAE, O2TIE, O2E, O2SO[1:0]	Direct Register 33

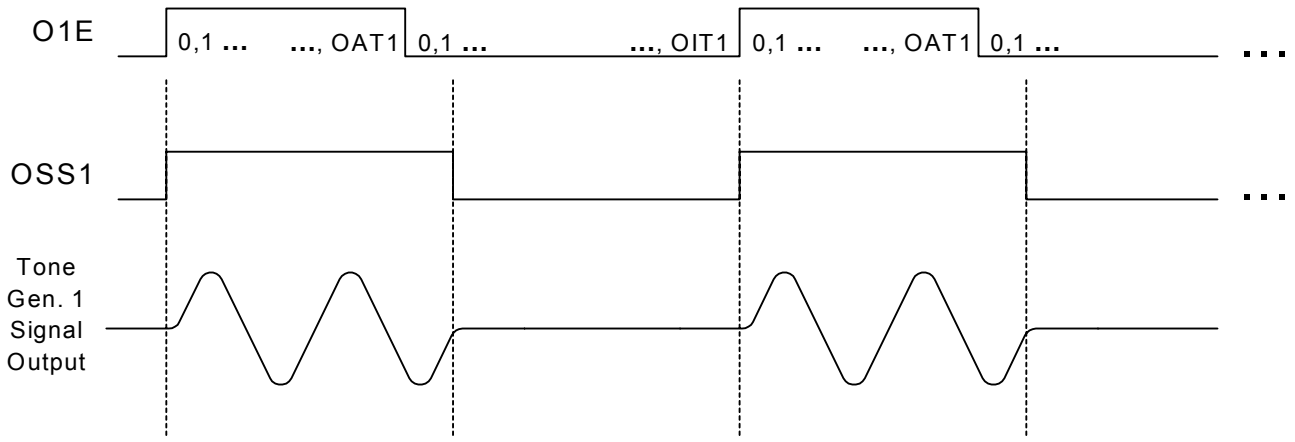


Figure 12. Tone Generator Timing Diagram

2.4.4. Enhanced FSK Waveform Generation

Enhanced FSK generation can be enabled by setting FSKEN = 1 (direct Register 108, bit 6) and REL = 1 (direct Register 32, bit 6). In this mode, the user can define mark (1) and space (0) attributes once during initialization by defining indirect registers 69–74. The user need only indicate 0-to-1 and 1-to-0 transitions in the information stream. By writing to FSKDAT (direct Register 52), this mode applies a 24 kHz sample rate to tone generator 1 to give additional resolution to timers and frequency generation. “AN32: Si321x Frequency Shift Keying (FSK) Modulation” gives detailed instructions on how to implement FSK in this mode. Additionally, sample source code is available from Silicon Laboratories upon request.

2.4.5. Tone Generator Interrupts

Both the active and inactive timers can generate their own interrupt to signal “on/off” transitions to the software. The timer interrupts for tone generator 1 can be individually enabled by setting the O1AE and O1IE bits (direct Register 21, bits 0 and 1, respectively). Timer interrupts for tone generator two are O2AE and O2IE (direct Register 21, bits 2 and 3, respectively). A pending interrupt for each of the timers is determined by reading the O1AP, O1IP, O2AP, and O2IP bits in the Interrupt Status 1 register (direct Register 18, bits 0 through 3, respectively).

2.5. Ringing Generation

The ProSLIC provides fully programmable internal balanced ringing with or without a dc offset to ring a wide variety of terminal devices. All parameters associated with ringing are software programmable: ringing frequency, waveform, amplitude, dc offset, and ringing cadence. Both sinusoidal and trapezoidal ringing waveforms are supported, and the trapezoidal crest factor is programmable. Ringing signals of up to 88 V peak or more can be generated, enabling the ProSLIC to drive a 5 REN (1380 Ω + 40 μF) ringer load across loop lengths of 2000 feet (160 Ω) or more.

2.5.1. Ringing Architecture

The ringing generator architecture is nearly identical to that of the tone generator. The sinusoid ringing waveform is generated using an internal two-pole resonance oscillator circuit with programmable frequency and amplitude. However, since ringing frequencies are very low compared to the audio band signaling frequencies, the ringing waveform is generated at a 1 kHz rate instead of 16 kHz.

The ringing generator has two timers that function the same as for the tone generator timers. They allow on/off cadence settings up to 8 seconds on/ 8 seconds off. In addition to controlling ringing cadence, these timers control the transition into and out of the ringing state. Table 26 summarizes the list of registers used for ringing generation.

Note: Tone generator 2 should not be enabled concurrently with the ringing generator due to resource sharing within the hardware.

Table 26. Registers for Ringing Generation

Parameter	Range/ Description	Register Bits	Location
Ringing Waveform	Sine/Trapezoid	TSWS	Direct Register 34
Ringing Voltage Offset Enable	Enabled/ Disabled	RVO	Direct Register 34
Ringing Active Timer Enable	Enabled/ Disabled	RTAE	Direct Register 34
Ringing Inactive Timer Enable	Enabled/ Disabled	RTIE	Direct Register 34
Ringing Oscillator Enable	Enabled/ Disabled	ROE	Direct Register 34
Ringing Oscillator Active Timer	0 to 8 seconds	RAT[15:0]	Direct Registers 48 and 49
Ringing Oscillator Inactive Timer	0 to 8 seconds	RIT[15:0]	Direct Registers 50 and 51
Linefeed Control (Initiates Ringing State)	Ringing State = 100b	LF[2:0]	Direct Register 64
High Battery Voltage	0 to –94.5 V	VBATH[5:0]	Direct Register 74
Ringing dc voltage offset	0 to 94.5 V	ROFF[15:0]	Indirect Register 6
Ringing frequency	15 to 100 Hz	RCO[15:0]	Indirect Register 7

Table 26. Registers for Ringing Generation (Continued)

Ringing amplitude	0 to 94.5 V	RNGX[15:0]	Indirect Register 8
Ringing initial phase	Sets initial phase for sinewave and period for trapezoid	RNGY[15:0]	Indirect Register 9
Common Mode Bias Adjust During Ringing	0 to 22.5 V	VCMR[3:0]	Indirect Register 27
Note: The ProSLIC uses registers that are both directly and indirectly mapped. A "direct" register is one that is mapped directly. An "indirect" register is one that is accessed using the indirect access registers (direct registers 28 through 31).			

When the ringing state is invoked by writing LF[2:0] = 100 (direct Register 64), the ProSLIC will go into the ringing state and start the first ring. At the expiration of RAT, the ProSLIC will turn off the ringing waveform and will go to the on-hook transmission state. At the expiration of RIT, ringing will again be initiated. This process will continue as long as the two timers are enabled and the Linefeed Control register is set to the ringing state.

2.5.2. Sinusoidal Ringing

To configure the ProSLIC for sinusoidal ringing, the frequency and amplitude are initialized by writing to the following indirect registers: RCO, RNGX, and RNGY. The equations for RCO, RNGX, RNGY are as follows:

$$RCO = coeff \times (2^{15})$$

where

$$coeff = \cos\left(\frac{2\pi f}{1000\ Hz}\right)$$

and f = desired ringing frequency in hertz.

$$RNGX = \frac{1}{4} \times \sqrt{\frac{1-coeff}{1+coeff}} \times 2^{15} \times \frac{\text{Desired } V_{PK}(0 \text{ to } 94.5\ V)}{96\ V}$$

$$RNGY = 0$$

In selecting a ringing amplitude, the peak TIP-to-RING ringing voltage must be greater than the selected on-hook line voltage setting (VOC, direct Register 72). For example, to generate a 70 V_{PK} 20 Hz ringing signal, the equations are as follows:

$$coeff = \cos\left(\frac{2\pi \times 20}{1000\ Hz}\right) = 0.99211$$

$$RCO = 0.99211 \times (2^{15}) = 32509 = 7EFDh$$

$$RNGX = \frac{1}{4} \times \sqrt{\frac{0.00789}{1.99211}} \times 2^{15} \times \frac{70}{96} = 376 = 0177h$$

$$RNGY = 0$$

In addition, the user must select the sinusoidal ringing waveform by writing TSWS = 0 (direct Register 34, bit 0).

2.5.3. Trapezoidal Ringing

In addition to the sinusoidal ringing waveform, the ProSLIC supports trapezoidal ringing. Figure 13 illustrates a trapezoidal ringing waveform with offset V_{ROFF}.

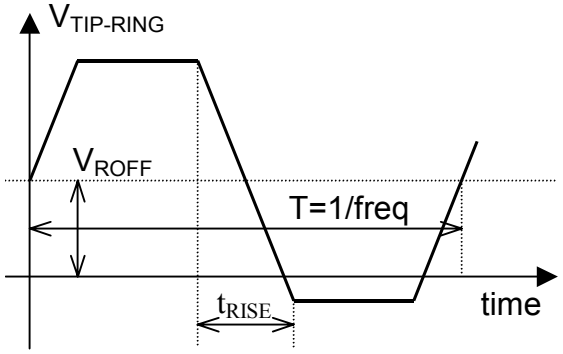


Figure 13. Trapezoidal Ringing Waveform

To configure the ProSLIC for trapezoidal ringing, the user should follow the same basic procedure as in the Sinusoidal Ringing section, but using the following equations:

$$RNGY = \frac{1}{2} \times Period \times 8000$$

$$RNGX = \frac{\text{Desired } V_{PK}}{96\ V} \times (2^{15})$$

$$RCO = \frac{2 \times RNGX}{t_{RISE} \times 8000}$$

RCO is a value which is added or subtracted from the waveform to ramp the signal up or down in a linear fashion. This value is a function of rise time, period, and amplitude, where rise time and period are related through the following equation for the crest factor of a trapezoidal waveform.

$$t_{RISE} = \frac{3}{4}T\left(1 - \frac{1}{CF^2}\right)$$

where T = ringing period, and CF = desired crest factor.

For example, to generate a 71 V_{PK}, 20 Hz ringing signal, the equations are as follows:

$$RNGY(20\ Hz) = \frac{1}{2} \times \frac{1}{20\ Hz} \times 8000 = 200 = C8h$$

$$RNGX(71\ V_{PK}) = \frac{71}{96} \times 2^{15} = 24235 = 5EABh$$

For a crest factor of 1.3 and a period of 0.05 seconds (20 Hz), the rise time requirement is 0.0153 seconds.

$$RCO(20\ Hz,\ 1.3\ crest\ factor) = \frac{2 \times 24235}{0.0153 \times 8000} = 396 = 018Ch$$

In addition, the user must select the trapezoidal ringing waveform by writing TSWS = 1 in direct Register 34.

2.5.4. Ringing DC voltage Offset

A dc offset can be added to the ac ringing waveform by defining the offset voltage in ROFF (indirect Register 6). The offset, V_{ROFF}, is added to the ringing signal when RVO is set to 1 (direct Register 34, bit 1). The value of ROFF is calculated as follows:

$$ROFF = \frac{V_{ROFF}}{96} \times 2^{15}$$

2.5.5. Linefeed Considerations During Ringing

Care must be taken to keep the generated ringing signal within the ringing voltage rails (GNDA and V_{BAT}) to maintains proper biasing of the external bipolar transistors. If the ringing signal nears the rails, a distorted ringing signal and excessive power dissipation in the external transistors will result.

To prevent this invalid operation, set the VBATH value (direct Register 74) to a value higher than the maximum peak ringing voltage. The discussion below outlines the considerations and equations that govern the selection of the VBATH setting for a particular desired peak ringing voltage.

First, the required amount of ringing overhead voltage, V_{OVR}, is calculated based on the maximum value of current through the load, $I_{LOAD,PK}$, the minimum current gain of Q5 and Q6, and a reasonable voltage required to keep Q5 and Q6 out of saturation. For ringing signals up to V_{PK} = 87 V, V_{OVR} = 7.5 V is a safe value. However, to determine V_{OVR} for a specific case, use the equations below.

$$I_{LOAD,PK} = \frac{V_{AC,PK}}{R_{LOAD}} + I_{OS} = V_{AC,PK} \times \frac{N_{REN}}{6.9\ k\Omega} + I_{OS}$$

where:

N_{REN} is the ringing REN load (max value = 5),

I_{OS} is the offset current flowing in the line driver circuit (max value = 2 mA), and

$V_{AC,PK}$ = amplitude of the ac ringing waveform.

It is good practice to provide a buffer of a few more milliamperes for $I_{LOAD,PK}$ to account for possible line leakages, etc. The total $I_{LOAD,PK}$ current should be smaller than 80 mA.

$$V_{OVR} = I_{LOAD,PK} \times \frac{\beta + 1}{\beta} \times (80.6\ \Omega + 1\ V)$$

where β is the minimum expected current gain of transistors Q5 and Q6.

The minimum value for VBATH is therefore given by the following:

$$VBATH = V_{AC,PK} + V_{ROFF} + V_{OVR}$$

The ProSLIC is designed to create a fully balanced ringing waveform, meaning that the TIP and RING common mode voltage, (V_{TIP} + V_{RING})/2, is fixed. This voltage is referred to as VCM_RING and is automatically set to the following:

$$VCM\_RING = \frac{VBATH - VCMR}{2}$$

VCMR is an indirect register which provides the headroom by the ringing waveform with respect to the VBATH rail. The value is set as a 4-bit setting in indirect Register 27 with an LSB voltage of 1.5 V/LSB. Register 27 should be set with the calculated V_{OVR} to provide voltage headroom during ringing.

Silicon revisions C and higher support the option to briefly increase the maximum differential current limit between the voltage transition of TIP and RING from ringing to a dc linefeed state. This mode is enabled by setting ILIMEN = 1 (direct Register 108, bit 7).

2.5.6. Ring Trip Detection

A ring trip event signals that the terminal equipment has gone off-hook during the ringing state. The ProSLIC performs ring trip detection digitally using its on-chip monitor A/D converter. The functional blocks required to implement ring trip detection is shown in Figure 14. The primary input to the system is the Loop Current Sense (LCS) value provided by the current monitoring circuitry and reported in direct Register 79. LCS data is processed by the input signal processor when the ProSLIC is in the ringing state as indicated by the

Linefeed Shadow register (direct Register 64). The data then feeds into a programmable digital low pass filter, which removes unwanted ac signal components before threshold detection.

The output of the low pass filter is compared to a programmable threshold, RPTP (indirect Register 16). The threshold comparator output feeds a programmable debouncing filter. The output of the debouncing filter remains in its present state unless the input remains in the opposite state for the entire period of time programmed by the ring trip debounce interval, RTDI[6:0] (direct Register 70). If the debounce interval has been satisfied, the RTP bit of direct Register 68 will be set to indicate that a valid ring trip has occurred. A ring trip interrupt is generated if enabled by the RTIE bit (direct Register 22). Table 27 lists the registers that must be written or monitored to correctly detect a ring trip condition.

The recommended values for RPTP, NRTP, and RTDI vary according to the programmed ringing frequency. Register values for various ringing frequencies are given in Table 28.

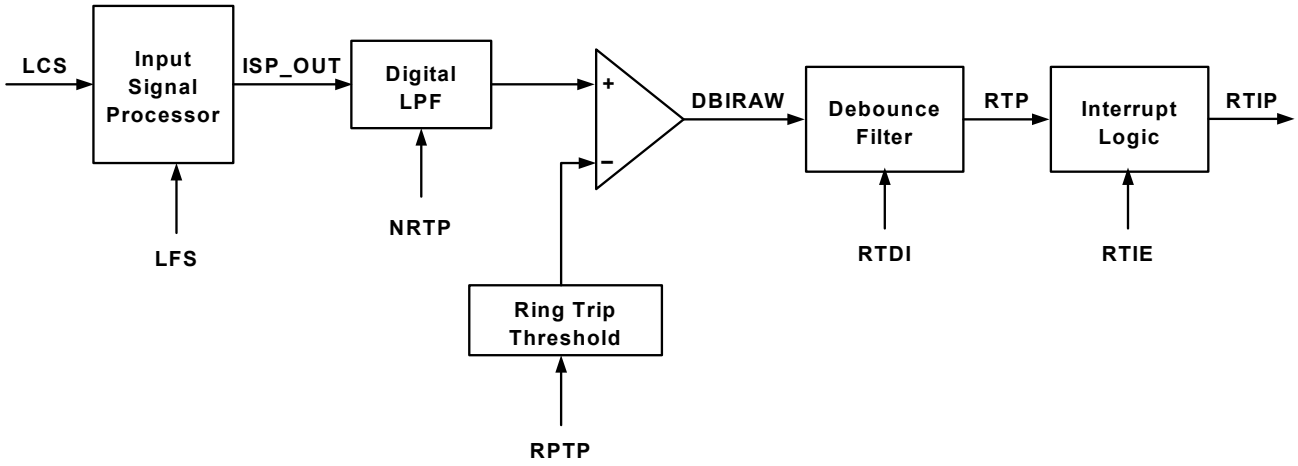


Figure 14. Ring Trip Detector

Table 27. Associated Registers for Ring Trip Detection

Parameter	Register	Location
Ring Trip Interrupt Pending	RTIP	Direct Register 19
Ring Trip Interrupt Enable	RTIE	Direct Register 22
Ring Trip Detect Debounce Interval	RTDI[6:0]	Direct Register 70
Ring Trip Threshold	RPTP[5:0]	Indirect Register 16
Ring Trip Filter Coefficient	NRTP[12:0]	Indirect Register 23
Ring Trip Detect Status (monitor only)	RTP	Direct Register 68
Note: The ProSLIC uses registers that are both directly and indirectly mapped. A “direct” register is one that is mapped directly. An “indirect” register is one that is accessed using the indirect access registers (direct registers 28 through 31).		

Table 28. Recommended Ring Trip Values for Ringing

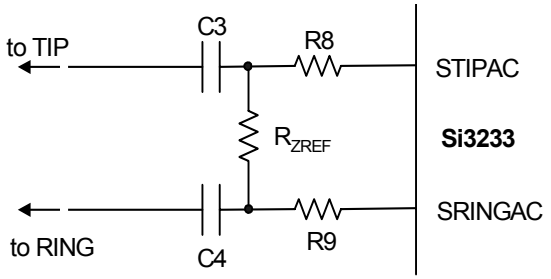
Ringing Frequency	NRTP		RPTP		RTDI	
Hz	decimal	hex	decimal	hex	decimal	hex
16.667	64	0200	34 mA	3600	15.4 ms	0F
20	100	0320	34 mA	3600	12.3 ms	0B
30	112	0380	34 mA	3600	8.96 ms	09
40	128	0400	34 mA	3600	7.5 ms	07
50	213	06A8	34 mA	3600	5 ms	05
60	256	0800	34 mA	3600	4.8 ms	05

2.6. Two-Wire Impedance Matching

The ProSLIC provides on-chip programmable two-wire impedance settings to meet a wide variety of worldwide two-wire return loss requirements. The two-wire impedance is programmed by loading one of the eight available impedance values into the TISS[2:0] bits of the Two-Wire Impedance Synthesis Control register (direct Register 10). If direct Register 10 is not explicitly set, the default setting of 600 Ω will be loaded into the TISS register.

The ProSLIC also provides a means to compensate for degraded subscriber loop conditions involving excessive line capacitance (leakage). The CLC[1:0] bits of direct Register 10 increase the ac signal magnitude to compensate for the additional loss at the high end of the audio frequency range. The default setting of CLC[2:0] assumes no line capacitance.

To support 600 Ω + 1 µF and 900 Ω + 2.16 µF applications, an external resistor, RZREF, must be inserted into the application circuit as shown in Figure 15.



For 600 + 1 µF, RZREF = 12 kΩ and C3, C4 = 100 nF.
For 900 + 2.16 µF, RZREF = 18 kΩ and C3, C4 = 220 nF.

Figure 15. R_{ZREF} External Resistor Placement

2.7. Clock Generation

The ProSLIC will generate the necessary internal clock frequencies from the PCLK input. PCLK must be synchronous to the 8 kHz FSYNC clock and run at one of the following rates: 256 kHz, 512 kHz, 768 kHz, 1.024 MHz, 1.536 MHz, 2.048 MHz, 4.096 MHz or 8.192 MHz. The ratio of the PCLK rate to the FSYNC rate is determined via a counter clocked by PCLK. The three-bit ratio information is automatically transferred into an internal register, PLL_MULT, following a reset of the ProSLIC. The PLL_MULT is used to control the internal PLL which multiplies PCLK as needed to generate 16.384 MHz rate needed to run the internal filters and other circuitry.

The PLL clock synthesizer settles very quickly following power up. However, the settling time depends on the PCLK frequency and it can be approximately predicted by the following equation:

$$T_{SETTLE} = \frac{64}{F_{PCLK}}$$

2.8. PLL Free-run Operation

The Si3233 is capable of operating in the absence of a valid PCLK signal. This feature can be enabled at any time after initialization by setting the PFR bit (register 14, bit 3). When enabled, the Si3233 internally gates off the buffered PCLK signal and applies a reference voltage input to the PLL. This allows the DC/DC converter to operate correctly and enables a nominal battery voltage to remain on the line. The PCLK pin must be held either high or low during PLL Free-run operation. To exit the PLL Free-run mode, valid PCLK and FSYNC signals must be reestablished and the Si3233 RESET pin must be asserted. The direct and indirect registers must then be reloaded with the desired initialization settings. Capturing and storing the calibration results (direct registers 98–107) before entering the PLL free-run mode is recommended since the results can then be manually reloaded after exiting the PLL free-run mode without executing a calibration routine. Note that audio signal generation will not be accurate during this mode of operation and therefore it is not recommended.

2.9. Interrupt Logic

The ProSLIC is capable of generating interrupts for the following events:

- Loop current/ring ground detected
- Ring trip detected
- Power alarm
- Active timer 1 expired
- Inactive timer 1 expired
- Active timer 2 expired
- Inactive timer 2 expired
- Ringing active timer expired
- Ringing inactive timer expired
- Indirect register access complete

The interface to the interrupt logic consists of six registers. Three interrupt status registers contain 1 bit for each of the above interrupt functions. These bits will be set when an interrupt is pending for the associated resource. Three interrupt enable registers also contain 1 bit for each interrupt function. In the case of the interrupt enable registers, the bits are active high. Refer to the appropriate functional description section for operational details of the interrupt functions.

When a resource reaches an interrupt condition, it will

signal an interrupt to the interrupt control block. The interrupt control block will then set the associated bit in the interrupt status register if the enable bit for that interrupt is set. The INT pin is a NOR of the bits of the interrupt status registers. Therefore, if a bit in the interrupt status registers is asserted, IRQ will assert low. Upon receiving the interrupt, the interrupt handler should read interrupt status registers to determine which resource is requesting service. To clear a pending interrupt, write the desired bit in the appropriate interrupt status register to 1. Writing a 0 has no effect. This provides a mechanism for clearing individual bits when multiple interrupts occur simultaneously. While the interrupt status registers are non-zero, the INT pin will remain asserted.

2.10. Serial Peripheral Interface

The control interface to the ProSLIC is a 4-wire interface modeled after commonly available micro-controller and serial peripheral devices. The interface consists of a clock (SCLK), chip select ($\overline{CS}$), serial data input (SDI), and serial data output (SDO). Data is transferred a byte at a time with each register access consisting of a pair of byte transfers. Figures 16 and 17 illustrate read and write operation in the SPI bus.

The first byte of the pair is the command/address byte. The MSB of this byte indicates register read when 1 and a register write when 0. The remaining seven bits of the command/address byte indicate the address of the register to be accessed. The second byte of the pair is the data byte. Because the falling edge of $\overline{CS}$ provides resynchronization of the SPI state machine in the event of a framing error, it is recommended (but not required) that $\overline{CS}$ be taken high between byte transfers as shown in Figures 16 and 17. During a read operation, the SDO becomes active and the 8-bit contents of the register are driven out MSB first. The SDO will be high impedence on either the falling edge of SCLK following the LSB, or the rising of $\overline{CS}$ as specified by the SPIM bit (direct Register 0, bit 6). SDI is a “don’t care” during the data portion of read operations. During write operations, data is driven into the ProSLIC via the SDI pin MSB first. The SDO pin will remain high impedance during write operations. Data always transitions with the falling edge of the clock and is latched on the rising edge. The clock should return to a logic high when no transfer is in progress.

There are a number of variations of usage on this four-wire interface:

- **Continuous clocking**. During continuous clocking, the data transfers are controlled by the assertion of the $\overline{CS}$ pin. $\overline{CS}$ must assert before the falling edge of SCLK on which the first bit of data is expected during a read cycle, and must remain low for the duration of the 8-‘bit transfer (command/address or data).
- **SDI/SDO wired operation.** Independent of the clocking options described, SDI and SDO can be treated as two separate lines or wired together if the master is capable of tristating its output during the data byte transfer of a read operation.
- **Daisy chain mode.** This mode allows communication with banks of up to eight ProSLIC devices using one chip select signal. When the SPIDC bit in the SPI Mode Select register is set, data transfer mode changes to a 3-byte operation: a chip select byte, an address/control byte, and a data byte. Using the circuit shown in Figure 18, a single device may select from the bank of devices by setting the appropriate chip select bit to 1. Each device uses the LSB of the chip select byte, shifts the data right by one bit, and passes the chip select byte using the SDITHRU pin to the next device in the chain. Address/control and data bytes are unaltered.

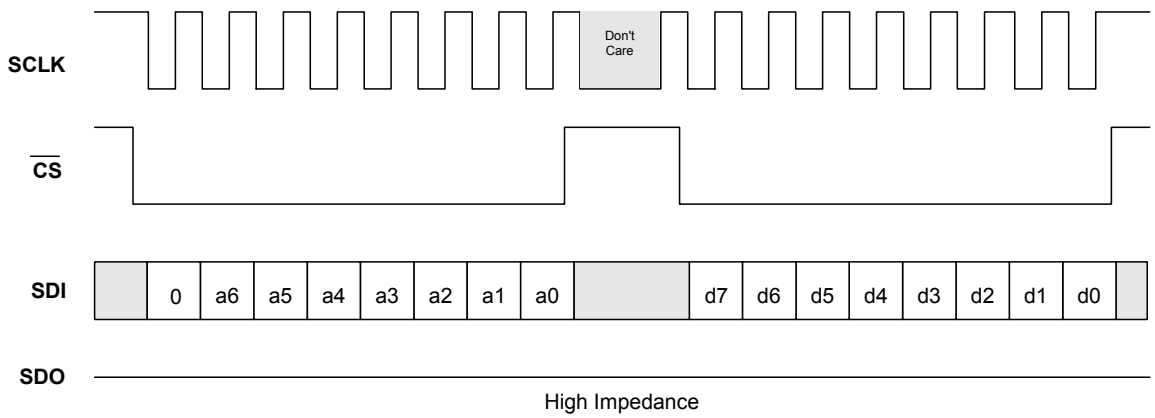


Figure 16. Serial Write 8-Bit Mode

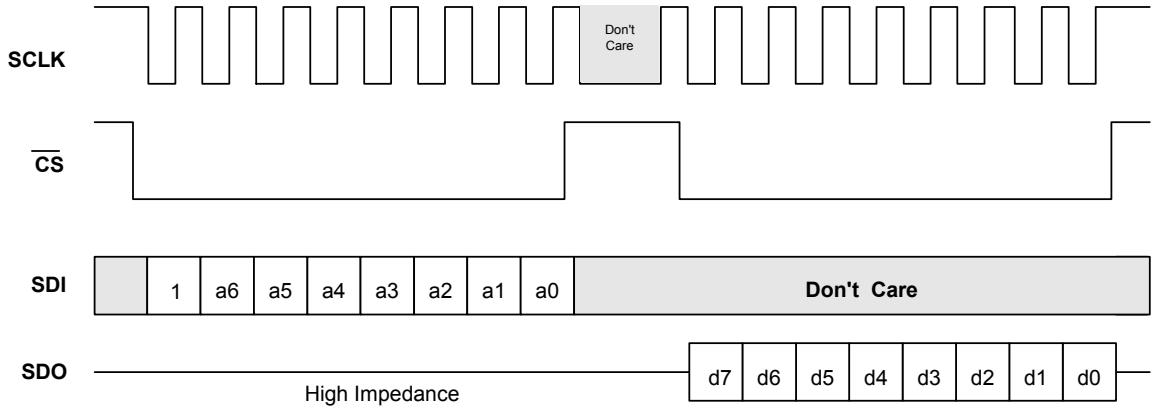
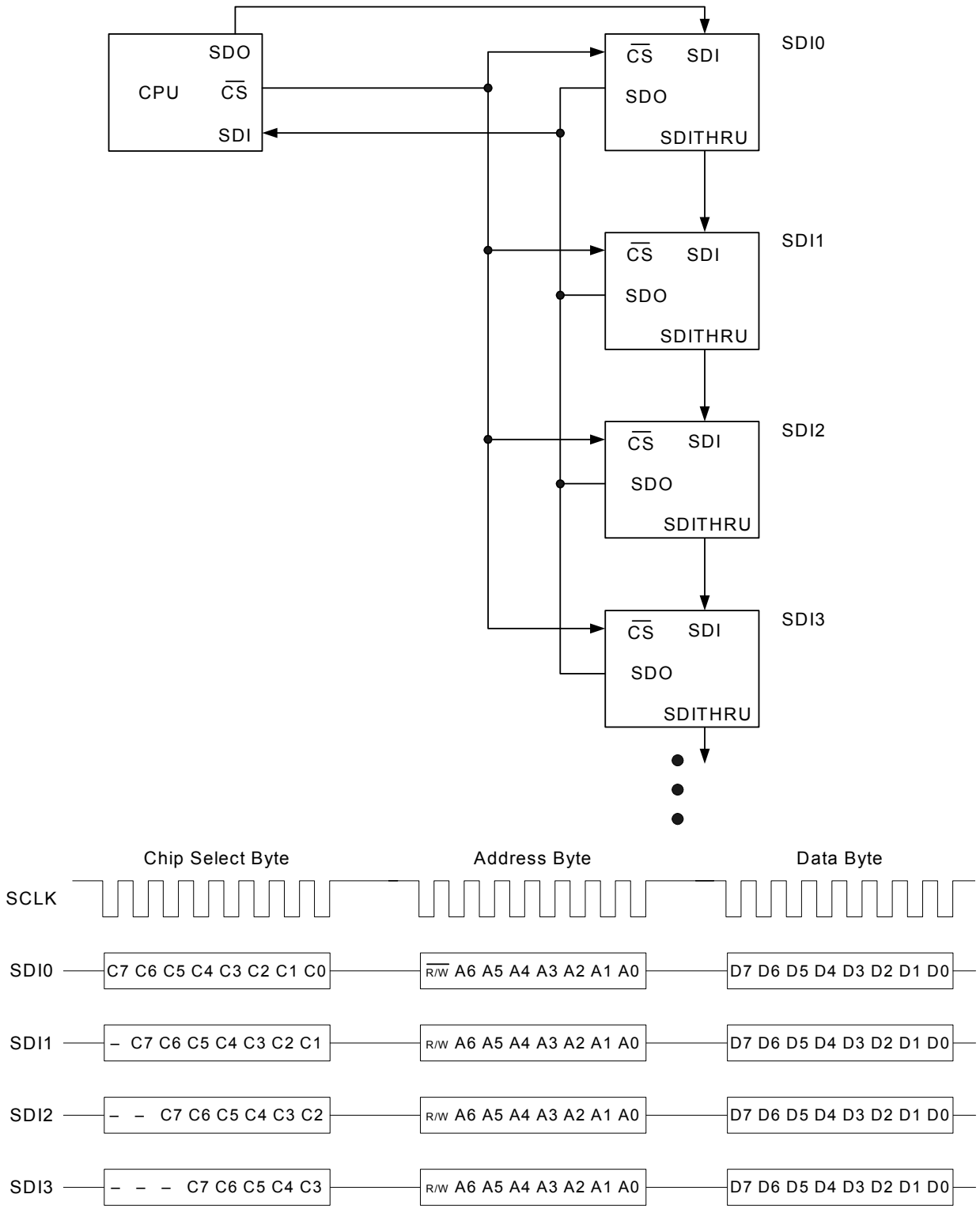


Figure 17. Serial Read 8-Bit Mode



Note: During chip select byte, SDITHRU = SDI delayed by one SCLK. Each device daisy-chained looks at the LSB of the chip select byte for its chip select.

Figure 18. SPI Daisy Chain Mode

3. Control Registers

Indirect registers are accessed through direct registers 28 through 31. Instructions on how to access them is described in “4. Indirect Registers” beginning on page 85.

Note: Any register not listed here is reserved and must not be written.

Table 29. Direct Register Summary

Register	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Setup									
0	SPI Mode Select	SPIDC	SPIM	PNI[1:0]		RNI[3:0]			
Audio									
9	Audio Gain Control							ARX[1:0]	
10	Two-Wire Impedance Synthesis Control			CLC[1:0]		TISE	TISS[2:0]		
11	Reserved								
Powerdown									
14	Power Down Control 1				DCOF	PFR		BIASOF	SLICOF
15	Power Down Control 2					DACM	DACON	GMM	GMON
Interrupts									
18	Interrupt Status 1	PMIP	PMAP	RGIP	RGAP	O2IP	O2AP	O1IP	O1AP
19	Interrupt Status 2	Q6AP	Q5AP	Q4AP	Q3AP	Q2AP	Q1AP	LCIP	RTIP
20	Interrupt Status 3						CMCP	INDP	DTMFP
21	Interrupt Enable 1	PMIE	PMAE	RGIE	RGAE	O2IE	O2AE	O1IE	O1AE
22	Interrupt Enable 2	Q6AE	Q5AE	Q4AE	Q3AE	Q2AE	Q1AE	LCIE	RTIE
23	Interrupt Enable 3						CMCE	INDE	DTMFE
Indirect Register Access									
28	Indirect Data Access—Low Byte	IDA[7:0]							
29	Indirect Data Access—High Byte	IDA[15:8]							
30	Indirect Address	IAA[7:0]							
31	Indirect Address Status								IAS
Oscillators									
32	Oscillator 1 Control	OSS1	REL	OZ1	O1TAE	O1TIE	O1E	O1SO[1:0]	
33	Oscillator 2 Control	OSS2		OZ2	O2TAE	O2TIE	O2E	O2SO[1:0]	
34	Ringing Oscillator Control	RSS		RDAC	RTAE	RTIE	ROE	RVO	TSWS
36	Oscillator 1 Active Timer—Low Byte	OATI[7:0]							
37	Oscillator 1 Active Timer—High Byte	OAT1[15:8]							

Table 29. Direct Register Summary (Continued)

Register	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
38	Oscillator 1 Inactive Timer—Low Byte	OIT1[7:0]							
39	Oscillator 1 Inactive Timer—High Byte	OIT1[15:8]							
40	Oscillator 2 Active Timer—Low Byte	OAT2[7:0]							
41	Oscillator 2 Active Timer—High Byte	OAT2[15:8]							
42	Oscillator 2 Inactive Timer—Low Byte	OIT2[7:0]							
43	Oscillator 2 Inactive Timer—High Byte	OIT2[15:8]							
48	Ringing Oscillator Active Timer—Low Byte	RAT[7:0]							
49	Ringing Oscillator Active Timer—High Byte	RAT[15:8]							
50	Ringing Oscillator Inactive Timer—Low Byte	RIT[7:0]							
51	Ringing Oscillator Inactive Timer—High Byte	RIT[15:8]							
52	FSK Data								FSKDAT
SLIC									
63	Loop Closure Debounce Interval for Automatic Ringing	LCD[7:0]							
64	Linefeed Control		LFS[2:0]				LF[2:0]		
65	External Bipolar Transistor Control		SQH	CBY	ETBE	ETBO[1:0]		ETBA[1:0]	
66	Battery Feed Control				VOV	FVBAT			TRACK
67	Automatic/Manual Control		MNCM	MNDIF	SPDS		AORD	AOLD	AOPN
68	Loop Closure/Ring Trip Detect Status						DBIRAW	RTP	LCR
69	Loop Closure Debounce Interval		LCDI[6:0]						
70	Ring Trip Detect Debounce Interval		RTDI[6:0]						
71	Loop Current Limit						ILIM[2:0]		
72	On-Hook Line Voltage		VSGN	VOC[5:0]					
73	Common Mode Voltage			VCM[5:0]					
74	High Battery Voltage			VBATH[5:0]					

Table 29. Direct Register Summary (Continued)

Register	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
75	Low Battery Voltage			VBATL[5:0]					
76	Power Monitor Pointer						PWRMP[2:0]		
77	Line Power Output Monitor	PWROM[7:0]							
78	Loop Voltage Sense		LVSP	LVS[5:0]					
79	Loop Current Sense		LCSP	LCS[5:0]					
80	TIP Voltage Sense	VTIP[7:0]							
81	RING Voltage Sense	VRING[7:0]							
82	Battery Voltage Sense 1	VBATS1[7:0]							
83	Battery Voltage Sense 2	VBATS2[7:0]							
84	Transistor 1 Current Sense	IQ1[7:0]							
85	Transistor 2 Current Sense	IQ2[7:0]							
86	Transistor 3 Current Sense	IQ3[7:0]							
87	Transistor 4 Current Sense	IQ4[7:0]							
88	Transistor 5 Current Sense	IQ5[7:0]							
89	Transistor 6 Current Sense	IQ6[7:0]							
92	DC-DC Converter PWM Period	DCN[7:0]							
93	DC-DC Converter Switching Delay	DCCAL		DCPOL	DCTOF[4:0]				
94	PWM Pulse Width	DCPW[7:0]							
95	Reserved								
96	Calibration Control/ Status Register 1		CAL	CALSP	CALR	CALT	CALD	CALC	CALIL
97	Calibration Control/ Status Register 2				CALM1	CALM2	CALDAC	CALADC	CALCM
98	RING Gain Mismatch Calibration Result				CALGMR[R4:0]				
99	TIP Gain Mismatch Calibration Result				CALGMT[4:0]				
100	Differential Loop Current Gain Calibration Result				CALGD[4:0]				

Table 29. Direct Register Summary (Continued)

Register	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
101	Common Mode Loop Current Gain Calibration Result				CALGC[4:0]				
102	Current Limit Calibration Result					CALGIL[3:0]			
103	Monitor ADC Offset Calibration Result	CALMG1[3:0]				CALMG2[3:0]			
104	Analog DAC/ADC Offset					DACP	DACN	ADCP	ADCN
105	DAC Offset Calibration Result	DACOF[7:0]							
106	Common Mode Balance Calibration Result			CMBAL[5:0]					
107	DC Peak Voltage Calibration Result					CMDCPK[3:0]			
108	Enhancement Enable	ILIMEN	FSKEN	DCSU			LCVE	DCFIL	HYSTEN

Register 0. SPI Mode Select

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	SPIDC	SPIM	PNI[1:0]		RNI[3:0]			
Type	R/W	R/W	R		R			

Reset settings = 00xx_xxxx

Bit	Name	Function
7	SPIDC	**SPI Daisy Chain Mode Enable.** 0 = Disable SPI daisy chain mode. 1 = Enable SPI daisy chain mode.
6	SPIM	**SPI Mode.** 0 = Causes SDO to tri-state on rising edge of SCLK of LSB. 1 = Normal operation; SDO tri-states on rising edge of $\overline{CS}$.
5:4	PNI[1:0]	**Part Number Identification.** 00 = Si3233 01 = Reserved 10 = Reserved 11 = Si3233M
3:0	RNI[3:0]	**Revision Number Identification.** 0001 = Revision A, 0010 = Revision B, 0011 = Revision C, etc.

Register 9. Audio Gain Control

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name							ARX[1:0]	
Type	R/W							

Reset settings = 0000_0000

Bit	Name	Function
7:2	Reserved	Read returns zero.
1:0	ARX[1:0]	**Analog Receive Path Gain.** 00 = 0 dB 01 = –3.5 dB 10 = 3.5 dB 11 = Mute **Note:** ARX affects internally generated audio signals only. Audio received on IGMN/IGMP pins is not impacted.

Register 10. Two-Wire Impedance Synthesis Control

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name			CLC[1:0]		TISE	TISS[2:0]		
Type	R/W				R/W	R/W		

Reset settings = 0000_1000

Bit	Name	Function
7:6	Reserved	Read returns zero.
5:4	CLC[1:0]	**Line Capacitance Compensation.** 00 = Off 01 = 4.7 nF 10 = 10 nF 11 = Reserved
3	TISE	**Two-Wire Impedance Synthesis Enable.** 0 = Two-wire impedance synthesis disabled. 1 = Two-wire impedance synthesis enabled.
2:0	TISS[2:0]	**Two-Wire Impedance Synthesis Selection.** 000 = 600 Ω 001 = 900 Ω 010 = Japan (600 Ω + 1 µF); requires R_{ZREF} = 12 kΩ and C3, C4 = 100 nF 011 = 900 Ω + 2.16 µF; requires R_{ZREF} = 18 kΩ and C3, C4 = 220 nF 100 = CTR21 270 Ω + (750 Ω || 150 nF) 101 = Australia/New Zealand 220 Ω + (820 Ω || 120 nF) 110 = Slovakia/Slovenia/South Africa 220 Ω + (820 Ω || 115 nF) 111 = China 200 Ω + (680 Ω || 100 nF)

Register 14. Power Down Control 1

Si3233								
Bit	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Name				DCOF	MOF		BIASOF	SLICOF
Type				R/W	R/W		R/W	R/W

Reset settings = 0001_0000

Bit	Name	Function
7:5	Reserved	Read returns zero.
4	DCOF	**DC-DC Converter Power-Off Control.** 0 = Automatic power control. 1 = Override automatic control and force dc-dc circuitry off.
3	PFR	**PLL Free-Run Control.** 0 = Normal operation. 1 = PLL free-run mode enabled.
2	Reserved	Read returns zero.
1	BIASOF	**DC Bias Power-Off Control.** 0 = Automatic power control. 1 = Override automatic control and force dc bias circuitry off.
0	SLICOF	**SLIC Power-Off Control.** 0 = Automatic power control. 1 = Override automatic control and force SLIC circuitry off.

Register 15. Power Down Control 2

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name					DACM	DACON	GMM	GMON
Type					R/W	R/W	R/W	R/W

Reset settings = 0000_0000

Bit	Name	Function
7:4	Reserved	Read returns zero.
3	DACM	**Digital to Analog Converter Manual/Automatic Power Control.** 0 = Automatic power control. 1 = Manual power control; DACON controls on/off state.
2	DACON	**Digital to Analog Converter On/Off Power Control.** When DACM = 1: 0 = Digital to analog converter powered off. 1 = Digital to analog converter powered on. DACON has no effect when DACM = 0.
1	GMM	**Transconductance Amplifier Manual/Automatic Power Control.** 0 = Automatic power control. 1 = Manual power control; GMON controls on/off state.
0	GMON	**Transconductance Amplifier On/Off Power Control.** When GMM = 1: 0 = Analog to digital converter powered off. 1 = Analog to digital converter powered on. GMON has no effect when GMM = 0.

Register 18. Interrupt Status 1

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name			RGIP	RGAP	O2IP	O2AP	O1IP	O1AP
Type			R/W	R/W	R/W	R/W	R/W	R/W

Reset settings = 0000_0000

Bit	Name	Function
7:6	Reserved	**Read returns zero.**
5	RGIP	**Ringing Inactive Timer Interrupt Pending.** Writing 1 to this bit clears a pending interrupt. 0 = No interrupt pending. 1 = Interrupt pending.
4	RGAP	**Ringing Active Timer Interrupt Pending.** Writing 1 to this bit clears a pending interrupt. 0 = No interrupt pending. 1 = Interrupt pending.
3	O2IP	**Oscillator 2 Inactive Timer Interrupt Pending.** Writing 1 to this bit clears a pending interrupt. 0 = No interrupt pending. 1 = Interrupt pending.
2	O2AP	**Oscillator 2 Active Timer Interrupt Pending.** Writing 1 to this bit clears a pending interrupt. 0 = No interrupt pending. 1 = Interrupt pending.
1	O1IP	**Oscillator 1 Inactive Timer Interrupt Pending.** Writing 1 to this bit clears a pending interrupt. 0 = No interrupt pending. 1 = Interrupt pending.
0	O1AP	**Oscillator 1 Active Timer Interrupt Pending.** Writing 1 to this bit clears a pending interrupt. 0 = No interrupt pending. 1 = Interrupt pending.

Register 19. Interrupt Status 2

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	Q6AP	Q5AP	Q4AP	Q3AP	Q2AP	Q1AP	LCIP	RTIP
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Reset settings = 0000_0000

Bit	Name	Function
7	Q6AP	**Power Alarm Q6 Interrupt Pending.** Writing 1 to this bit clears a pending interrupt. 0 = No interrupt pending. 1 = Interrupt pending.
6	Q5AP	**Power Alarm Q5 Interrupt Pending.** Writing 1 to this bit clears a pending interrupt. 0 = No interrupt pending. 1 = Interrupt pending.
5	Q4AP	**Power Alarm Q4 Interrupt Pending.** Writing 1 to this bit clears a pending interrupt. 0 = No interrupt pending. 1 = Interrupt pending.
4	Q3AP	**Power Alarm Q3 Interrupt Pending.** Writing 1 to this bit clears a pending interrupt. 0 = No interrupt pending. 1 = Interrupt pending.
3	Q2AP	**Power Alarm Q2 Interrupt Pending.** Writing 1 to this bit clears a pending interrupt. 0 = No interrupt pending. 1 = Interrupt pending.
2	Q1AP	**Power Alarm Q1 Interrupt Pending.** Writing 1 to this bit clears a pending interrupt. 0 = No interrupt pending. 1 = Interrupt pending.
1	LCIP	**Loop Closure Transition Interrupt Pending.** Writing 1 to this bit clears a pending interrupt. 0 = No interrupt pending. 1 = Interrupt pending.
0	RTIP	**Ring Trip Interrupt Pending.** Writing 1 to this bit clears a pending interrupt. 0 = No interrupt pending. 1 = Interrupt pending.

Register 20. Interrupt Status 3

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name							INDP	
Type	R/W							

Reset settings = 0000_0000

Bit	Name	Function
7:2	Reserved	Read returns zero.
1	INDP	**Indirect Register Access Serviced Interrupt.** This bit is set once a pending indirect register service request has been completed. Writing 1 to this bit clears a pending interrupt. 0 = No interrupt pending. 1 = Interrupt pending.
0	Reserved	Read returns zero.

Register 21. Interrupt Enable 1

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name			RGIE	RGAE	O2IE	O2AE	O1IE	O1AE
Type			R/W	R/W	R/W	R/W	R/W	R/W

Reset settings = 0000_0000

Bit	Name	Function
7:6	Reserved	Read returns zero.
5	RGIE	**Ringing Inactive Timer Interrupt Enable.** 0 = Interrupt masked. 1 = Interrupt enabled.
4	RGAE	**Ringing Active Timer Interrupt Enable.** 0 = Interrupt masked. 1 = Interrupt enabled.
3	O2IE	**Oscillator 2 Inactive Timer Interrupt Enable.** 0 = Interrupt masked. 1 = Interrupt enabled.
2	O2AE	**Oscillator 2 Active Timer Interrupt Enable.** 0 = Interrupt masked. 1 = Interrupt enabled.
1	O1IE	**Oscillator 1 Inactive Timer Interrupt Enable.** 0 = Interrupt masked. 1 = Interrupt enabled.
0	O1AE	**Oscillator 1 Active Timer Interrupt Enable.** 0 = Interrupt masked. 1 = Interrupt enabled.

Register 22. Interrupt Enable 2

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	Q6AE	Q5AE	Q4AE	Q3AE	Q2AE	Q1AE	LCIE	RTIE
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Reset settings = 0000_0000

Bit	Name	Function
7	Q6AE	**Power Alarm Q6 Interrupt Enable.** 0 = Interrupt masked. 1 = Interrupt enabled.
6	Q5AE	**Power Alarm Q5 Interrupt Enable.** 0 = Interrupt masked. 1 = Interrupt enabled.
5	Q4AE	**Power Alarm Q4 Interrupt Enable.** 0 = Interrupt masked. 1 = Interrupt enabled.
4	Q3AE	**Power Alarm Q3 Interrupt Enable.** 0 = Interrupt masked. 1 = Interrupt enabled.
3	Q2AE	**Power Alarm Q2 Interrupt Enable.** 0 = Interrupt masked. 1 = Interrupt enabled.
2	Q1AE	**Power Alarm Q1 Interrupt Enable.** 0 = Interrupt masked. 1 = Interrupt enabled.
1	LCIE	**Loop Closure Transition Interrupt Enable.** 0 = Interrupt masked. 1 = Interrupt enabled.
0	RTIE	**Ring Trip Interrupt Enable.** 0 = Interrupt masked. 1 = Interrupt enabled.

Register 23. Interrupt Enable 3

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name							INDE	
Type	R/W							

Reset settings = 0000_0000

Bit	Name	Function
7:2	Reserved	Read returns zero.
1	INDE	**Indirect Register Access Serviced Interrupt Enable.** 0 = Interrupt masked. 1 = Interrupt enabled.
0	Reserved	Read returns zero.

Register 28. Indirect Data Access—Low Byte

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	IDA[7:0]							
Type	R/W							

Reset settings = 0000_0000

Bit	Name	Function
7:0	IDA[7:0]	**Indirect Data Access—Low Byte.** A write to IDA followed by a write to IAA will place the contents of IDA into an indirect register at the location referenced by IAA at the next indirect register update (16 kHz update rate—a write operation). Writing IAA only will load IDA with the value stored at IAA at the next indirect memory update (a read operation).

Register 29. Indirect Data Access—High Byte

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	IDA[15:8]							
Type	R/W							

Reset settings = 0000_0000

Bit	Name	Function
7:0	IDA[15:8]	**Indirect Data Access—High Byte.** A write to IDA followed by a write to IAA will place the contents of IDA into an indirect register at the location referenced by IAA at the next indirect register update (16 kHz update rate—a write operation). Writing IAA only will load IDA with the value stored at IAA at the next indirect memory update (a read operation).

Register 30. Indirect Address

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	IAA[7:0]							
Type	R/W							

Reset settings = xxxx_xxxx

Bit	Name	Function
7:0	IAA[7:0]	**Indirect Address Access.** A write to IDA followed by a write to IAA will place the contents of IDA into an indirect register at the location referenced by IAA at the next indirect register update (16 kHz update rate—a write operation). Writing IAA only will load IDA with the value stored at IAA at the next indirect memory update (a read operation).

Register 31. Indirect Address Status

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name								IAS
Type								R

Reset settings = 0000_0000

Bit	Name	Function
7:1	Reserved	Read returns zero.
0	IAS	**Indirect Access Status.** 0 = No indirect memory access pending. 1 = Indirect memory access pending.

Register 32. Oscillator 1 Control

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	OSS1	REL	OZ1	O1TAE	O1TIE	O1E	O1SO[1:0]	
Type	R	R/W	R/W	R/W	R/W	R/W	R/W	

Reset settings = 0000_0000

Bit	Name	Function
7	OSS1	**Oscillator 1 Signal Status.** 0 = Output signal inactive. 1 = Output signal active.
6	REL	**Oscillator 1 Automatic Register Reload.** This bit should be set for FSK signaling. 0 = Oscillator 1 will stop signaling after inactive timer expires. 1 = Oscillator 1 will continue to read register parameters and output signals.
5	OZ1	**Oscillator 1 Zero Cross Enable.** 0 = Signal terminates after active timer expires. 1 = Signal terminates at zero crossing after active timer expires.
4	O1TAE	**Oscillator 1 Active Timer Enable.** 0 = Disable timer. 1 = Enable timer.
3	O1TIE	**Oscillator 1 Inactive Timer Enable.** 0 = Disable timer. 1 = Enable timer.
2	O1E	**Oscillator 1 Enable.** 0 = Disable oscillator. 1 = Enable oscillator.
1:0	O1SO[1:0]	**Oscillator 1 Signal Output Routing.** 00 = Unassigned path (output not connected). 01 = Assign to transmit path. 10 = Assign to receive path. 11 = Assign to both paths.

Register 33. Oscillator 2 Control

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	OSS2		OZ2	O2TAE	O2TIE	O2E	O2SO[1:0]	
Type	R		R/W	R/W	R/W	R/W	R/W	

Reset settings = 0000_0000

Bit	Name	Function
7	OSS2	**Oscillator 2 Signal Status.** 0 = Output signal inactive. 1 = Output signal active.
6	Reserved	Read returns zero.
5	OZ2	**Oscillator 2 Zero Cross Enable.** 0 = Signal terminates after active timer expires. 1 = Signal terminates at zero crossing.
4	O2TAE	**Oscillator 2 Active Timer Enable.** 0 = Disable timer. 1 = Enable timer.
3	O2TIE	**Oscillator 2 Inactive Timer Enable.** 0 = Disable timer. 1 = Enable timer.
2	O2E	**Oscillator 2 Enable.** 0 = Disable oscillator. 1 = Enable oscillator.
1:0	O2SO[1:0]	**Oscillator 2 Signal Output Routing.** 00 = Unassigned path (output not connected) 01 = Assign to transmit path. 10 = Assign to receive path. 11 = Assign to both paths.

Register 34. Ringing Oscillator Control

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	RSS		RDAC	RTAE	RTIE	ROE	RVO	TSWS
Type	R		R	R/W	R/W	R	R/W	R/W

Reset settings = 0000_0000

Bit	Name	Function
7	RSS	**Ringing Signal Status.** 0 = Ringing oscillator output signal inactive. 1 = Ringing oscillator output signal active.
6	Reserved	Read returns zero.
5	RDAC	**Ringing Signal DAC/Linefeed Cross Indicator.** For ringing signal start and stop, output to TIP and RING is suspended to ensure continuity with dc linefeed voltages. RDAC indicates that ringing signal is actually present at TIP and RING. 0 = Ringing signal not present at TIP and RING. 1 = Ringing signal present at TIP and RING.
4	RTAE	**Ringing Active Timer Enable.** 0 = Disable timer. 1 = Enable timer.
3	RTIE	**Ringing Inactive Timer Enable.** 0 = Disable timer. 1 = Enable timer.
2	ROE	**Ringing Oscillator Enable.** 0 = Ringing oscillator disabled. 1 = Ringing oscillator enabled.
1	RVO	**Ringing Voltage Offset.** 0 = No dc offset added to ringing signal. 1 = DC offset added to ringing signal.
0	TSWS	**Trapezoid/Sinusoid Waveshape Select.** 0 = Sinusoid 1 = Trapezoid

Register 36. Oscillator 1 Active Timer—Low Byte

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	OAT1[7:0]							
Type	R/W							

Reset settings = 0000_0000

Bit	Name	Function
7:0	OAT1[7:0]	**Oscillator 1 Active Timer.** LSB = 125 μs

Register 37. Oscillator 1 Active Timer—High Byte

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	OAT1[15:8]							
Type	R/W							

Reset settings = 0000_0000

Bit	Name	Function
7:0	OAT1[15:8]	**Oscillator 1 Active Timer.**

Register 38. Oscillator 1 Inactive Timer—Low Byte

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	OIT1[7:0]							
Type	R/W							

Reset settings = 0000_0000

Bit	Name	Function
7:0	OIT1[7:0]	**Oscillator 1 Inactive Timer.** LSB = 125 μs

Register 39. Oscillator 1 Inactive Timer—High Byte

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	OIT1[15:8]							
Type	R/W							

Reset settings = 0000_0000

Bit	Name	Function
7:0	OIT1[15:8]	**Oscillator 1 Inactive Timer.**

Register 40. Oscillator 2 Active Timer—Low Byte

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	OAT2[7:0]							
Type	R/W							

Reset settings = 0000_0000

Bit	Name	Function
7:0	OAT2[7:0]	**Oscillator 2 Active Timer.** LSB = 125 μs

Register 41. Oscillator 2 Active Timer—High Byte

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	OAT2[15:8]							
Type	R/W							

Reset settings = 0000_0000

Bit	Name	Function
7:0	OAT2[15:8]	**Oscillator 2 Active Timer.**

Register 42. Oscillator 2 Inactive Timer—Low Byte

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	OIT2[7:0]							
Type	R/W							

Reset settings = 0000_0000

Bit	Name	Function
7:0	OIT2[7:0]	**Oscillator 2 Inactive Timer.** LSB = 125 μs

Register 43. Oscillator 2 Inactive Timer—High Byte

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	OIT2[15:8]							
Type	R/W							

Reset settings = 0000_0000

Bit	Name	Function
7:0	OIT2[15:8]	**Oscillator 2 Inactive Timer.**

Register 48. Ringing Oscillator Active Timer—Low Byte

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	RAT[7:0]							
Type	R/W							

Reset settings = 0000_0000

Bit	Name	Function
7:0	RAT[7:0]	**Ringing Active Timer.** LSB = 125 μs

Register 49. Ringing Oscillator Active Timer—High Byte

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	RAT[15:8]							
Type	R/W							

Reset settings = 0000_0000

Bit	Name	Function
7:0	RAT[15:8]	**Ringing Active Timer.**

Register 50. Ringing Oscillator Inactive Timer—Low Byte

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	RIT[7:0]							
Type	R/W							

Reset settings = 0000_0000

Bit	Name	Function
7:0	RIT[7:0]	**Ringing Inactive Timer.** LSB = 125 μs

Register 51. Ringing Oscillator Inactive Timer—High Byte

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	RIT[15:8]							
Type	R/W							

Reset settings = 0000_0000

Bit	Name	Function
7:0	RIT[15:8]	**Ringing Inactive Timer.**

Register 52. FSK Data

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name								FSKDAT
Type								R/W

Reset settings = 0000_0000

Bit	Name	Function
7:1	Reserved	Read returns zero.
0	FSKDAT	**FSK Data.** When FSKEN = 1 (direct Register 108, bit 6) and REL = 1 (direct Register 32, bit 6), this bit serves as the buffered input for FSK generation bit stream data.

Register 63. Loop Closure Debounce Interval

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	LCD[7:0]							
Type	R/W							

Reset settings = 0011_0010 (revision C); 0101_0100 (subsequent revisions)

Bit	Name	Function
7:0	LCD[7:0]	**Loop Closure Debounce Interval for Automatic Ringing.** This register sets the loop closure debounce interval for the ringing silent period when using automatic ringing cadences. The value may be set between 0 ms (0x00) and 159 ms (0x7F) in 1.25 ms steps.

Register 64. Linefeed Control

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name		LFS[2:0]				LF[2:0]		
Type	R					R/W		

Reset settings = 0000_0000

Bit	Name	Function
7	Reserved	Read returns zero.
6:4	LFS[2:0]	**Linefeed Shadow.** This register reflects the actual realtime linefeed state. Automatic operations may cause actual linefeed state to deviate from the state defined by linefeed register (e.g., when linefeed equals ringing state, LFS will equal on-hook transmission state during ringing silent period and ringing state during ring burst). 000 = Open 001 = Forward active 010 = Forward on-hook transmission 011 = TIP open 100 = Ringing 101 = Reverse active 110 = Reverse on-hook transmission 111 = RING open
3	Reserved	Read returns zero.
2:0	LF[2:0]	**Linefeed.** Writing to this register sets the linefeed state. 000 = Open 001 = Forward active 010 = Forward on-hook transmission 011 = TIP open 100 = Ringing 101 = Reverse active 110 = Reverse on-hook transmission 111 = RING open

Register 65. External Bipolar Transistor Control

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name		SQH	CBY	ETBE	ETBO[1:0]		ETBA[1:0]	
Type		R/W	R/W	R/W	R/W		R/W	

Reset settings = 0110_0001

Bit	Name	Function
7	Reserved	Read returns zero.
6	SQH	**Audio Squelch.** 0 = No squelch. 1 = STIPAC and SRINGAC pins squelched.
5	CBY	**Capacitor Bypass.** 0 = Capacitors CP (C1) and CM (C2) in circuit. 1 = Capacitors CP (C1) and CM (C2) bypassed.
4	ETBE	**External Transistor Bias Enable.** 0 = Bias disabled. 1 = Bias enabled.
3:2	ETBO[1:0]	**External Transistor Bias Levels—On-Hook Transmission State.** DC bias current which flows through external BJTs in the on-hook transmission state. Increasing this value increases the compliance of the ac longitudinal balance circuit. 00 = 4 mA 01 = 8 mA 10 = 12 mA 11 = Reserved
1:0	ETBA[1:0]	**External Transistor Bias Levels—Active Off-Hook State.** DC bias current which flows through external BJTs in the active off-hook state. Increasing this value increases the compliance of the ac longitudinal balance circuit. 00 = 4 mA 01 = 8 mA 10 = 12 mA 11 = Reserved

Register 66. Battery Feed Control

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name				VOV	FVBAT			TRACK
Type				R/W	R/W			R/W

Reset settings = 0000_0011

Bit	Name	Function
7:5	Reserved	Read returns zero.
4	VOV	**Overhead Voltage Range Increase.** This bit selects the programmable range for V_{OV}, which is defined in indirect Register 41. 0 = V_{OV} = 0 V to 9 V 1 = V_{OV} = 0 V to 13.5 V
3	FVBAT	**V_{BAT} Manual Setting.** 0 = Normal operation 1 = V_{BAT} tracks VBATH register.
2:1	Reserved	Read returns zero.
0	TRACK	**DC-DC Converter Tracking Mode.** 0 = $\|V_{BAT}\|$ will not decrease below VBATL. 1 = V_{BAT} tracks V_{RING}.

Register 67. Automatic/Manual Control

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name		MNCM	MNDIF	SPDS		AORD	AOLD	AOPN
Type		R/W	R/W	R/W		R/W	R/W	R/W

Reset settings = 0001_1111

Bit	Name	Function
7	Reserved	Read returns zero.
6	MNCM	**Common Mode Manual/Automatic Select.** 0 = Automatic control. 1 = Manual control, in which TIP (forward) or RING (reverse) forces voltage to follow VCM value.
5	MNDIF	**Differential Mode Manual/Automatic Select.** 0 = Automatic control. 1 = Manual control (forces differential voltage to follow VOC value).
4	SPDS	**Speed-Up Mode Enable.** 0 = Speed-up disabled. 1 = Automatic speed-up.
3	Reserved	Read returns zero.
2	AORD	**Automatic/Manual Ring Trip Detect.** 0 = Manual mode. 1 = Enter off-hook active state automatically upon ring trip detect.
1	AOLD	**Automatic/Manual Loop Closure Detect.** 0 = Manual mode. 1 = Enter off-hook active state automatically upon loop closure detect.
0	AOPN	**Power Alarm Automatic/Manual Detect.** 0 = Manual mode. 1 = Enter open state automatically upon power alarm.

Register 68. Loop Closure/Ring Trip Detect Status

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name						DBIRAW	RTP	LCR
Type						R	R	R

Reset settings = 0000_0000

Bit	Name	Function
7:3	Reserved	Read returns zero.
2	DBIRAW	**Ring Trip/Loop Closure Unfiltered Output.** State of this bit reflects the realtime output of ring trip and loop closure detect circuits before debouncing. 0 = Ring trip/loop closure threshold exceeded. 1 = Ring trip/loop closure threshold not exceeded.
1	RTP	**Ring Trip Detect Indicator (Filtered Output).** 0 = Ring trip detect has not occurred. 1 = Ring trip detect occurred.
0	LCR	**Loop Closure Detect Indicator (Filtered Output).** 0 = Loop closure detect has not occurred. 1 = Loop closure detect has occurred.

Register 69. Loop Closure Debounce Interval

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name		LCDI[6:0]						
Type	R/W							

Reset settings = 0000_1010

Bit	Name	Function
7	Reserved	Read returns zero.
6:0	LCDI[6:0]	**Loop Closure Debounce Interval.** The value written to this register defines the minimum steady state debounce time. Value may be set between 0 ms (0x00) to 159 ms (0x7F) in 1.25 ms steps. Default value = 12.5 ms.

Register 70. Ring Trip Detect Debounce Interval

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name		RTDI[6:0]						
Type	R/W							

Reset settings = 0000_1010

Bit	Name	Function
7	Reserved	Read returns zero.
6:0	RTDI[6:0]	**Ring Trip Detect Debounce Interval.** The value written to this register defines the minimum steady state debounce time. The value may be set between 0 ms (0x00) to 159 ms (0x7F) in 1.25 ms steps. Default value = 12.5 ms.

Register 71. Loop Current Limit

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name						ILIM[2:0]		
Type	R/W							

Reset settings = 0000_0000

Bit	Name	Function
7:3	Reserved	Read returns zero.
2:0	ILIM[2:0]	**Loop Current Limit.** The value written to this register sets the constant loop current. The value may be set between 20 mA (0x00) and 41 mA (0x07) in 3 mA steps.

Register 72. On-Hook Line Voltage

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name		VSGN	VOC[5:0]					
Type	R/W		R/W					

Reset settings = 0010_0000

Bit	Name	Function
7	Reserved	Read returns zero.
6	VSGN	**On-Hook Line Voltage.** The value written to this bit sets the on-hook line voltage polarity (V_{TIP}–V_{RING}). 0 = V_{TIP}–$V_{RING}$is positive 1 = V_{TIP}–V_{RING} is negative
5:0	VOC[5:0]	**On-Hook Line Voltage.** The value written to this register sets the on-hook line voltage (V_{TIP}–V_{RING}). Value may be set between 0 V (0x00) and 94.5 V (0x3F) in 1.5 V steps. Default value = 48 V.

Register 73. Common Mode Voltage

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name			VCM[5:0]					
Type	R/W							

Reset settings = 0000_0010

Bit	Name	Function
7:6	Reserved	Read returns zero.
5:0	VCM[5:0]	**Common Mode Voltage.** The value written to this register sets V_{TIP} for forward active and forward on-hook transmission states and V_{RING} for reverse active and reverse on-hook transmission states. The value may be set between 0 V (0x00) and –94.5 V (0x3F) in 1.5 V steps. Default value = –3 V.

Register 74. High Battery Voltage

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name			VBATH[5:0]					
Type	R/W							

Reset settings = 0011_0010

Bit	Name	Function
7:6	Reserved	Read returns zero.
5:0	VBATH[5:0]	**High Battery Voltage.** The value written to this register sets high battery voltage. VBATH must be greater than or equal to VBATL. The value may be set between 0 V (0x00) and –94.5 V (0x3F) in 1.5 V steps. Default value = –75 V.

Register 75. Low Battery Voltage

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name			VBATL[5:0]					
Type	R/W							

Reset settings = 0001_0000

Bit	Name	Function
7:6	Reserved	Read returns zero.
5:0	VBATL[5:0]	**Low Battery Voltage.** The value written to this register sets low battery voltage. VBATH must be greater than or equal to VBATL. The value may be set between 0 V (0x00) and –94.5 V (0x3F) in 1.5 V steps. Default value = –24 V.

Register 76. Power Monitor Pointer

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name						PWRMP[2:0]		
Type	R/W							

Reset settings = 0000_0000

Bit	Name	Function
7:3	Reserved	Read returns zero.
2:0	PWRMP[2:0]	**Power Monitor Pointer.** Selects the external transistor from which to read power output. The power of the selected transistor is read in the PWROM register. 000 = Q1 001 = Q2 010 = Q3 011 = Q4 100 = Q5 101 = Q6 110 = Undefined 111 = Undefined

Register 77. Line Power Output Monitor

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	PWROM[7:0]							
Type	R							

Reset settings = 0000_0000

Bit	Name	Function
7:0	PWROM[7:0]	**Line Power Output Monitor.** This register reports the realtime power output of the transistor selected using PWRMP. The range is 0 W (0x00) to 7.8 W (0xFF) in 30.4 mW steps for Q1, Q2, Q5, and Q6. The range is 0 W (0x00) to 0.9 W (0xFF) in 3.62 mW steps for Q3 and Q4.

Register 78. Loop Voltage Sense

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name		LVSP	LVS[5:0]					
Type	R		R					

Reset settings = 0000_0000

Bit	Name	Function
7	Reserved	Read returns zero.
6	LVSP	**Loop Voltage Sense Polarity.** This register reports the polarity of the differential loop voltage ($V_{TIP} - V_{RING}$). 0 = Positive loop voltage ($V_{TIP} > V_{RING}$). 1 = Negative loop voltage ($V_{TIP} < V_{RING}$).
5:0	LVS[5:0]	**Loop Voltage Sense Magnitude.** This register reports the magnitude of the differential loop voltage ($V_{TIP}–V_{RING}$). The range is 0 V to 94.5 V in 1.5 V steps.

Register 79. Loop Current Sense

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name		LCSP	LCS[5:0]					
Type	R		R					

Reset settings = 0000_0000

Bit	Name	Function
7	Reserved	Read returns zero.
6	LCSP	**Loop Current Sense Polarity.** This register reports the polarity of the loop current. 0 = Positive loop current (forward direction). 1 = Negative loop current (reverse direction).
5:0	LCS[5:0]	**Loop Current Sense Magnitude.** This register reports the magnitude of the loop current. The range is 0 mA to 78.75 mA in 1.25 mA steps.

Register 80. TIP Voltage Sense

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	VTIP[7:0]							
Type	R							

Reset settings = 0000_0000

Bit	Name	Function
7:0	VTIP[7:0]	**TIP Voltage Sense.** This register reports the realtime voltage at TIP with respect to ground. The range is 0 V (0x00) to –95.88 V (0xFF) in .376 V steps.

Register 81. RING Voltage Sense

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	VRING[7:0]							
Type	R							

Reset settings = 0000_0000

Bit	Name	Function
7:0	VRING[7:0]	**RING Voltage Sense.** This register reports the realtime voltage at RING with respect to ground. The range is 0 V (0x00) to –95.88 V (0xFF) in .376 V steps.

Register 82. Battery Voltage Sense 1

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	VBATS1[7:0]							
Type	R							

Reset settings = 0000_0000

Bit	Name	Function
7:0	VBATS1[7:0]	**Battery Voltage Sense 1.** This register is one of two registers that reports the realtime voltage at V_{BAT} with respect to ground. The range is 0 V (0x00) to –95.88 V (0xFF) in .376 V steps.

Register 83. Battery Voltage Sense 2

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	VBATS2[7:0]							
Type	R							

Reset settings = 0000_0000

Bit	Name	Function
7:0	VBATS2[7:0]	**Battery Voltage Sense 2.** This register is one of two registers that reports the realtime voltage at V_{BAT} with respect to ground. The range is 0 V (0x00) to –95.88 V (0xFF) in .376 V steps.

Register 84. Transistor 1 Current Sense

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	IQ1[7:0]							
Type	R							

Reset settings = xxxx_xxxx

Bit	Name	Function
7:0	IQ1[7:0]	**Transistor 1 Current Sense.** This register reports the realtime current through Q1. The range is 0 A (0x00) to 81.35 mA (0xFF) in .319 mA steps. If ETBE = 1, the reported value does not include the additional ETBO/A current.

Register 85. Transistor 2 Current Sense

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	IQ2[7:0]							
Type	R							

Reset settings = xxxx_xxxx

Bit	Name	Function
7:0	IQ2[7:0]	**Transistor 2 Current Sense.** This register reports the realtime current through Q2. The range is 0 A (0x00) to 81.35 mA (0xFF) in .319 mA steps. If ETBE = 1, the reported value does not include the additional ETBO/A current.

Register 86. Transistor 3 Current Sense

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	IQ3[7:0]							
Type	R							

Reset settings = xxxx_xxxx

Bit	Name	Function
7:0	IQ3[7:0]	**Transistor 3 Current Sense.** This register reports the realtime current through Q3. The range is 0 A (0x00) to 9.59 mA (0xFF) in 37.6 μA steps.

Register 87. Transistor 4 Current Sense

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	IQ4[7:0]							
Type	R							

Reset settings = xxxx_xxxx

Bit	Name	Function
7:0	IQ4[7:0]	**Transistor 4 Current Sense.** This register reports the realtime current through Q4. The range is 0 A (0x00) to 9.59 mA (0xFF) in 37.6 μA steps.

Register 88. Transistor 5 Current Sense

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	IQ5[7:0]							
Type	R							

Reset settings = xxxx_xxxx

Bit	Name	Function
7:0	IQ5[7:0]	**Transistor 5 Current Sense.** This register reports the realtime current through Q5. The range is 0 A (0x00) to 80.58 mA (0xFF) in .316 mA steps.

Register 89. Transistor 6 Current Sense

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	IQ6[7:0]							
Type	R							

Reset settings = xxxx_xxxx

Bit	Name	Function
7:0	IQ6[7:0]	**Transistor 6 Current Sense.** This register reports the realtime current through Q6. The range is 0 A (0x00) to 80.58 mA (0xFF) in .316 mA steps.

Register 92. DC-DC Converter PWM Period

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	DCN[7]	1	DCN[5:0]					
Type	R/W	R	R/W					

Reset settings = 1111_1111

Bit	Name	Function
7:0	DCN[7:0]	**DC-DC Converter Period.** This bit sets the PWM period for the dc-dc converter. The range is 3.906 µs (0x40) to 15.564 µs (0xFF) in 61.035 ns steps. Bit 6 is fixed to one and read-only, so there are two ranges of operation: 3.906 µs–7.751 µs, used for MOSFET transistor switching. 11.719 µs–15.564 µs, used for BJT transistor switching.

Register 93. DC-DC Converter Switching Delay

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	DCCAL		DCPOL	DCTOF[4:0]				
Type	R/W		R	R/W				

Reset settings = 0001_0100 (Si3233)

Reset settings = 0011_0100 (Si3233M)

Bit	Name	Function
7	DCCAL	**DC-DC Converter Peak Current Monitor Calibration Status.** Writing a one to this bit starts the dc-dc converter peak current monitor calibration routine. 0 = Normal operation. 1 = Calibration being performed.
6	Reserved	Read returns zero.
5	DCPOL	**DC-DC Converter Feed Forward Pin (DCFF) Polarity.** This read-only register bit indicates the polarity relationship of the DCFF pin to the DCDRV pin. Two versions of the Si3233 are offered to support the two relationships. 0 = DCFF pin polarity is opposite of DCDRV pin (Si3233). 1 = DCFF pin polarity is same as DCDRV pin (Si3233M).
4:0	DCTOF[4:0]	**DC-DC Converter Minimum Off Time.** This register sets the minimum off time for the pulse width modulated dc-dc converter control. T_{OFF} = (DCTOF + 4) x 61.035 ns.

Register 94. DC-DC Converter PWM Pulse Width

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	DCPW[7:0]							
Type	R							

Reset settings = 0000_0000

Bit	Name	Function
7:0	DCPW[7:0]	**DC-DC Converter Pulse Width.** Pulse width of DCDRV is given by PW = (DCPW – DCTOF – 4) x 61.035 ns.

Register 96. Calibration Control/Status Register 1

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name		CAL	CALSP	CALR	CALT	CALD	CALC	CALIL
Type		R/W	R/W	R/W	R/W	R/W	R/W	R/W

Reset settings = 0001_1111

Bit	Name	Function
7	Reserved	Read returns zero.
6	CAL	**Calibration Control/Status Bit.** Setting this bit begins calibration of the entire system. 0 = Normal operation or calibration complete. 1 = Calibration in progress.
5	CALSP	**Calibration Speedup.** Setting this bit shortens the time allotted for V_{BAT} settling at the beginning of the calibration cycle. 0 = 300 ms 1 = 30 ms
4	CALR	**RING Gain Mismatch Calibration.** 0 = Normal operation or calibration complete. 1 = Calibration enabled or in progress.
3	CALT	**TIP Gain Mismatch Calibration.** 0 = Normal operation or calibration complete. 1 = Calibration enabled or in progress.
2	CALD	**Differential DAC Gain Calibration.** 0 = Normal operation or calibration complete. 1 = Calibration enabled or in progress.
1	CALC	**Common Mode DAC Gain Calibration.** 0 = Normal operation or calibration complete. 1 = Calibration enabled or in progress.
0	CALIL	**I_{LIM} Calibration.** 0 = Normal operation or calibration complete. 1 = Calibration enabled or in progress.

Register 97. Calibration Control/Status Register 2

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name				CALM1	CALM2	CALDAC	CALADC	CALCM
Type				R/W	R/W	R/W	R/W	R/W

Reset settings = 0001_1111

Bit	Name	Function
7:5	Reserved	Read returns zero.
4	CALM1	**Monitor ADC Calibration 1.** 0 = Normal operation or calibration complete. 1 = Calibration enabled or in progress.
3	CALM2	**Monitor ADC Calibration 2.** 0 = Normal operation or calibration complete. 1 = Calibration enabled or in progress.
2	CALDAC	**DAC Calibration.** Setting this bit begins calibration of the audio DAC offset. 0 = Normal operation or calibration complete. 1 = Calibration enabled or in progress.
1	CALADC	**ADC Calibration.** Setting this bit begins calibration of the audio ADC offset. 0 = Normal operation or calibration complete. 1 = Calibration enabled or in progress.
0	CALCM	**Common Mode Balance Calibration.** Setting this bit begins calibration of the ac longitudinal balance. 0 = Normal operation or calibration complete. 1 = Calibration enabled or in progress.

Register 98. RING Gain Mismatch Calibration Result

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name				CALGMR[4:0]				
Type	R/W							

Reset settings = 0001_0000

Bit	Name	Function
7:5	Reserved	Read returns zero.
4:0	CALGMR[4:0]	**Gain Mismatch of IE Tracking Loop for RING Current.**

Register 99. TIP Gain Mismatch Calibration Result

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name				CALGMT[4:0]				
Type	R/W							

Reset settings = 0001_0000

Bit	Name	Function
7:5	Reserved	Read returns zero.
4:0	CALGMT[4:0]	**Gain Mismatch of IE Tracking Loop for TIP Current.**

Register 100. Differential Loop Current Gain Calibration Result

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name				CALGD[4:0]				
Type	R/W							

Reset settings = 0001_0001

Bit	Name	Function
7:5	Reserved	Read returns zero.
4:0	CALGD[4:0]	**Differential DAC Gain Calibration Result.**

Register 101. Common Mode Loop Current Gain Calibration Result

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name				CALGC[4:0]				
Type	R/W							

Reset settings = 0001_0001

Bit	Name	Function
7:5	Reserved	Read returns zero.
4:0	CALGC[4:0]	**Common Mode DAC Gain Calibration Result.**

Register 102. Current Limit Calibration Result

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name					CALGIL[3:0]			
Type	R/W							

Reset settings = 0000_1000

Bit	Name	Function
7:5	Reserved	Read returns zero.
3:0	CALGIL[3:0]	**Current Limit Calibration Result.**

Register 103. Monitor ADC Offset Calibration Result

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	CALMG1[3:0]				CALMG2[3:0]			
Type	R/W				R/W			

Reset settings = 1000_1000

Bit	Name	Function
7:4	CALMG1[3:0]	**Monitor ADC Offset Calibration Result 1.**
3:0	CALMG2[3:0]	**Monitor ADC Offset Calibration Result 2.**

Register 104. Analog DAC/ADC Offset

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name					DACP	DACN	ADCP	ADCN
Type					R/W	R/W	R/W	R/W

Reset settings = 0000_0000

Bit	Name	Function
7:4	Reserved	Read returns zero.
3	DACP	**Positive Analog DAC Offset.**
2	DACN	**Negative Analog DAC Offset.**
1	ADCP	**Positive Analog ADC Offset.**
0	ADCN	**Negative Analog ADC Offset.**

Register 105. DAC Offset Calibration Result

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	DACOF[7:0]							
Type	R/W							

Reset settings = 0000_0000

Bit	Name	Function
7:0	DACOF[7:0]	**DAC Offset Calibration Result.**

Register 106. Common Mode Calibration Result

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name			CMBAL[5:0]					
Type	R/W							

Reset settings = 0010_0000

Bit	Name	Function
7:6	Reserved	Read returns zero.
5:0	CMBAL[5:0]	**Common Mode Calibration Result.**

Register 107. DC Peak Current Monitor Calibration Result

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name					CMDCPK[3:0]			
Type	R/W							

Reset settings = 0000_1000

Bit	Name	Function
7:4	Reserved	Read returns zero.
3:0	CMDCPK[3:0]	**DC Peak Current Monitor Calibration Result.**

Register 108. Enhancement Enable

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	ILIMEN	FSKEN	DCSU			LCVE	DCFIL	HYSTEN
Type	R/W	R/W	R/W			R/W	R/W	R/W

Reset settings = 0000_0000

Bit	Name	Function
7	ILIMEN	**Current Limit Increase.** When enabled, this bit temporarily increases the maximum differential current limit at the end of a ring burst to enable a faster settling time to a dc linefeed state. 0 = The value programmed in ILIM (direct Register 71) is used. 1 = The maximum differential loop current limit is temporarily increased to 41 mA.
6	FSKEN	**FSK Generation Enhancement.** When enabled, this bit will increase the clocking rate of tone generator 1 to 24 kHz only when the REL bit (direct Register 32, bit 6) is set. Also, dedicated oscillator registers are used for FSK generation (indirect registers 99–104). Audio tones are generated using this new higher frequency, and oscillator 1 active and inactive timers have a finer bit resolution of 41.67 μs. This provides greater resolution during FSK caller ID signal generation. 0 = Tone generator always clocked at 16 kHz; OSC1, OSC1X., and OSC1Y are always used. 1 = Tone generator module clocked at 24 kHz and dedicated FSK registers used only when REL = 1; otherwise clocked at 16 kHz.
5	DCSU	**DC-DC Converter Control Speedup.** When enabled, this bit invokes a multi-threshold error control algorithm which allows the dc-dc converter to adjust more quickly to voltage changes. 0 = Normal control algorithm used. 1 = Multi-threshold error control algorithm used.
4:3	Reserved	**Read returns zero.**

Bit	Name	Function
2	LCVE	**Voltage-Based Loop Closure.** Enables loop closure to be determined by the TIP-to-RING voltage rather than loop current. 0 = Loop closure determined by loop current. 1 = Loop closure determined by TIP-to-RING voltage.
1	DCFIL	**DC-DC Converter Squelch.** When enabled, this bit squelches noise in the audio band from the dc-dc converter control loop. 0 = Voice band squelch disabled. 1 = Voice band squelch enabled.
0	HYSTEN	**Loop Closure Hysteresis Enable.** When enabled, this bit allows hysteresis to the loop closure calculation. The upper and lower hysteresis thresholds are defined by indirect registers 28 and 43, respectively. 0 = Loop closure hysteresis disabled. 1 = Loop closure hysteresis enabled.

4. Indirect Registers

Indirect registers are not directly mapped into memory but are accessible through the IDA and IAA registers. A write to IDA followed by a write to IAA is interpreted as a write request to an indirect register. In this case, the contents of IDA are written to indirect memory at the location referenced by IAA at the next indirect register update. A write to IAA without first writing to IDA is interpreted as a read request from an indirect register. In this case, the value located at IAA is written to IDA at the next indirect register update. Indirect registers are updated at a rate of 16 kHz. For pending indirect register transfers, IAS (direct Register 31) will be one until serviced. In addition an interrupt, IND (Register 20), can be generated upon completion of the indirect transfer.

Table 30. Si3230 to Si3233 Indirect Register Cross Reference

Si3230 Indirect Register	Si3233 Indirect Register	Indirect Register Name	Si3230 Indirect Register	Si3233 Indirect Register	Indirect Register Name	Si3230 Indirect Register	Si3233 Indirect Register	Indirect Register Name
13	0	OSC1	27	14	ADCG	38	25	NQ34
14	1	OSC1X	28	15	LCRT	39	26	NQ56
15	2	OSC1Y	29	16	RPTP	40	27	VCMR
16	3	OSC2	30	17	CML	41	64	VMIND
17	4	OSC2X	31	18	CMH	43	66	LCRTL
18	5	OSC2Y	32	19	PPT12	99	69	FSK0X
19	6	ROFF	33	20	PPT34	100	70	FSK0
20	7	RCO	34	21	PPT56	101	71	FSK1X
21	8	RNGX	35	22	NCLR	102	72	FSK1
22	9	RNGY	36	23	NRTP	103	73	FSK01
26	13	DACG	37	24	NQ12	104	74	FSK10

All values are represented in twos-complement format.

Note: The values of all indirect registers are undefined following the reset state.

4.1. Oscillators

See functional description sections of tone generation, ringing, and pulse metering for guidelines on computing register values. All values are represented in twos-complement format.

Note: The values of all indirect registers are undefined following the reset state. Shaded areas denote bits that can be read and written but should be written to zeroes.

Table 31. Oscillator Indirect Registers Summary

Addr	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	OSC1[15:0]															
1	OSC1X[15:0]															
2	OSC1Y[15:0]															
3	OSC2[15:0]															
4	OSC2X[15:0]															
5	OSC2Y[15:0]															
6		ROFF[5:0]														

Table 31. Oscillator Indirect Registers Summary (Continued)

Addr	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
7	RCO[15:0]															
8	RNGX[15:0]															
9	RNGY[15:0]															

Table 32. Oscillator Indirect Registers Description

Addr	Description	Reference Page
0	**Oscillator 1 Frequency Coefficient.** Sets tone generator 1 frequency.	27
1	**Oscillator 1 Amplitude Register.** Sets tone generator 1 signal amplitude.	27
2	**Oscillator 1 Initial Phase Register.** Sets initial phase of tone generator 1 signal.	27
3	**Oscillator 2 Frequency Coefficient.** Sets tone generator 2 frequency.	27
4	**Oscillator 2 Amplitude Register.** Sets tone generator 2 signal amplitude.	27
5	**Oscillator 2 Initial Phase Register.** Sets initial phase of tone generator 2 signal.	27
6	**Ringing Oscillator DC Offset.** Sets dc offset component (V_{TIP}–V_{RING}) to ringing waveform. The range is 0 to 94.5 V in 1.5 V increments.	29
7	**Ringing Oscillator Frequency Coefficient.** Sets ringing generator frequency.	29
8	**Ringing Oscillator Amplitude Register.** Sets ringing generator signal amplitude.	29
9	**Ringing Oscillator Initial Phase Register.** Sets initial phase of ringing generator signal.	29

4.2. Digital Programmable Gain/Attenuation

See functional description sections of digital programmable gain/attenuation for guidelines on computing register values. All values are represented in twos-complement format.

Note: The values of all indirect registers are undefined following the reset state. Shaded areas denote bits that can be read and written but should be written to zeroes.

Table 33. Digital Programmable Gain/Attenuation Indirect Registers Summary

Addr	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
13	DACG[11:0]															
14	ADCG[11:0]															

Table 34. Digital Programmable Gain/Attenuation Indirect Registers Description

Addr.	Description
13	**Receive Path Digital to Analog Converter Gain/Attenuation.** This register sets gain/attenuation for the receive path. The digitized signal is effectively multiplied by DACG to achieve gain/attenuation. A value of 0x00 corresponds to –∞ dB gain (mute). A value of 0x400 corresponds to unity gain. A value of 0x7FF corresponds to a gain of 6 dB.
14	**Transmit Path Analog to Digital Converter Gain/Attenuation.** This register sets gain/attenuation for the transmit path. The digitized signal is effectively multiplied by ADCG to achieve gain/attenuation. A value of 0x00 corresponds to –∞ dB gain (mute). A value of 0x400 corresponds to unity gain. A value of 0x7FF corresponds to a gain of 6 dB.

4.3. SLIC Control

See descriptions of linefeed interface and power monitoring for guidelines on computing register values. All values are represented in twos-complement format.

Note: The values of all indirect registers are undefined following the reset state. Shaded areas denote bits that can be read and written but should be written to zeroes.

Table 35. SLIC Control Indirect Registers Summary

Addr	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
15		LCRT[5:0]														
16		RPTP[5:0]														
17				CML[5:0]												
18				CMH[5:0]												
19		PPT12[7:0]														
20		PPT34[7:0]														
21		PPT56[7:0]														
22	NCLR[12:0]															
23	NRTP[12:0]															
24	NQ12[12:0]															
25	NQ34[12:0]															
26	NQ56[12:0]															
27				VCMR[3:0]												
64				VMIND[3:0]												
66		LCRTL[5:0]														

Table 36. SLIC Control Indirect Registers Description

Addr	Description
15	**Loop Closure Threshold.** Loop closure detection threshold. This register defines the upper bounds threshold if hysteresis is enabled (direct Register 108, bit 0). The range is 0–80 mA in 1.27 mA steps. See "2.2.6. Loop Closure Detection" on page 22.
16	**Ring Trip Threshold.** Ring trip detection threshold during ringing. See "2.5.6. Ring Trip Detection" on page 31.
17	**Common Mode Minimum Threshold for Speed-Up.** This register defines the negative common mode voltage threshold. Exceeding this threshold enables a wider bandwidth of dc linefeed control for faster settling times. The range is 0–23.625 V in 0.375 V steps.
18	**Common Mode Maximum Threshold for Speed-Up.** This register defines the positive common mode voltage threshold. Exceeding this threshold enables a wider bandwidth of dc linefeed control for faster settling times. The range is 0–23.625 V in 0.375 V steps.
19	**Power Alarm Threshold for Transistors Q1 and Q2.**

Table 36. SLIC Control Indirect Registers Description (Continued)

Addr	Description
20	**Power Alarm Threshold for Transistors Q3 and Q4.**
21	**Power Alarm Threshold for Transistors Q5 and Q6.**
22	**Loop Closure Filter Coefficient.**
23	**Ring Trip Filter Coefficient.**
24	**Thermal Low Pass Filter Pole for Transistors Q1 and Q2.**
25	**Thermal Low Pass Filter Pole for Transistors Q3 and Q4.**
26	**Thermal Low Pass Filter Pole for Transistors Q5 and Q6.**
27	**Common Mode Bias Adjust During Ringing.** Recommended value of 0 decimal.
64	**DC-DC Converter V_{OV} Voltage (Si3233 only).** This register sets the overhead voltage, V_{OV}, to be supplied by the dc-dc converter. When the VOV bit = 0 (direct Register 66, bit 4), V_{OV} should be set between 0 and 9 V (VMIND = 0 to 6h). When the VOV bit = 1, V_{OV} should be set between 0 and 13.5 V (VMIND = 0 to 9h).
66	**Loop Closure Threshold—Lower Bound.** This register defines the lower threshold for loop closure hysteresis, which is enabled in bit 0 of direct Register 108. The range is 0–80 mA in 1.27 mA steps.

4.4. FK Control

For detailed instructions on FSK signal generation, refer to “Application Note 32: FSK Generation” (AN32). These registers support enhanced FSK generation mode, which is enabled by setting FSKEN = 1 (direct Register 108, bit 6) and REL = 1 (direct Register 32, bit 6).

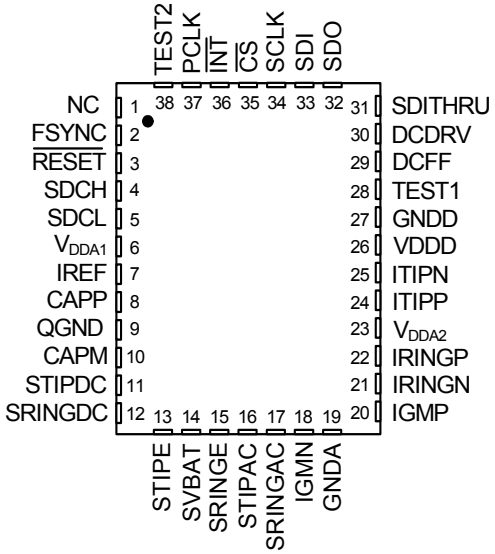
Table 37. FSK Control Indirect Registers Summary

Addr	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
69	FSK0X[15:0]															
70	FSK0[15:0]															
71	FSK1X[15:0]															
72	FSK1[15:0]															
73	FSK01[15:0]															
74	FSK10[15:0]															

Table 38. FSK Control Indirect Registers Description

Addr	Description	Reference Page
69	**FSK Amplitude Coefficient for Space.** When FSKEN = 1 and REL = 1, this register sets the amplitude to be used when generating a space or “0”. When the active timer (OAT1) expires, the value of this register is loaded into oscillator 1 instead of OSC1X.	29 and AN32
70	**FSK Frequency Coefficient for Space.** When FSKEN = 1 and REL = 1, this register sets the frequency to be used when generating a space or “0”. When the active timer (OAT1) expires, the value of this register is loaded into oscillator 1 instead of OSC1.	29 and AN32
71	**FSK Amplitude Coefficient for Mark.** When FSKEN = 1 and REL = 1, this register sets the amplitude to be used when generating a mark or “1”. When the active timer (OAT1) expires, the value of this register is loaded into oscillator 1 instead of OSC1X.	29 and AN32
72	**FSK Frequency Coefficient for Mark.** When FSKEN = 1 and REL = 1, this register sets the frequency to be used when generating a mark or “1”. When the active timer (OAT1) expires, the value of this register is loaded into oscillator 1 instead of OSC1.	29 and AN32
73	**FSK Transition Parameter from 0 to 1.** When FSKEN = 1 and REL = 1, this register defines a gain correction factor that is applied to signal amplitude when transitioning from a space (0) to a mark (1).	29 and AN32
74	**FSK Transition Parameter from 1 to 0.** When FSKEN = 1 and REL = 1, this register defines a gain correction factor that is applied to signal amplitude when transitioning from a mark (1) to a space (0).	29 and AN32

5. Pin Descriptions: Si3233

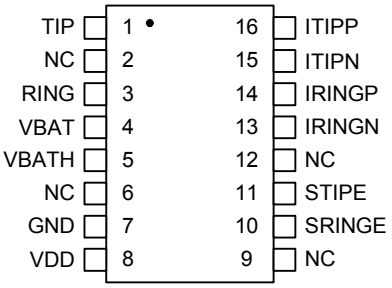


Pin #	Name	Description
35	$\overline{CS}$	**Chip Select.** Active low. When inactive, SCLK and SDI are ignored and SDO is high impedance. When active, the serial port is operational.
36	$\overline{INT}$	**Interrupt.** Maskable interrupt output. Open drain output for wire-ORed operation.
37	PCLK	**PCM Bus Clock.** Clock input.
38	TEST2	**Test.** Enables test modes for Silicon Labs internal testing. This pin should always be tied to ground for normal operation.
1	NC	**No Connect.**
2	FSYNC	**Frame Synch.** 8 kHz frame synchronization signal for the PCM bus. May be short or long pulse format.
3	$\overline{RESET}$	**Reset.** Active low input. Hardware reset used to place all control registers in the default state.
4	SDCH	**DC Monitor.** DC-DC converter monitor input used to detect overcurrent situations in the converter.
5	SDCL	**DC Monitor.** DC-DC converter monitor input used to detect overcurrent situations in the converter.
6	VDDA1	**Analog Supply Voltage.** Analog power supply for internal analog circuitry.
7	IREF	**Current Reference.** Connects to an external resistor used to provide a high accuracy reference current.

Pin #	Name	Description
8	CAPP	**SLIC Stabilization Capacitor.** Capacitor used in low pass filter to stabilize SLIC feedback loops.
9	QGND	**Component Reference Ground.**
10	CAPM	**SLIC Stabilization Capacitor.** Capacitor used in low pass filter to stabilize SLIC feedback loops.
11	STIPDC	**TIP Sense.** Analog current input used to sense voltage on the TIP lead.
12	SRINGDC	**RING Sense.** Analog current input used to sense voltage on the RING lead.
13	STIPE	**TIP Emitter Sense.** Analog current input used to sense voltage on the Q6 emitter lead.
14	SVBAT	**VBAT Sense.** Analog current input used to sense voltage on dc-dc converter output voltage lead.
15	SRINGE	**RING Emitter Sense.** Analog current input used to sense voltage on the Q5 emitter lead.
16	STIPAC	**TIP Transmit Input.** Analog ac input used to detect voltage on the TIP lead.
17	SRINGAC	**RING Transmit Input.** Analog ac input used to detect voltage on the RING lead.
18	IGMN	**Differential Audio Input.** Connect to external codec.
19	GNDA	**Analog Ground.** Ground connection for internal analog circuitry.
20	IGMP	**Differential Audio Input.** Connect to external codec.
21	IRINGN	**Negative Ring Current Control.** Analog current output driving Q3.
22	IRINGP	**Positive Ring Current Control.** Analog current output driving Q2.
23	VDDA2	**Analog Supply Voltage.** Analog power supply for internal analog circuitry.
24	ITIPP	**Positive TIP Current Control.** Analog current output driving Q1.
25	ITIPN	**Negative TIP Current Control.** Analog current output driving Q4.
26	VDDD	**Digital Supply Voltage.** Digital power supply for internal digital circuitry.
27	GNDD	**Digital Ground.** Ground connection for internal digital circuitry.

Pin #	Name	Description
28	TEST1	**Test.** Enables test modes for Silicon Labs internal testing. This pin should always be tied to ground for normal operation.
29	DCFF	**DC Feed-Forward/High Current General Purpose Output.** Feed-forward drive of external bipolar transistors to improve dc-dc converter efficiency.
30	DCDRV	**DC Drive/Battery Switch.** DC-DC converter control signal output which drives external bipolar transistor. Battery switch control signal output which drives external bipolar transistor.
31	SDITHRU	**SDI Passthrough.** Cascaded SDI output signal for daisy-chain mode.
32	SDO	**Serial Port Data Out.** Serial port control data output.
33	SDI	**Serial Port Data In.** Serial port control data input.
34	SCLK	**Serial Port Bit Clock Input.** Serial port clock input. Controls the serial data on SDO and latches the data on SDI.

6. Pin Descriptions: Si3201



Pin #	Name	Input/ Output	Description
1	TIP	I/O	**TIP Output**—Connect to the TIP lead of the subscriber loop.
2, 6, 9, 12	NC	—	**No Internal Connection**—Do not connect to any electrical signal.
3	RING	I/O	**RING Output**—Connect to the RING lead of the subscriber loop.
4	VBAT	—	**Operating Battery Voltage**—Connect to the battery supply.
5	VBATH	—	**High Battery Voltage**—This pin is internally connected to VBAT.
7	GND	—	**Ground**—Connect to a low impedance ground plane.
8	VDD	—	**Supply Voltage**—Main power supply for all internal circuitry. Connect to a 3.3 V or 5 V supply. Decouple locally with a 0.1 μF/6 V capacitor.
10	SRINGE	O	**RING Emitter Sense Output**—Connect to the SRINGE pin of the Si321x pin.
11	STIPE	O	**TIP Emitter Sense Output**—Connect to the STIPE pin of the Si321x pin.
13	IRINGN	I	**Negative RING Current Control**—Connect to the IRINGN lead of the Si321x.
14	IRINGP	I	**Positive RING Current Drive**—Connect to the IRINGP lead of the Si321x.
15	ITIPN	I	**Negative TIP Current Control**—Connect to the ITIPN lead of the Si321x.
16	ITIPP	I	**Positive TIP Current Control**—Connect to the ITIPP lead of the Si321x.
Bottom-Side Exposed Pad		—	**Exposed Thermal Pad**—Connect to the bulk ground plane.

7. Ordering Guide[1,2,3]

Device	Description	DCFF Pin Output	Package	Temp Range
Si3233-X-FM	ProSLIC	$\overline{\text{DCDRV}}$	QFN-38	0 to 70 °C
Si3233-X-GM	ProSLIC	$\overline{\text{DCDRV}}$	QFN-38	–40 to 85 °C
Si3233M-X-FM	ProSLIC	DCDRV	QFN-38	0 to 70 °C
Si3233M-X-GM	ProSLIC	DCDRV	QFN-38	–40 to 85 °C
Si3201-X-FS	Line Interface	n/a	SOIC-16	0 to 70 °C
Si3201-X-GS	Line Interface	n/a	SOIC-16	–40 to 85 °C

Notes:
1. “X” denotes product revision.
2. Add an “R” at the end of the device to denote tape and reel options; 2500 quantity per reel.
3. All devices are lead-free and RoHS-compliant.

8. Package Outline: 38-Pin QFN

Figure 19 illustrates the package details for the Si3233. Table 39 lists the values for the dimensions shown in the illustration.

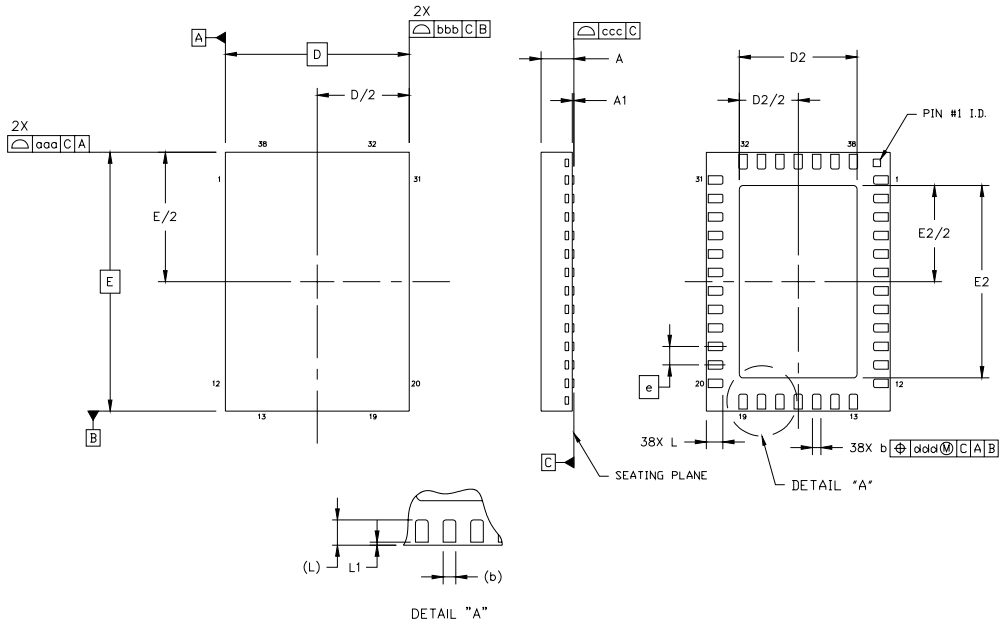


Figure 19. 38-Pin Quad Flat No-Lead Package (QFN)

Table 39. Package Diagram Dimensions[1,2,3]

Symbol	Millimeters		
	Min	Nom	Max
A	0.75	0.85	0.95
A1	0.00	0.01	0.05
b	0.18	0.23	0.30
D		5.00 BSC	
D2	3.10	3.20	3.30
e		0.50 BSC	
E		7.00 BSC	
E2	5.10	5.20	5.30
L	0.35	0.45	0.55
L1	0.03	0.05	0.08
aaa	—	—	0.10
bbb	—	—	0.10
ccc	—	—	0.08
ddd	—	—	0.10

Notes:
1. Dimensioning and tolerancing per ANSI Y14.5M-1994.
2. The drawing conforms to the JEDEC Solid State Outline MO-220, Variation VHKD-1.
3. Recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for Small Body Components.

9. Package Outline: 16-Pin SOIC

Figure 20 illustrates the package details for the Si3201. Table 40 lists the values for the dimensions shown in the illustration.

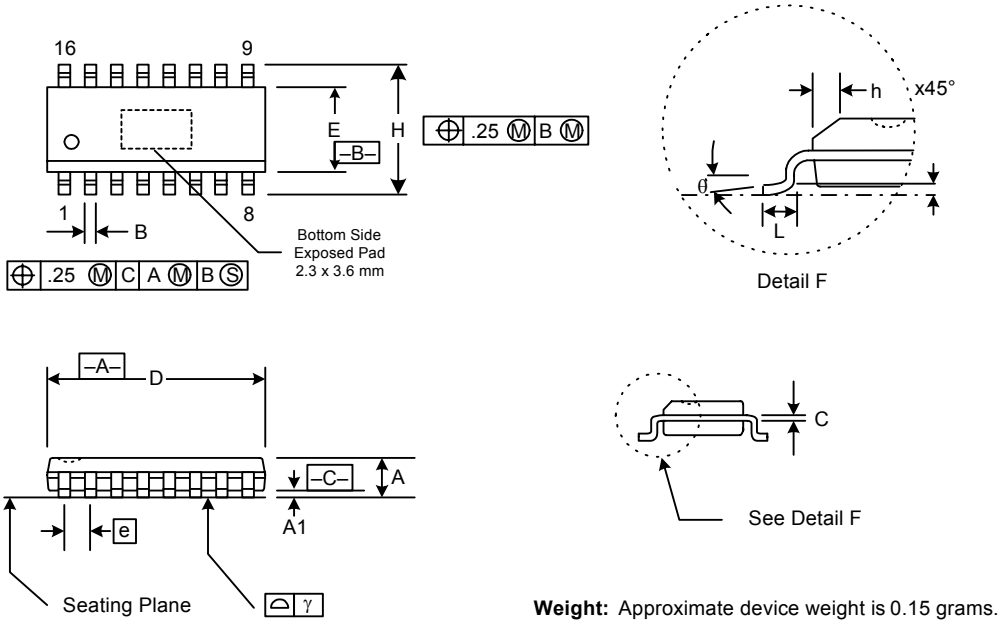


Figure 20. 16-pin Small Outline Integrated Circuit (SOIC) Package

Table 40. Package Diagram Dimensions

Symbol	Millimeters	
	Min	Max
A	1.35	1.75
A1	0	0.15
B	.33	.51
C	.19	.25
D	9.80	10.00
E	3.80	4.00
e	1.27 BSC	
H	5.80	6.20
h	.25	.50
L	.40	1.27
γ	—	0.10
θ	0º	8º

DOCUMENT CHANGE LIST

Revision 0.1 to Revision 0.5

- Updated Section "2.6. Two-Wire Impedance Matching" on page 34 and Register 10, “Two-Wire Impedance Synthesis Control,” on page 44.
- Removed invalid reference to ZEXT bit.

NOTES:

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