Data Sheet
March 1997

microelectronics group

Lucent Technologies
Bell Labs Innovations

L7554 Low-Power SLIC

Features

- Low active power (typical 165 mW during on-hook transmission)
- Sleep state for low idle power (76 mW)
- Quiet Tip/Ring polarity reversal
- Supports meter pulse injection
- Spare op amp for meter pulse filtering
- –24 V to –72 V power supply operation
- Distortion-free on-hook transmission
- Convenient operating states:
  — Forward powerup
  — Polarity reversal powerup
  — Forward low-power scan
  — Polarity reversal low-power scan
  — Ground start
  — Disconnect (high impedance)
- Adjustable supervision functions:
  — Off-hook detector with longitudinal rejection
  — Ground key detector
  — Ring trip detector
- Independent, adjustable, dc and ac parameters:
  — dc feed resistance
  — Loop current limit
  — Termination impedance
- Thermal protection

Description

This electronic subscriber loop interface circuit (SLIC) is optimized for low-power consumption while providing an extensive set of features.

Quiet polarity reversal is possible because the ac path is uninterrupted during transition.

The L7554 includes the ground start state and a summing node for meter pulse injection to 2.2 Vrms. A spare, uncommitted op amp is included for meter pulse filtering.

The device is being offered in two versions, based upon maximum battery. The L7554AP is guaranteed to –60 V, and the L7554BP is guaranteed to –72 V.

The device is available in a 44-pin PLCC package. It is built by using a 90 V complementary bipolar (CBIC) process.

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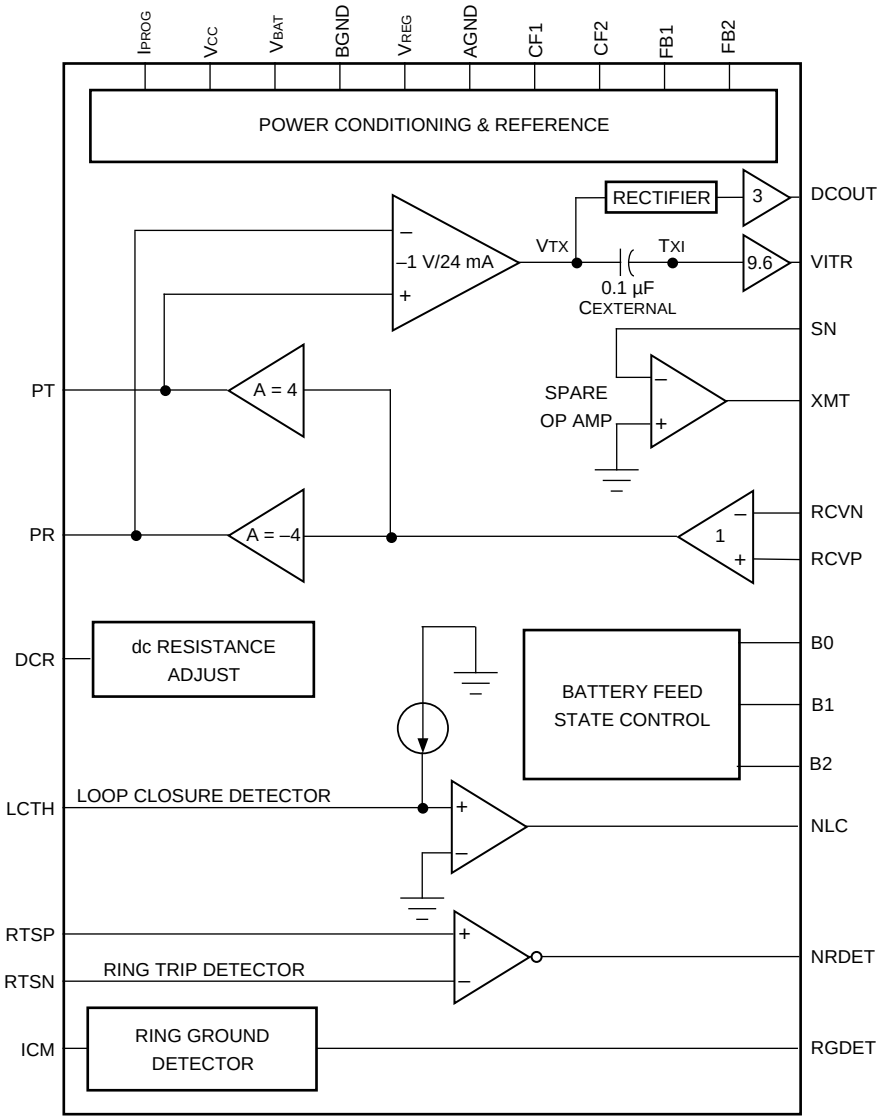

12-2569 (C)

Figure 1. Functional Diagram

Pin Information

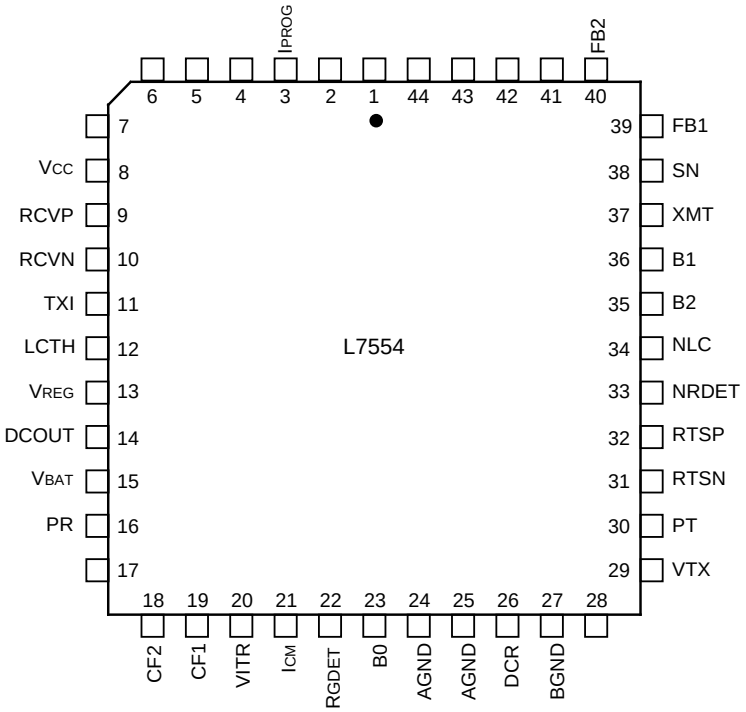

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Figure 2. Pin Diagram (PLCC Chip)

Table 1. Pin Descriptions

Pin	Symbol	Type	Description
3	IPROG	I	**Current-Limit Program Input.** A resistor to DCOUT sets the dc current limit of the device.
8	VCC	—	**+5 V Power Supply.**
9	RCVP	I	**Receive ac Signal Input (Noninverting).** This high-impedance input controls the ac differential voltage on Tip and Ring.
10	RCVN	I	**Receive ac Signal Input (Inverting).** This high-impedance input controls the ac differential voltage on Tip and Ring.
11	TXI	—	**ac/dc Separation.** Connect a 0.1 µF capacitor from this pin to VTX**.**
12	LCTH	I	**Loop Closure Threshold Input.** Connect a resistor to DCOUT to set off-hook threshold.
13	VREG	I	**Regulated Negative dc Battery Voltage.** Can be connected to an external regulator. Otherwise, connect to VBAT.
14	DCOUT	O	**dc Output Voltage.** This output is a voltage that is directly proportional to the absolute value of the differential Tip/Ring current.
15	VBAT	—	**Battery Supply.** Negative high-voltage power supply.
16	PR	I/O	**Protected Ring.** The output of the ring driver amplifier and input to loop sensing circuitry. Connect to loop through overvoltage protection.
18	CF2	—	**Filter Capacitor 2.** Connect a 0.1 µF capacitor from this pin to AGND.
19	CF1	—	**Filter Capacitor 1.** Connect a 0.47 µF capacitor from this pin to pin CF2.

Pin Information (continued)

Table 1. Pin Descriptions (continued)

Pin	Symbol	Type	Description
20	VITR	O	**Transmit ac Output Voltage.** This output is a voltage that is directly proportional to the differential ac Tip/Ring current.
21	ICM	I	**Common-Mode Current Sense.** To program ring ground sense threshold, connect a resistor to VCC and connect a capacitor to AGND to filter 50/60 Hz. If unused, the pin can be left unconnected.
22	RGDET	O	**Ring Ground Detect.** When high, this open-collector output indicates the presence of a ring ground. To use, connect a 100 kΩ resistor to VCC.
23	B0	I	**State Control Input.** B0, B1, and B2 determine the state of the SLIC. See Table 2.
24	AGND	—	**Analog Signal Ground**.
25	AGND	—	**Analog Signal Ground.**
26	DCR	I	**dc Resistance for Low Loop Currents.** Leave open for dc feed resistance of 118 Ω, or short to DCOUT for 618 Ω. Intermediate values can be set by a simple resistor divider from DCOUT to ground with the tap at DCR.
27	BGND	—	**Battery Ground.** Ground return for the battery supply.
29	VTX	O	This output is a voltage that is directly proportional to the differential Tip/Ring current.
30	PT	I/O	**Protected Tip**. The output of the tip driver amplifier and input to loop sensing. Connect to loop through overvoltage protection.
31	RTSN	I	**Ring Trip Sense Negative**. Connect this pin to the ringing generator signal through a high-value resistor.
32	RTSP	I	**Ring Trip Sense Positive**. Connect this pin to the ring relay and the ringer series resistor through a high-value resistor.
33	NRDET	O	**Ring Trip Detector Output**. When low, this logic output indicates that ringing is tripped.
34	NLC	O	**Loop Detector Output**. When low, this logic output indicates an off-hook condition.
35	B2	I	**State Control Input**. B0, B1, and B2 determine the state of the SLIC. See Table 2.
36	B1	I/O	**State Control Input**. B0, B1, and B2 determine the state of the SLIC. See Table 2.
37	XMT	O	**Transmit ac Output Voltage**. The output of the uncommitted operational amplifier.
38	SN	I	**Summing Node**. The inverting input of the uncommitted operational amplifier. A resistor or network to XMT sets the gain.
39	FB1	I	**Forward Battery Slowdown.** A 0.1 µF capacitor from FB1 to AGND and from FB2 to AGND will ramp the polarity reversal transition for added flexibility in applications requiring quiet polarity reversal. If not needed, the pin can be left open.
40	FB2	I	**Forward Battery Slowdown.** A 0.1 µF capacitor from FB2 to AGND and from FB1 to AGND will ramp the polarity reversal transition for added flexibility in applications requiring quiet polarity reversal. If not needed, the pin can be left open.

Functional Description

Table 2. Input State Coding

B0	B1	B2	State/Definition
1	1	1	**Powerup, Forward Battery.** Normal talk and battery feed state. Pin PT is positive with respect to PR. On-hook transmission is enabled.
1	1	0	**Powerup, Reverse Battery.** Normal talk and battery feed state. Pin PR is positive with respect to PT. On-hook transmission is enabled.
0	1	1	**Ground Start.** Tip drive amplifier is turned off. The device presents a high-impedance (>100 kΩ) to the PT pin and a current-limited battery to the PR pin. Output pin RGDET indicates current flowing in the ring lead.
0	1	0	**Low-Power Scan, Reverse Battery.** Except for off-hook supervision, all circuits are shut down to conserve power. Pin PR is positive with respect to PT. On-hook transmission is disabled.
0	0	1	**Low-Power Scan, Forward Battery.** Except for off-hook supervision, all circuits are shut down to conserve power. Pin PT is positive with respect to PR. On-hook transmission is disabled.
0	0	0	**Disconnect.** The Tip and Ring amplifiers are turned off and the SLIC goes to a high-impedance state (>100 kΩ).

Table 3. Supervision Coding

Pin NLC	Pin NRDET	Pin RGDET
0 = off-hook 1 = on-hook	0 = ring trip 1 = no ring trip	1 = ring ground 0 = no ring ground

Absolute Maximum Ratings (T_A = 25 °C)

Stresses in excess of the absolute maximum ratings can cause permanent damage to the device. These are absolute stress ratings only. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operational sections of the data sheet. Exposure to absolute maximum ratings for extended periods can adversely affect device reliability.

Parameter	Symbol	Value	Unit
5 V Power Supply	V_{CC}	7.0	V
Battery (Talking) Supply	V_{BAT}	–75	V
Logic Input Voltage	—	–0.5 to +7.0	V
Analog Input Voltage	—	–7.0 to +7.0	V
Maximum Junction Temperature	T_J	165	°C
Storage Temperature Range	T_{stg}	–40 to +125	°C
Relative Humidity Range	R_H	5 to 95	%
Ground Potential Difference (BGND to AGND)	—	±3	V
PT or PR Fault Voltage (dc)	V_{PT}, V_{PR}	(V_{BAT} – 5) to +3	V
PT or PR Fault Voltage (10 x 1000 µs)	V_{PT}, V_{PR}	(V_{BAT} – 15) to +15	V
Current into Ring Trip Inputs	I_{RTSP}, I_{RTSN}	±240	µA

Note: The IC can be damaged unless all ground connections are applied before, and removed after, all other connections. Furthermore, when powering the device, the user must guarantee that no external potential creates a voltage on any pin of the device that exceeds the device ratings. Some of the known examples of conditions that cause such potentials during powerup are the following: 1) an inductor connected to Tip and Ring can force an overvoltage on V_{BAT} through the protection devices if the V_{BAT} connection chatters, and 2) inductance in the V_{BAT} lead could resonate with the V_{BAT} filter capacitor to cause a destructive overvoltage.

Recommended Operating Conditions

Parameter	Min	Typ	Max	Unit
Ambient Temperature	–40	—	85	°C
V_{CC} Supply Voltage	4.75	5.0	5.25	V
V_{BAT} Supply Voltage: L7554AP L7554BP	 –24 –24	 –40 –48	 –60 –72	V V
Loop Closure Threshold-detection Programming Range	—	10	I_{LIM}	mA
dc Loop Current-limit Programming Range	5	40	45	mA
On- and Off-hook 2-wire Signal Level	—	1	2.2	Vrms
ac Termination Impedance Programming Range	150	600	1300	Ω

Electrical Characteristics

Minimum and maximum values are testing requirements. Typical values are characteristic of the device and are the result of engineering evaluations. Typical values are for information purposes only and are not part of the testing requirements. Minimum and maximum values apply across the entire temperature range (–40 °C to +85 °C) and the entire battery range unless otherwise specified. Typical is defined as 25 °C, V_{CC} = 5.0 V, V_{BAT} = –48 V, and I_{LIM} = 40 mA. Positive currents flow into the device. Test circuit is Figure 4 unless noted.

Table 4. Power Supply

Parameter	Min	Typ	Max	Unit
Power Supply—Powerup, No Loop Current I_{CC} I_{BAT} (V_{BAT} = –48 V) Power Dissipation (V_{BAT} = –48 V)	 — — —	 4.1 –3.0 165	 4.8 –3.5 191	 mA mA mW
Power Supply—Low-Power Scan, Forward Bat, No Loop Current I_{CC} I_{BAT} (V_{BAT} = –48 V) Power Dissipation (V_{BAT} = –48 V)	 — — —	 2.7 –1.4 82	 3.7 –1.7 100	 mA mA mW
Power Supply Rejection 500 Hz to 3 kHz (See Figures 5, 6, 15, and 16.)[1] V_{CC} V_{BAT}	 35 45	 — —	 — —	 dB dB
Thermal Protection Shutdown (Tjc)	—	175	—	°C
Thermal Resistance, Junction to Ambient (θ_{JA})	—	47	—	°C/W

1. This parameter is not tested in production. It is guaranteed by design and device characterization.

Electrical Characteristics (continued)

Table 5. 2-Wire Port

Parameter	Min	Typ	Max	Unit
Tip or Ring Drive Current = dc + Longitudinal + Signal Currents	65	—	—	mA
Signal Current	15	—	—	mArms
Longitudinal Current Capability per Wire[1]	8.5	15	—	mArms
dc Loop Current Limit[2] R_{LOOP} = 100 Ω Programmability Range Accuracy (20 mA < I_{LIM} < 40 mA)	 — 5 —	 I_{LIM} — —	 — 45 ±12	 mA mA %
Powerup Open Loop Voltage Levels Common-mode Voltage Differential Voltage: V_{BAT} = –48 V, Temperature = 25 °C V_{BAT} = –72 V, Temperature = 85 °C (L7554BP)	 — $\lvert V_{BAT} + 7.0 \rvert$ $\lvert V_{BAT} + 10.0 \rvert$	 $V_{BAT}/2$ $\lvert V_{BAT} + 6.5 \rvert$ $\lvert V_{BAT} + 6.8 \rvert$	 — $\lvert V_{BAT} + 6.0 \rvert$ —	 V V V
Disconnect State PT Resistance ($V_{BAT} < V_{PT} < 0$ V) PR Resistance ($V_{BAT} < V_{PR} < 0$ V)	 100 100	 143 133	 — —	 kΩ kΩ
Ground Start State PT Resistance	 100	 143	 —	 kΩ
dc Feed Resistance (for I_{LOOP} below regulation level)	90	113	133	Ω
Loop Resistance Range (–3.17 dBm overload into 600 Ω; not including protection) I_{LOOP} = 20 mA at V_{BAT} = –48 V I_{LOOP} = 20 mA at V_{BAT} = –24 V	 1900 700	 — —	 — —	 Ω Ω
Longitudinal to Metallic Balance—*IEEE* [3] Std. 455 (See Figure 7.)[4] 50 Hz to 1 kHz 1 kHz to 3 kHz	 64 60	 75 70	 — —	 dB dB
Metallic to Longitudinal Balance 200 Hz to 4 kHz	 46	 —	 —	 dB
RFI Rejection (See Figure 8.)[5] 0.5 Vrms, 50 Ω Source, 30% AM Mod. 1 kHz 500 kHz to 100 MHz	 —	 –55	 –45	 dBV

1. The longitudinal current is independent of dc loop current.
2. Current-limit I_{LIM} is programmed by a resistor, R_{PROG}, from pin I_{PROG} to DCOUT. I_{LIM} is specified at the loop resistance where current limiting begins (see Figure 25). Select R_{PROG} (kΩ) = 1.67 x I_{LIM} (mA).
3. *IEEE* is a registered trademark of The Institute of Electrical and Electronics Engineers, Inc.
4. Longitudinal balance of circuit card will depend on loop series resistance matching (see Figures 23 and 24).
5. This parameter is not tested in production. It is guaranteed by design and device characterization.

Electrical Characteristics (continued)

Table 6. Analog Pin Characteristics

Parameter	Min	Typ	Max	Unit
Differential PT/PR Current Sense (DCOUT) Gain (PT/PR to DCOUT) Offset Voltage @ I_{LOOP} = 0, V_{BAT} = –48 V	 –119 –200	 –125 —	 –127 200	 V/A mV
Loop Closure Detector Threshold[1] Programming Accuracy	 —	 —	 ±20	 %
Ring Ground Detector Threshold[2] R_{ICM} = 83 kΩ Programming Accuracy	 3 —	 6 —	 10 ±25	 kΩ %
Ring Trip Comparator Input Offset Voltage	 —	 —	 ±10	 mV
RCVN, RCVP Input Bias Current	 —	 –0.2	 –1	 µA

1. Loop closure threshold is programmed by resistor R_{LCTH} from pin LCTH to pin DCOUT.
2. Ring ground threshold is programmed by resistor R_{ICM2} from pin ICM to V_{CC}.

Table 7. Uncommitted Op Amp Characteristics

Parameter	Min	Typ	Max	Unit
Input Offset Voltage Input Offset Current Input Bias Current Differential Input Resistance	— — — —	±5 ±10 200 1.5	— — — —	mV nA nA MΩ
Output Voltage Swing (R_L = 10 kΩ) Output Resistance (A_{VCL} = 1)	— —	±3.5 2.0	— —	Vpk Ω
Small Signal GBW	—	700	—	kHz

Electrical Characteristics (continued)

Table 8. ac Feed Characteristics

Parameter	Min	Typ	Max	Unit
ac Termination Impedance[1]	150	—	1300	Ω
Longitudinal Impedance[2]	—	40	46	Ω
Total Harmonic Distortion—200 Hz to 4 kHz[2]				
Off-hook	—	—	0.3	%
On-hook	—	—	1.0	%
Transmit Gain, f = 1 kHz (PT/PR to VITR)	—	–400	—	V/A
Transmit Accuracy in dB, 25 °C	–0.15	0	0.15	dB
Transmit Accuracy in dB, Full Temperature Range	–0.22	0	0.22	dB
Receive + Gain, f = 1 kHz (RCVP to PT/PR)	—	8.00	—	–
Receive – Gain, f = 1 kHz (RCVN to PT/PR)	—	–8.00	—	–
Receive Accuracy in dB, 25 °C	–0.18	0	0.18	dB
Receive Accuracy in dB, Full Temperature Range	–0.25	0	0.25	dB
Gain vs. Frequency (transmit and receive)				
(600 Ω termination; reference 1 kHz[2])				
200 Hz to 300 Hz	–1.00	0.0	0.05	dB
300 Hz to 3.4 kHz	–0.3	0.0	0.05	dB
3.4 kHz to 16 kHz	–0.5	–0.1	0.3	dB
16 kHz to 266 kHz	—	—	2.0	dB
Gain vs. Level (transmit and receive)(reference 0 dBV[2])				
–50 dB to +3 dB	–0.05	0	0.05	dB
Return Loss[3]				
200 Hz to 500 Hz	20	24	—	dB
500 Hz to 3400 Hz	26	29	—	dB
2-wire Idle-channel Noise (600 Ω termination)				
Psophometric	—	–87	–77	dBmp
C-message	—	2	12	dBrnC
3 kHz Flat	—	10	20	dBrn
Transmit Idle-channel Noise				
Psophometric	—	–82	–77	dBmp
C-message	—	7	12	dBrnC
3 kHz flat	—	15	20	dBrn
Transhybrid Loss[3]				
200 Hz to 500 Hz	21	24	—	dB
500 Hz to 3400 Hz	26	29	—	dB

1. Set by external components. Any complex impedance R1 + R2 || C between 150 Ω and 1300 Ω can be synthesized.
2. This parameter is not tested in production. It is guaranteed by design and device characterization.
3. Return loss and transhybrid loss are functions of device gain accuracies and the external hybrid circuit. Guaranteed performance assumes 1% tolerance of external components.

Electrical Characteristics (continued)

Table 9. Logic Inputs and Outputs

All outputs except RGDET are open-collector with internal pull-up resistor. RGDET is open-collector without internal pull-up.

Parameter	Symbol	Min	Typ	Max	Unit
Input Voltages					
Low Level (permissible range)	V_{IL}	–0.5	0.4	0.7	V
High Level (permissible range)	V_{IH}	2.0	2.4	V_{CC}	V
Input Currents					
Low Level (V_{CC} = 5.25 V, V_I = 0.4 V)	I_{IL}	—	–115	–200	µA
High Level (V_{CC} = 5.25 V, V_I = 2.4 V)	I_{IH}	—	–60	–100	µA
Output Voltages (open-collector with internal pull-up resistor)					
Low Level (V_{CC} = 4.75 V, I_{OL} = 360 µA)	V_{OL}	0	0.2	0.4	V
High Level (V_{CC} = 4.75 V, I_{OH} = –20 µA)	V_{OH}	2.4	—	V_{CC}	V

Ring Trip Requirements

- Ringing signal:
  - — Voltage, minimum 35 Vrms, maximum 100 Vrms.
  - — Frequency, 17 Hz to 23 Hz.
  - — Crest factor, 1.4 to 2.
- Ringing trip:
  - — ≤100 ms (typical), ≤250 ms (V_{BAT} = –33 V, loop length = 530 Ω).
- Pretrip:
  - — The circuits in Figure 3 will not cause ringing trip.

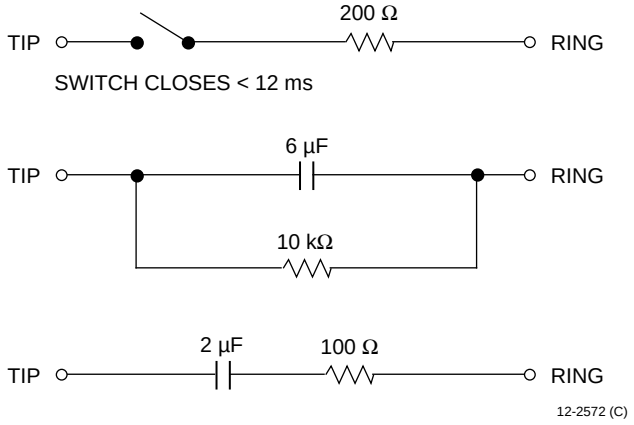


Figure 3. Ring Trip Circuits

Test Configurations

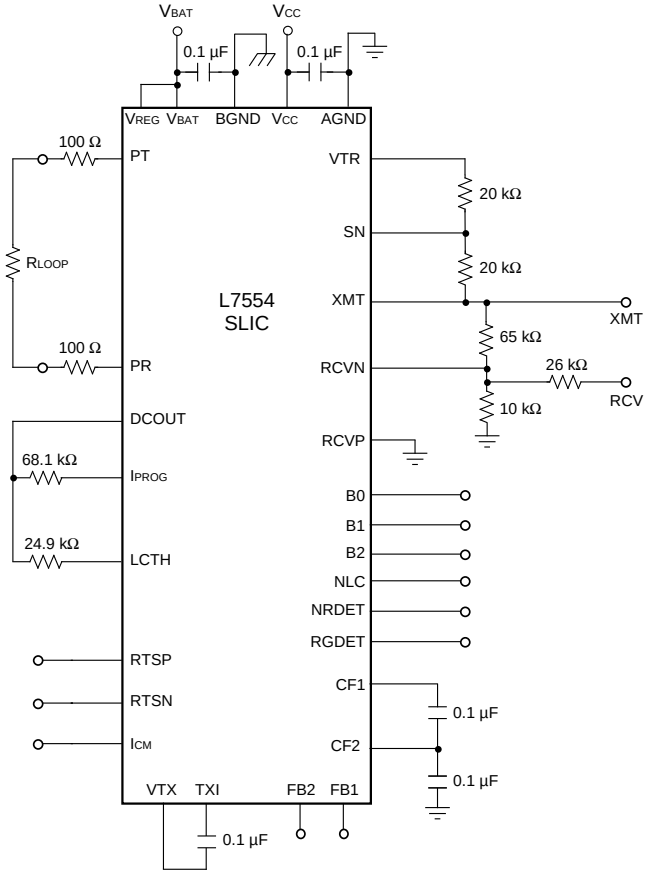


Figure 4. L7554 Basic Test Circuit

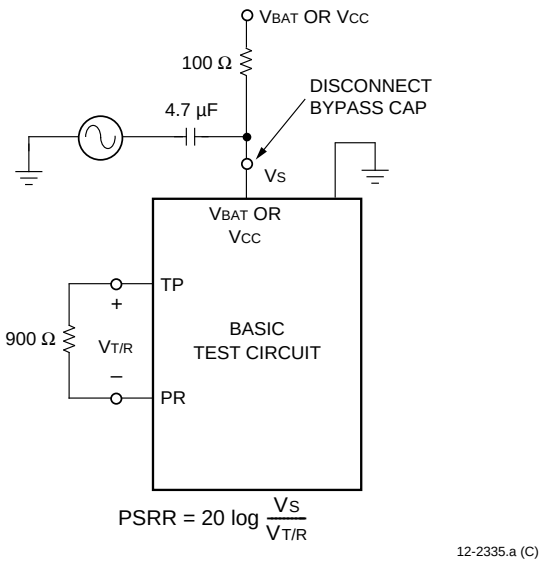


Figure 5. Metallic PSRR

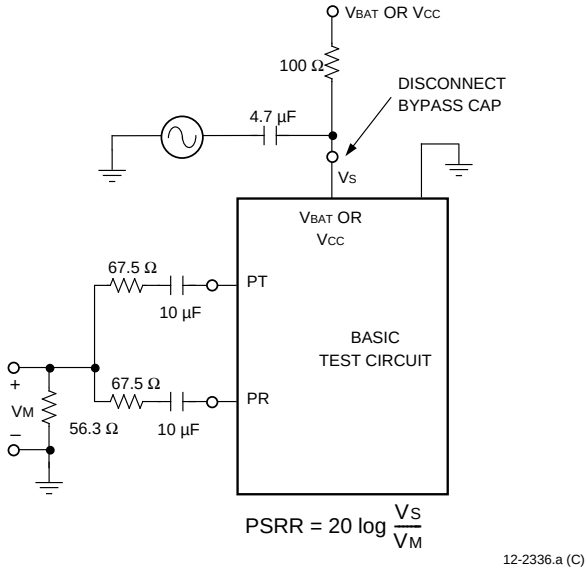
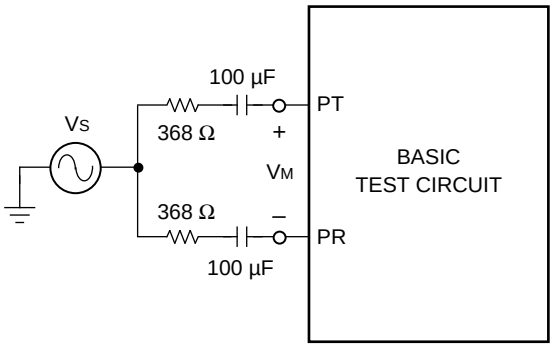


Figure 6. Longitudinal PSRR

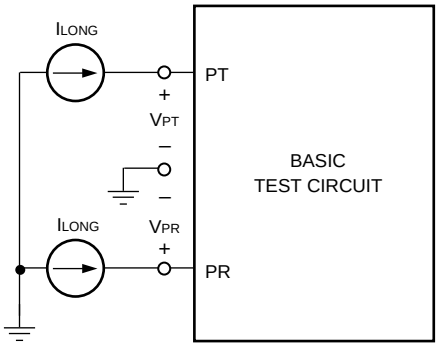
Test Configurations (continued)



$$\text{LONGITUDINAL BALANCE} = 20 \log \frac{V_S}{V_M}$$

12-2584 (C)

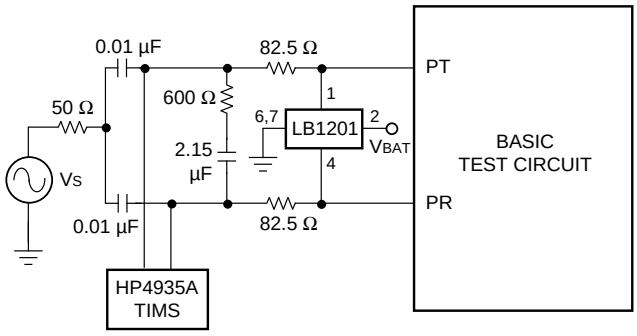
Figure 7. Longitudinal Balance



$$Z_{LONG} = \frac{\Delta V_{PT}}{\Delta I_{LONG}} \text{ OR } \frac{\Delta V_{PR}}{\Delta I_{LONG}}$$

12-2585 (C)

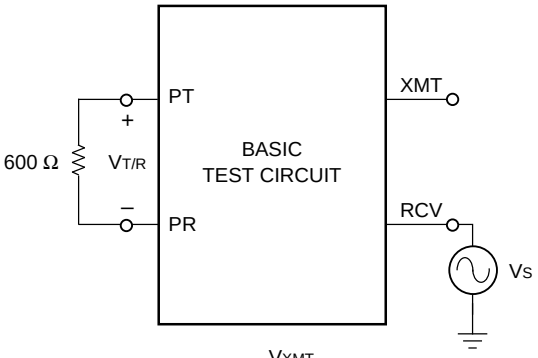
Figure 9. Longitudinal Impedance



VS = 0.5 Vrms 30% AM 1 kHz MODULATION,
f = 500 kHz—1 MHz
DEVICE IN POWERUP MODE, 600 Ω TERMINATION

12-2586 (C)

Figure 8. RFI Rejection



$$G_{XMT} = \frac{V_{XMT}}{V_{T/R}}$$

$$G_{RCV} = \frac{V_{T/R}}{V_{RCV}}$$

12-2587 (C)

Figure 10. ac Gains

Applications

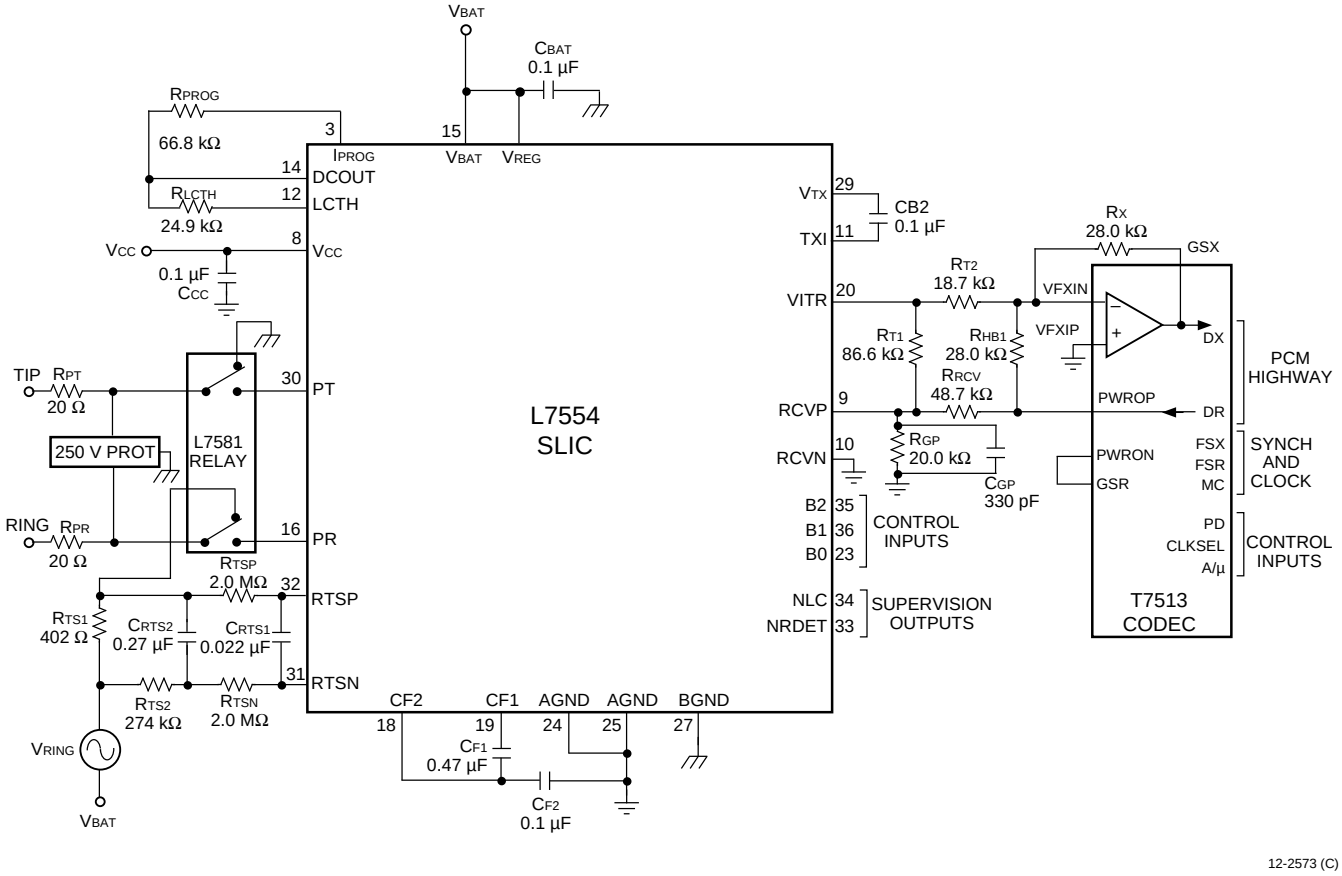


Figure 11. Basic Loop Start Application Circuit Using T7513 Type Codec

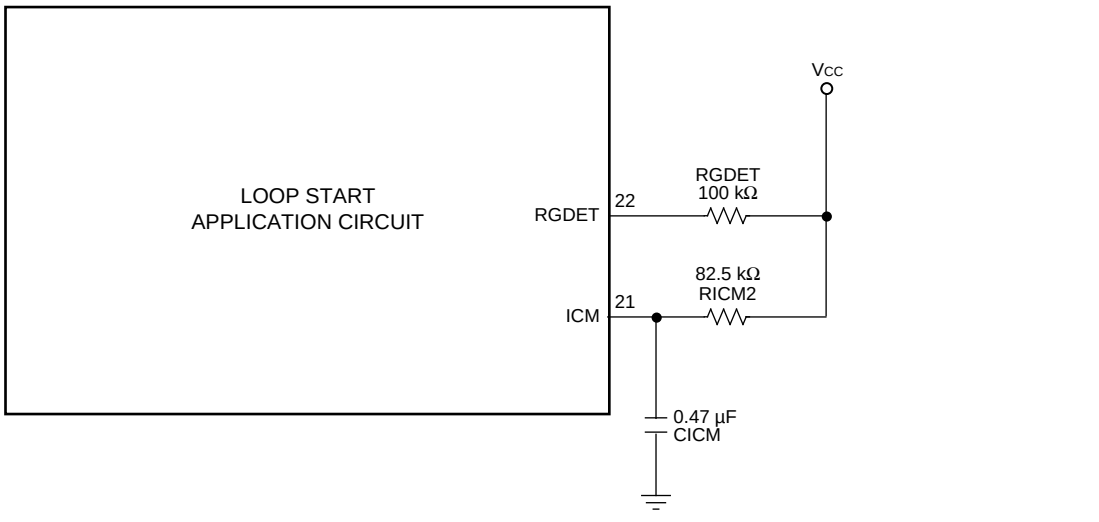


Figure 12. Ground Start Application Circuit

Applications (continued)

Table 10. Parts List for Loop Start and Ground Start Applications

Name	Value	Function
Integrated Circuits		
SLIC	L7554	Subscriber loop interface circuit (SLIC).
Protector	250 V Thyristor type	Secondary protection.
Ringing Relay	L7581	Switches ringing signals.
Codec	T7513	First-generation codec.
Overvoltage Protection		
R_{PT}	20 Ω, Fusible	Protection resistor.
R_{PR}	20 Ω, Fusible	Protection resistor.
Power Supply		
C_{BAT1}	0.1 µF, 20%, 100 V	V_{BAT} filter capacitor.
C_{CC}	0.1 µF, 20%, 10 V	V_{CC} filter.
C_{F1}	0.47 µF, 20%, 100 V	With C_{F2}, improves idle channel noise.
C_{F2}	0.1 µF, 20%, 100 V	With C_{F1}, improves idle channel noise.
dc Profile		
R_{PROG}	66.8 kΩ, 1%, 1/4 W	Sets dc loop current limit.
ac Characteristics		
C_{B2}	0.1 µF, 20%, 100 V	ac/dc separation capacitor.
C_{GB}	330 µF, 20%, 10 V	Loop stability.
R_{T1}	86.6 kΩ, 1%, 1/4 W	With R_{GP} and R_{RCV}, sets ac termination impedance.
R_{RCV}	48.7 kΩ, 1%, 1/4 W	With R_{GP} and R_{T1}, sets receive gain.
R_{GP}	20.0 kΩ, 1%, 1/4 W	With R_{T1} and R_{RCV}, sets ac termination impedance and receive gain.
C_{GP}	330 pF, 10 V, 20%	Loop stability.
R_{T2}	18.7 kΩ, 1%, 1/4 W	With R_X, sets transmit gain in codec.
R_X	28.0 kΩ, 1%, 1/4 W	With R_{T2}, sets transmit gain in codec.
R_{HB1}	28.0 kΩ, 1%, 1/4 W	Sets hybrid balance.
Supervision		
R_{LCTH}	24.9 kΩ, 1%, 1/4 W	Sets loop closure (off-hook) threshold.
R_{TS1}	402 Ω, 5%, 2 W	Ringing source series resistor.
R_{TS2}	274 kΩ, 5%, 1/4 W	With C_{RTS2}, forms first pole of a double pole, 2 Hz ring trip sense filter.
C_{RTS1}	0.022 µF, 20%, 5 V	With R_{TSN}, R_{TSP}, forms second 2 Hz filter pole.
C_{RTS2}	0.27 µF, 20%, 100 V	With R_{TS2}, forms first 2 Hz filter pole.
R_{TSN}	2 MΩ, 5%, 1/4 W	With C_{RTS1}, R_{TSP}, forms second 2 Hz filter pole.
R_{TSP}	2 MΩ, 5%, 1/4 W	With C_{RTS1}, R_{TSN}, forms second 2 Hz filter pole.
Ground Start		
C_{ICM}	0.47 µF, 20%, 10 V	Provides 60 Hz filtering for ring ground detection.
R_{GDET}	100 kΩ, 20%, 1/4 W	Digital output pull-up resistor.
R_{ICM2}	82.5 kΩ, 1%, 1/4 W	Sets ring ground detection threshold.

Applications (continued)

Design Considerations

Table 11 shows the design parameters of the application circuit shown in Figure 11. Components that are adjusted to program these values are also shown.

Table 11. 600 Ω Design Parameters

Design Parameter	Parameter Value	Components Adjusted
Loop Closure Threshold	10 mA	R_{LCTH}
dc Loop Current Limit	40 mA	R_{PROG}
dc Feed Resistance	183 Ω	R_{PT}, R_{PR}
2-wire Signal Overload Level	3.14 dBm	—
ac Termination Impedance	600 Ω	R_{T1}, R_{GP}, R_{RCV}
Hybrid Balance Line Impedance	600 Ω	R_{HB1}
Transmit Gain	0 dB	R_{T2}, R_X
Receive Gain	0 dB	R_{RCV}, R_{GP}, R_{T1}

Applications (continued)

Characteristic Curves

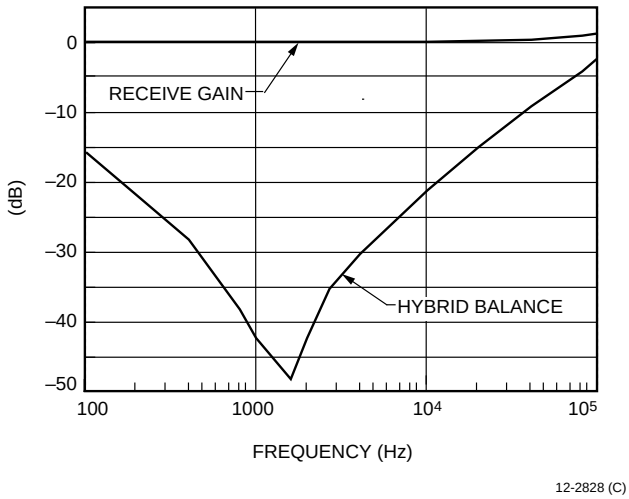


Figure 13. 7551 Receive Gain and Hybrid Balance vs. Frequency

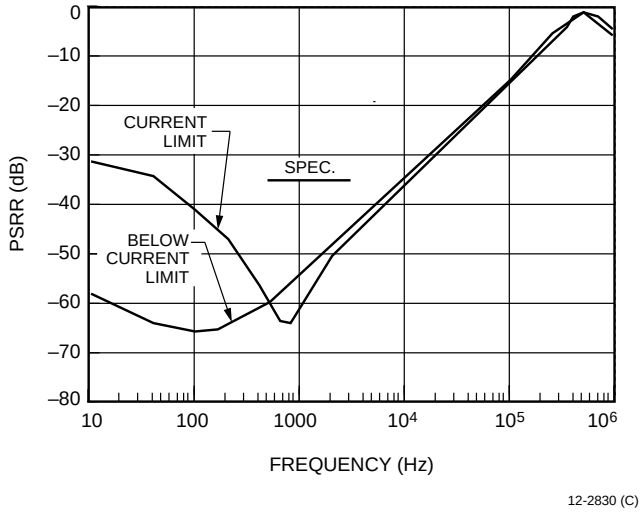


Figure 15. 7551 Typical V_{CC} Power Supply Rejection

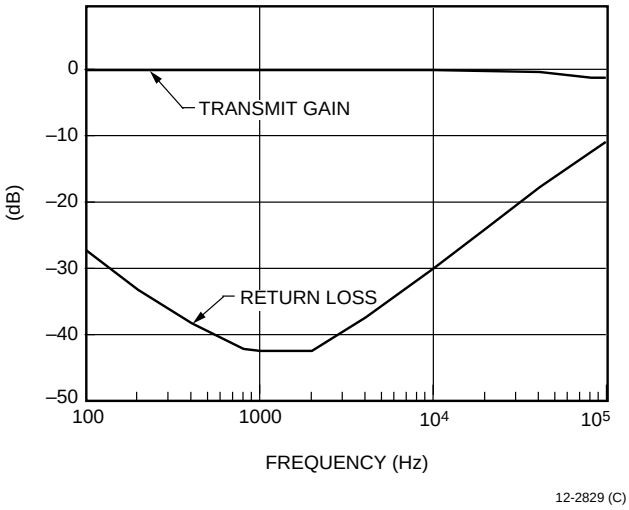


Figure 14. 7551 Transmit Gain and Return Loss vs. Frequency

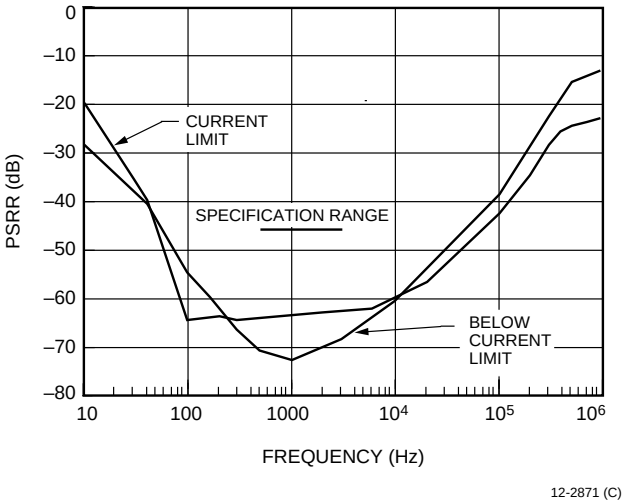
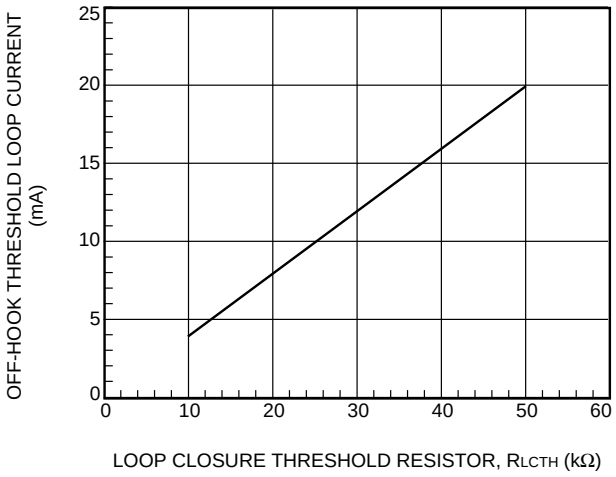


Figure 16. 7551 Typical V_{BAT} Power Supply Rejection

Applications (continued)

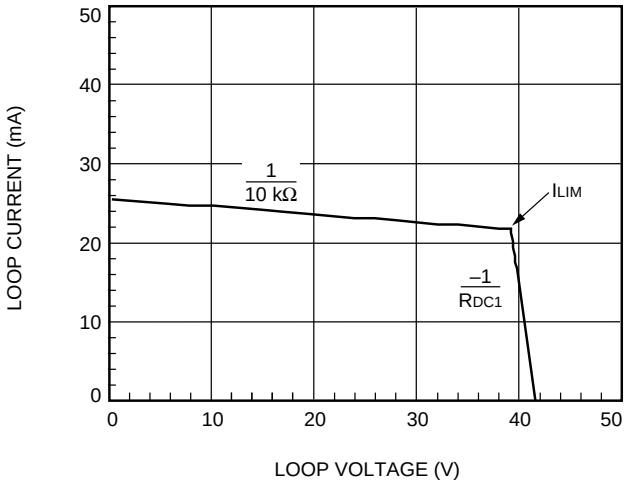
Characteristic Curves (continued)



Note: VBAT = –48 V.

12-3015 (C)

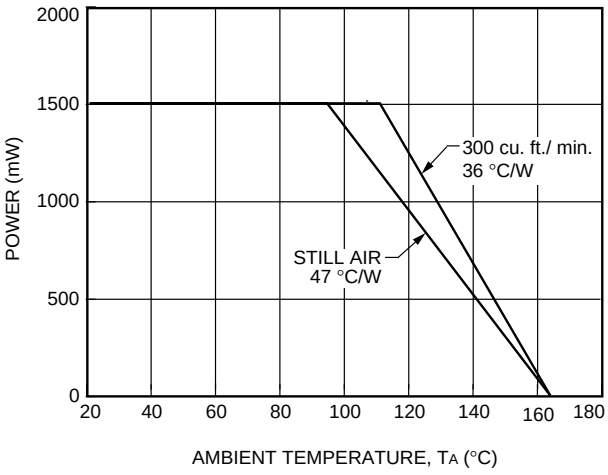
Figure 17. Loop Closure Program Resistor Selection



Note: VBAT = –48 V; ILIM = 22 mA; RDC1 = 113 Ω.

12-3050 (C)

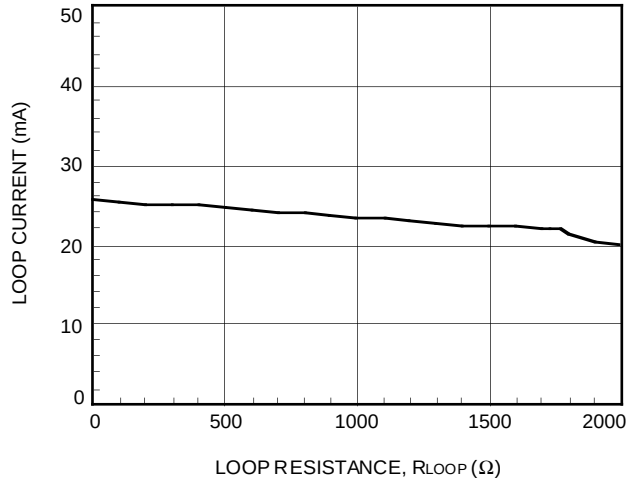
Figure 19. Loop Current vs. Loop Voltage



Note: Tip lead is open; VBAT = –48 V.

12-3016 (C)

Figure 18. Ring Ground Detection Programming



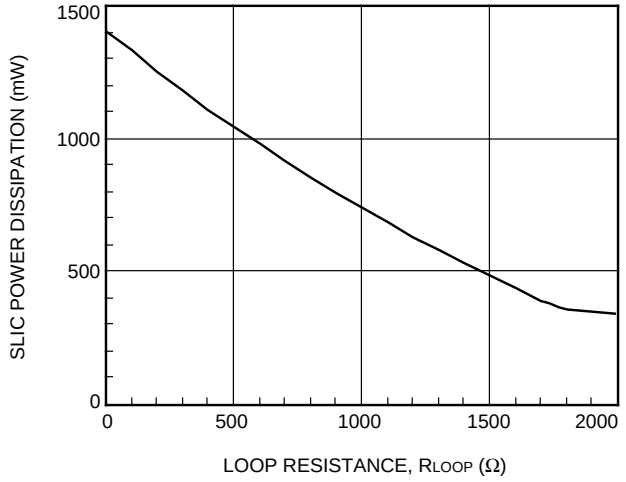
Note: VBAT = –48 V; ILIM = 22 mA; RDC1 = 113 Ω.

12-3051 (C)

Figure 20. Loop Current vs. Loop Resistance

Applications (continued)

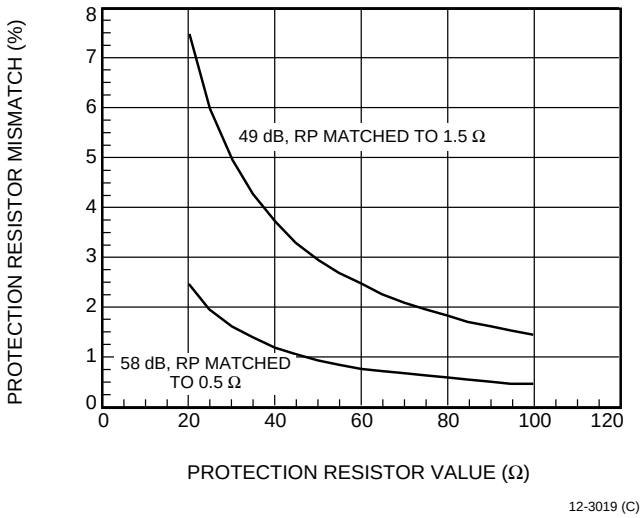
Characteristic Curves (continued)



Note: VBAT = –48 V; ILIM = 22 mA; RDC1 = 113 Ω.

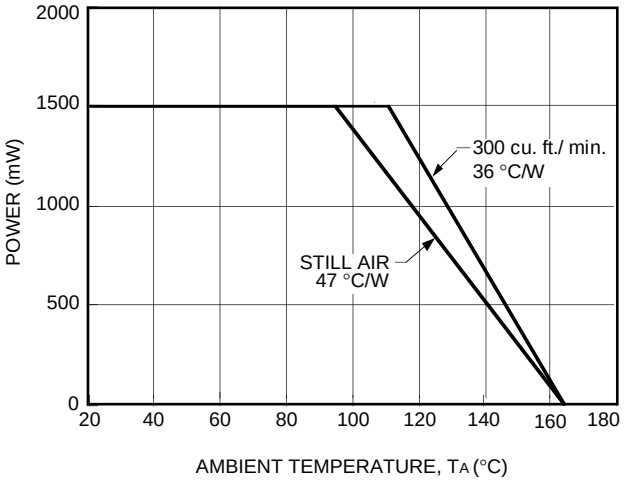
12-3052 (C)

Figure 21. 7551 Typical SLIC Power Dissipation vs. Loop Resistance



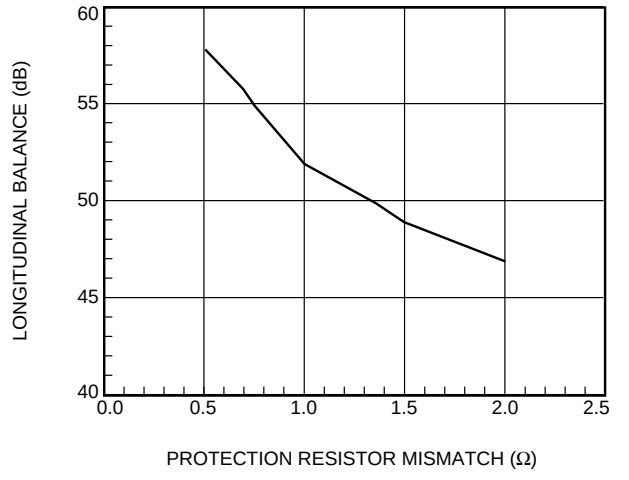
12-3019 (C)

Figure 23. Longitudinal Balance Resistor Mismatch Requirements



12-2825 (C)

Figure 22. Power Derating



12-3021 (C)

Figure 24. Longitudinal Balance vs. Protection Resistor Mismatch

Applications (continued)

dc Applications

Battery Feed

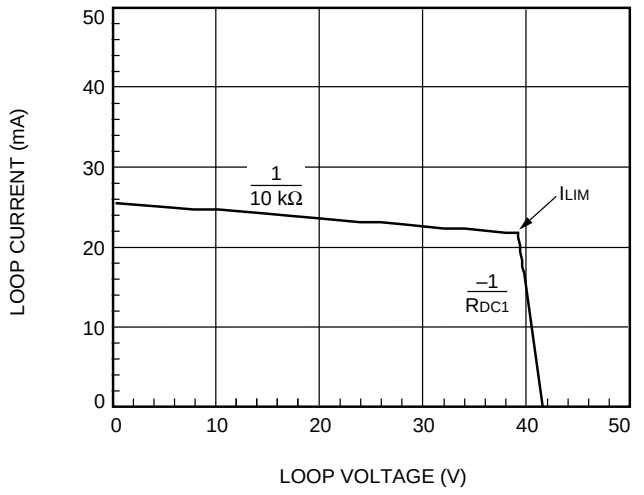
The dc feed characteristic can be described by:

$$V_{T/R} = \frac{(|V_{BAT}| - V_{OH}) \times R_L}{R_L + 2R_P + Rdc}$$

$$I_L = \frac{|V_{BAT}| - V_{OH}}{R_L + 2R_P + Rdc}$$

where:
I_L = dc loop current.
$V_{T/R}$ = dc loop voltage.
$|V_{BAT}|$ = battery voltage magnitude.
V_{OH} = overhead voltage. This is the difference between the battery voltage and the open loop Tip/Ring voltage.
R_L = loop resistance, not including protection resistors.
R_P = protection resistor value.
Rdc = SLIC internal dc feed resistance.

The design begins by drawing the desired dc template. An example is shown in Figure 25.



Note: V_{BAT} = –48 V; I_{LIM} = 22 mA; R_{DC1} = 113 Ω.

12-3050 (C)

Figure 25. Loop Current vs. Loop Voltage

Starting from the on-hook condition and going through to a short circuit, the curve passes through two regions:

Region 1; On-hook and low loop currents. The slope corresponds to the dc resistance of the SLIC, R_{DC1} (default is 113 Ω typical). The open-circuit voltage is the battery voltage less the overhead voltage of the device, V_{OH} (default is 6.5 V typical). These values are suitable for most applications, but can be adjusted if needed. For more information, see the sections entitled Adjusting dc Feed Resistance and Adjusting Overhead Voltage.

Region 2; Current limit. The dc current is limited to a value determined by external resistor R_{PROG}. This region of the dc template has a high resistance (10 kΩ).

Calculate the external resistor as follows:

$$R_{PROG}\ (k\Omega) = 1.67\ I_{LIM}\ (mA)$$

Overhead Voltage

In order to drive an on-hook ac signal, the SLIC must set up the Tip and Ring voltage to a value less than the battery voltage. The amount that the open loop voltage is decreased relative to the battery is referred to as the overhead voltage. Expressed as an equation,

$$V_{OH} = |V_{BAT}| - (V_{PT} - V_{PR})$$

Without this buffer voltage, amplifier saturation will occur and the signal will be clipped. The 7551 is automatically set at the factory to allow undistorted on-hook transmission of a 3.17 dBm signal into a 900 Ω loop impedance. For applications where higher signal levels are needed, e.g., periodic pulse metering, the 2-wire port of the SLIC can be programmed with pin DCR.

The drive amplifiers are capable of 4 Vrms minimum (V_{AMP}). Referring to Figure 26, the internal resistance has a worst-case value of 46 Ω. So, the maximum signal the device can guarantee is:

$$V_{T/R} = 4\ V\left(\frac{|Z_{T/R}|}{|Z_{T/R}| + 2(R_P + 46)}\right)$$

Thus, $R_P \leq 35\ \Omega$ allows 2.2 Vrms metering signals. The next step is to determine the amount of overhead voltage needed. The peak voltage at output of Tip and Ring amplifiers is related to the peak signal voltage by:

$$\hat{V}_{amp} = \hat{V}_{T/R}\left(1 + \frac{2(R_P + 40\ \Omega)}{|Z_{T/R}|}\right)$$

Applications (continued)

dc Applications (continued)

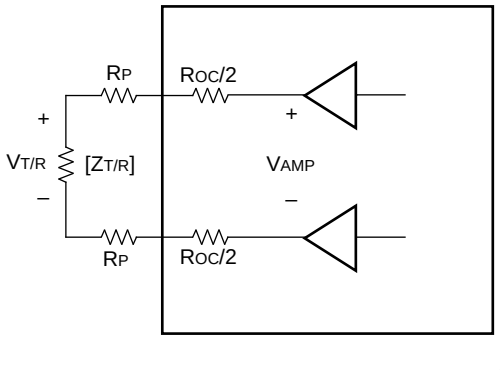


Figure 26. SLIC 2-Wire Output Stage

In addition to the required peak signal level, the SLIC needs about 2 V from each power supply to bias the amplifier circuitry. It can be thought of as an internal saturation voltage. Combining the saturation voltage and the peak signal level, the required overhead can be expressed as:

$$V_{OH} = V_{SAT} + \left(1 + \frac{2(R_P + 40\,\Omega)}{|Z_{T/R}|}\right)\hat{V}_{T/R}$$

$$= V_{SAT} + \left(1 + \frac{2(R_P + 40\,\Omega)}{|Z_{T/R}|}\right)\sqrt{\frac{2|Z_{T/R}|}{1000}} \times 10^{dBm/20}$$

where V_{SAT} is the combined internal saturation voltage between the Tip/Ring amplifiers and V_{SAT} (4.0 V typ.). R_P (Ω) is the protection resistor value, and 40 Ω is the output series resistance of each internal amplifier. $Z_{T/R}$ (Ω) is the ac loop impedance.

Example 1, On-hook Transmission of a Meter Pulse:

Signal level: 2.2 Vrms into 200 Ω
35 Ω protection resistors
I_{LOOP} = 0 (on-hook transmission of the metering signal)

$$V_{OH} = 4.0 + \left(1 + \frac{2(35 + 40)}{200}\right)\sqrt{2}(2.2)$$

$$= 9.4\ V$$

Accounting for V_{SAT} tolerance of 0.5 V, a nominal overhead of 9.9 V would ensure transmission of an undistorted 2.2 V metering signal.

Adjusting Overhead Voltage

To adjust the open loop 2-wire voltage, pin DCR is programmed at the midpoint of a resistive divider from ground to either –5 V or V_{BAT}. In the case of –5 V, the overhead voltage will be independent of the battery voltage. Figure 27 shows the equivalent input circuit to adjust the overhead.

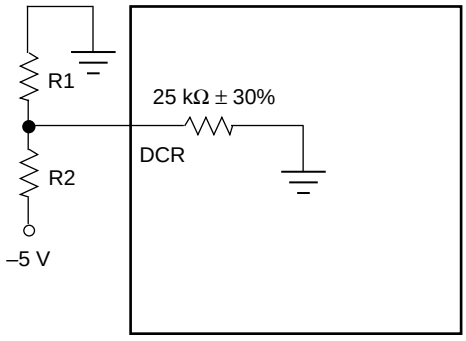


Figure 27. Equivalent Circuit for Adjusting the Overhead Voltage

The overhead voltage is programmed by using the following equation:

$$V_{OH} = 6.5 - 4\,V_{DCR}$$

$$= 6.5 - 4\left(-5 \times \left(\frac{R_1 \parallel 25\,k\Omega}{R_2 + R_1 \parallel 25\,k\Omega}\right)\right)$$

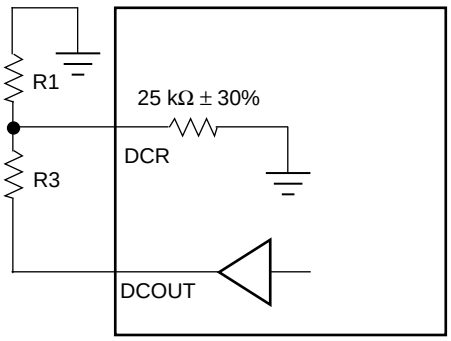
$$= 6.5 + 20\left(\frac{R_1 \parallel 25\,k\Omega}{R_2 + R_1 \parallel 25\,k\Omega}\right)$$

Applications (continued)

dc Applications (continued)

Adjusting dc Feed Resistance

The dc feed resistance may be adjusted with the help of Figure 28.



12-2560 (C)

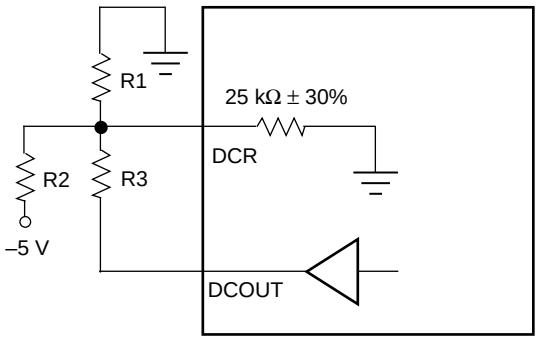
Figure 28. Equivalent Circuit for Adjusting the dc Feed Resistance

$$Rdc = 113\ \Omega + 500\ \Omega \frac{\Delta V_{DCR}}{\Delta V_{DCOUT}}$$

$$= 113\ \Omega + 500\ \Omega \left(\frac{R_1 \| 25\,k\Omega}{R_3 + R_1 \| 25\,k\Omega} \right)$$

Adjusting Overhead Voltage and dc Feed Resistance Simultaneously

The following paragraphs describe the independent setting of the overhead voltage and the dc feed resistance. If both need to be set to customized values, combine the two circuits as shown in Figure 29.



12-2561 (C)

Figure 29. Adjusting Both Overhead Voltage and dc Feed Resistance

This is an equivalent circuit for adjusting both the dc feed resistance and overhead voltage together.

The adjustments can be made by the simple superposition of the overhead and dc feed equations:

$$V_{OH} = 6.5 + 20\left(\frac{R_1 \| 25\ k\Omega \| R_3}{R_2 + R_1 \| 25\ k\Omega \| R_3} \right)$$

$$Rdc = 113\ \Omega + 500\ \Omega \left(\frac{R_1 \| 25\ k\Omega}{R_3 + R_1 \| 25\ k\Omega} \right)$$

When selecting external components, select R1 on the order of 5 kΩ to minimize the programming inaccuracy caused by the internal 25 kΩ resistor. Lower values can be used; the only disadvantage is the power consumption of the external resistors.

Loop Range

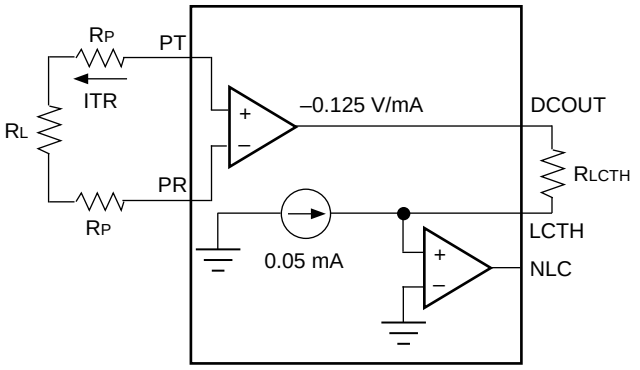
The equation below can be rearranged to provide the loop range for a required loop current:

$$R_L = \frac{|V_{BAT}| - V_{OH}}{I_L} - 2R_P - Rdc$$

Off-Hook Detection

The loop closure comparator has built-in longitudinal rejection, eliminating the need for an external 60 Hz filter. This applies in both powerup and low-power scan states. The loop-closure detection threshold is set by resistor R_{LCTH}. Referring to Figure 30, NLC is high in an on-hook condition ($I_{TR} = 0$, $V_{DCOUT} = 0$), and $V_{LCTH} = 0.05\ mA \times R_{LCTH}$. The off-hook comparator goes low when V_{LCTH} crosses zero and then goes negative:

$$V_{LCTH} = 0.05\ mA \times R_{LCTH} + V_{DCOUT}$$
$$= 0.05 \times R_{LCTH} - 0.125\ V/mA \times I_{TR}$$
$$R_{LCTH}(k\Omega) = 2.5 \times I_{TR}(mA)$$



12-2553.a (C)

Figure 30. Off-Hook Detection Circuit

Applications (continued)

dc Applications (continued)

Ring Trip Detection

The ring trip circuit is a comparator that has a special input section optimized for this application. The equivalent circuit is shown in Figure 31, along with its use in an application using unbalanced, battery-backed ringing.

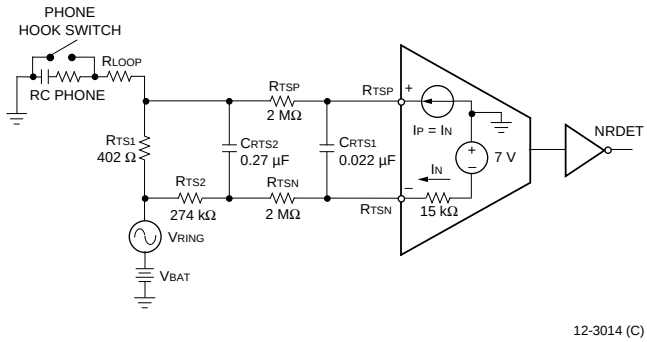


Figure 31. Ring Trip Equivalent Circuit and Equivalent Application

The comparator input voltage compliance is V_{CC} to V_{BAT}, and the maximum current is 240 µA in either direction. Its application is straightforward. A resistance (R_{TSN} + R_{TS2}) in series with the R_{TSN} input establishes a current that is repeated in the R_{TSP} input. A slightly lower resistance (R_{TSP}) is placed in series with the R_{TSP} input. When ringing is being injected, no dc current flows through R_{TS1}, so the R_{TSP} input is at a lower potential than R_{TSN}. When enough dc loop current flows, the R_{TSP} input voltage increases to trip the comparator. In Figure 31, a low-pass filter with a double pole at 2 Hz was implemented to prevent false ring trip.

The following example illustrates how the detection circuit of Figure 31 will trip at 12.5 mA dc loop current using a –48 V battery.

$$I_N = \frac{-7 - (-48)}{2.289\ k\Omega}$$

$$= 17.9\ \mu A$$

The current I_N is repeated as I_P in the positive comparator input. The voltage at comparator input R_{TSP} is:

$$V_{RTSP} = V_{BAT} + I_{LOOP(dc)} \times R_{TS1} + I_P \times R_{TSP}$$

Using this equation and the values in the example, the voltage at input R_{TSP} is –12 V during ringing injection ($I_{LOOP(dc)}$ = 0). Input R_{TSP} is, therefore, at a level of 5 V below R_{TSN}. When enough dc loop current flows through R_{TS1} to raise its dc drop to 5 V, the comparator will trip. In this example,

$$I_{LOOP(dc)} = \frac{5\ V}{402\ \Omega}$$

$$= 12.5\ mA$$

Ring Ground Detection

Pin ICM sinks a current proportional to the longitudinal loop current. It is also connected to an internal comparator whose output is pin RGDET. In a ground start application where Tip is open, the ring ground current is half differential and half common mode. In this case, to set the ring ground current threshold, connect a resistor R_{ICM} from pin ICM to V_{CC}. Select the resistor according to the following relation:

$$R_{ICM}(k\Omega) = \frac{V_{CC} \times 120}{I_{RG}(mA)}$$

The above equation is shown graphically in Figure 18. It applies for the case of Tip open. The more general equation can be used in ground key application to detect a common-mode current I_{CM}:

$$R_{ICM}(k\Omega) = \frac{V_{CC} \times 60}{I_{CM}(mA)}$$

Applications (continued)

ac Design

There are four key ac design parameters. **Termination impedance** is the impedance looking into the 2-wire port of the line card. It is set to match the impedance of the telephone loop in order to minimize echo return to the telephone set. **Transmit gain** is measured from the 2-wire port to the PCM highway, while **receive gain** is done from the PCM highway to the transmit port. Finally, the **hybrid balance** network cancels the unwanted amount of the receive signal that appears at the transmit port.

At this point in the design, the codec needs to be selected. The discrete network between the SLIC and the codec can then be designed. The following is a brief codec feature and selection summary.

First-Generation Codecs

These perform the basic filtering, A/D (transmit), D/A (receive), and μ-law/A-law companding. They all have an op amp in front of the A/D converter for transmit gain setting and hybrid balance (cancellation at the summing node). Depending on the type, some have differential analog input stages, differential analog output stages, and μ-law/A-law selectability. This generation of codecs have the lowest cost. They are most suitable for applications with fixed gains, termination impedance, and hybrid balance.

Second-Generation Codecs

This class of devices includes a microprocessor interface for software control of the gains and hybrid balance. The hybrid balance is included in the device. ac programmability adds application flexibility and saves several passive components and also adds several I/O latches that are needed in the application. However, there is no transmit op amp, since the transmit gain and hybrid balance are set internally.

Third-Generation Codecs

This class of devices includes the gains, termination impedance, and hybrid balance—all under microprocessor control. Depending on the device, it may or may not include latches.

Selection Criteria

In the codec selection, increasing software control and flexibility are traded for device cost. To help decide, it may be useful to consider the following. Will the application require only one value for each gain and impedance? Will the board be used in different countries with different requirements? Will several versions of the board be built? If so, will one version of the board be most of the production volume? Does the application need only real termination impedance? Does the hybrid balance need to be adjusted in the field?

In the following examples, use of a first-generation codec is shown. The equations for second- and third-generation codecs are simply subsets of these. There are two examples: The first shows the simplest circuit, which uses a minimum number of discrete components to synthesize a real termination impedance. The second example shows the use of the uncommitted op amp to synthesize a complex termination. The design has been automated in a DOS-based program, available on request.

Applications (continued)

ac Design (continued)

ac equivalent circuits using a T7513 Codec are shown in Figures 32 and 33.

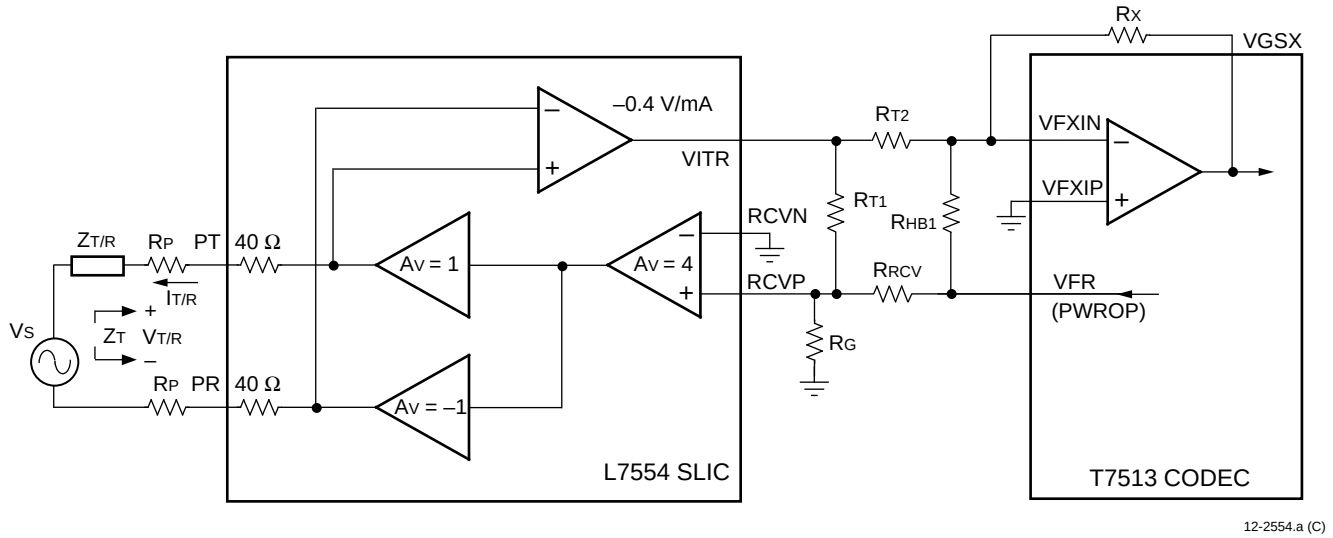


Figure 32. ac Equivalent Circuit Not Including Spare Op Amp

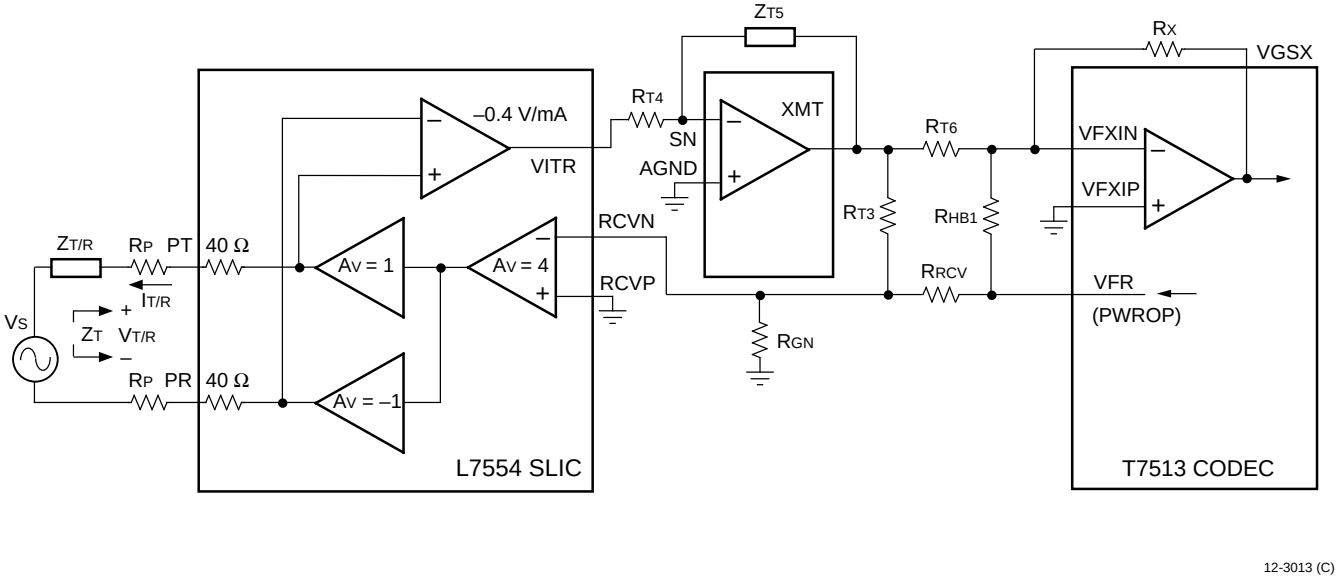


Figure 33. ac Equivalent Circuit Including Spare Op Amp

Applications (continued)

ac Design (continued)

Example 1, Real Termination

The following design equations refer to the circuit in Figure 32. Use these to synthesize real termination impedance.

Termination Impedance:

$$z_t = \frac{V_{T/R}}{-i_{tr}}$$

$$z_t = 2R_P + 80\,\Omega + \frac{3200}{1 + \frac{R_{T1}}{R_{GP}} + \frac{R_{T1}}{R_{RCV}}}$$

Receive Gain:

$$g_{rcv} = \frac{V_{T/R}}{v_{fr}}$$

$$g_{rcv} = \frac{8}{\left(1 + \frac{R_{RCV}}{R_{T1}} + \frac{R_{RCV}}{R_{GP}}\right)\left(1 + \frac{z_t}{Z_{T/R}}\right)}$$

Transmit Gain:

$$g_{tx} = \frac{v_{gsx}}{V_{T/R}}$$

$$g_{tx} = \frac{R_X}{R_{T2}} \times \frac{400}{Z_{T/R}}$$

Hybrid Balance:

$$\text{hbal} = 20\log\left(\frac{V_{gsx}}{Vfr}\right)$$

To optimize the hybrid balance, the sum of the currents at the VFX input of the codec op amp should be set to 0. The following expressions assume that the test network is the same as the termination impedance.

$$h_{bal} = 20\log\left(\frac{R_X}{R_{HB}} - g_{tx} \times g_{rcv}\right)$$

Example 2, Complex Termination:

For complex termination, the spare op amp is used (see Figure 33).

$$z_t = 2R_P + 80\,\Omega + \frac{3200}{1 + \frac{R_{T3}}{R_{GN}} + \frac{R_{T3}}{R_{RCV}}}\left(\frac{Z_{T5}}{R_{T4}}\right)$$

$$= 2R_P + 80\,\Omega + k(Z_{T5})$$

$$grcv = \frac{8}{\left(1 + \frac{R_{RCV}}{R_{T3}} + \frac{R_{RCV}}{R_{GN}}\right)\left(1 + \frac{z_t}{Z_{T/R}}\right)}$$

$$gtx = \frac{-R_X}{R_{T6}} \times \frac{400}{Z_{T/R}} \times \frac{Z_{T5}}{R_{T4}}$$

The hybrid balance equation is the same as in Example 1.

PCB Layout Information

Make the leads to BGND and V_{BAT} as wide as possible for thermal and electrical reasons. Also, maximize the amount of PCB copper in the area of—and specifically on—the leads connected to this device for the lowest operating temperature.

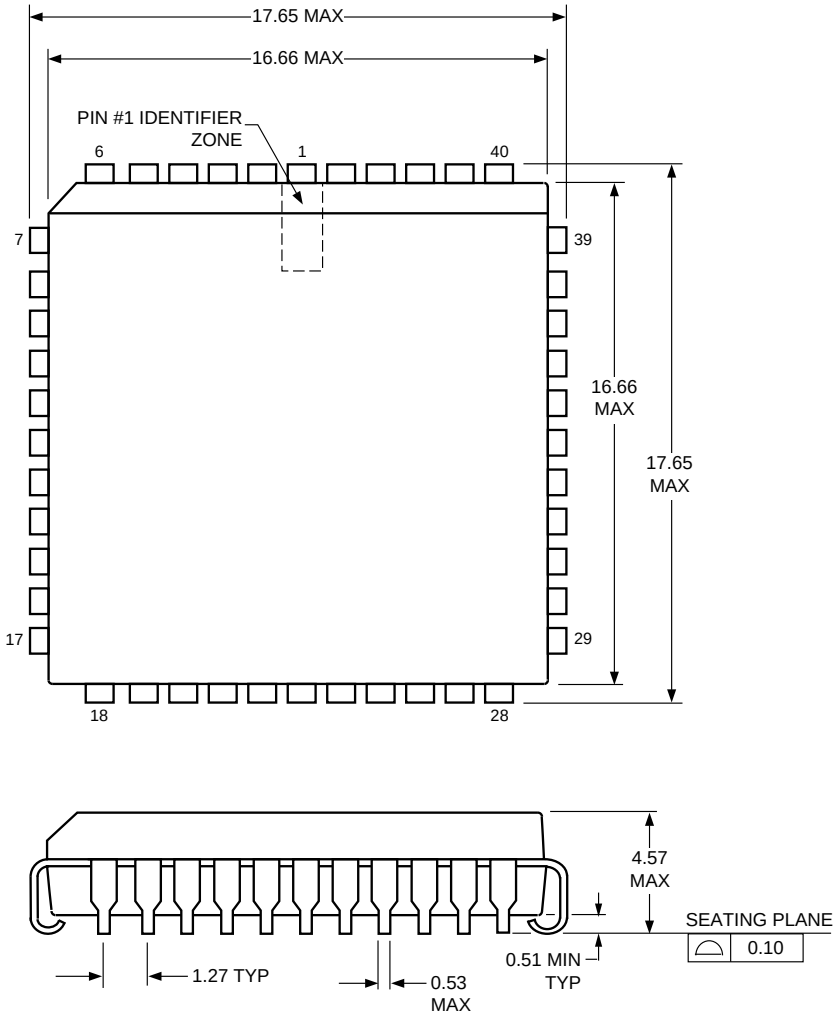
When powering the device, ensure that no external potential creates a voltage on any pin of the device that exceeds the device ratings. In this application, some of the conditions that cause such potentials during power-up are the following: 1) an inductor connected to PT and PR (this can force an overvoltage on V_{BAT} through the protection devices if the V_{BAT} connection chatters) and 2) inductance in the V_{BAT} lead (this could resonate with the V_{BAT} filter capacitor to cause a destructive overvoltage).

This device is normally used on a circuit card that is subjected to hot plug-in, meaning the card is plugged into a biased backplane connector. In order to prevent damage to the IC, all ground connections must be applied before, and removed after, all other connections.

Outline Diagram

44-Pin PLCC

Controlling dimensions are in millimeters.



5-2506r7 (C)

Ordering Information

Device Part No.	Description	Package	Comcode
ATTL7554AP	Low-Power SLIC, –60 V	44-Pin PLCC	107080921
ATTL7554AP–TR*	Low-Power SLIC, –60 V	44-Pin PLCC (Tape and Reel)	107177172
ATTL7554BP	Low-Power SLIC, –72 V	44-Pin PLCC	107548927
ATTL7554BP–TR*	Low-Power SLIC, –72 V	44-Pin PLCC (Tape and Reel)	107548943

*Devices on tape and reel must be ordered in 1000-piece increments.

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