Macronix NBit™ Memory Family

64M-BIT [x 1] CMOS SERIAL eLiteFlash™ MEMORY

FEATURES

GENERAL

- Serial Peripheral Interface (SPI) compatible -- Mode 0 and Mode 3
- 67,108,864 x 1 bit structure
- 128 Equal Sectors with 64K byte each
  - Any sector can be erased
- Single Power Supply Operation
  - 2.7 to 3.6 volt for read, erase, and program operations
- Latch-up protected to 100mA from -1V to Vcc +1V
- Low Vcc write inhibit is from 1.5V to 2.5V

PERFORMANCE

- High Performance
  - Fast access time: 50MHz serial clock (30pF + 1TTL Load)
  - Fast program time: 3ms/page (typical, 256-byte per page)
  - Fast erase time: 1s/sector (typical, 64K-byte per sector) and 128s/chip (typical)
  - Acceleration mode:
    - Program time: 2.4ms/page (typical)
    - Erase time: 0.8s/sector (typical) and 102s/chip (typical)
- Low Power Consumption
  - Low active read current: 30mA (max.) at 50MHz
  - Low active programming current: 30mA (max.)
  - Low active erase current: 38mA (max.)
  - Low standby current: 50uA (max.)
  - Deep power-down mode 1uA (typical)
- Minimum 10K erase/program cycle for array
- Minimum 100K erase/program cycle for additional 4Kb

SOFTWARE FEATURES

- Input Data Format
  - 1-byte Command code
- Auto Erase and Auto Program Algorithm
  - Automatically erases and verifies data at selected sector
  - Automatically programs and verifies data at selected page by an internal algorithm that automatically times the program pulse widths (Any page to be programed should have page in the erased state first)
- Status Register Feature
- Electronic Identification
  - JEDEC 2-byte Device ID
  - RES command, 1-byte Device ID
  - REMS command, ADD=00H will output the manufacturer's ID first and ADD=01H will output device ID first
- Additional 4Kb sector independent from main memory for parameter storage to eliminate EEPROM from system

HARDWARE FEATURES

- SCLK Input
  - Serial clock input
- SI Input
  - Serial Data Input
- SO/PO7
  - Serial Data Output or Parallel mode Data output/input
- WP#/ACC Pin
  - Hardware write protection and Program/erase acceleration
- HOLD# pin
  - pause the chip without diselecting the chip (not for paralled mode, please connect HOLD# pin to VCC during parallel mode)
- PO0~PO6
  - for parallel mode data output/input
- PACKAGE
  - 16-pin SOP (300mil)
  - **All Pb-free devices are RoHS Compliant**

GENERAL DESCRIPTION

The MX25L6405 is a CMOS 67,108,864 bit serial eLiteFlash™ Memory, which is configured as 8,388,608 x 8 internally. The MX25L6405 features a serial peripheral interface and software protocol allowing operation on a simple 3- wire bus. The three bus signals are a clock input (SCLK), a serial data input (SI), and a serial data output (SO). SPI access to the device is enabled by CS# input.

The MX25L6405 provide sequential read operation on whole chip. User may start to read from any byte of the array. While the end of the array is reached, the device will wrap around to the beginning of the array and continuously outputs data until CS# goes high.

After program/erase command is issued, auto program/ erase algorithms which program/erase and verify the specified page locations will be executed. Program command is executed on a page (256 bytes) basis, and erase command is executed on both chip and sector (64K bytes) basis.

To provide user with ease of interface, a status register is included to indicate the status of the chip. The status read command can be issued to detect completion and error flag status of a program or erase operation.

To increase user's factory throughputs, a parallel mode is provided. The performance of read/program is dramatically improved than serial mode on programmer machine.

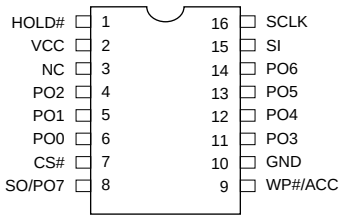
When the device is not in operation and CS# is high, it is put in standby mode and draws less than 50uA DC current.

The additional 4Kb sector with 100K erase/program endurance cycles is suitable for parameter storage and replaces the EEPROM on system.

The MX25L6405 utilizes MXIC's proprietary memory cell which reliably stores memory contents even after 10K program and erase cycles.

PIN CONFIGURATIONS

16-PIN SOP (300 mil)

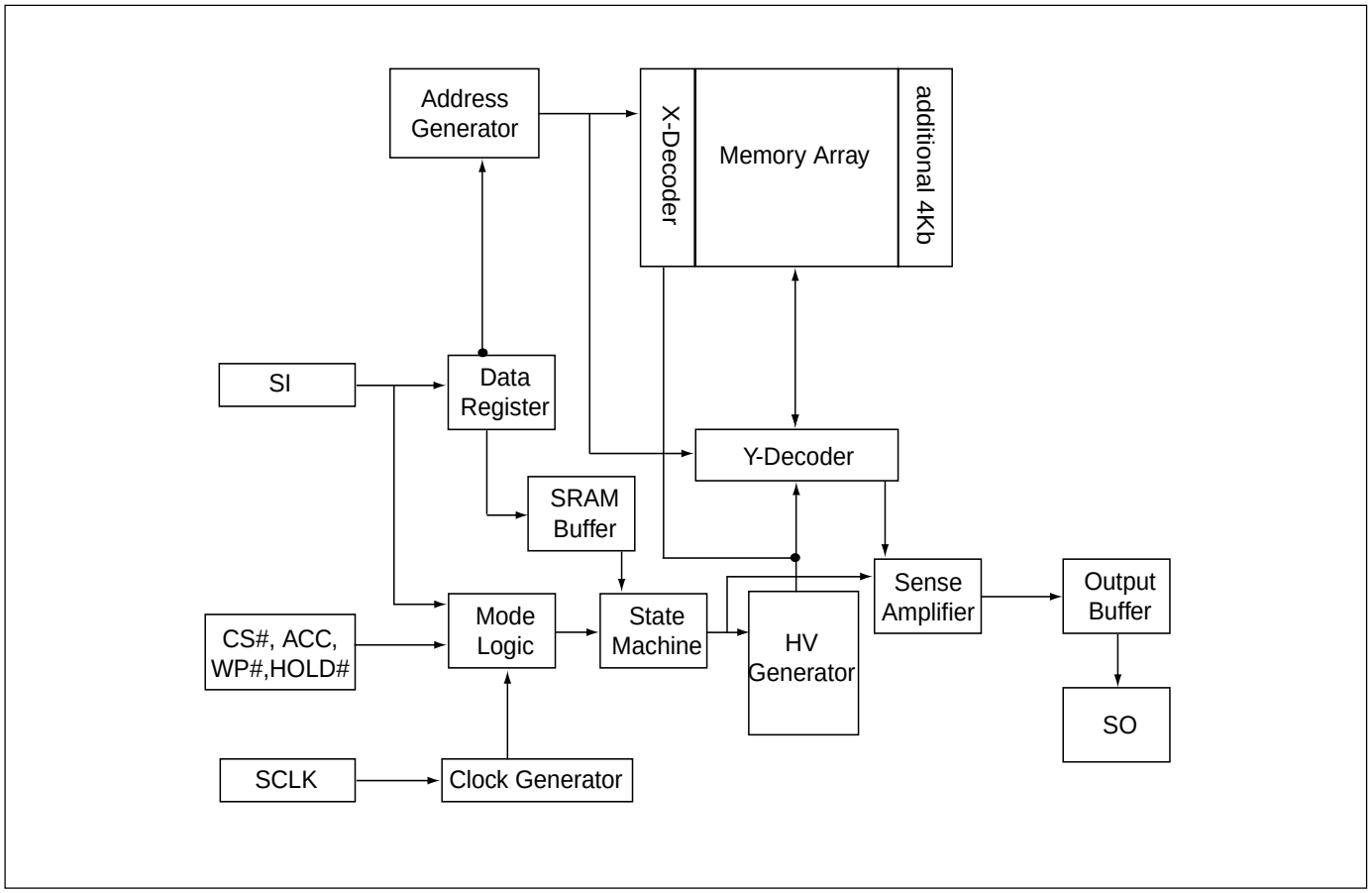


PIN DESCRIPTION

SYMBOL	DESCRIPTION
CS#	Chip Select
SI	Serial Data Input
SO/PO7(1)	Serial Data Output or Parallel Data output/input
SCLK	Clock Input
HOLD#(2)	Hold, to pause the serial communication (HOLD# is not for parallel mode)
WP#/ACC	Write Protection: connect to GND; 12V for program/erase acceleration: connect to 12V
VCC	+ 3.3V Power Supply
GND	Ground
PO0~PO6	Parallel data output/input (PO0~PO6 can be connected to NC in serial mode)
NC	No Internal Connection

Note:
1. PO0~PO7 are not provided on 8-LAND SON package.
2. HOLD# is recommended to connect to VCC during parallel mode.

BLOCK DIAGRAM



DATA PROTECTION

The MX25L6405 are designed to offer protection against accidental erasure or programming caused by spurious system level signals that may exist during power transition. During power up the device automatically resets the state machine in the Read mode. In addition, with its control register architecture, alteration of the memory contents only occurs after successful completion of specific command sequences. The device also incorporates several features to prevent inadvertent write cycles resulting from VCC power-up and power-down transition or system noise.

- Power-on reset and tPUW: to avoid sudden power switch by system power supply transition, the power-on reset and tPUW (internal timer) may protect the Flash.

- Valid command length checking: The command length will be checked whether it is at byte base and completed on byte boundary.

- Write Enable (WREN) command: WREN command is required to set the Write Enable Latch bit (WEL) before other command to change data. The WEL bit will return to reset stage under following situation:
  - Power-up
  - Write Disable (WRDI) command completion
  - Write Status Register (WRSR) command completion
  - Page Program (PP) command completion
  - Sector Erase (SE) command completion
  - Block Erase (BE) command completion
  - Chip Erase (CE) command completion

- Software Protection Mode (SPM): by using BP0-BP2 bits to set the part of Flash protected from data change.

- Hardware Protection Mode (HPM): by using WP# going low to protect the BP0-BP2 bits and SRWD bit from data change.

- Deep Power Down Mode: By entering deep power down mode, the flash device also is under protected from writing all commands except Release from deep power down mode command (RDP) and Read Electronic Signature command (RES).

Table 1. Protected Area Sizes

Status bit				Protection Area
BP3 (note2)	BP2	BP1	BP0	
0	0	0	0	None
0	0	0	1	Upper 128th (Sector 127)
0	0	1	0	Upper 64th (two sectors: 126 and 127)
0	0	1	1	Upper 32nd (four sectors: 124 to 127)
0	1	0	0	Upper sixteenth (eight sectors: 120 to 127)
0	1	0	1	Upper eigthth (sixteen sectors: 112 to 127)
0	1	1	0	Upper quarter (thirty-two sectors: 96 to 127)
0	1	1	1	Upper half (thirty-two sectors: 64 to 127)
1	0	0	0	All
1	0	0	1	
1	0	1	0	
1	0	1	1	
1	1	0	0	
1	1	0	1	
1	1	1	0	
1	1	1	1	

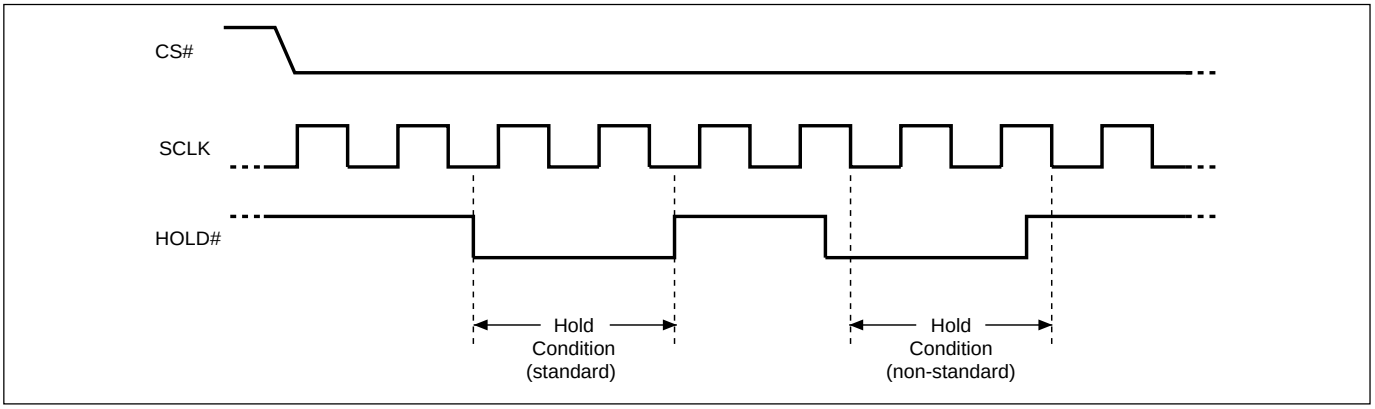
Note :
1. The device is ready to accept a Chip Erase instruction if, and only if, all Block Protect (BP3, BP2, BP1, BP0) are 0.

HOLD FEATURE

HOLD# pin signal goes low to hold any serial communications with the device. The HOLD feature will not stop the operation of write status register, programming, or erasing in progress.

The operation of HOLD requires Chip Select(CS#) keeping low and starts on falling edge of HOLD# pin signal while Serial Clock (SCLK) signal is being low (if Serial Clock signal is not being low, HOLD operation will not start until Serial Clock signal being low). The HOLD condition ends on the rising edge of HOLD# pin signal while Serial Clock(SCLK) signal is being low(if Serial Clock signal is not being low, HOLD operation will not end until Serial Clock being low), see Figure 1.

Figure 1. Hold Condition Operation

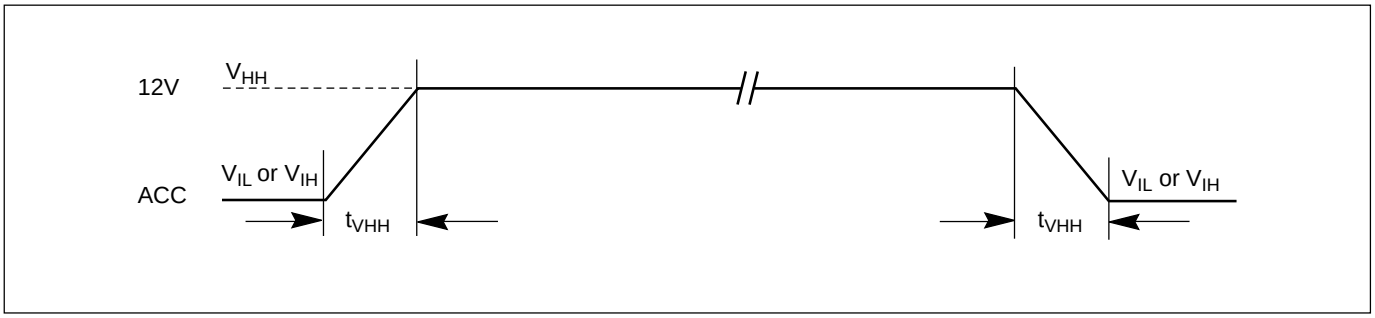


The Serial Data Output (SO) is high impedance, both Serial Data Input (SI) and Serial Clock (SCLK) are don't care during the HOLD operation. If Chip Select (CS#) drives high during HOLD operation, it will reset the internal logic of the device. To re-start communication with chip, the HOLD# must be at high and CS# must be at low.

PROGRAM/ERASE ACCELERATION

To activate the program/erase acceleration function requires ACC pin connecting to 12V voltage (see Figure 2), and then to be followed by the normal program/erase process. By utilizing the program/erase acceleration operation, the performances are improved as shown on table of "ERASE AND PROGRAM PERFORMACE".

Figure 2. ACCELERATED PROGRAM TIMING DIAGRAM



Note: tVHH (VHH Rise and Fall Time) min. 250ns

Table 2. COMMAND DEFINITION

COMMAND (byte)	WREN (write Enable)	WRDI (write disable)	RDID (read ident-ification)	RDSR (read status register)	WRSR (write status register)	READ (read data)	Fast Read (fast read data)	Parallel Mode
1st	06 Hex	04 Hex	9F Hex	05 Hex	01 Hex	03 Hex	0B Hex	55 Hex
2nd						AD1	AD1	
3rd						AD2	AD2	
4th						AD3	AD3	
5th							x	
Action	sets the (WEL) write enable latch bit	reset the (WEL) write enable latch bit	output the manufacturer ID and 2-byte device ID	to read out the status register	to write new values to the status register	n bytes read out until CS# goes high		Enter and stay in Parallel Mode until power off

COMMAND (byte)	SE (Sector Erase)	CE (Chip Erase)	PP (Page Program)	DP (Deep Power Down)	EN4K (Enter 4Kb sector)	EX4K (Exit 4Kb sector)	RDP (Release from Deep Power-down)	RES(Read Electronic ID)	REMS (Read Electronic Manufacturer & Device ID)
1st	20 or D8 Hex	60 or C7 Hex	02 Hex	B9 Hex	A5 Hex	B5 Hex	AB Hex	AB Hex	90 Hex
2nd	AD1		AD1					x	x
3rd	AD2		AD2					x	x
4th	AD3		AD3					x	ADD (1)
5th									
Action					Enter the additional 4Kb sector	Exit the additional 4Kb sector			Output the manufacturer ID and device ID

(1) ADD=00H will output the manufacturer's ID first and ADD=01H will output device ID first.

(2) It is not recommended to adopt any other code which is not in the above command definition table.

Table 3. Memory Organization

Sector	Address Range	
127	7F0000h	7FFFFFh
126	7E0000h	7EFFFFh
125	7D0000h	7DFFFFh
124	7C0000h	7CFFFFh
123	7B0000h	7BFFFFh
122	7A0000h	7AFFFFh
121	790000h	79FFFFh
120	780000h	78FFFFh
119	770000h	77FFFFh
118	760000h	76FFFFh
117	750000h	75FFFFh
116	740000h	74FFFFh
115	730000h	73FFFFh
114	720000h	72FFFFh
113	710000h	71FFFFh
112	700000h	70FFFFh
111	6F0000h	6FFFFFh
110	6E0000h	6EFFFFh
109	6D0000h	6DFFFFh
108	6C0000h	6CFFFFh
107	6B0000h	6BFFFFh
106	6A0000h	6AFFFFh
105	690000h	69FFFFh
104	680000h	68FFFFh
103	670000h	67FFFFh
102	660000h	66FFFFh
101	650000h	65FFFFh
100	640000h	64FFFFh
99	630000h	63FFFFh
98	620000h	62FFFFh
97	610000h	61FFFFh
96	600000h	60FFFFh
95	5F0000h	5FFFFFh
94	5E0000h	5EFFFFh
93	5D0000h	5DFFFFh
92	5C0000h	5CFFFFh
91	5B0000h	5BFFFFh
90	5A0000h	5AFFFFh
89	590000h	59FFFFh
88	580000h	58FFFFh

Sector	Address Range	
87	570000h	57FFFFh
86	560000h	56FFFFh
85	550000h	55FFFFh
84	540000h	54FFFFh
83	530000h	53FFFFh
82	520000h	52FFFFh
81	510000h	51FFFFh
80	500000h	50FFFFh
79	4F0000h	4FFFFFh
78	4E0000h	4EFFFFh
77	4D0000h	4DFFFFh
76	4C0000h	4CFFFFh
75	4B0000h	4BFFFFh
74	4A0000h	4AFFFFh
73	490000h	49FFFFh
72	480000h	48FFFFh
71	470000h	47FFFFh
70	460000h	46FFFFh
69	450000h	45FFFFh
68	440000h	44FFFFh
67	430000h	43FFFFh
66	420000h	42FFFFh
65	410000h	41FFFFh
64	400000h	40FFFFh
63	3F0000h	3FFFFFh
62	3E0000h	3EFFFFh
61	3D0000h	3DFFFFh
60	3C0000h	3CFFFFh
59	3B0000h	3BFFFFh
58	3A0000h	3AFFFFh
57	390000h	39FFFFh
56	380000h	38FFFFh
55	370000h	37FFFFh
54	360000h	36FFFFh
53	350000h	35FFFFh
52	340000h	34FFFFh
51	330000h	33FFFFh
50	320000h	32FFFFh
49	310000h	31FFFFh
48	300000h	30FFFFh

Sector	Address Range	
47	2F0000h	2FFFFFh
46	2E0000h	2EFFFFh
45	2D0000h	2DFFFFh
44	2C0000h	2CFFFFh
43	2B0000h	2BFFFFh
42	2A0000h	2AFFFFh
41	290000h	29FFFFh
40	280000h	28FFFFh
39	270000h	27FFFFh
38	260000h	26FFFFh
37	250000h	25FFFFh
36	240000h	24FFFFh
35	230000h	23FFFFh
34	220000h	22FFFFh
33	210000h	21FFFFh
32	200000h	20FFFFh
31	1F0000h	1FFFFFh
30	1E0000h	1EFFFFh
29	1D0000h	1DFFFFh
28	1C0000h	1CFFFFh
27	1B0000h	1BFFFFh
26	1A0000h	1AFFFFh
25	190000h	19FFFFh
24	180000h	18FFFFh
23	170000h	17FFFFh
22	160000h	16FFFFh
21	150000h	15FFFFh
20	140000h	14FFFFh
19	130000h	13FFFFh
18	120000h	12FFFFh
17	110000h	11FFFFh
16	100000h	10FFFFh
15	0F0000h	0FFFFFh
14	0E0000h	0EFFFFh
13	0D0000h	0DFFFFh
12	0C0000h	0CFFFFh
11	0B0000h	0BFFFFh
10	0A0000h	0AFFFFh
9	090000h	09FFFFh
8	080000h	08FFFFh
7	070000h	07FFFFh

Sector	Address Range	
6	060000h	06FFFFh
5	050000h	05FFFFh
4	040000h	04FFFFh
3	030000h	03FFFFh
2	020000h	02FFFFh
1	010000h	01FFFFh
0	000000h	00FFFFh

DEVICE OPERATION

1. Before a command is issued, status register should be checked to ensure device is ready for the intended operation.

2. When incorrect command is inputted to this LSI, this LSI becomes standby mode and keeps the standby mode until next CS# falling edge. In standby mode, SO pin of this LSI should be High-Z.

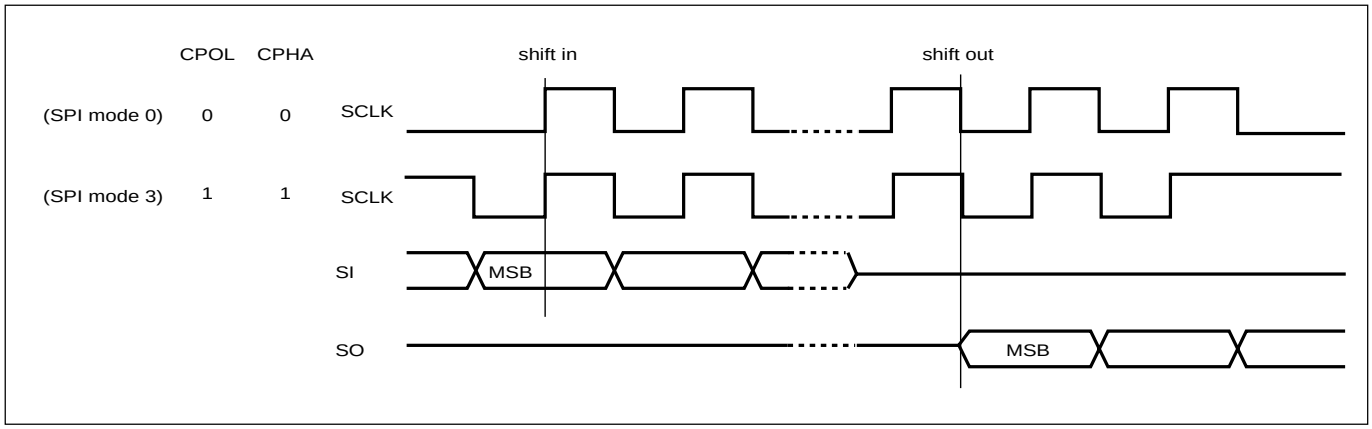
3. When correct command is inputted to this LSI, this LSI becomes active mode and keeps the active mode until next CS# rising edge.

4. Input data is latched on the rising edge of Serial Clock(SCLK) and data shifts out on the falling edge of SCLK. The difference of SPI mode 0 and mode 3 is shown as Figure 3.

5. For the following instructions: RDID, RDSR, READ, FAST_READ, RES, and REMS-the shifted-in instruction sequence is followed by a data-out sequence. After any bit of data being shifted out, the CS# can be high. For the following instructions: WREN, WRDI, WRSR, Parallel Mode, SE, CE, PP, EN4K, EX4K, RDP and DP the CS# must go high exactly at the byte boundary; otherwise, the instruction will be rejected and not executed.

6. During the progress of Write Status Register, Program, Erase operation, to access the memory array is neglected and not affect the current operation of Write Status Register, Program, Erase.

Figure 3. SPI Modes Supported



Note:
CPOL indicates clock polarity of SPI master, CPOL=1 for SCLK high while idle, CPOL=0 for SCLK low while not transmitting. CPHA indicates clock phase. The combination of CPOL bit and CPHA bit decides which SPI mode is supported.

COMMAND DESCRIPTION

(1) Write Enable (WREN)

The Write Enable (WREN) instruction is for setting Write Enable Latch (WEL) bit. For those instructions like PP, SE, CE, and WRSR, which are intended to change the device content, should be set every time after the WREN instruction setting the WEL bit.

The sequence of issuing WREN instruction is: CS# goes low-> sending WREN instruction code-> CS# goes high. (see Figure 12)

(2) Write Disable (WRDI)

The Write Disable (WRDI) instruction is for re-setting Write Enable Latch (WEL) bit.

The sequence of issuing WRDI instruction is: CS# goes low-> sending WRDI instruction code-> CS# goes high. (see Figure 13)

The WEL bit is reset by following situations:

- Power-up
- Write Disable (WRDI) instruction completion
- Write Status Register (WRSR) instruction completion
- Page Program (PP) instruction completion
- Sector Erase (SE) instruction completion
- Chip Erase (CE) instruction completion

(3) Read Identification (RDID)

The RDID instruction is for reading the manufacturer ID of 1-byte and followed by Device ID of 2-byte. The MXIC Manufacturer ID is C2(hex), the memory type ID is 20(hex) as the first-byte device ID, and the individual device ID of second-byte ID is as followings: 17(hex) for MX25L6405.

The sequence of issuing RDID instruction is: CS# goes low-> sending RDID instruction code -> 24-bits ID data out on SO -> to end RDID operation can use CS# to high at any time during data out. (see Figure. 14)

While Program/Erase operation is in progress, it will not decode the RDID instruction, so there's no effect on the cycle of program/erase operation which is currently in progress. When CS# goes high, the device is at standby stage.

(4) Read Status Register (RDSR)

The RDSR instruction is for reading Status Register Bits. The Read Status Register can be read at any time (even in program/erase/write status register condition) and continuously. It is recommended to check the Write in Progress (WIP) bit before sending a new instruction when a program, erase, or write status register operation is in progress.

The sequence of issuing RDSR instruction is: CS# goes low-> sending RDSR instruction code-> Status Register data out on SO (see Figure. 15)

The definition of the status register bits is as below:

WIP bit. The Write in Progress (WIP) bit, a volatile bit, indicates whether the device is busy in program/erase/write status register progress. When WIP bit sets to 1, which means the device is busy in program/erase/write status register progress. When WIP bit sets to 0, which means the device is not in progress of program/erase/write status register cycle.

WEL bit. The Write Enable Latch (WEL) bit, a volatile bit, indicates whether the device is set to internal write enable latch. When WEL bit sets to 1, which means the internal write enable latch is set, the device can accept program/erase/write status register instruction. When WEL bit sets to 0, which means no internal write enable latch; the device will not accept program/erase/write status register instruction.

BP3, BP2, BP1, BP0 bits. The Block Protect (BP3, BP2, BP1, BP0) bits, non-volatile bits, indicate the protected area(as defined in table 1) of the device to against the program/erase instruction without hardware protection mode being set. To write the Block Protect (BP3, BP2, BP1, BP0) bits requires the Write Status Register (WRSR) instruction to be executed. Those bits define the protected area of the memory to against Page Program (PP), Sector Erase (SE), and Chip Erase(CE) instructions (only if all Block Protect bits set to 0, the CE instruction can be executed)

Program/erase error bit. When the program/erase bit set to 1, there is an error occurred in last program/erase operation. The Flash may accept a new program/erase command to re-do program/erase operation.

SRWD bit. The Status Register Write Disable (SRWD) bit, non-volatile bit, is operated together with Write Protection (WP#) pin for providing hardware protection mode. The hardware protection mode requires SRWD sets to 1 and WP# pin signal is low stage. In the hardware protection mode, the Write Status Register (WRSR) instruction is no longer accepted for execution and the SRWD bit and Block Protect bits (BP3, BP2, BP1, BP0) are read only.

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
SRWD Status Register Write Protect	Program/ erase error	BP3 the level of protected block	BP2 the level of protected block	BP1 the level of protected block	BP0 the level of protected block	WEL (write enable latch)	WIP (write in progress bit)
1= status register write disable	1=error	(note 1)	(note 1)	(note 1)	(note 1)	1=write enable 0=not write enable	1=write operation 0=not in write operation

Note: 1. see the table "Protected Area Sizes"

(5) Write Status Register (WRSR)

The WRSR instruction is for changing the values of Status Register Bits. Before sending WRSR instruction, the Write Enable (WREN) instruction must be decoded and executed to set the Write Enable Latch (WEL) bit in advance. The WRSR instruction can change the value of Block Protect (BP3, BP2, BP1, BP0) bits to define the protected area of memory (as shown in table 1). The WRSR also can set or reset the Status Register Write Disable (SRWD) bit in accordance with Write Protection (WP#) pin signal. The WRSR instruction cannot be executed once the Hardware Protected Mode (HPM) is entered.

The sequence of issuing WRSR instruction is: CS# goes low-> sending WRSR instruction code-> Status Register data on SI-> CS# goes high. (see Figure 16)

The WRSR instruction has no effect on b6, b1, b0 of the status register for 64Mb device.

The CS# must go high exactly at the byte boundary; otherwise, the instruction will be rejected and not executed. The self-timed Write Status Register cycle time (tW) is initiated as soon as Chip Select (CS#) goes high. The Write in Progress (WIP) bit still can be check out during the Write Status Register cycle is in progress. The WIP sets 1 during the tW timing, and sets 0 when Write Status Register Cycle is completed, and the Write Enable Latch (WEL) bit is reset.

Table 4. Protection Modes

Mode	Status register condition	WP# and SRWD bit status	Memory
Software protection mode(SPM)	Status register can be written in (WEL bit is set to "1") and the SRWD, BP0-BP2 bits can be changed	WP#=1 and SRWD bit=0, or WP#=0 and SRWD bit=0, or WP#=1 and SRWD=1	The protected area cannot be program or erase.
Hardware protection mode (HPM)	The SRWD, BP0-BP2 of status register bits cannot be changed	WP#=0, SRWD bit=1	The protected area cannot be program or erase.

Note:
1. As defined by the values in the Block Protect (BP3, BP2, BP1, BP0) bits of the Status Register, as shown in Table 1.

As the above table showing, the summary of the Software Protected Mode (SPM) and Hardware Protected Mode (HPM).

Software Protected Mode (SPM):
- When SRWD bit=0, no matter WP# is low or high, the WREN instruction may set the WEL bit and can change the values of SRWD, BP3, BP2, BP1, BP0. The protected area, which is defined by BP3, BP2, BP1, BP0, is at software protected mode (SPM).
- When SRWD bit=1 and WP# is high, the WREN instruction may set the WEL bit can change the values of SRWD, BP3, BP2, BP1, BP0. The protected area, which is defined by BP3, BP2, BP1, BP0, is at software protected mode (SPM)

Note: If SRWD bit=1 but WP# is low, it is impossible to write the Status Register even if the WEL bit has previously been set. It is rejected to write the Status Register and not be executed.

Hardware Protected Mode (HPM):
- When SRWD bit=1, and then WP# is low (or WP# is low before SRWD bit=1), it enters the hardware protected mode (HPM). The data of the protected area is protected by software protected mode by BP3, BP2, BP1, BP0 and hardware protected mode by the WP# to against data modification.

Note: to exit the hardware protected mode requires WP# driving high once the hardware protected mode is entered. If the WP# pin is permanently connected to high, the hardware protected mode can never be entered; only can use software protected mode via BP3, BP2, BP1, BP0.

(6) Read Data Bytes (READ)

The read instruction is for reading data out. The address is latched on rising edge of SCLK, and data shifts out on the falling edge of SCLK at a maximum frequency fC. The first address byte can be at any location. The address is automatically increased to the next higher address after each byte data is shifted out, so the whole memory can be read out at a single READ instruction. The address counter rolls over to 0 when the highest address has been reached.

The sequence of issuing READ instruction is: CS# goes low-> sending READ instruction code-> 3-byte address on SI -> data out on SO-> to end READ operation can use CS# to high at any time during data out. (see Figure. 17)

(7) Read Data Bytes at Higher Speed (FAST_READ)

The FAST_READ instruction is for quickly reading data out. The address is latched on rising edge of SCLK, and data of each bit shifts out on the falling edge of SCLK at a maximum frequency fR. The first address byte can be at any location. The address is automatically increased to the next higher address after each byte data is shifted out, so the whole memory can be read out at a single FAST_READ instruction. The address counter rolls over to 0 when the highest address has been reached.

The sequence of issuing FAST_READ instruction is: CS# goes low-> sending FAST_READ instruction code-> 3-byte address on SI-> 1-dummy byte address on SI->data out on SO-> to end FAST_READ operation can use CS# to high at any time during data out. (see Figure. 18)

While Program/Erase/Write Status Register cycle is in progress, FAST_READ instruction is rejected without any impact on the Program/Erase/Write Status Register current cycle.

(8) Parallel Mode (Highly recommended for production throughputs increasing)

The parallel mode provides 8 bit inputs/outputs for increasing throughputs of factory production purpose. The parallel mode requires 55H command code, after writing the parallel mode command and then CS# going high, after that, the eLiteFlash™ Memory can be available to accept read/program/read status/read ID/RES/REMS command as the normal writing command procedure. The eLiteFlash™ Memory will be in parallel mode until VCC power-off.

a. Only effective for Read Array for normal read(not FAST_READ), Read Status, Read ID, Page Program, RES and REMS write data period. (refer to Figure 29~34)
b. For normal write command (by SI), No effect
c. Under parallel mode, the fastest access clock freq. will be changed to 1.5MHz(SCLK pin clock freq.)
d. For parallel mode, the tAA will be change to 50ns.

(9) Sector Erase (SE)

The Sector Erase (SE) instruction is for erasing the data of the chosen sector to be "1". A Write Enable (WREN) instruction must execute to set the Write Enable Latch (WEL) bit before sending the Sector Erase (SE). Any address of the sector (see table 3) is a valid address for Sector Erase (SE) instruction. The CS# must go high exactly at the byte boundary (the latest eighth of address byte been latched-in); otherwise, the instruction will be rejected and not executed.

The sequence of issuing SE instruction is: CS# goes low -> sending SE instruction code-> 3-byte address on SI -> CS# goes high. (see Figure 20)

The self-timed Sector Erase Cycle time (tSE) is initiated as soon as Chip Select (CS#) goes high. The Write in Progress (WIP) bit still can be check out during the Sector Erase cycle is in progress. The WIP sets 1 during the tSE timing, and sets 0 when Sector Erase Cycle is completed, and the Write Enable Latch (WEL) bit is reset. If the page is protected by BP3, BP2, BP1, BP0 bits, the Sector Erase (SE) instruction will not be executed on the page.

(10) Chip Erase (CE)

The Chip Erase (CE) instruction is for erasing the data of the whole chip to be "1". A Write Enable (WREN) instruction must execute to set the Write Enable Latch (WEL) bit before sending the Chip Erase (CE). Any address of the sector (see table 3) is a valid address for Chip Erase (CE) instruction. The CS# must go high exactly at the byte boundary(the latest eighth of address byte been latched-in); otherwise, the instruction will be rejected and not executed.

The sequence of issuing CE instruction is: CS# goes low-> sending CE instruction code-> CS# goes high. (see Figure 21)

The self-timed Chip Erase Cycle time (tCE) is initiated as soon as Chip Select (CS#) goes high. The Write in Progress (WIP) bit still can be check out during the Chip Erase cycle is in progress. The WIP sets 1 during the tBE timing, and sets 0 when Chip Erase Cycle is completed, and the Write Enable Latch (WEL) bit is reset. If the chip is protected by BP3, BP2, BP1, BP0 bits, the Chip Erase (CE) instruction will not be executed. It will be only executed when BP3, BP2, BP1, BP0 all set to "0".

(11) Page Program (PP)

The Page Program (PP) instruction is for programming the memory to be "0". A Write Enable (WREN) instruction must execute to set the Write Enable Latch (WEL) bit before sending the Page Program (PP). If the eight least significant address bits (A7-A0) are not all 0, all transmitted data which goes beyond the end of the current page are programmed from the start address if the same page (from the address whose 8 least significant address bits (A7-A0) are all 0). The CS# must keep during the whole Page Program cycle. The CS# must go high exactly at the byte boundary(the latest eighth of address byte been latched-in); otherwise, the instruction will be rejected and not executed. If more than 256 bytes are sent to the device, the data of the last 256-byte is programmed at the request page and previous data will be disregarded. If less than 256 bytes are sent to the device, the data is programmed at the request address of the page without effect on other address of the same page.

The sequence of issuing PP instruction is: CS# goes low-> sending PP instruction code-> 3-byte address on SI-> at least 1-byte on data on SI-> CS# goes high. (see Figure 19)

The self-timed Page Program Cycle time (tPP) is initiated as soon as Chip Select (CS#) goes high. The Write in Progress (WIP) bit still can be check out during the Page Program cycle is in progress. The WIP sets 1 during the tPP timing, and sets 0 when Page Program Cycle is completed, and the Write Enable Latch (WEL) bit is reset. If the page is protected by BP3, BP2, BP1, BP0 bits, the Page Program (PP) instruction will not be executed.

(12) Enter 4Kbit Mode (EN4K) and Exit 4Kbit Mode (EX4K)

Enter and Exit 4kbit mode (EN4K & EX4K) (see Figure 27 & 28)
EN4K and EX4K will not be executed when the chip is in busy state. Enter 4kbit mode then the read and write command will be executed on this 4kbit. All read and write command sequence is the same as the normal array. The address of this 4k bits is: A22~A9=0 (for 64Mb) and A8~A0 customer defined.

Note 1: Chip erase and WRSR will not be executed in 4kbit mode. During Enter 4Kbit Mode, the following instructions can be accepted: WREN, WRDI, RDID, RDSR, FAST_READ, READ, SE, PP, DP, RDP, RES, REMS.
Note 2: Chip erase can't erase this 4kbit
About the fail status:
Bit6 of the status register is used to state fail status, bit6=1 means program or erase have been failed. Any new write command will clear this bit.

(13) Deep Power-down (DP)

The Deep Power-down (DP) instruction is for setting the device on the minimizing the power consumption (to entering the Deep Power-down mode), the standby current is reduced from ISB1 to ISB2). The Deep Power-down mode requires the Deep Power-down (DP) instruction to enter, during the Deep Power-down mode, the device is not active and all Write/ Program/Erase instruction are ignored. When CS# goes high, it's only in standby mode not deep power-down mode. It's different from Standby mode.

The sequence of issuing DP instruction is: CS# goes low-> sending DP instruction code-> CS# goes high. (see Figure 22)

Once the DP instruction is set, all instruction will be ignored except the Release from Deep Power-down mode (RDP) and Read Electronic Signature (RES) instruction. (RES instruction to allow the ID been read out). When Power-down, the deep power-down mode automatically stops, and when power-up, the device automatically is in standby mode. For RDP instruction the CS# must go high exactly at the byte boundary (the latest eighth bit of instruction code been latched-in); otherwise, the instruction will not executed. As soon as Chip Select (CS#) goes high, a delay of tDP is required before entering the Deep Power-down mode and reducing the current to ISB2.

(14) Release from Deep Power-down (RDP), Read Electronic Signature (RES)

The Release from Deep Power-down (RDP) instruction is terminated by driving Chip Select (CS#) High. When Chip Select (CS#) is driven High, the device is put in the Stand-by Power mode. If the device was not previously in the Deep Power-down mode, the transition to the Stand-by Power mode is immediate. If the device was previously in the Deep Power-down mode, though, the transition to the Stand-by Power mode is delayed by tRES2, and Chip Se-lect (CS#) must remain High for at least tRES2(max), as specified in Table 6. Once in the Stand-by Power mode, the device waits to be selected, so that it can receive, decode and execute instructions.

RES instruction is for reading out the old style of 8-bit Electronic Signature, whose values are shown as table of ID Definitions. This is not the same as RDID instruction. It is not recommended to use for new design. For new deisng, please use RDID instruction. Even in Deep power-down mode, the RDP, RES, and REMS are also allowed to be executed, only except the device is in progress of program/erase/write cycle; there's no effect on the current program/erase/write cycle in progress.

The sequence is shown as Figure 23,24,25.

The RES instruction is ended by CS# goes high after the ID been read out at least once. The ID outputs repeatedly if

continuously send the additional clock cycles on SCLK while CS# is at low. If the device was not previously in Deep Power-down mode, the device transition to standby mode is immediate. If the device was previously in Deep Power-down mode, there's a delay of tRES2 to transit to standby mode, and CS# must remain to high at least tRES2(max). Once in the standby mode, the device waits to be selected, so it can be receive, decode, and execute instruction.

The RDP instruction is for releasing from Deep Power Down Mode.

(15) Read Electronic Manufacturer ID & Device ID (REMS)

The REMS instruction is an alternative to the Release from Power-down/Device ID instruction that provides both the JEDEC assigned manufacturer ID and the specific device ID.

The REMS instruction is very similar to the Release from Power-down/Device ID instruction. The instruction is initiated by driving the CS# pin low and shift the instruction code "90h" followed by two dummy bytes and one bytes address (A7~A0). After which, the Manufacturer ID for MXIC (C2h) and the Device ID are shifted out on the falling edge of SCLK with most significant bit (MSB) first as shown in figure 25. The Device ID values are listed in Table of ID Definitions on page 20. If the one-byte address is initially set to 01h, then the device ID will be read first and then followed by the Manufacturer ID. The Manufacturer and Device IDs can be read continuously, alternating from one to the other. The instruction is completed by driving CS# high.

Table of ID Definitions:

1. RDID:			
	manufacturer ID	memory type	memory density
MX25L6405	C2	20	17
2. RES:			
	device ID		
MX25L6405	16		
3. REMS:			
	manufacturer ID	device ID	
MX25L6405	C2	16	

POWER-ON STATE

The device is at below states when power-up:
- Standby mode (please note it is not deep power-down mode)
- Write Enable Latch (WEL) bit is reset

The device must not be selected during power-up and power-down stage unless the VCC achieves below correct level:
- VCC minimum at power-up stage and then after a delay of tVSL
- GND at power-down

Please note that a pull-up resistor on CS# may ensure a safe and proper power-up/down level.

An internal power-on reset (POR) circuit may protect the device from data corruption and inadvertent data change during power up state. When VCC is lower than VWI (POR threshold voltage value), the internal logic is reset and the flash device has no response to any command.

For further protection on the device, after VCC reaching the VWI level, a tPUW time delay is required before the device is fully accessible for commands like write enable(WREN), page program (PP), sector erase(SE), chip erase(CE) and write status register(WRSR). If the VCC does not reach the VCC minimum level, the correct operation is not guaranteed. The write, erase, and program command should be sent after the below time delay:
- tPUW after VCC reached VWI level
- tVSL after VCC reached VCC minimum level

The device can accept read command after VCC reached VCC minimum and a time delay of tVSL, even time of tPUW has not passed.
Please refer to the figure of "power-up timing".

Note:
- To stabilize the VCC level, the VCC rail decoupled by a suitable capacitor close to package pins is recommended.(generally around 0.1uF)
- At power-down stage, the VCC drops below VWI level, all operations are disable and device has no response to any command. The data corruption might occur during the stage while a write, program, erase cycle is in progress.

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

RATING	VALUE
Ambient Operating Temperature	-40°C to 85°C for Industrial grade 0°C to 70°C for Commercial grade
Storage Temperature	-55°C to 125°C
Applied Input Voltage	-0.5V to 4.6V
Applied Output Voltage	-0.5V to 4.6V
VCC to Ground Potential	-0.5V to 4.6V

Notes :
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is stress rating only and functional operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended period may affect reliability.
2. Specifications contained within the following tables are subject to change.
3. During voltage transitions, all pins may overshoot to 4.6V or -0.5V for period up to 20ns.
4. All input and output pins may overshoot to VCC+0.5V while VCC+0.5V is smaller than or equal to 4.6V.

Figure 4.Maximum Negative Overshoot Waveform

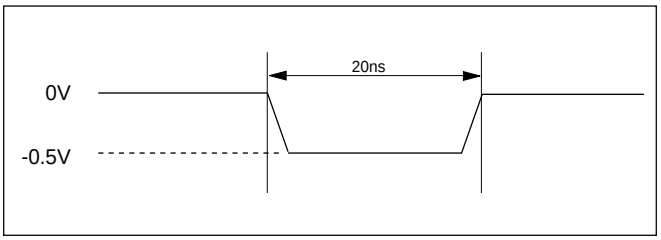
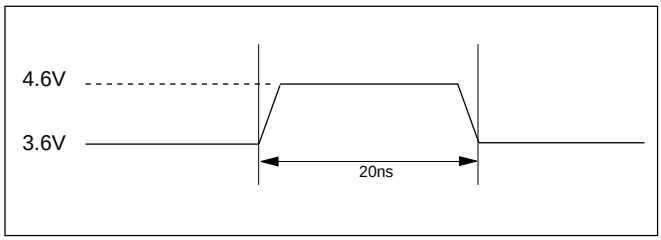


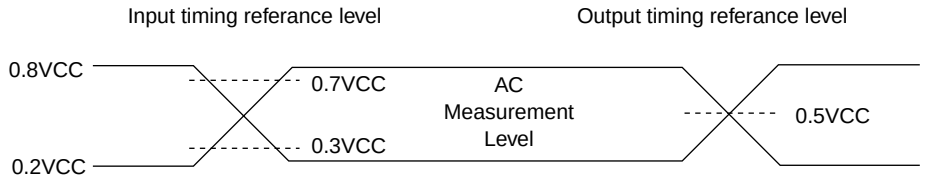
Figure 5. Maximum Positive Overshoot Waveform



CAPACITANCE TA = 25°C, f = 1.0 MHz

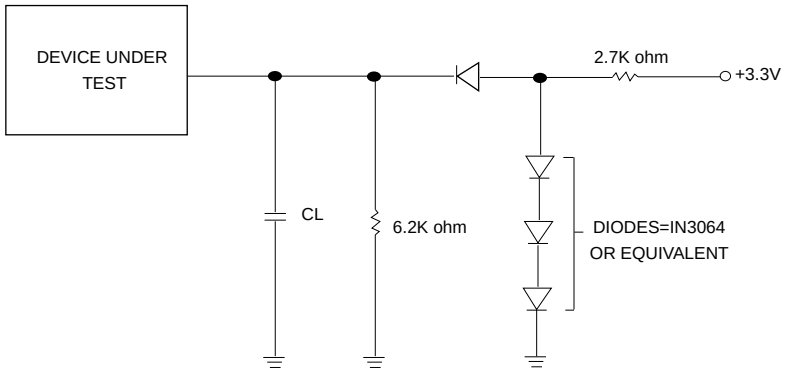
SYMBOL	PARAMETER	MIN.	TYP	MAX.	UNIT	CONDITIONS
CIN	Input Capacitance			10	pF	VIN = 0V
COUT	Output Capacitance			10	pF	VOUT = 0V

Figure 6. INPUT TEST WAVEFORMS AND MEASUREMENT LEVEL



Note: Input pulse rise and fall time are <5ns

Figure 7. OUTPUT LOADING



CL=30pF Including jig capacitance

Table 5. DC CHARACTERISTICS (Temperature = -40°C to 85°C for Industrial grade, Temperature = 0°C to 70°C for Commercial grade, VCC = 2.7V ~ 3.6V)

SYMBOL	PARAMETER	NOTES	MIN.	TYP	MAX.	UNITS	TEST CONDITIONS
ILI	Input Load Current	1			± 2	uA	VCC = VCC Max VIN = VCC or GND
ILO	Output Leakage Current	1			± 2	uA	VCC = VCC Max VIN = VCC or GND
ISB1	VCC Standby Current	1			50	uA	VIN = VCC or GND CS# = VCC
ISB2	Deep Power-down Current			1	10	uA	VIN = VCC or GND CS# = VCC
ICC1	VCC Read	1			30 30 10 20	mA mA mA mA	f=50MHz (serial) f=1.5MHz (parallel) f=20MHz (serial) f=1.2MHz (parallel)
ICC2	VCC Program Current (PP)	1			30	mA	Program in Progress CS# = VCC
ICC3	VCC Write Status Register (WRSR) Current				30	mA	Program status register in progress CS#=VCC
ICC4	VCC Sector Erase Current (SE)	1			38	mA	Erase in Progress CS#=VCC
ICC5	VCC Chip Erase Current (CE)	1			38	mA	Erase in Progress CS#=VCC
VHH	Voltage for ACC Program Acceleration	1	11.5		12.5	V	VCC=2.7V~3.6V
VIL	Input Low Voltage		-0.5		0.3VCC	V	
VIH	Input High Voltage		0.7VCC		VCC+0.4	V	
VOL	Output Low Voltage				0.4	V	IOL = 1.6mA
VOH	Output High Voltage		VCC-0.2			V	IOH = -100uA

Notes :
1. Typical values at VCC = 3.3V, T = 25°C. These currents are valid for all product versions (package and speeds).
2. Typical value is calculated by simulation.

Table 6. AC CHARACTERISTICS (Temperature = -40°C to 85°C for Industrial grade, Temperature = 0°C to 70°C for Commercial grade, VCC = 2.7V ~ 3.6V)

Symbol	Alt.	Parameter		Min.	Typ.	Max.	Unit
fSCLK	fC	Clock Frequency for the following instructions: FAST_READ, PP, SE, BE, DP, RES,REMS, RDP WREN, WRDI, RDID, RDSR, WRSR, EN4K, EX4K	Serial	D.C.		50	MHz
			Parallel			1.5	MHz
fRSCLK	fR	Clock Frequency for READ instructions	Serial	D.C.		20	MHz
			Parallel			1.2	MHz
tCH(1)	tCLH	Clock High Time	Serial	9			ns
			Parallel	180			ns
tCL(1)	tCLL	Clock Low Time	Serial	9			ns
			Parallel	180			ns
tCLCH(2)		Clock Rise Time (3) (peak to peak)	Serial	0.1			V/ns
			Parallel	2			V/ns
tCHCL(2)		Clock Fall Time (3) (peak to peak)	Serial	0.1			V/ns
			Parallel	2			V/ns
tSLCH	tCSS	S Active Setup Time (relative to C)		5			ns
tCHSL	S	Not Active Hold Time (relative to C)		5			ns
tDVCH	tDSU	Data In Setup Time		2			ns
tCHDX	tDH	Data In Hold Time		5			ns
tCHSH		S Active Hold Time (relative to C)		5			ns
tSHCH		S Not Active Setup Time (relative to C)		5			ns
tSHSL	tCSH	S Deselect Time		100			ns
tSHQZ(2)	tDIS	Output Disable Time				8	ns
tCLQV	tV	Clock Low to Output Valid				8	ns
tCLQX	tHO	Output Hold Time		0			ns
tHLCH		HOLD# Setup Time (relative to C)		5			ns
tCHHH		HOLD# Hold Time (relative to C)		5			ns
tHHCH		HOLD Setup Time (relative to C)		5			ns
tCHHL		HOLD Hold Time (relative to C)		5			ns
tHHQX(2)	tLZ	HOLD to Output Low-Z				8	ns
tHLQZ(2)	tHZ	HOLD# to Output High-Z				8	ns
tWHSL(4)		Write Protect Setup Time		20			ns
tSHWL(4)		Write Protect Hold Time		100			ns
tDP(2)		S High to Deep Power-down Mode				3	ms
tRES1(2)		S High to Standby Mode without Electronic Signature Read				30	ms
tRES2(2)		S High to Standby Mode with Electronic Signature Read				30	ms
tW		Write Status	SRWD, BP3, BP2, BP1, BP0		90	500	ms
		Register Cycle Time	WIP, WEL		20	30	ns
tPP		Page Program Cycle Time			3	12	ms
tSE		Sector Erase Cycle Time			1	3	s
tCE		Chip Erase Cycle Time			128	256	s

Notes :
1. tCH + tCL must be greater than or equal to 1/ fC
2. Value guaranteed by characterization, not 100% tested in production.
3. Expressed as a slew-rate.
4. Only applicable as a constraint for a WRSR instruction when SRWD is set at 1.
5. Test condition is shown as Figure 3.

Table 7. Power-Up Timing and VWI Threshold

Symbol	Parameter	Min.	Max.	Unit
tVSL(1)	VCC(min) to S low	30		us
tPUW(1)	Time delay to Write instruction	1	10	ms
VWI(1)	Write Inhibit Voltage	1.5	2.5	V

Note: 1. These parameters are characterized only.

INITIAL DELIVERY STATE

The device is delivered with the memory array erased: all bits are set to 1 (each byte contains FFh). The Status Register contains 00h (all Status Register bits are 0).

Figure 8. Serial Input Timing

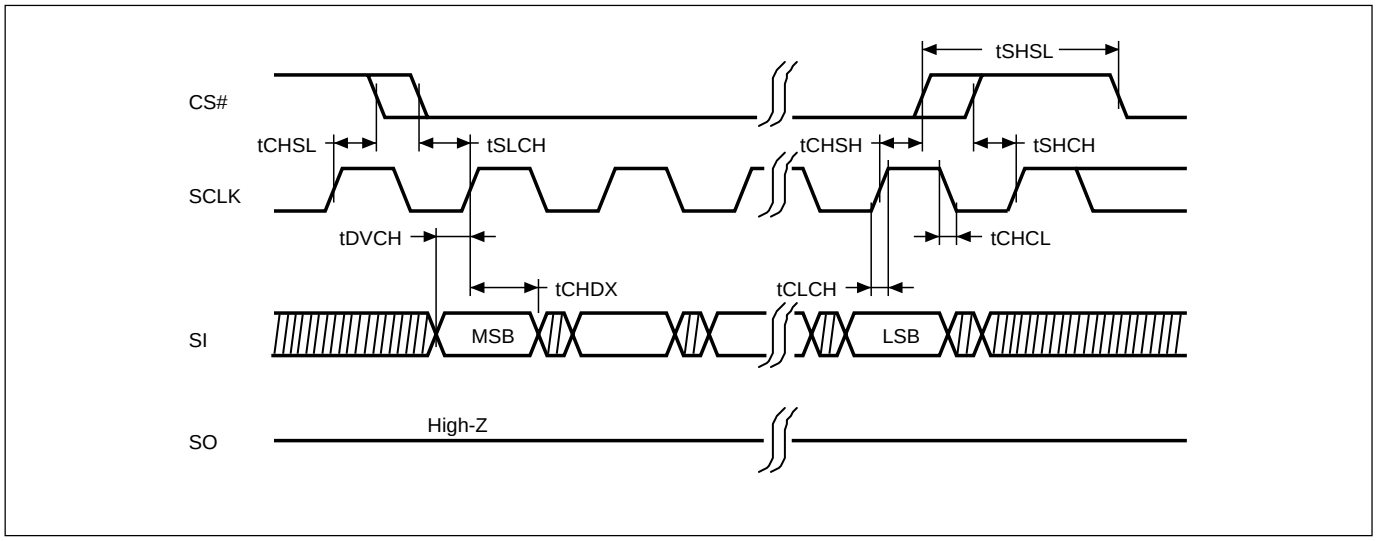


Figure 9. Output Timing

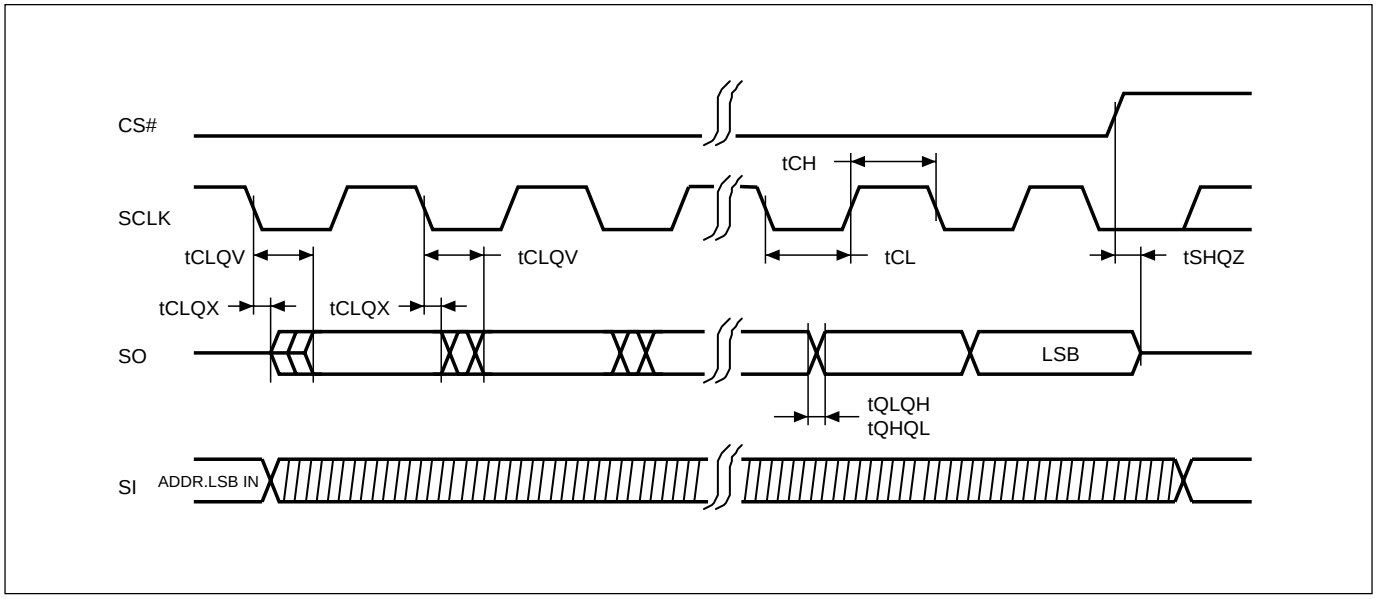
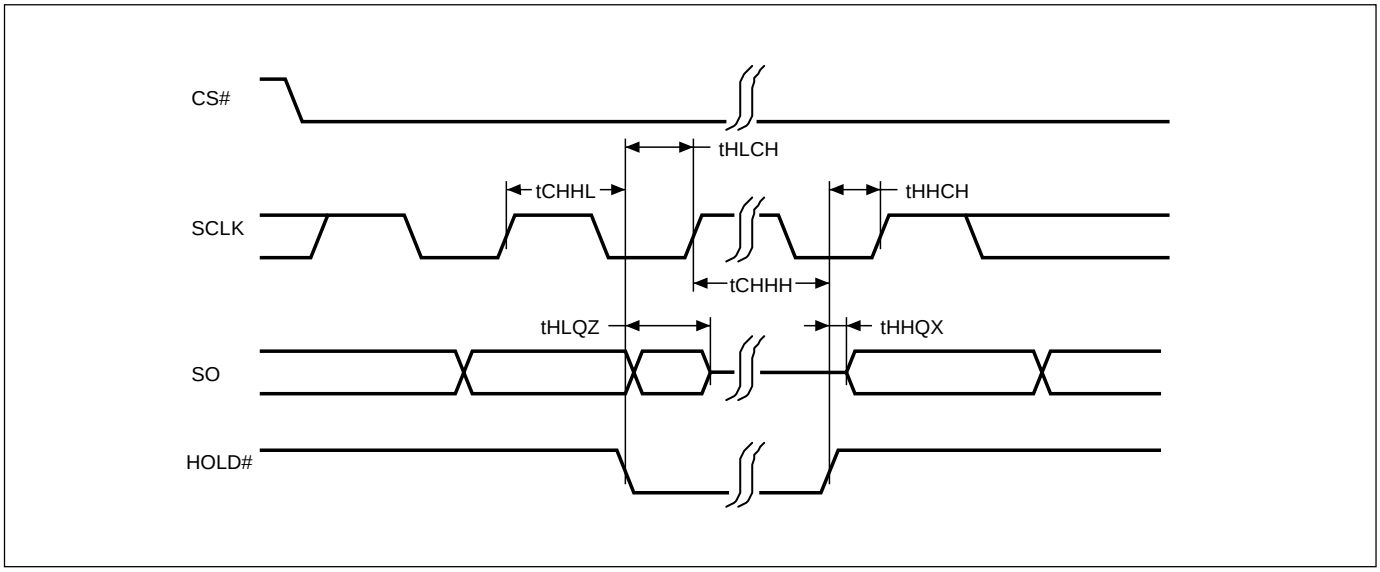


Figure 10. Hold Timing



* SI is "don't care" during HOLD operation.

Figure 11. WP# Disable Setup and Hold Timing during WRSR when SRWD=1

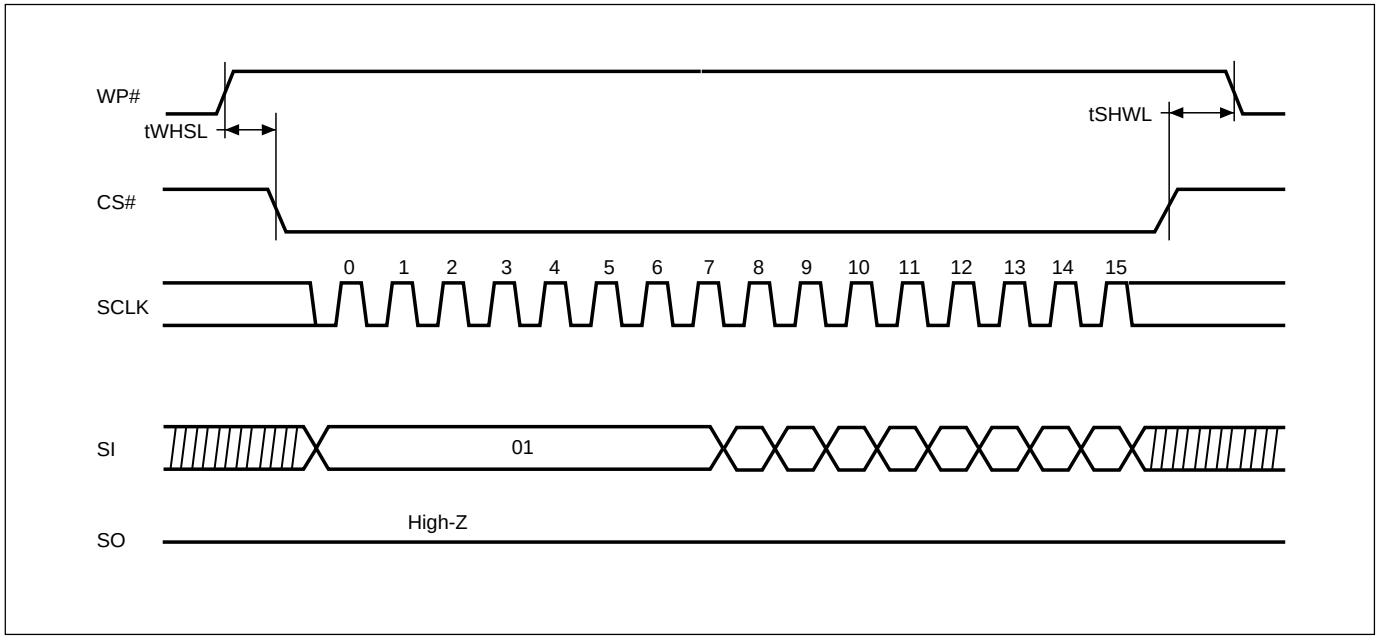


Figure 12. Write Enable (WREN) Sequence (Command 06)

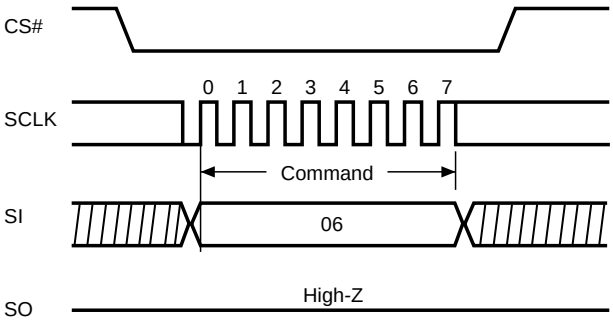


Figure 13. Write Disable (WRDI) Sequence (Command 04)

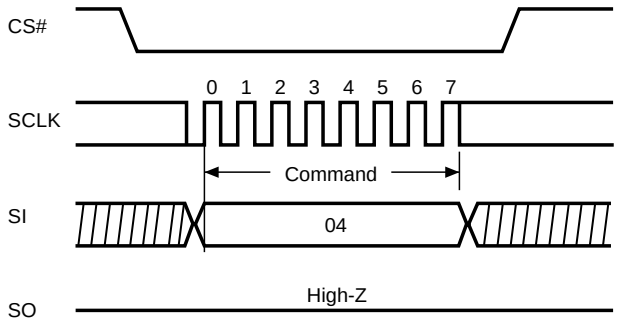
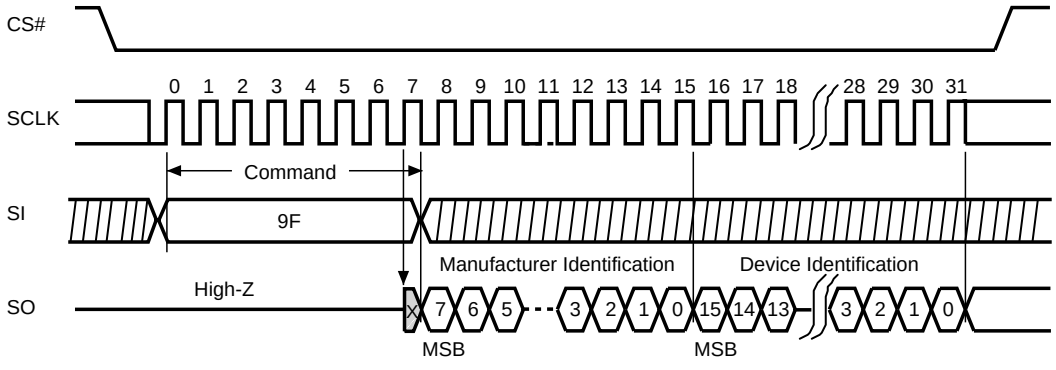
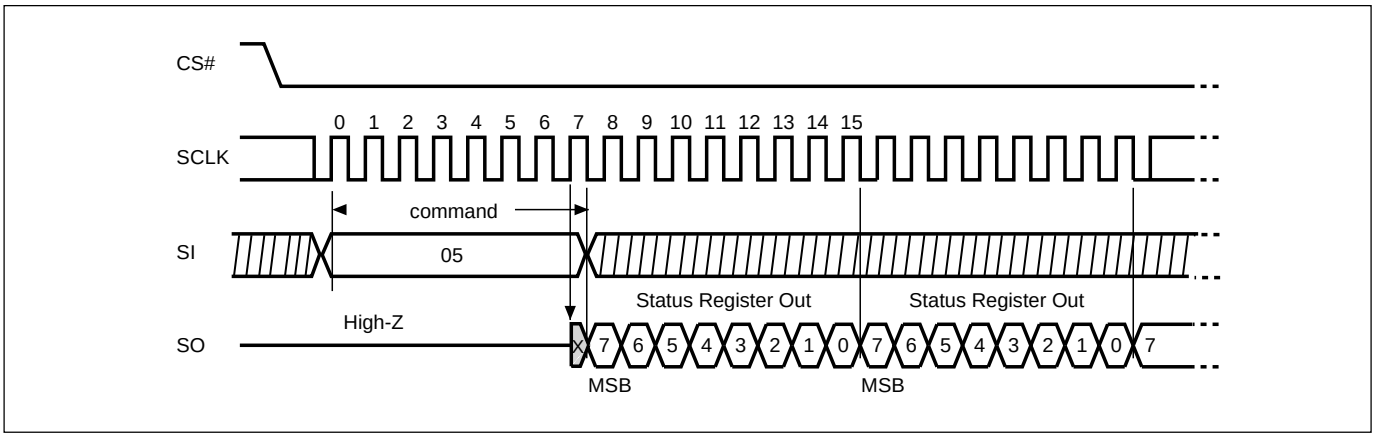


Figure 14. Read Identification (RDID) Sequence (Command 9F)



Notes: In serial RDID and RDSR mode, output pin SO will be enabled at 8th clock's rising edge. That means, MXIC's drip will enable output half a cycle in advance compare with other compatible vendor's spec.

Figure 15. Read Status Register (RDSR) Sequence (Command 05)



Notes: In serial RDID and RDSR mode, output pin SO will be enabled at 8th clock's rising edge. That means, MXIC's drip will enable output half a cycle in advance compare with other compatible vendor's spec.

Figure 16. Write Status Register (WRSR) Sequence (Command 01)

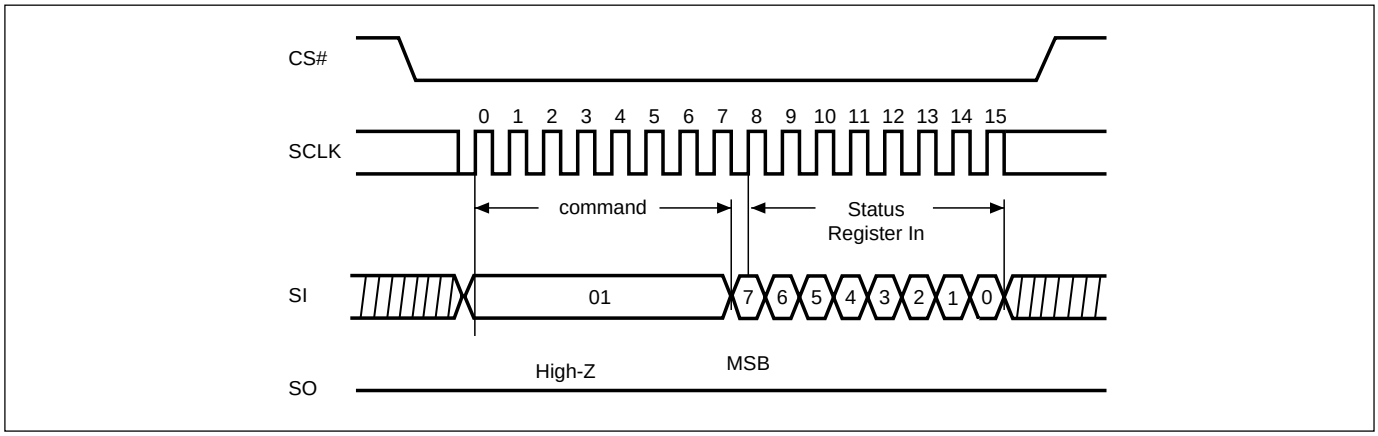
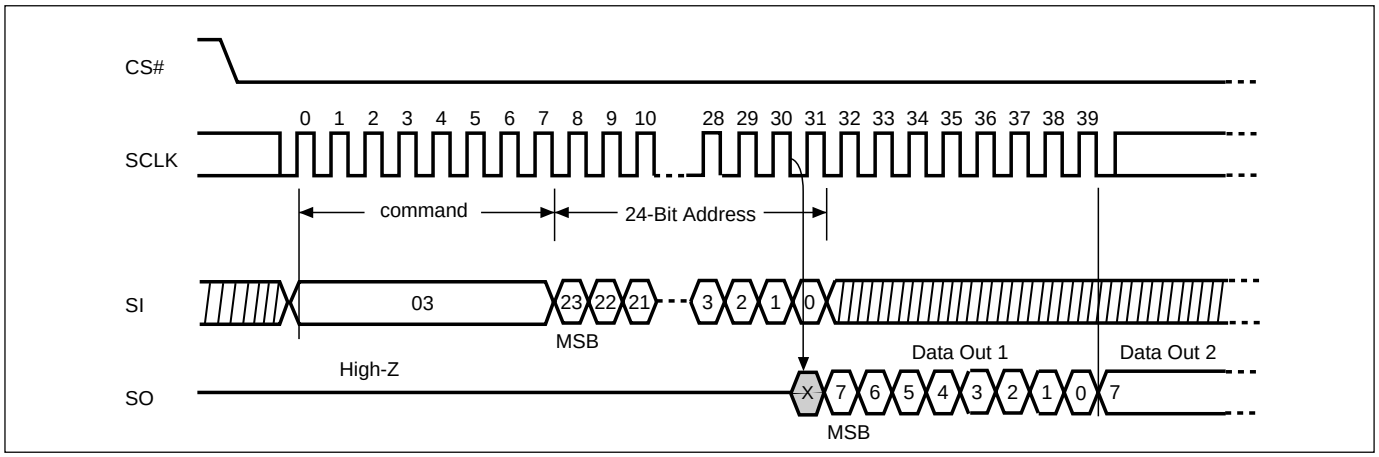
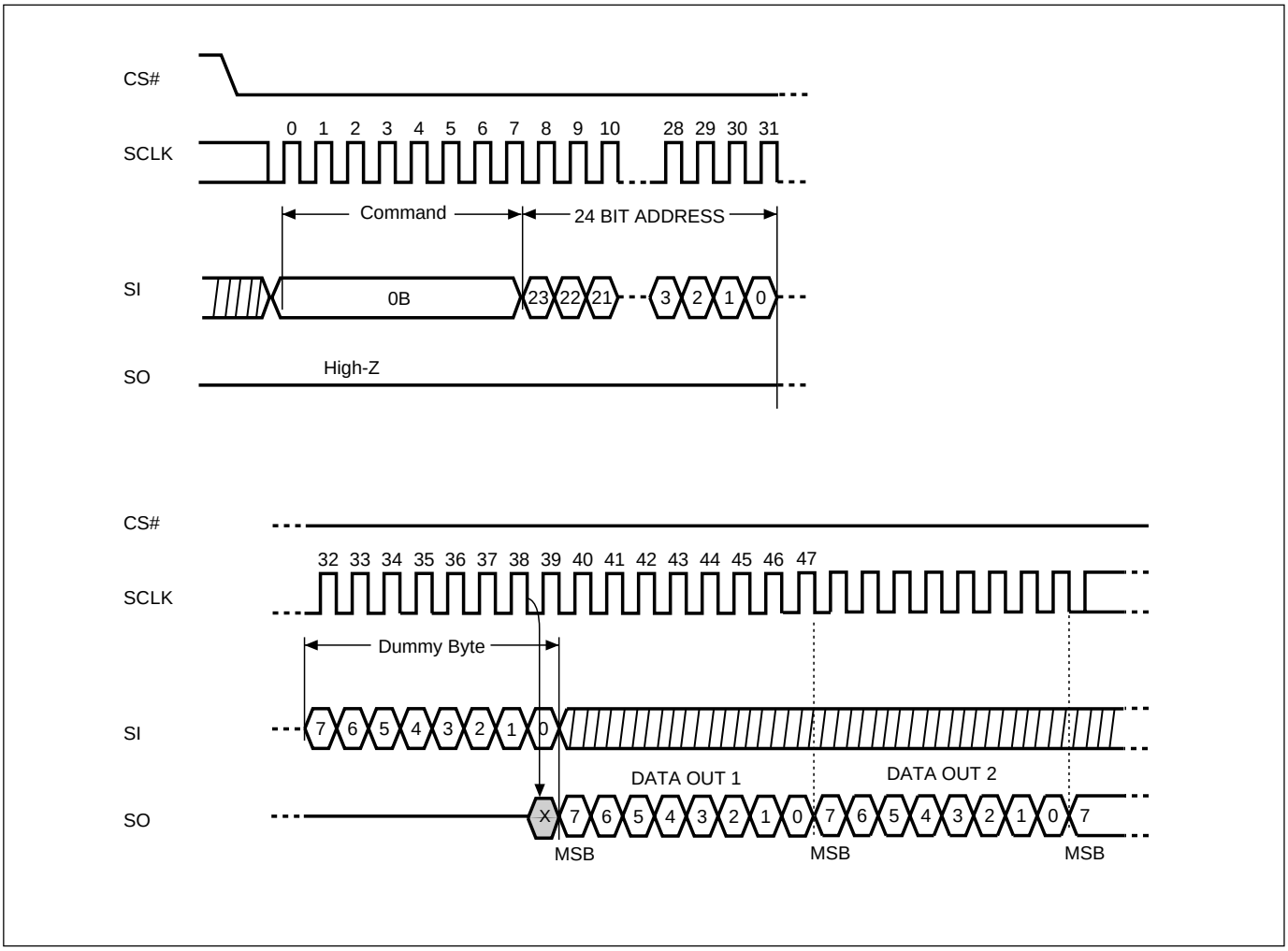


Figure 17. Read Data Bytes (READ) Sequence (Command 03)



Notes: In READ mode, FAST_READ mode, RES mode and REMS mode, MXIC IC will enable output an entire cycle in advance compare with other compatible vendor's spec. Detail condition please reference the waveform.

Figure 18. Read Data Bytes at Higher Speed (FAST_READ) Sequence (Command 0B)



Notes: In READ mode, FAST_READ mode, RES mode and REMS mode, MXIC IC will enable output an entire cycle in advance compare with other compatible vendor's spec. Detail condition please reference the waveform.

Figure 19. Page Program (PP) Instruction Sequence

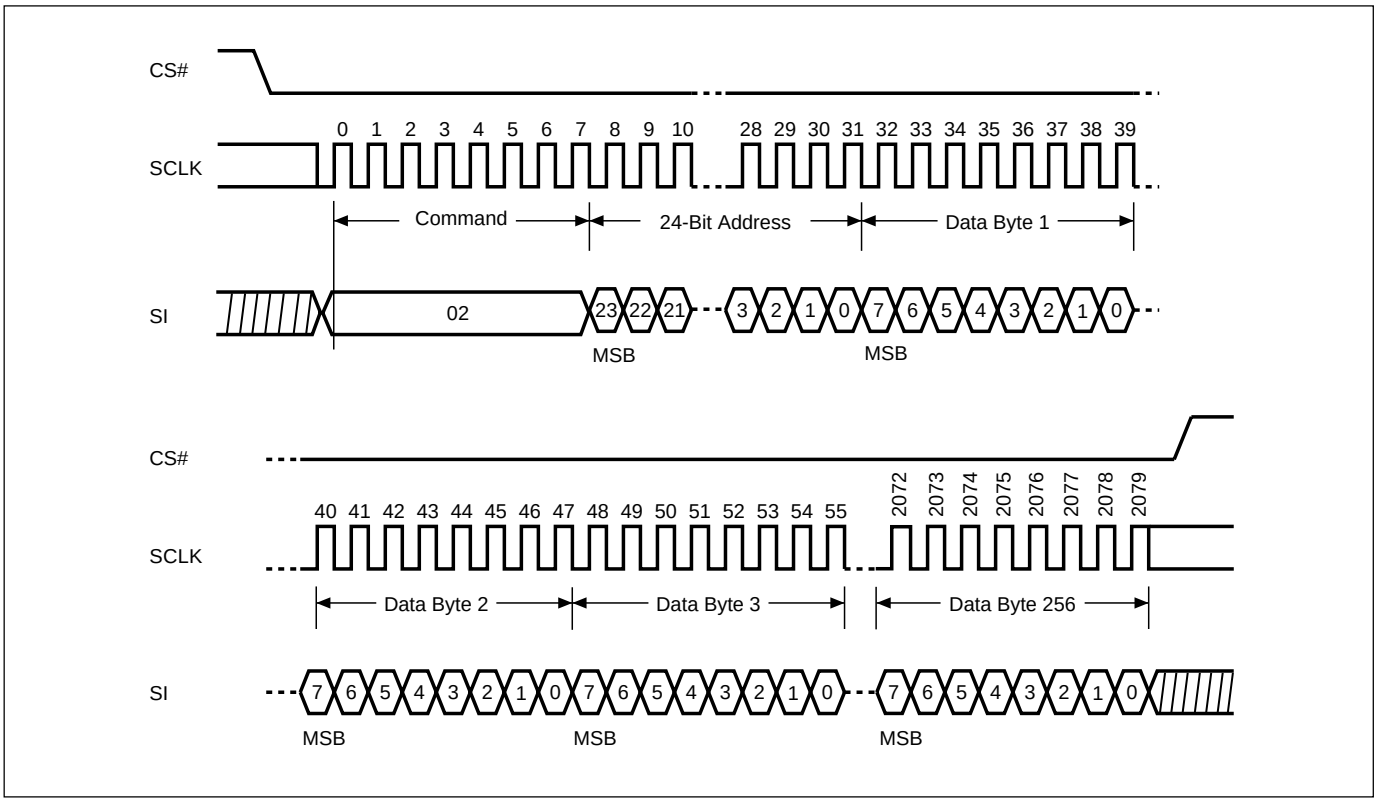
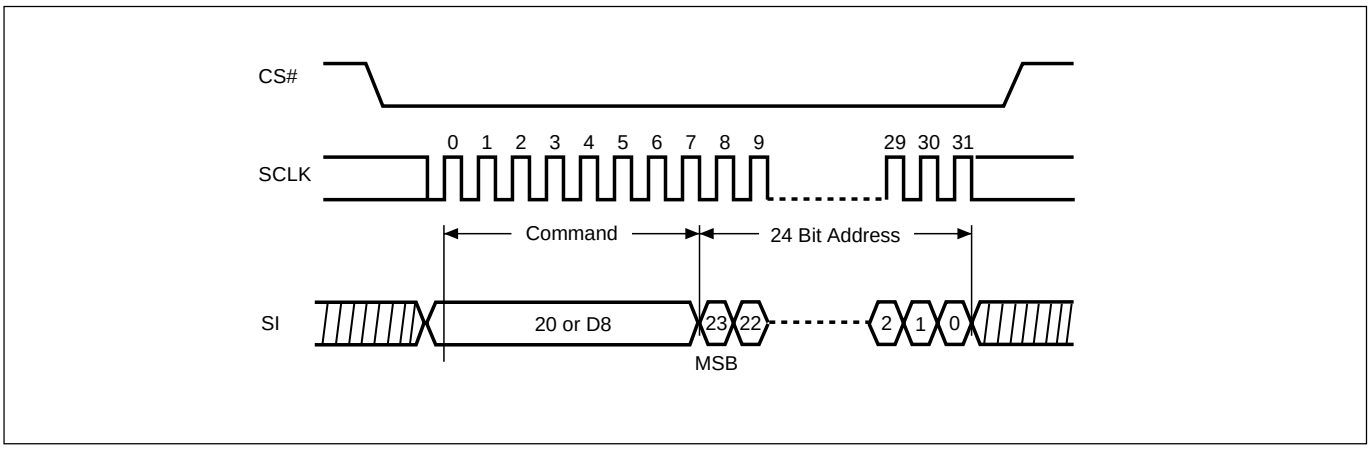
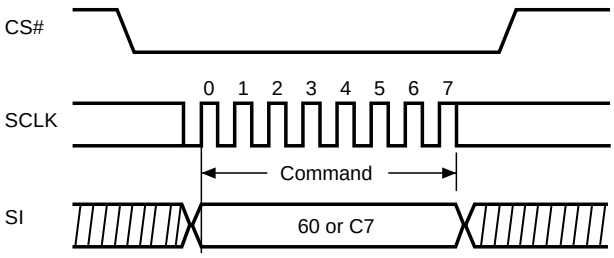


Figure 20. Sector Erase (SE) Instruction Sequence



Note: SE command is 20(hex) or D8(hex).

Figure 21. Chip Erase (CE) Sequence (Command 60 or C7)



Note: CE command is 60(hex) or C7(hex).

Figure 22. Deep Power-down (DP) Sequence (Command B9)

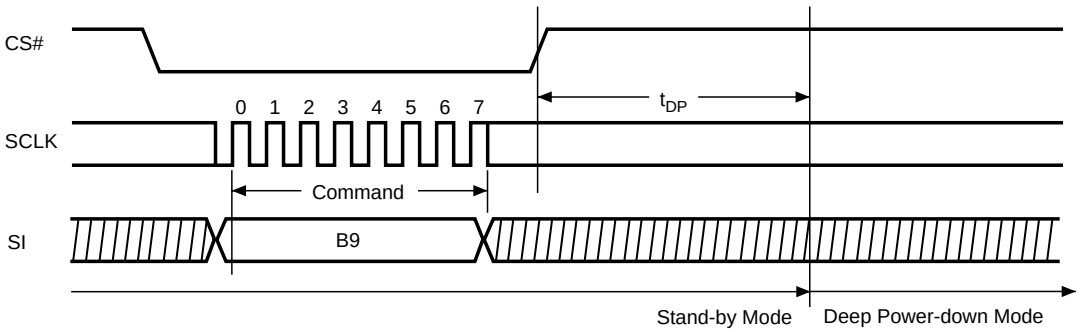
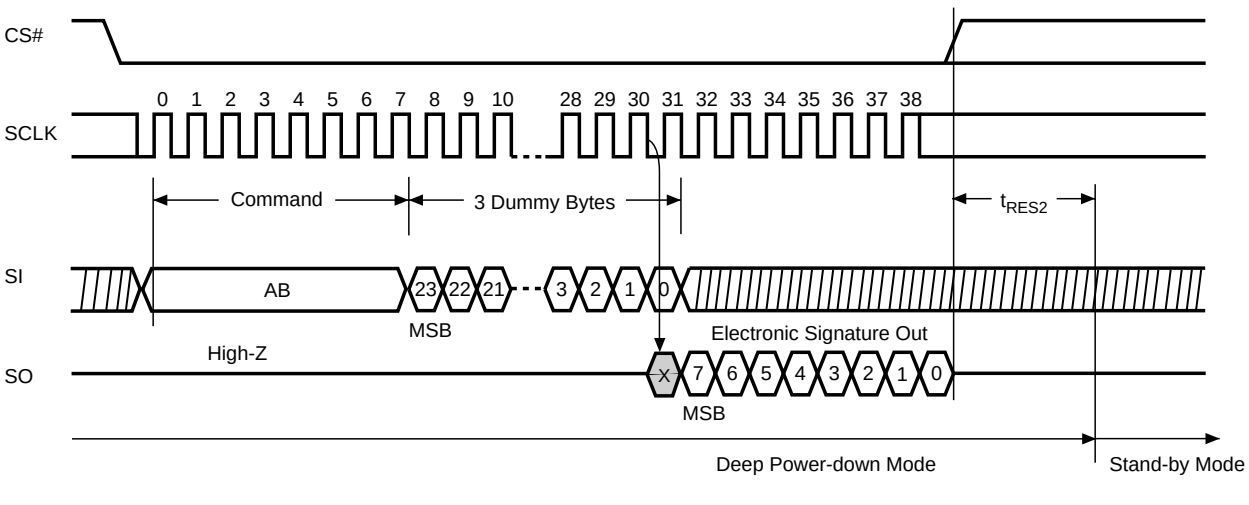


Figure 23. Release from Deep Power-down and Read Electronic Signature (RES) Sequence (Command AB)



Notes: In READ mode, FAST_READ mode, RES mode and REMS mode, MXIC IC will enable output an entire cycle in advance compare with other compatible vendor's spec. Detail condition please reference the waveform.

Figure 24. Release from Deep Power-down (RDP) Sequence (Command AB)

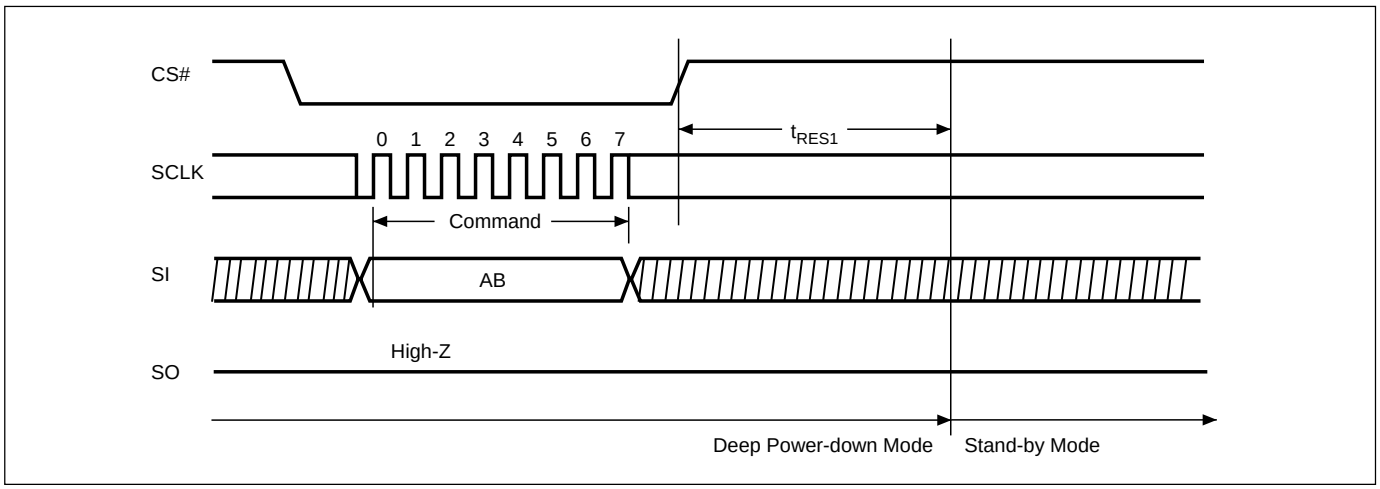
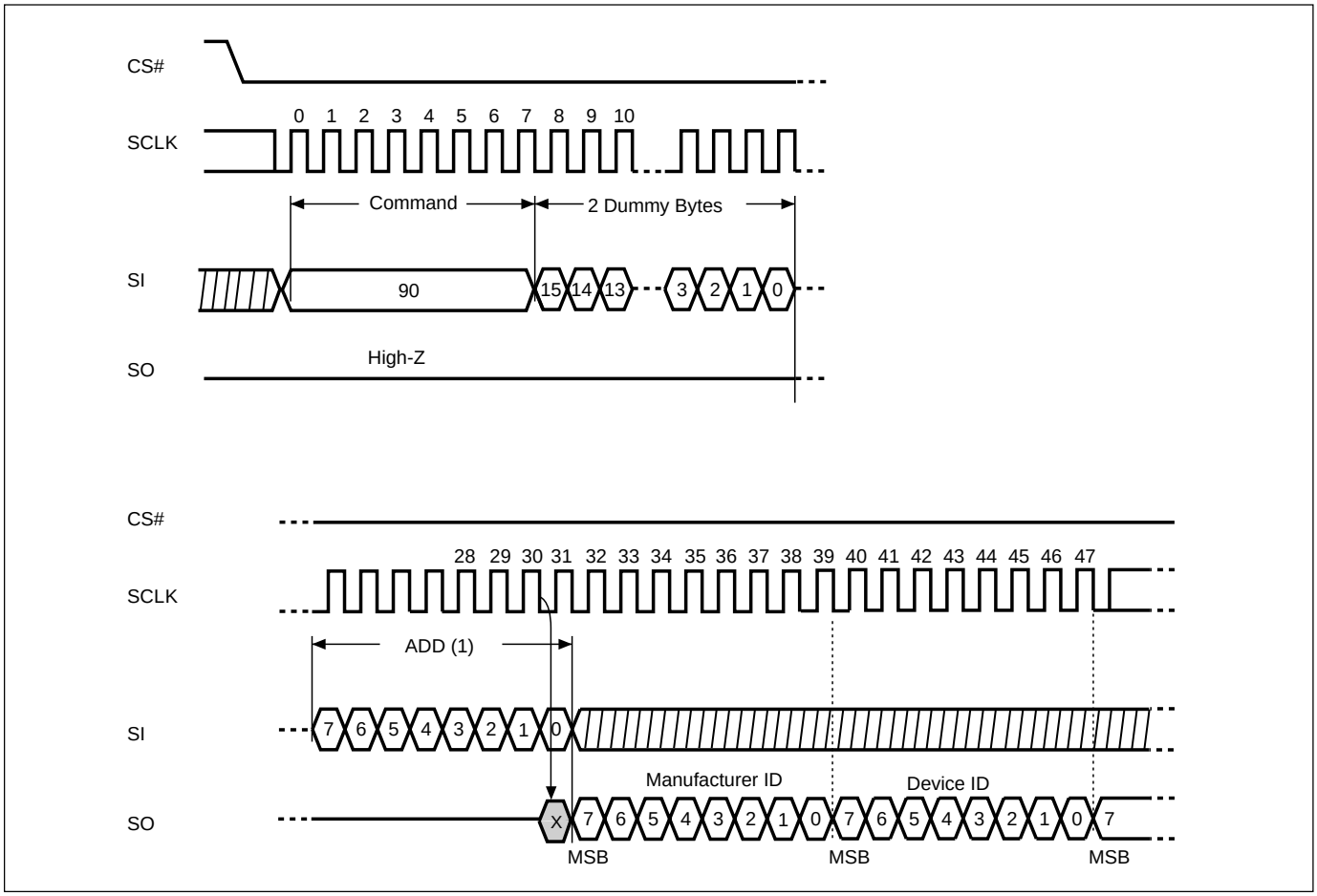


Figure 25. Read Electronic Manufacturer & Device ID (REMS) Sequence (Command 90)



Notes:

(1) ADD=00H will output the manufacturer's ID first and ADD=01H will output device ID first

(2) In READ mode, FAST_READ mode, RES mode and REMS mode, MXIC IC will enable output an entire cycle in advance compare with other compatible vendor's spec. Detail condition please reference the waveform.

Figure 26. Power-up Timing

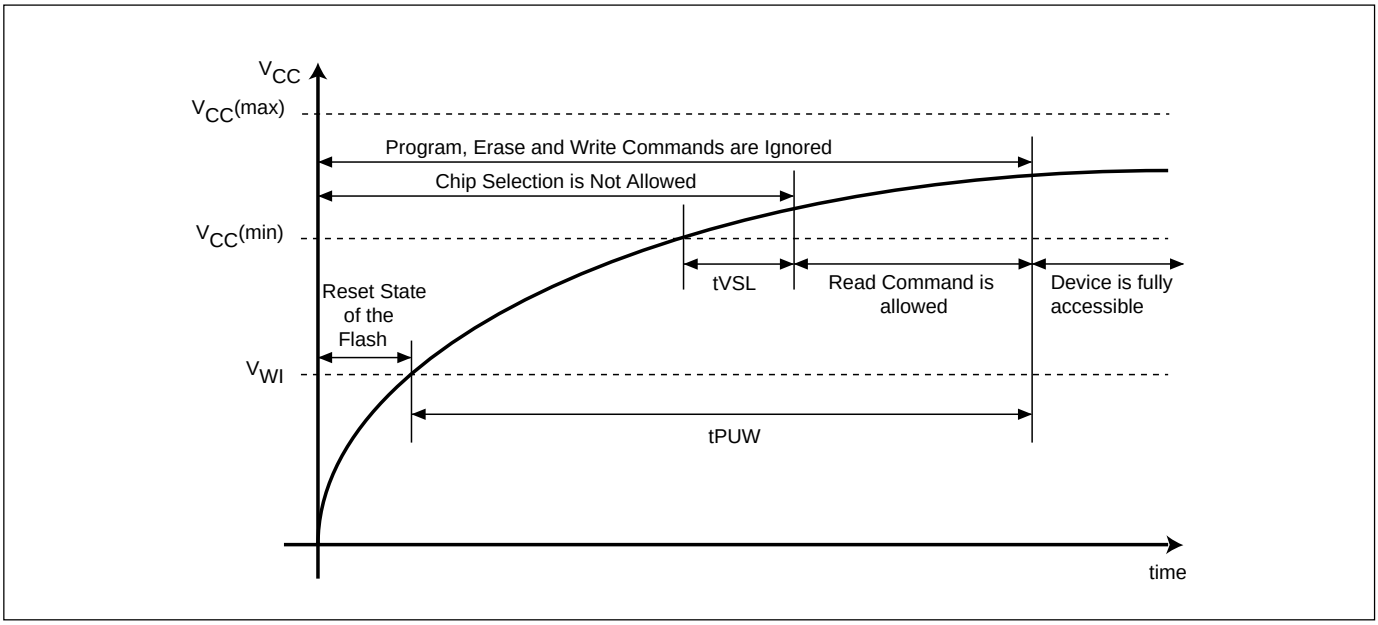


Figure 27. Enter 4Kbit Mode (EN4K) Sequence (Command A5)

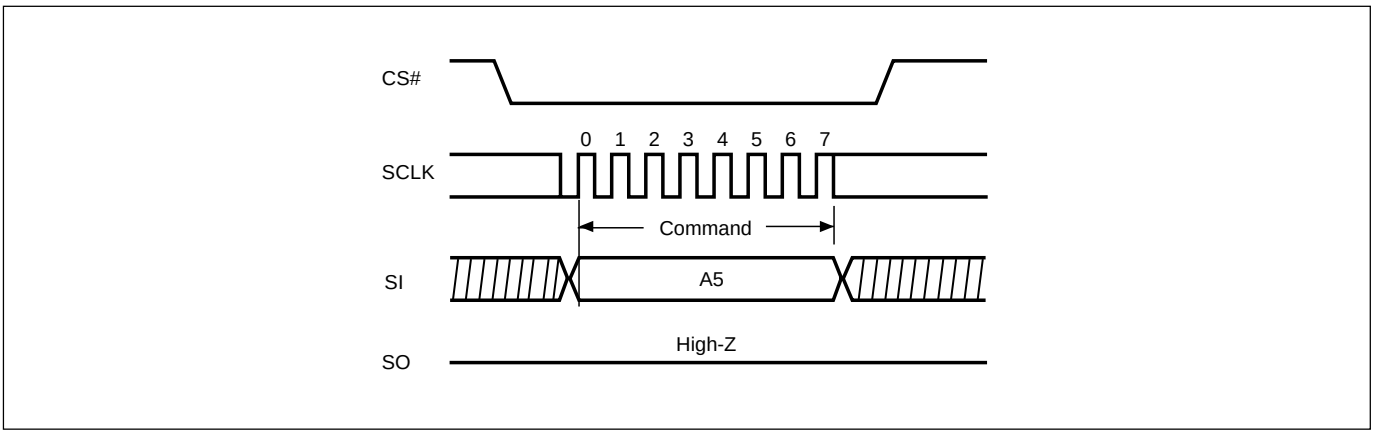
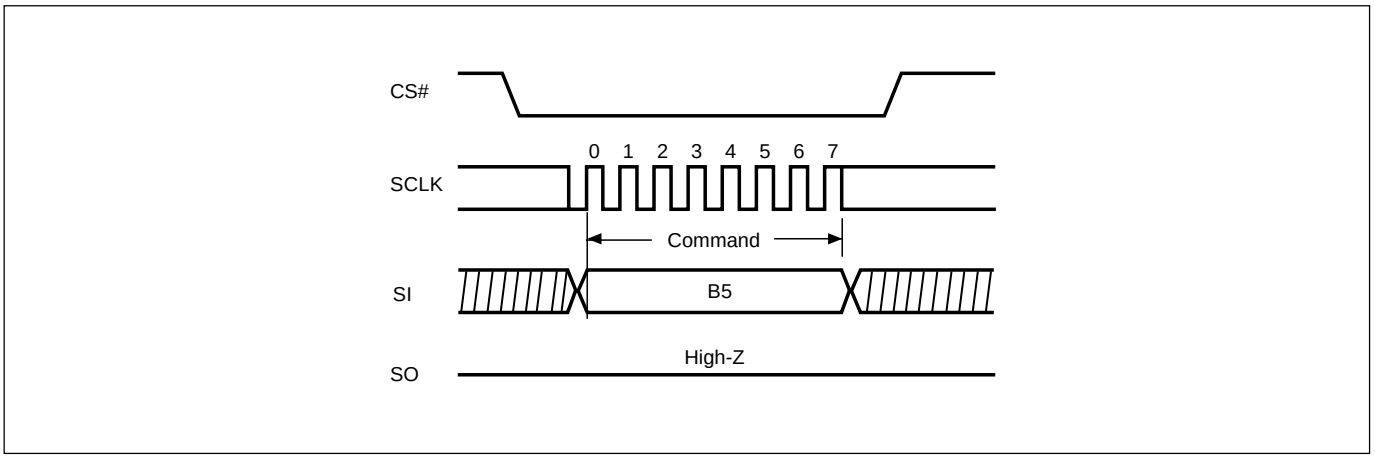


Figure 28. Exit 4Kbit Mode (EX4K) Sequence (Command B5)

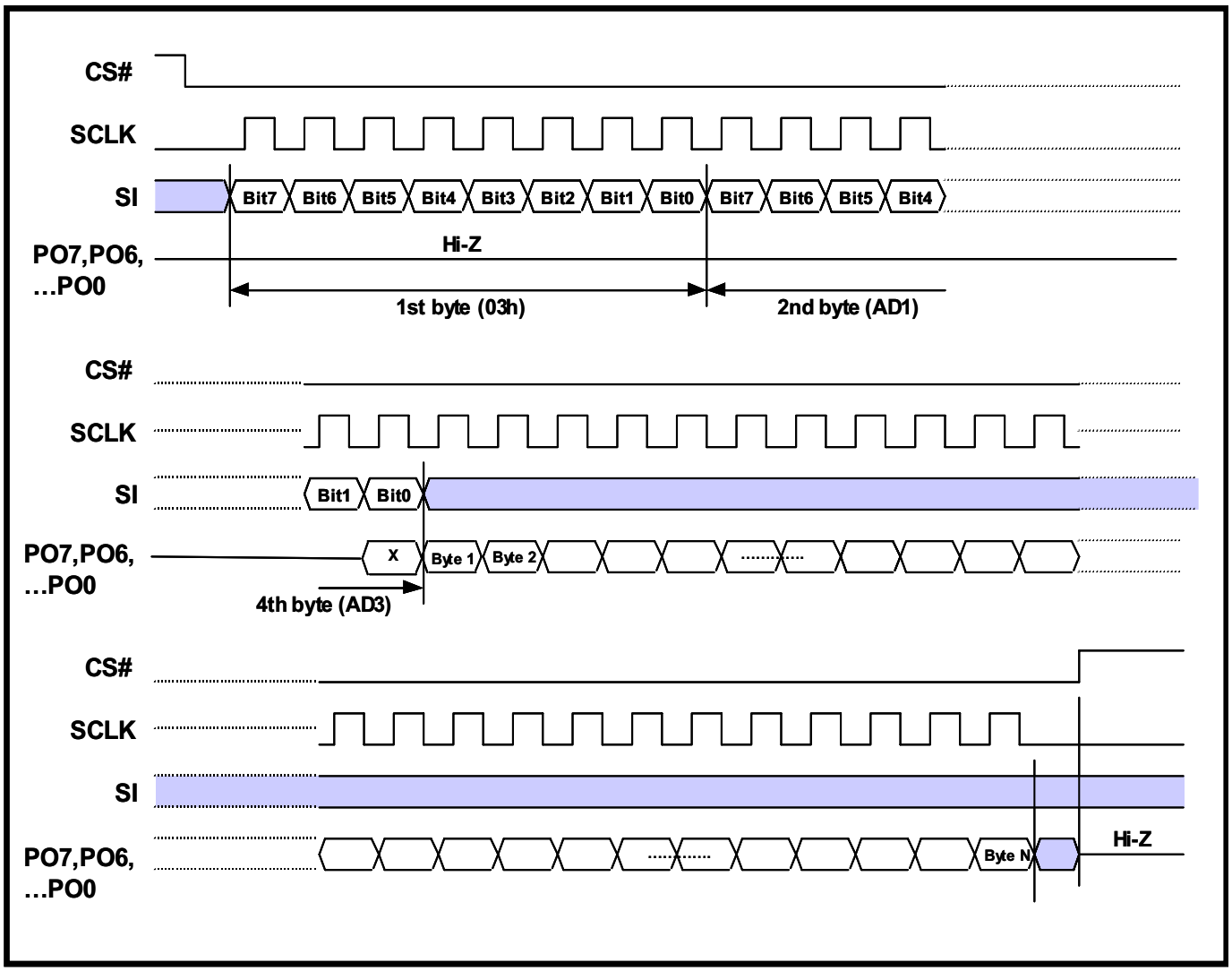


Note:
Enter and Exit 4kbit mode (EN4K & EX4K)
EN4K and EX4K will not be executed when the chip is in busy state. Enter 4kbit mode then the read and write command will be executed on this 4kbit. All read and write command sequence is the same as the normal array. The address of this 4k bits is: A22~A9=0 (for 64Mb), A8~A0 customer defined.

Note 1: Chip erase and WRSR will not be executed in 4kbit mode
Note 2: Chip erase can't erase this 4kbit

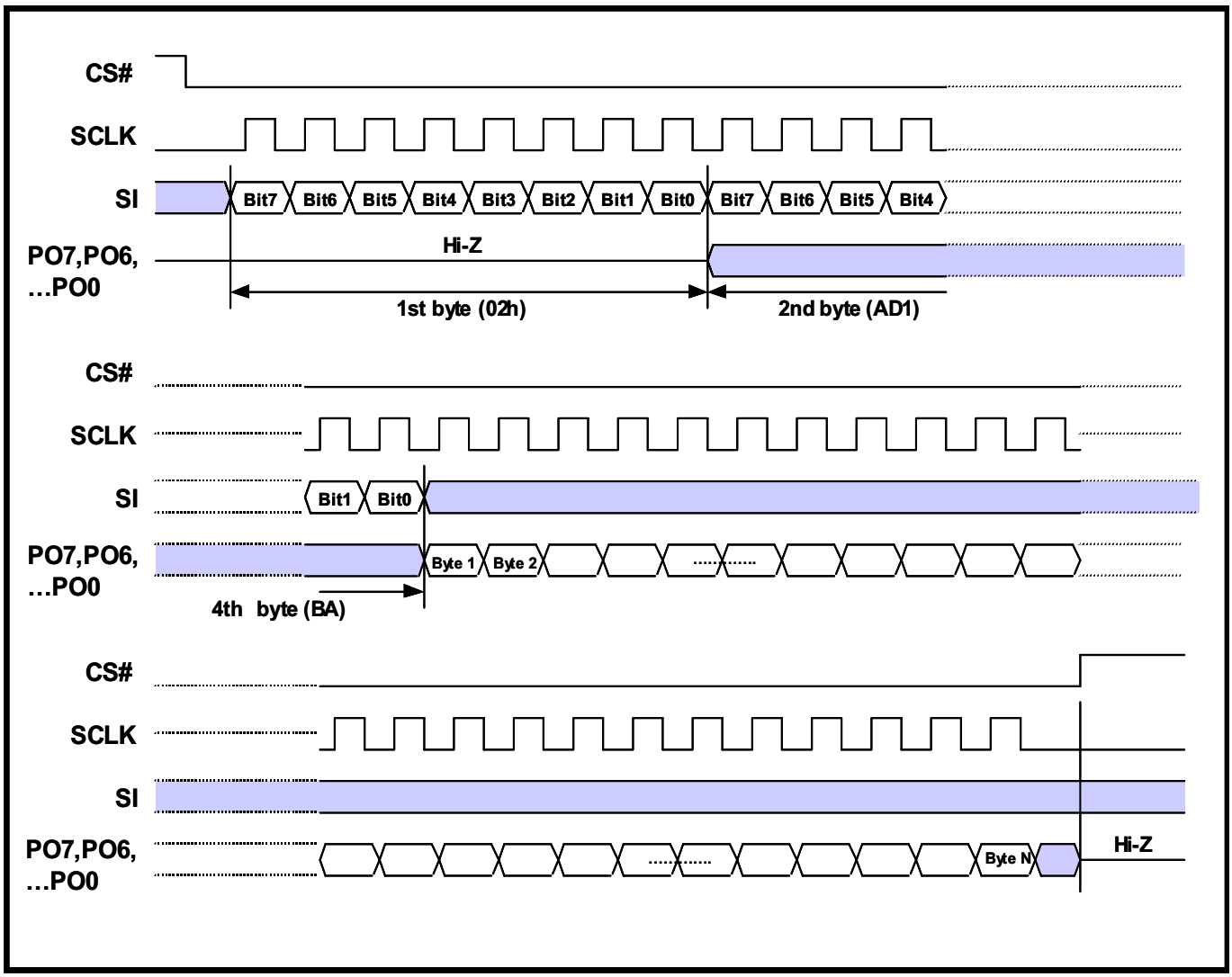
About the fail status:
Bit6 of the status register is used to state fail status, bit6=1 means program or erase have been failed. Any new write command will clear this bit.

Figure 29. READ ARRAY SEQUENCE (Parallel)



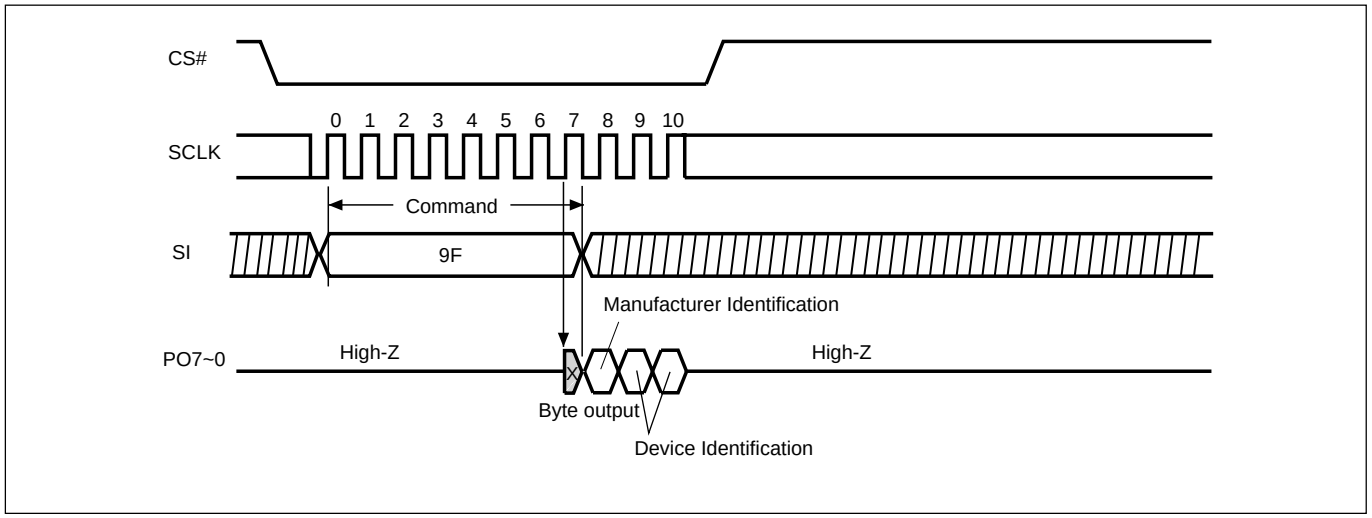
Notes :
1. 1st Byte='03h'
2. 2nd Byte=Address 1(AD1), AD23=BIT7, AD22=BIT6, AD21=BIT5, AD20=BIT4,....AD16=BIT0.
3. 3rd Byte=Address 2(AD2), AD15=BIT7, AD14=BIT6, AD13=BIT5, AD12=BIT4,....AD8=BIT0.
4. 4th Byte=Address 3(AD3), AD7=BIT7, AD6=BIT6, ...AD0=BIT0.
5. From Byte 5, SO Would Output Array Data.
6. Under parallel mode, the fastest access clock freq. will be changed to 1.2MHz(SCLK pin clock freq.).
7. To read array in parallel mode requires a parallel mode command (55H) before the read command. Once in the parallel mode, eLiteFlash™ Memory will not exit parallel mode until power-off.
8. In READ mode, RES mode and REMS mode, MXIC IC will enable output an entire cycle in advance compare with other compatible vendor's spec.

Figure 30. AUTO PAGE PROGRAM TIMING SEQUENCE (Parallel)



Notes :
1. 1st Byte='02h'
2. 2nd Byte=Address 1(AD1), AD23=BIT7, AD22=BIT6, AD21=BIT5, AD20=BIT4,....AD16=BIT0.
3. 3rd Byte=Address 2(AD2), AD15=BIT7, AD14=BIT6, AD13=BIT5, AD12=BIT4,....AD8=BIT0.
4. 4th Byte=Address 3(AD3), AD7=BIT7, AD6=BIT6, ...AD0=BIT0.
5. 5th byte: 1st write data byte.
6. Under parallel mode, the fastest access clock freq. will be changed to 1.2MHz(SCLK pin clock freq.).
7. To program in parallel mode requires a parallel mode command (55H) before the program command. Once in the parallel mode, eLiteFlash™ Memory will not exit parallel mode until power-off.

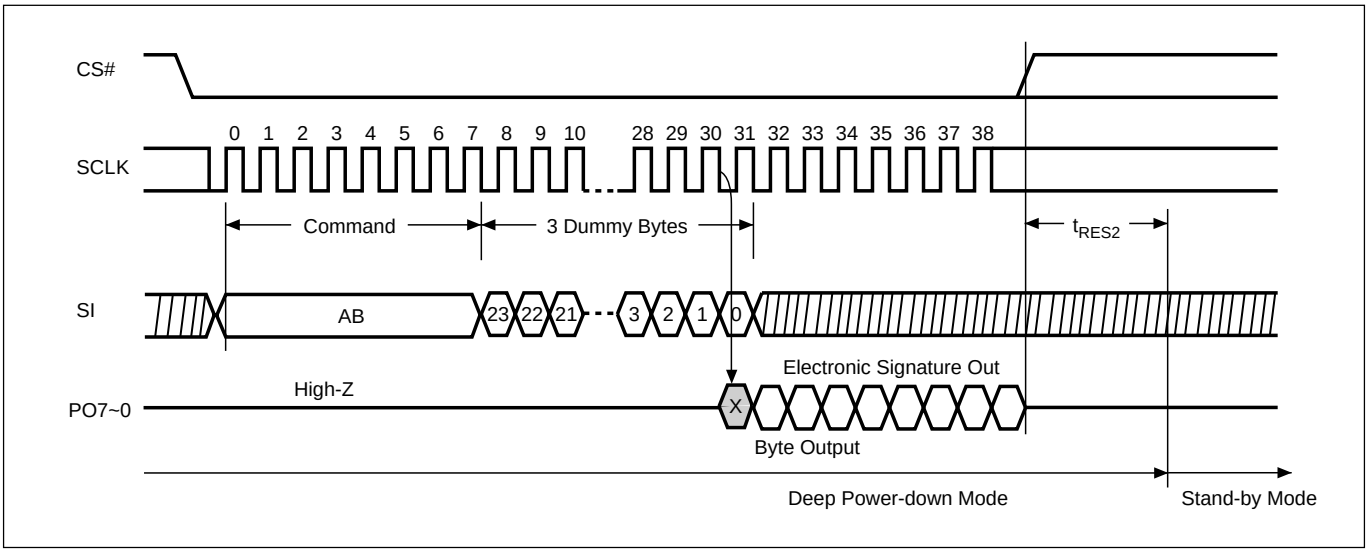
Figure 31. Read Identification (RDID) Sequence (Parallel)



Notes :

1. Under parallel mode, the fastest access clock freg. will be changed to 1.2MHz(SCLK pin clock freg.)
   To read identification in parallel mode, which requires a parallel mode command (55H) before the read identification command.
   Once in the parallel mode, eLiteFlash™ Memory will not exit parallel mode until power-off.
2. Only 1~3 bytes would be output for manufacturer and Device ID. It's same for serial RDID mode.
3. In serial RDID and RDSR mode, output pin SO will be enabled at 8th clock's rising edge. That means, MXIC's drip will enable output half a cycle in advance compare with other compatible vendor's spec.

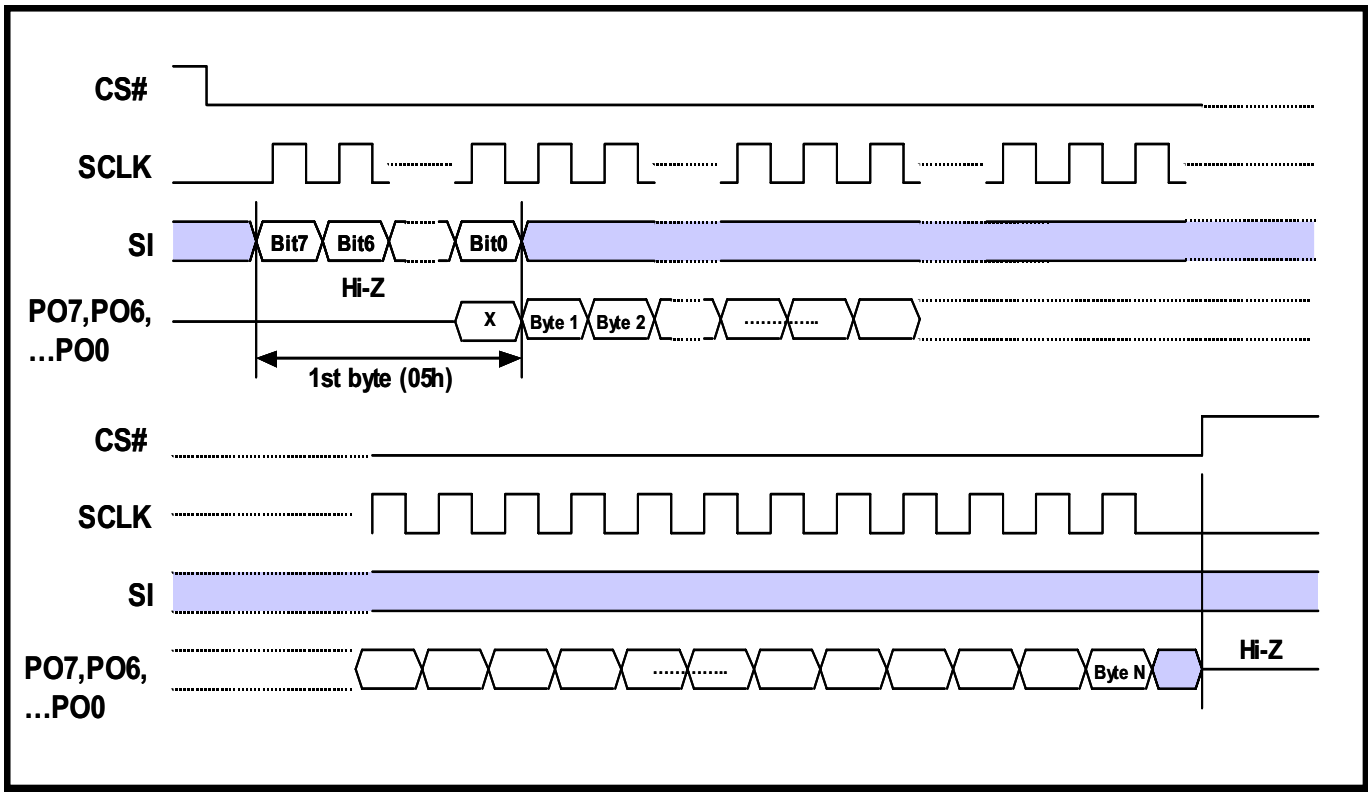
Figure 32. Release from Deep Power-down and Read Electronic Signature (RES) Sequence (Parallel)



Notes :

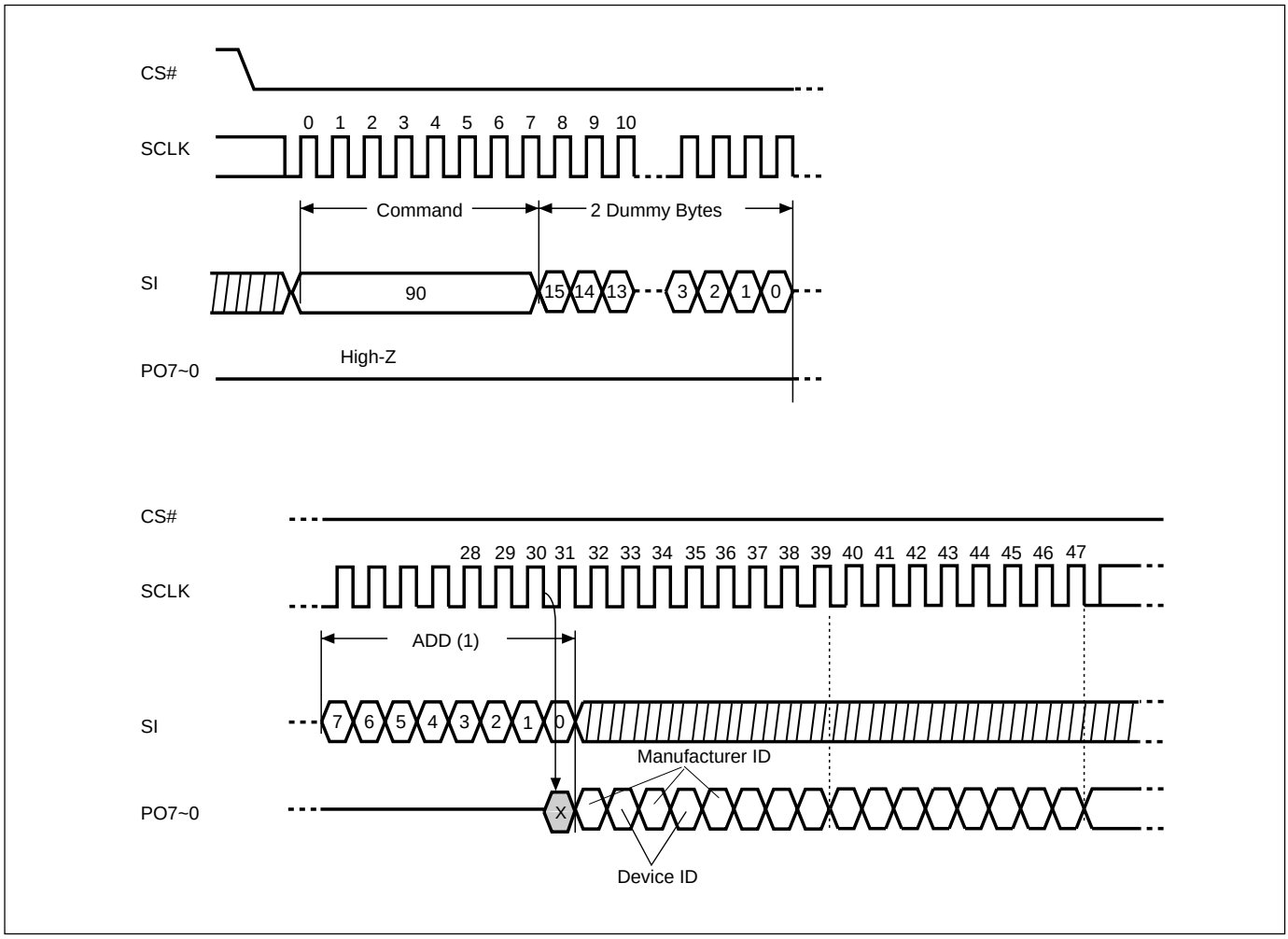
1. Under parallel mode, the fastest access clock freg. will be changed to 1.2MHz(SCLK pin clock freg.)
   To release from deep power-down mode and read ID in parallel mode, which requires a parallel mode command (55H) before the read status register command.
   Once in the parallel mode, eLiteFlash™ Memory will not exit parallel mode until power-off.
2. In READ mode, RES mode and REMS mode, MXIC IC will enable output an entire cycle in advance compare with other compatible vendor's spec.

Figure 33. READ STATUS REGISTER TIMING SEQUENCE (Parallel)



Notes :
1. 1st Byte='05h'
2. BIT7 status register write disable signal. BIT7=1, means SR write disable.
3. BIT6=0 ==> Program/erase is correct.
4. BIT5, 4, 3, 2 defines the level of protected block.
5. BIT1 write enable latch
6. BIT0=0 ==> Device is in ready state
7. Under parallel mode, the fastest access clock freq. will be changed to 1.2MHz(SCLK pin clock freq.).
   To read status register in parallel mode requires a parallel mode command (55H) before the read status register command.
   Once in the parallel mode, eLiteFlash™ Memory will not exit parallel mode until power-off.
8. In serial RDID and RDSR mode, output pin SO will be enabled at 8th clock's rising edge. That means, MXIC's drip will enable output half a cycle in advance compare with other compatible vendor's spec.

Figure 34. Read Electronic Manufacturer & Device ID (REMS) Sequence (Parallel)



Notes :

(1) ADD=00H will output the manufacturer's ID first and ADD=01H will output device ID first

(2) Under parallel mode, the fastest access clock freg. will be changed to 1.2MHz(SCLK pin clock freg.)
To read ID in parallel mode, which requires a parallel mode command (55H) before the read ID command.
Once in the parallel mode, eLiteFlash™ Memory will not exit parallel mode until power-off.

(3) In READ mode, RES mode and REMS mode, MXIC IC will enable output an entire cycle in advance compare with other compatible vendor's spec.

RECOMMENDED OPERATING CONDITIONS

At Device Power-Up

AC timing illustrated in Figure A is recommended for the supply voltages and the control signals at device power-up. If the timing in the figure is ignored, the device may not operate correctly.

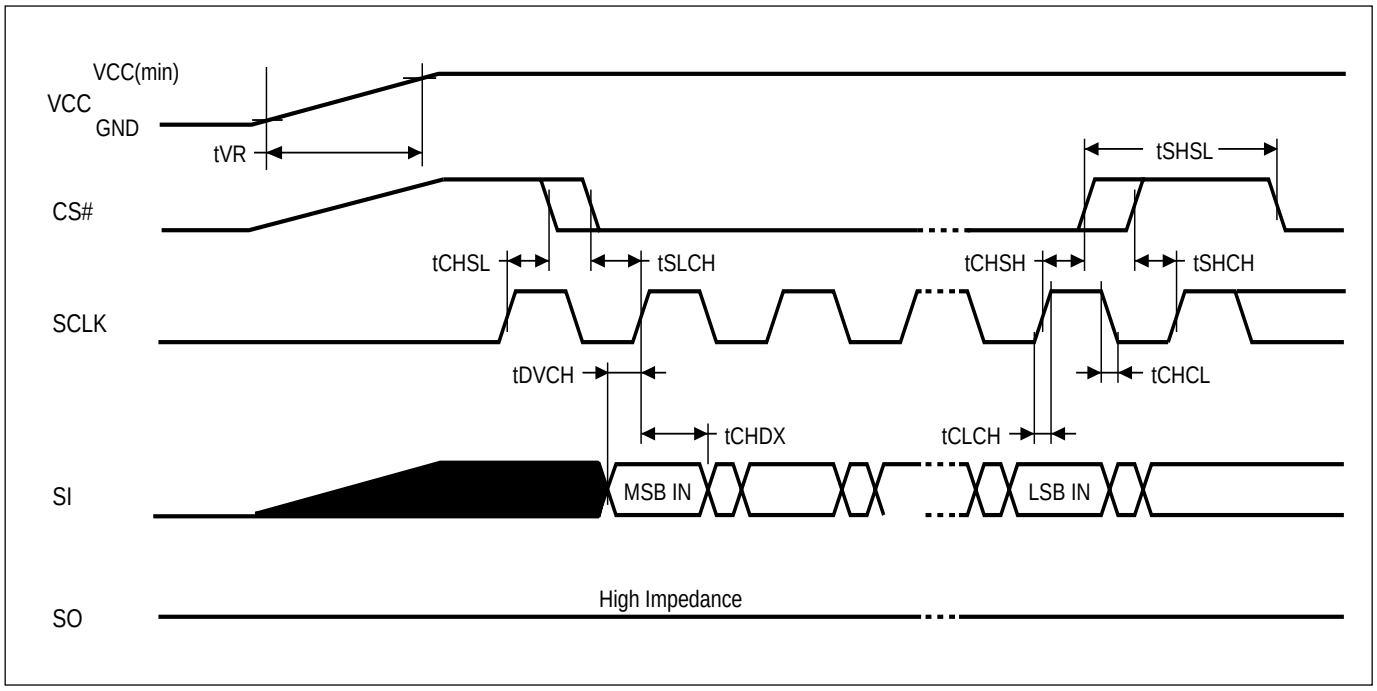


Figure A. AC Timing at Device Power-Up

Symbol	Parameter	Notes	Min.	Max.	Unit
tVR	VCC Rise Time	1	0.5	500000	us/V

Notes :
1. Sampled, not 100% tested.
2. For AC spec tCHSL, tSLCH, tDVCH, tCHDX, tSHSL, tCHSH, tSHCH, tCHCL, tCLCH in the figure, please refer to "AC CHARACTERISTICS" table.

ERASE AND PROGRAMMING PERFORMANCE

PARAMETER		Min.	TYP. (1)	Max. (2)	UNIT	Comments
Chip Erase Time			128	256	s	Note (4)
Chip Erase Time (with ACC=12V)			102	180	s	Note (4)
Sector erase Time			1	3	s	Note (4)
Sector erase Time (with ACC=12V)			0.8	2.4	s	Note (4)
Additional 4Kb Erase Time			25	50	mS	Note (4)
Page Programming Time			3	12	mS	Excludes system level overhead(3)
Page Programming Time (with ACC=12V)			2.4	9.6	mS	
Erase/Program Cycle	Main Array	10K			cycles	
	Additional 4Kb	100K			cycles	

Notes :
1. Typical program and erase time assumes the following conditions: 25°C, 3.0V, and all bits are programmed by checker-board pattern.
2. Under worst conditions of 70°C and 3.0V. Maximum values are up to including 10K program/erase cycles.
3. System-level overhead is the time required to execute the command sequences for the page program command.
4. Excludes 00H programming prior to erasure. (In the pre-programming step of the embedded erase algorithm, all bits are programmed to 00H before erasure)

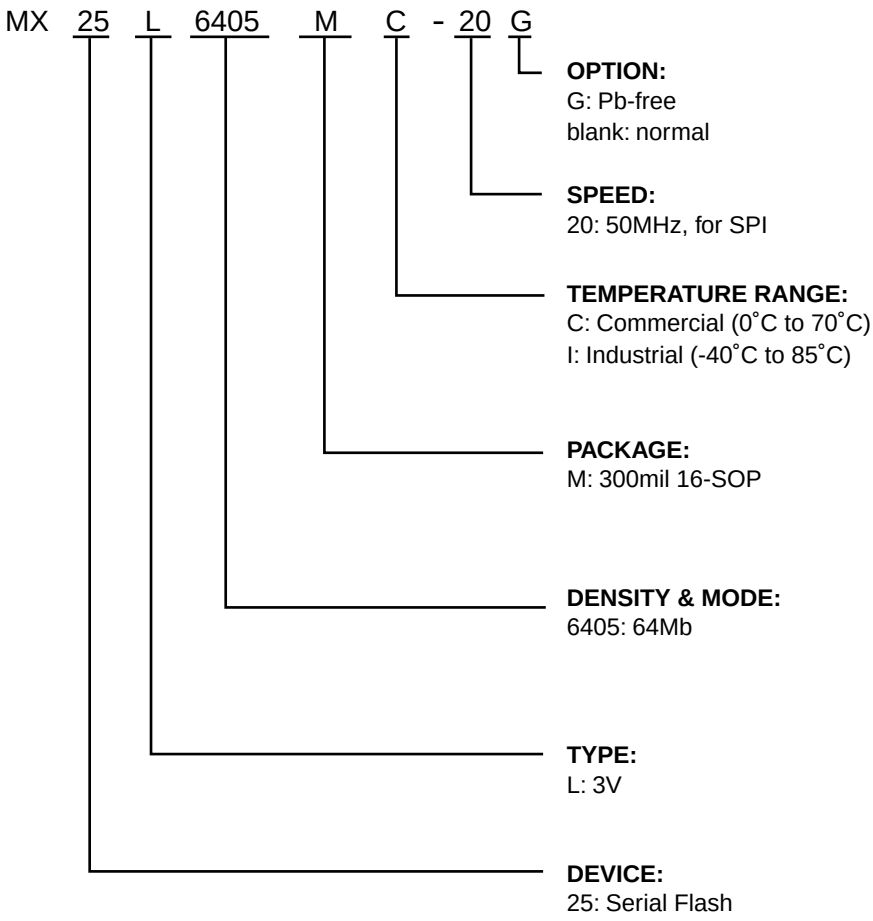
LATCH-UP CHARACTERISTICS

	MIN.	MAX.
Input Voltage with respect to GND on ACC	-1.0V	12.5V
Input Voltage with respect to GND on all power pins, SI, CS#	-1.0V	2 VCCmax
Input Voltage with respect to GND on SO	-1.0V	VCC + 1.0V
Current	-100mA	+100mA
Includes all pins except VCC. Test conditions: VCC = 3.0V, one pin at a time.		

ORDERING INFORMATION

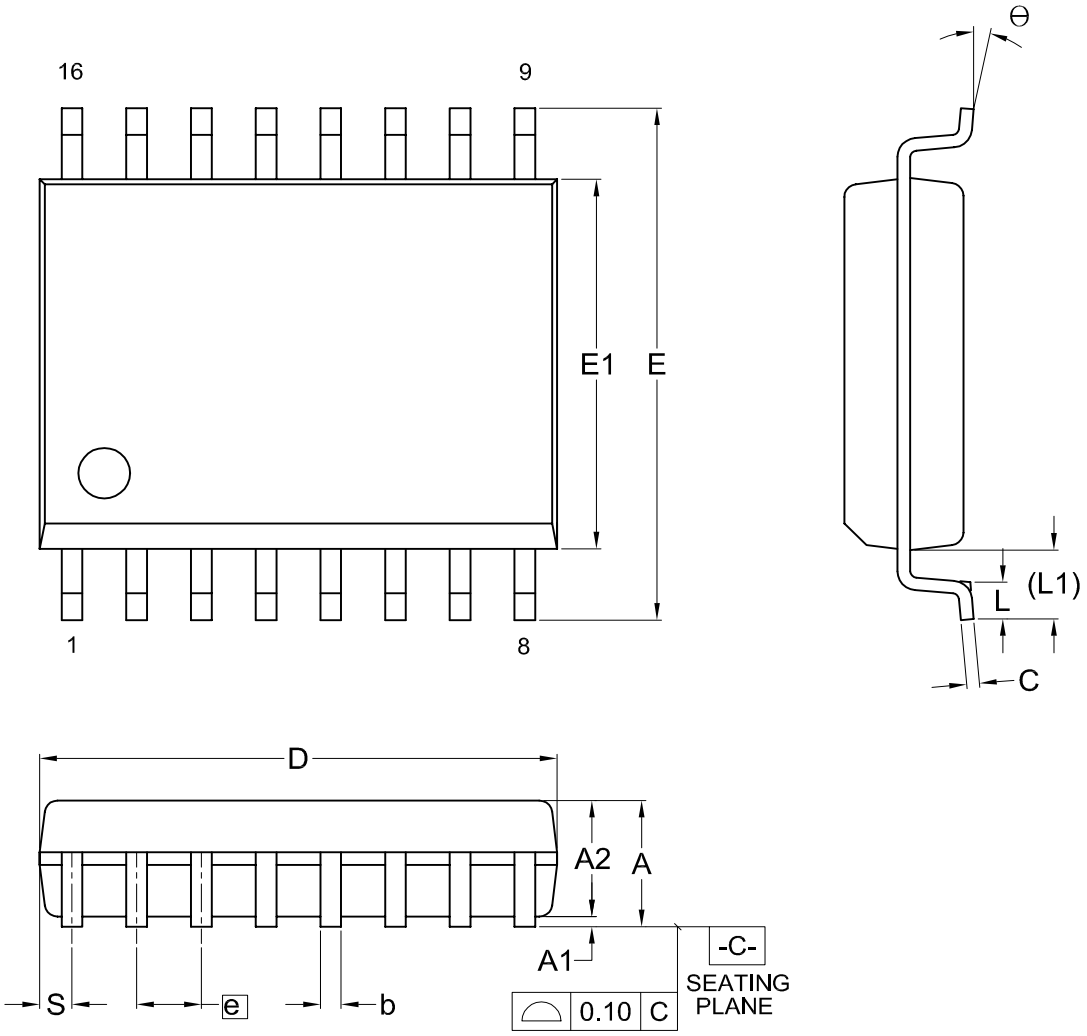
PART NO.	ACCESS TIME(ns)	OPERATING CURRENT(mA)	STANDBY CURRENT(uA)	Temperature	PACKAGE	Remark
MX25L6405MC-20	20	30	50	0~70°C	16-SOP	
MX25L6405MC-20G	20	30	50	0~70°C	16-SOP	Pb-free
MX25L6405MI-20	20	30	50	-40~85°C	16-SOP	
MX25L6405MI-20G	20	30	50	-40~85°C	16-SOP	Pb-free

PART NAME DESCRIPTION



PACKAGE INFORMATION

Title: Package Outline for SOP 16L (300MIL)



Dimensions (inch dimensions are derived from the original mm dimensions)

SYMBOL / UNIT		A	A1	A2	b	C	D	E	E1	e	L	L1	S	θ
mm	Min.	---	0.10	2.25	0.36	0.20	10.10	10.10	7.42	---	0.40	1.31	0.51	0
	Nom.	---	0.20	2.31	0.41	0.25	10.30	10.30	7.52	1.27	0.84	1.44	0.64	5
	Max.	2.65	0.30	2.40	0.51	0.30	10.50	10.50	7.60	---	1.27	1.57	0.77	8
Inch	Min.	---	0.004	0.089	0.014	0.008	0.397	0.397	0.292	---	0.016	0.052	0.020	0
	Nom.	---	0.008	0.091	0.016	0.010	0.405	0.405	0.296	0.050	0.033	0.057	0.025	5
	Max.	0.104	0.012	0.094	0.020	0.012	0.413	0.413	0.299	---	0.050	0.062	0.030	8

DWG.NO.	REVISION	REFERENCE			ISSUE DATE
		JEDEC	EIAJ		
6110-1402	8	MS-013			03-07-'06

REVISION HISTORY

Revision No.	Description	Page	Date
1.0	1. Removed "Preliminary" title	P1	JUL/15/2005
	2. Added "Recommended Operating Conditions"	P40	
	3. Added "additional 4Kb erase time" and "cycle time"	P41	
	4. Added "Part Name Description"	P43	
	5 To be separated from MX25L1605, MX25L3205, MX25L6405 to MX25L6405	All	
1.1	1. Improved chip erase time: without ACC=12V : 160s(typ.)/512s(max.)-->128s(typ.)/256s(max.) with ACC=12V : 128s(typ.)/410s(max.)-->102s(typ.)/180s(max.)	P1,22,41	AUG/03/2005
	2. Added description about Pb-free device is RoHS compliant	P1	
1.2	1. Format change	All	JUN/08/2006
1.3	1. Added statement	P46	NOV/06/2006

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