



LA5318V

Voltage-Dividing Voltage Generator for Multi-Voltage LCD Matrix Drive

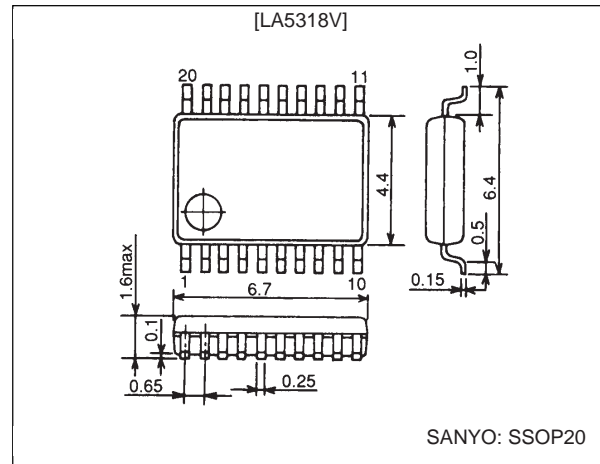
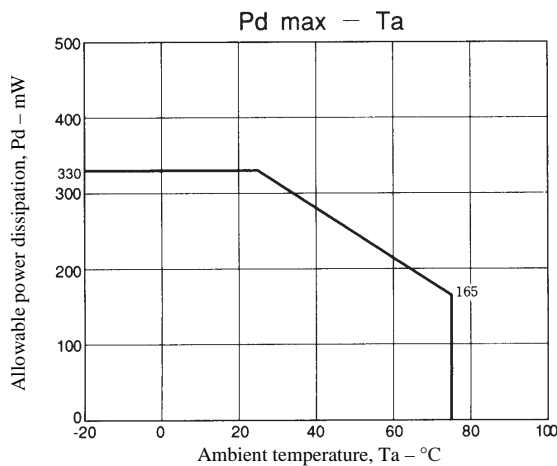
Overview

The LA5318V is a variable voltage-dividing voltage generator IC designed for driving LCD matrixes that require multiple voltages.

Package Dimensions

unit: mm

3179A-SSOP20



Specifications

Absolute Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	$V_{EE \text{ max}}$	$V_{CC} - V_{EE}$	36	V
Maximum output current	$I_{OUT \text{ max}}$	V1 to V4	Internal*	mA
Allowable power dissipation	$P_d \text{ max}$		330	mW
Operating temperature	T_{opr}		-20 to +75	°C
Storage temperature	T_{stg}		-30 to +125	°C

Notes: *The value stipulated in the conditions listed in the separate document shall be used as the maximum output current.

1. Continuous operation (without damage to the device) is guaranteed in the above ranges.
2. The output pins V1 to V4 may be shorted to the power supply or to ground for periods of up to 1 ms. (When $|V_{CC} - V_{EE}| < 35 \text{ V}$)

Operating Conditions at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V_{EE}	$V_{CC} - V_{EE}$	-35.5 to -6	V
Input voltage	V_{REF}	$V_{CC} - V_{REF}$: $V_{REF} \geq V_{EE}$	-35 to -6	V
Input current	I_{INR}	INR	-0.2 to 0	mA
Output current	I_{OUTR}	OUTR	0 to 50	mA
	$I_{OUT1, 2}$	V1, V2	-5 to +5	mA
	$I_{OUT3, 4}$	V3, V4	-10 to +5	mA

Note: V_{CC} and V_{EE} must be set up so that $|V1|$ and $|V_{EE} - V4|$ are at least 1 V.

SANYO Electric Co., Ltd. Semiconductor Business Headquarters

TOKYO OFFICE Tokyo Bldg., 1-10, 1 Chome, Ueno, Taito-ku, TOKYO, 110 JAPAN

82097HA(OT) No. 5670-1/4

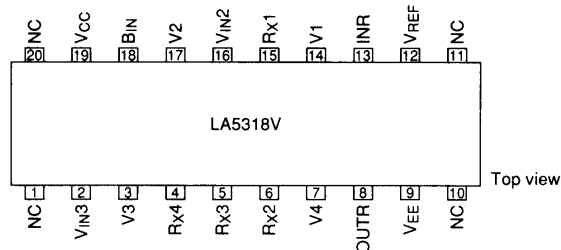
LA5318V

Operating Characteristics at $T_a = 25^\circ\text{C}$, $V_{CC} - V_{EE} = -20\text{ V}$, $V_{REF} = V_{EE}$, $R_X = 8R$, $B_{IN} = \text{OPEN}$

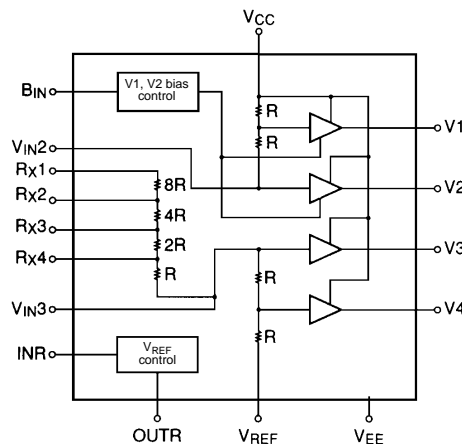
Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Current drain	I_{CC}, I_{EE}	$V_{CC} - V_{EE} = -20\text{ V}$, $R_X = 8R$, $INR = V_{CC} : V_{CC}, V_{EE}$		0.35	0.5	mA
Output voltage ratio 1	Ra1	$V2/V1$	1.96	2.00	2.04	
Output voltage ratio 2	Ra2	$(V_{REF} - V3)/(V_{REF} - V4)$	1.96	2.00	2.04	
Output voltage ratio 3	Rb1	$V_{REF}/V1$	11.64	12.00	12.36	
Output voltage ratio 4	Rb2	$V_{REF}/V2$	5.82	6.00	6.18	
Output voltage ratio 5	Rb3	$V_{REF}/(V_{REF} - V3)$	5.82	6.00	6.18	
Output voltage ratio 3	Rb4	$V_{REF}/(V_{REF} - V4)$	11.64	12.00	12.36	
Internal resistance ratio 1	R_{X1}	Referenced to the resistance R between R_{X4} and V_{IN3}		8		
Internal resistance ratio 2	R_{X2}			12		
Internal resistance ratio 3	R_{X3}			14		
Internal resistance ratio 4	R_{X4}			15		
Resistance	R	The value of R when the voltage across R_{X4} and V_{IN3} is 0.5 V.		30		k Ω
Load regulation 1	$\Delta V1$	$+0.1\text{ mA} < I_{OUT1} < +5\text{ mA} : V1$			± 20	mV
Load regulation 2	$\Delta V2$	$+0.1\text{ mA} < I_{OUT2} < +5\text{ mA} : V2$			± 20	mV
Load regulation 3	$\Delta V3$	$+0.1\text{ mA} < I_{OUT3} < +5\text{ mA} : V3$			± 20	mV
Load regulation 4	$\Delta V4$	$+0.1\text{ mA} < I_{OUT4} < +5\text{ mA} : V4$			± 20	mV
Load regulation -1A	$-\Delta V1A$	$-0.5\text{ mA} < I_{OUT1} < -0.1\text{ mA} : V1$			± 20	mV
Load regulation -2A	$-\Delta V2A$	$-0.5\text{ mA} < I_{OUT2} < -0.1\text{ mA} : V2$			± 20	mV
Load regulation -3	$-\Delta V3$	$-10\text{ mA} < I_{OUT3} < -0.1\text{ mA} : V3$			± 20	mV
Load regulation -4	$-\Delta V4$	$-10\text{ mA} < I_{OUT4} < -0.1\text{ mA} : V4$			± 20	mV
Load regulation -1B	$-\Delta V1B$	$-5\text{ mA} < I_{OUT1} < -0.1\text{ mA}$, $B_{IN} = \text{GND} : V1$			± 20	mV
Load regulation -2B	$-\Delta V2B$	$-5\text{ mA} < I_{OUT2} < -0.1\text{ mA}$, $B_{IN} = \text{GND} : V2$			± 20	mV
OUTR pin saturation voltage	V_{OUTR}	$I_{OUT} = 20\text{ mA}$, $V_{CC} - INR = 2.7 : \text{OUTR} - V_{EE}$			0.5	V

Note: For I_{OUT} , minus (-) indicates source current and plus (+) indicates sink current.

Pin Assignment

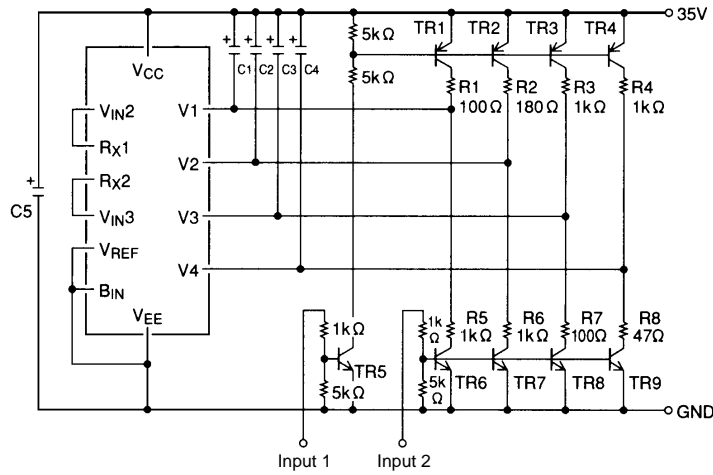


Block Diagram



(This circuit must be used with $V_{RX1} \geq V_{RX2} \geq V_{RX3} \geq V_{RX4}$.)

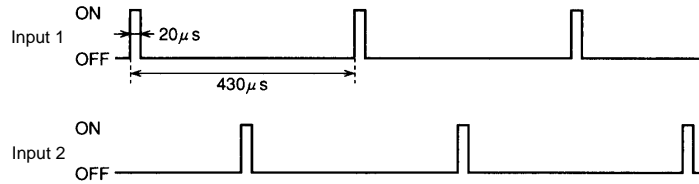
Maximum Output Current Load Test Conditions



$V_{CC} - V_{EE} = 35\text{ V}$, $R_X = 8R$, $C1$ to $C4 = 10\text{ }\mu\text{F}$, $C5 = 33\text{ }\mu\text{F}$, All resistors must be rated 1 W or higher.

TR1 to TR4; 2SA984 Rank E or F
 TR5 to TR9; 2SC2274 Rank E or F

Set the output load resistors (R1 to R8) so that currents of 25 to 30 mA maximum (except for the V3 and V4 source sides, which can handle about 60 mA) flow in the sink and source sides when high (on state) levels are input to inputs 1 and 2.



· V_{REF} control block

Determining the TR1 drive current

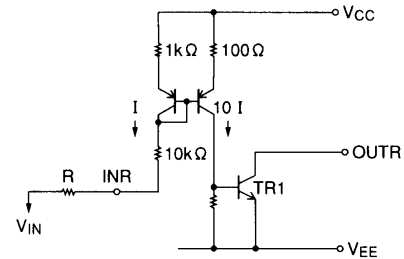
$$I = \frac{V_{CC} - V_{BE} - V_{IN}}{11\text{ k} + R}$$

($V_{BE} \approx 0.7\text{ V}$)

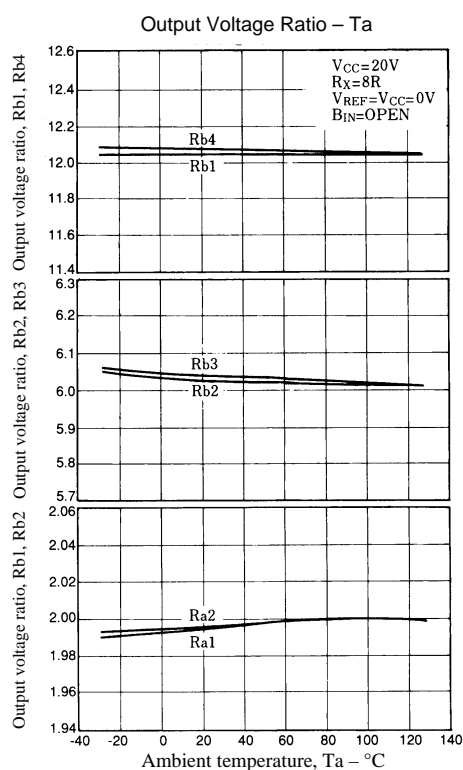
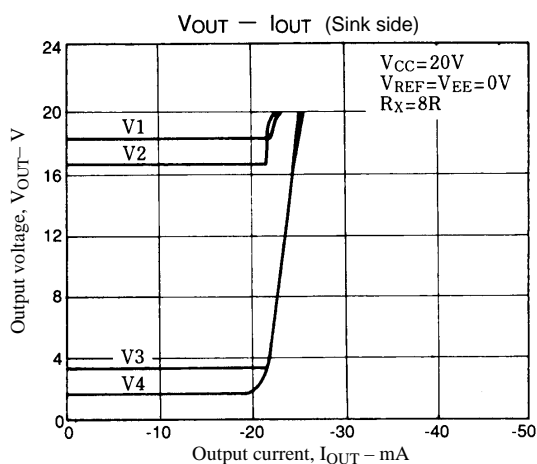
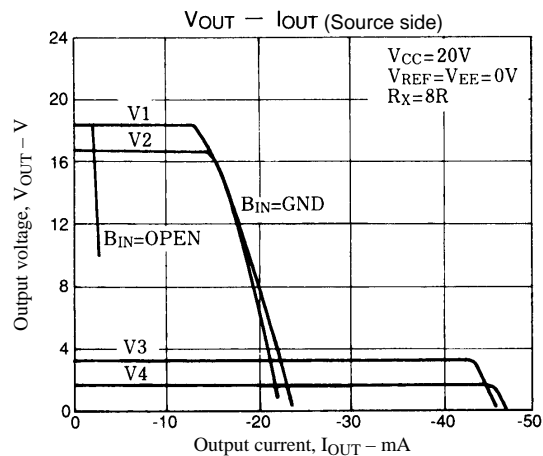
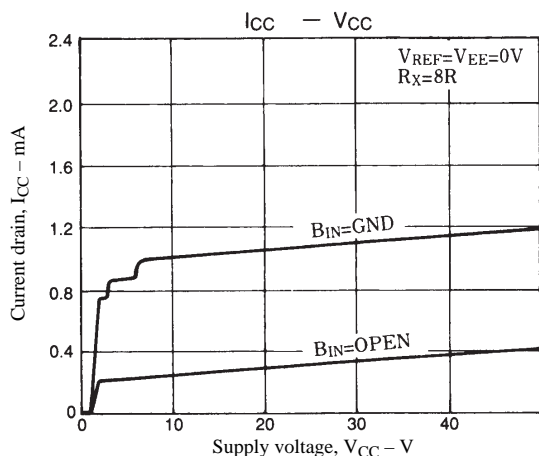
Drive current

$$I_O \approx 10I = \frac{V_{CC} - 0.7 - V_{IN}}{11\text{ k} + R} \times 10$$

Assume that the $TR1_{hFE}$ is 50 for this calculation.



Note: Connect INR to V_{CC} when INR and OUTR are not used.



- No products described or contained herein are intended for use in surgical implants, life-support systems, aerospace equipment, nuclear power control systems, vehicles, disaster/crime-prevention equipment and the like, the failure of which may directly or indirectly cause injury, death or property loss.
- Anyone purchasing any products described or contained herein for an above-mentioned use shall:
 - ① Accept full responsibility and indemnify and defend SANYO ELECTRIC CO., LTD., its affiliates, subsidiaries and distributors and all their officers and employees, jointly and severally, against any and all claims and litigation and all damages, cost and expenses associated with such use:
 - ② Not impose any responsibility for any fault or negligence which may be cited in any such claim or litigation on SANYO ELECTRIC CO., LTD., its affiliates, subsidiaries and distributors or any of their officers and employees jointly or severally.
- Information (including circuit diagrams and circuit parameters) herein is for example only; it is not guaranteed for volume production. SANYO believes information herein is accurate and reliable, but no guarantees are made or implied regarding its use or any infringements of intellectual property rights or other rights of third parties.

This catalog provides information as of August, 1997. Specifications and information herein are subject to change without notice.