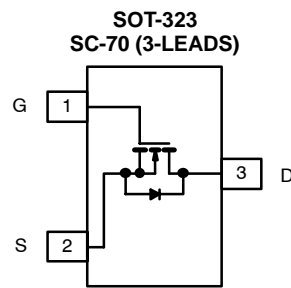




N-Channel 25-V (D-S) MOSFET

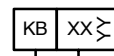
TrenchFET[®]
Power MOSFETs

PRODUCT SUMMARY			
V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)	Q_g (Typ)
25	0.350 @ $V_{GS} = 4.5$ V	0.75	1.3
	0.450 @ $V_{GS} = 2.5$ V	0.66	



Top View

Marking Code



Lot Traceability
and Date Code

Part # Code

Ordering Information: Si1304DL-T1

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)					
Parameter	Symbol	5 secs	Steady State	Unit	
Drain-Source Voltage	V_{DS}	25		V	
Gate-Source Voltage	V_{GS}	± 8			
Continuous Drain Current ($T_J = 150^\circ\text{C}$) ^a	I_D	$T_A = 25^\circ\text{C}$	0.75	0.70	A
		$T_A = 70^\circ\text{C}$	0.60	0.56	
Pulsed Drain Current	I_{DM}	3.0			
Continuous Diode Current (Diode Conduction) ^a	I_S	0.28	0.24		
Maximum Power Dissipation ^a	P_D	$T_A = 25^\circ\text{C}$	0.33	0.29	W
		$T_A = 70^\circ\text{C}$	0.21	0.19	
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 to 150		$^\circ\text{C}$	

THERMAL RESISTANCE RATINGS					
Parameter	Symbol	Typical	Maximum	Unit	
Maximum Junction-to-Ambient ^a	R_{thJA}	$t \leq 5$ sec	315	375	$^\circ\text{C/W}$
		Steady State	380	450	
Maximum Junction-to-Foot (Drain)	R_{thJF}	285	340		

Notes

a. Surface Mounted on 1" x 1" FR4 Board.

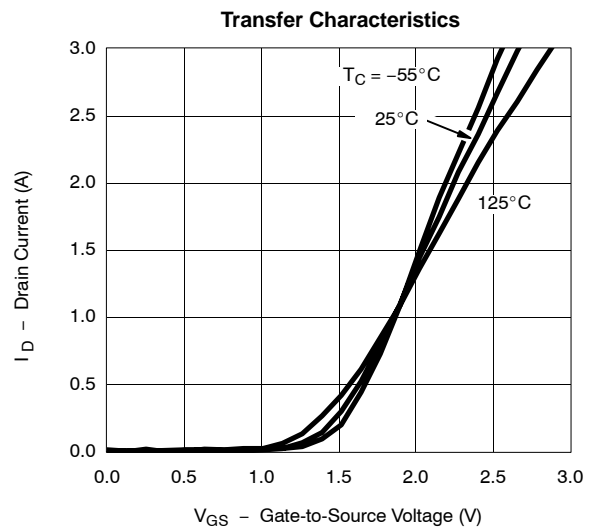
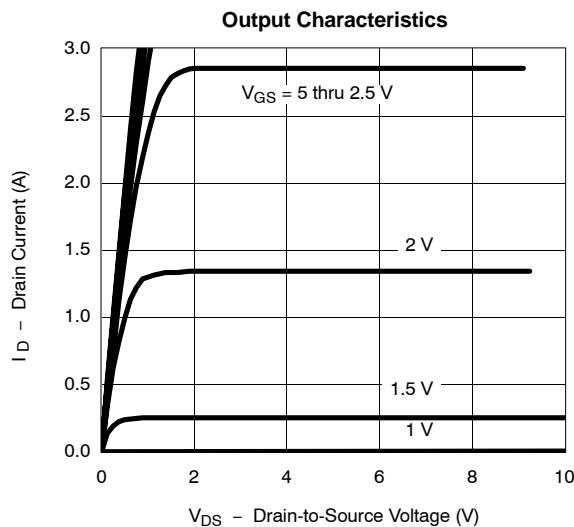
SPECIFICATIONS (T_J = 25 °C UNLESS OTHERWISE NOTED)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	0.6		1.3	V
Gate-Body Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ±8 V			±100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 25 V, V _{GS} = 0 V			1	μA
		V _{DS} = 25 V, V _{GS} = 0 V, T _J = 70 °C			5	
On-State Drain Current ^a	I _{D(on)}	V _{DS} = 5 V, V _{GS} = 4.5 V	3.0			A
Drain-Source On-State Resistance ^a	r _{DS(on)}	V _{GS} = 4.5 V, I _D = 0.75 A		0.280	0.350	Ω
		V _{GS} = 2.5 V, I _D = 0.50 A		0.355	0.450	
Forward Transconductance ^a	g _{fs}	V _{DS} = 15 V, I _D = 0.75 A		1.5		S
Diode Forward Voltage ^a	V _{SD}	I _S = 0.24 A, V _{GS} = 0 V		0.8	1.2	V
Dynamic^b						
Total Gate Charge	Q _g	V _{DS} = 15 V, V _{GS} = 4.5 V, I _D = 0.75 A		1.3	2.0	nC
Gate-Source Charge	Q _{gs}			0.31		
Gate-Drain Charge	Q _{gd}			0.5		
Turn-On Delay Time	t _{d(on)}	V _{DD} = 15 V, R _L = 20 Ω I _D ≅ 0.75 A, V _{GEN} = 4.5 V, R _g = 6 Ω		11	20	ns
Rise Time	t _r			18	30	
Turn-Off Delay Time	t _{d(off)}			17	30	
Fall Time	t _f			11	20	
Source-Drain Reverse Recovery Time	t _{rr}		I _F = 0.24 A, di/dt = 100 A/μs		30	

Notes

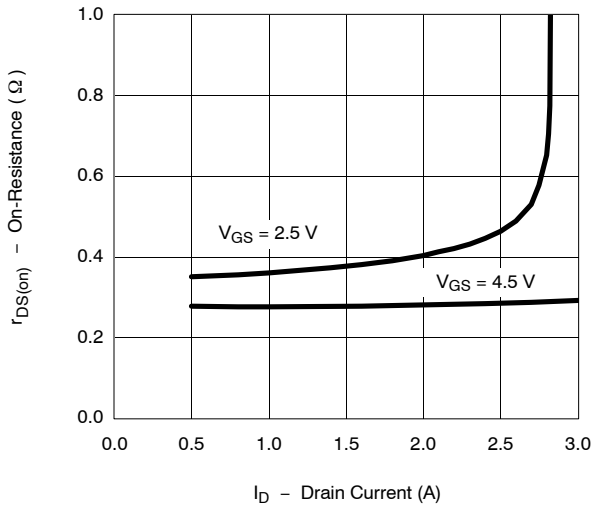
- a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.
b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

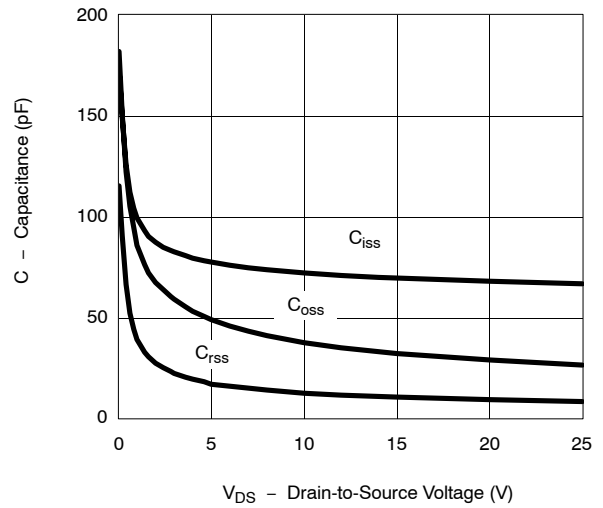
TYPICAL CHARACTERISTICS (25 °C UNLESS NOTED)

TYPICAL CHARACTERISTICS (25 °C UNLESS NOTED)

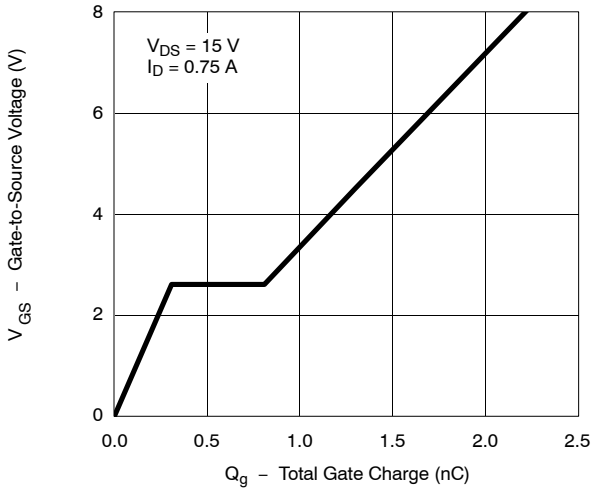
On-Resistance vs. Drain Current



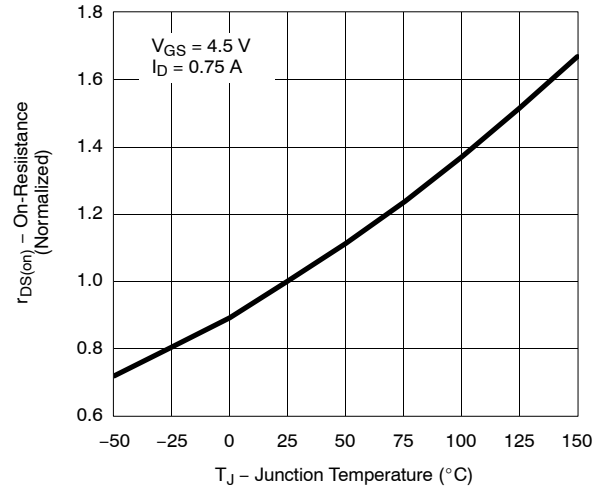
Capacitance



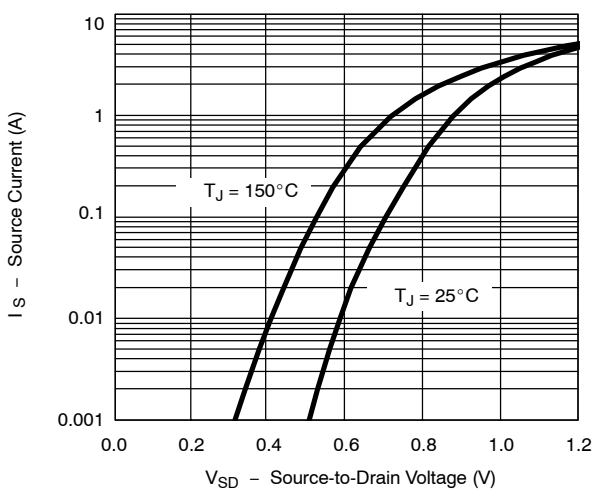
Gate Charge



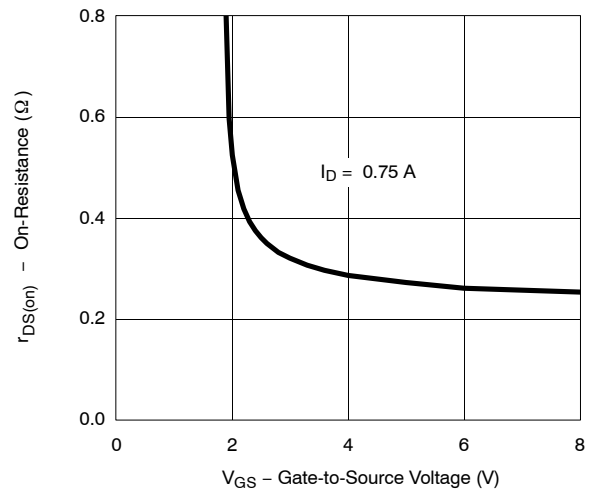
On-Resistance vs. Junction Temperature



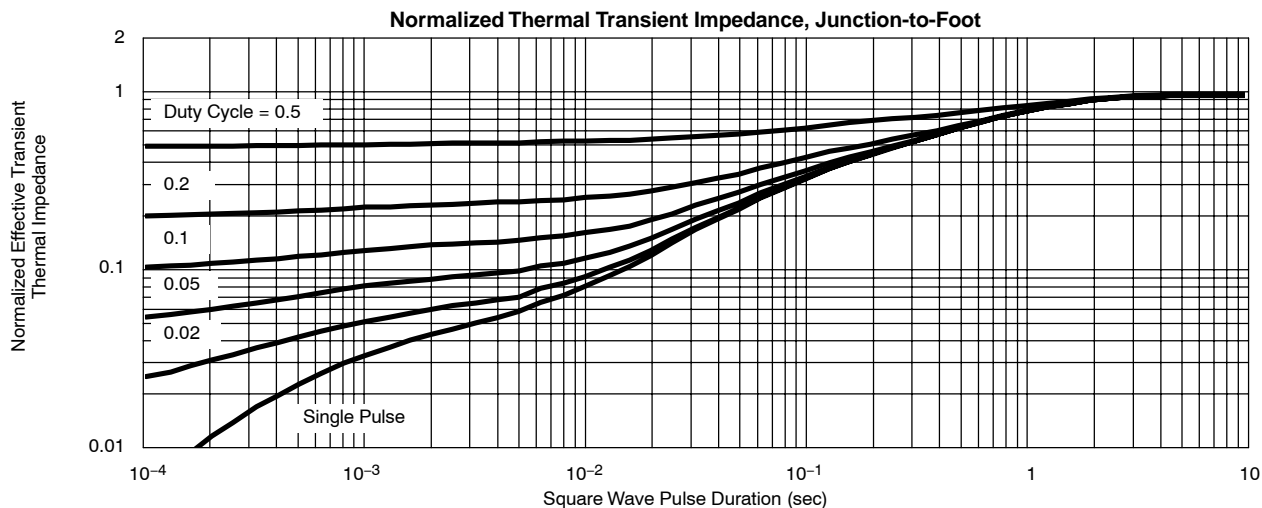
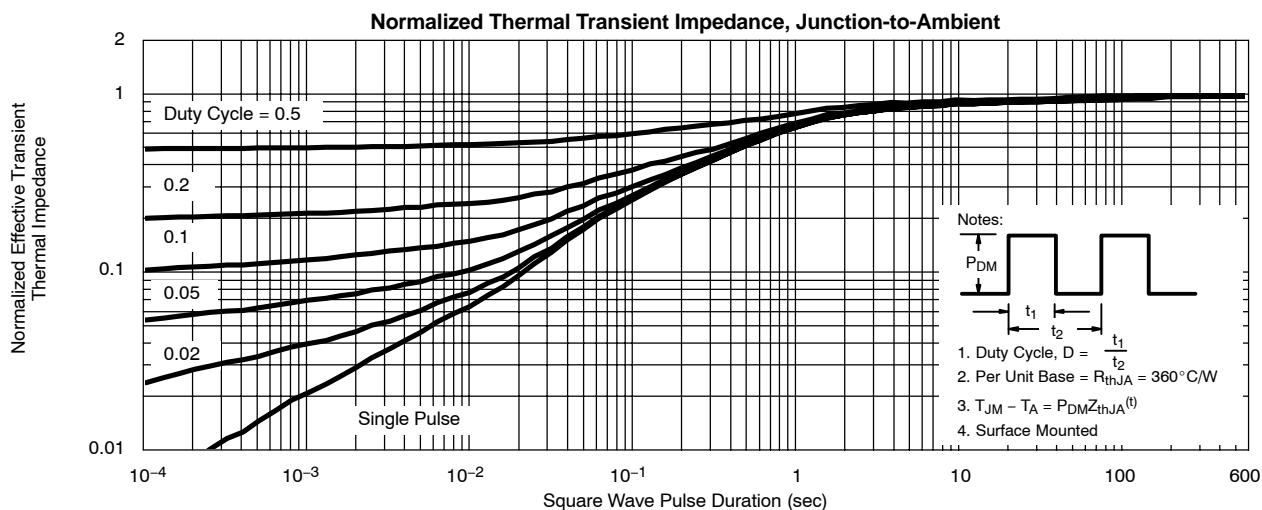
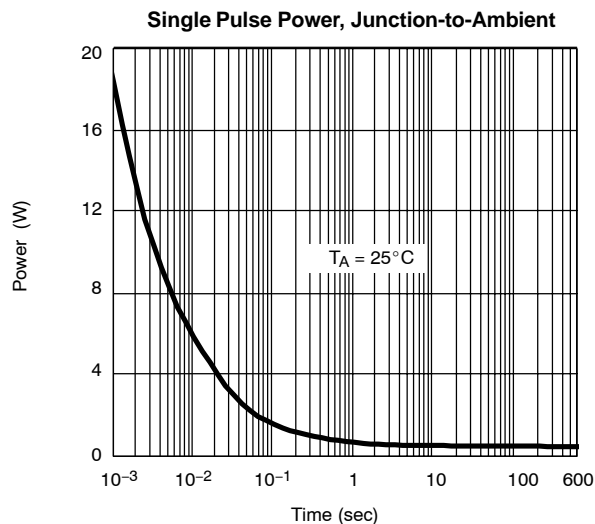
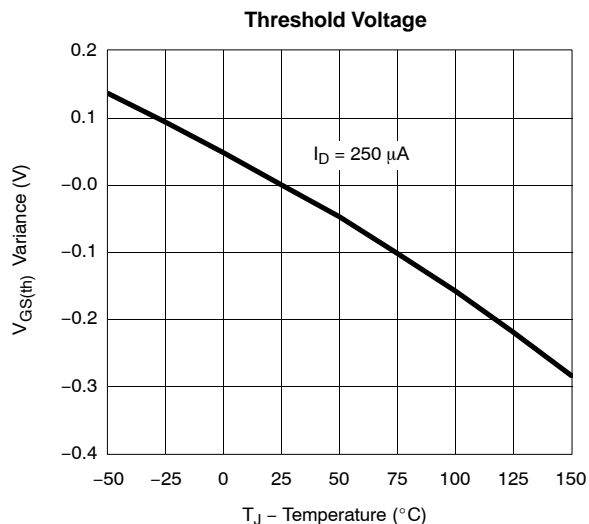
Source-Drain Diode Forward Voltage



On-Resistance vs. Gate-to-Source Voltage



TYPICAL CHARACTERISTICS (25 °C UNLESS NOTED)



Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see <http://www.vishay.com/ppg?71315>.



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