
HD66523

(240-Channel Common Driver with Internal LCD Timing Circuit)

HITACHI

Preliminary

Description

The HD66523 is a common driver for liquid crystal dot-matrix graphic display system. This device incorporates a 240 liquid crystal driver and an oscillator, and generates timing signals (line scanning signals and frame synchronizing signals) required for the liquid crystal display. It features a new LCD driving technique for better quality of display and low power dissipation. Combined with the HD66522, a 160-channel column driver with an internal RAM, the HD66523 is optimal for use in displays for portable information tools.

Features

- LCD timing generator: 1/200, 1/240 duty cycle timing are generated internally.
- Number of LCD drivers: 240
- Power supply voltage: 2.4V to 3.6V
- High voltage LCD drive circuit: $\pm 20V$
- LCD driving technique: Multi-line addressing for low power consumption.
- Programmable vertical retrace period: zero to 192 lines
- Low power consumption
- Internal display off function
- On-chip oscillator combined with external resistor and capacitor.
- Package: TCP

Pin Description

Classification	Symbol	Pin Name	I/O	Number of pins	Functions
Power supply	V _{CC}	V _{CC}	Power supply	2	V _{CC} -GND: logic power supply
	GND	GND	Power supply	2	
	VLCD1, VLCD2	VLCD	Power supply	2	Power supply for LCD driving circuit
	V _{EE1} , V _{EE2}	V _{EE}	Power supply	2	
	VRH1, VRH2	VRH	—	2	LCD drive level power supply
	VM1, VM2	VM	—	2	
	VRL1, VRL2	VRL	—	2	
Control signals	M/ \overline{S}	Master/Slave	I	1	Select master or slave mode.
	DUTY	Duty	I	1	Selects the display duty cycle. Low level: 1/200 display duty ratio High level: 1/240 display duty ratio
	BP4 to BP0	Blanking period	I	5	Set vertical retrace period
	\overline{DOC}	Display off control	I/O	1	Control the display-off function.
	$\overline{DISPOFF}$	Display off	I	1	Turn off the LCD. During display off, all LCD driver output VM level
	SHL	Shift left	I	1	Pin SHL switches the shift direction of the scanning direction.
	\overline{RESET}	Reset	I	1	Reset the LSI internally.
	CR, C, R	Oscillator	—	3	Oscillator with external resistor and capacitor
	TEST1, TEST0	Test	I	2	Test pins, must be connected to GND.
LCD timing	CL1	Clock 1	I/O	1	The bidirectional shift register shifts data at the falling edge of CL1. During master mode, this pin outputs a data transfer clock with a two times larger cycle than the internal oscillator (or the cycle of the external clock) with a duty of 50%. During slave mode, this pin inputs the external data transfer clock.
	FLM	First line marker	I/O	1	During master mode, pin FLM outputs the first line marker signal. During slave mode, this pin inputs the external data first line marker signal.
	FX1, FX0	Scanning function	I/O	2	Output scanning function signals during master mode. Input scanning function signals during slave mode.
	BLANK	Blank	O	1	This pin shows vertical retrace period.
LCD drive output	X1 to X240	X1 to X240	O	240	Select one from among three levels, VRH, VM and VRL.

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Table 1 M/ \overline{S} Signal Status

M/ \overline{S}	Mode	LCD Timing Generator	Status of CL1, FLM and \overline{DOC}
H	Master	1/200 or 1/240 duty cycle	Output
L	Slave	Stops	Input

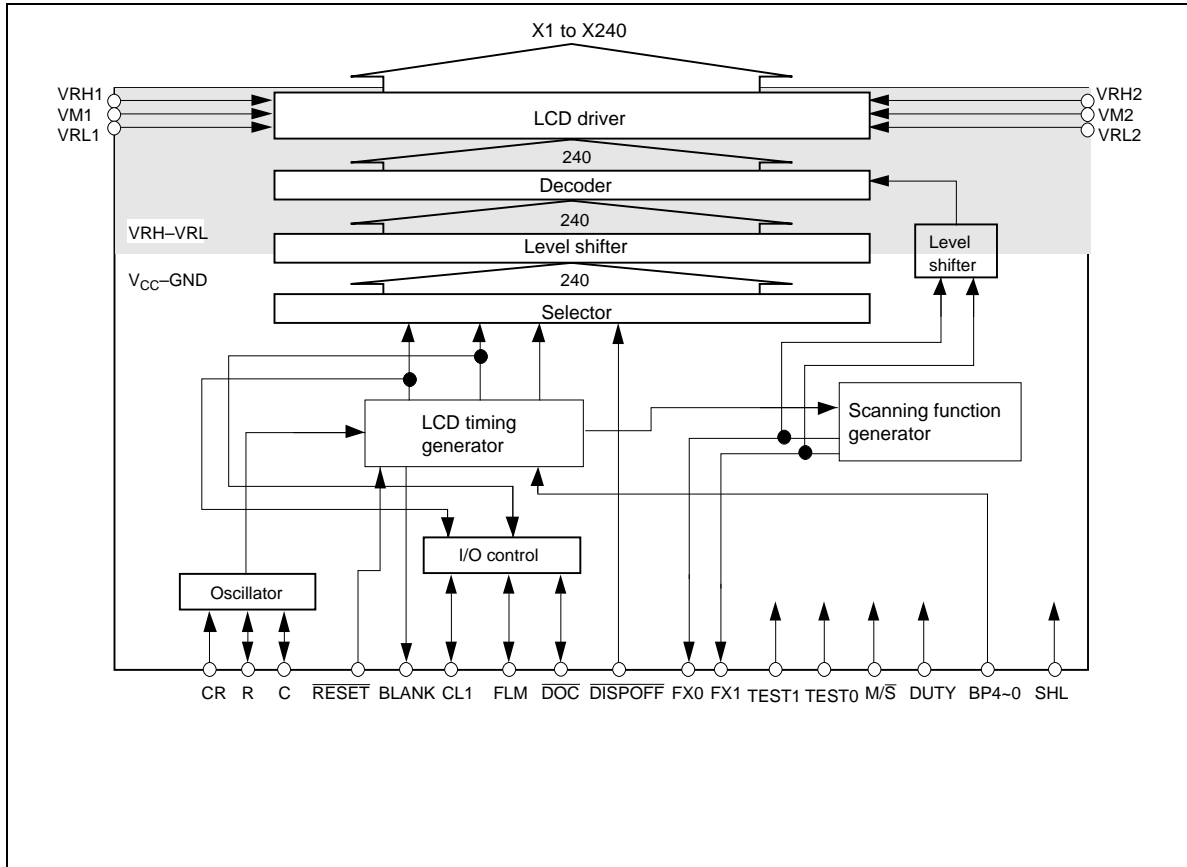
Table 2 Retrace period

BP4	BP3	BP2	BP1	BP0	Horizontal Retrace Period Number of lines
0	0	0	0	0	0
0	0	0	0	1	6
0	0	0	1	0	12
0	0	0	1	1	18
0	0	1	0	0	24
0	0	1	0	1	30
0	0	1	1	0	36
0	0	1	1	1	42
0	1	0	0	0	48
0	1	0	0	1	54
0	1	0	1	0	60
0	1	0	1	1	66
0	1	1	0	0	72
0	1	1	0	1	78
0	1	1	1	0	84
0	1	1	1	1	90
1	0	0	0	0	96
1	0	0	0	1	102
1	0	0	1	0	108
1	0	0	1	1	114
1	0	1	0	0	120
1	0	1	0	1	126
1	0	1	1	0	132
1	0	1	1	1	138
1	1	0	0	0	145
1	1	0	0	1	150
1	1	0	1	0	156
1	1	0	1	1	162
1	1	1	0	0	168
1	1	1	0	1	174
1	1	1	1	0	180
1	1	1	1	1	186

Table 3 Shift Direction

SHL	DUTY	Shift Direction
H	H	X240 → X1
	L	X200 → X1
L	H	X1 → X240
	L	X1 → X200

Internal Block Diagram



- 1. CR Oscillator:** The CR oscillator generates the HD66523 operation clock. During master mode, since the operation clock is needed, connect oscillation resistor R_t with oscillation capacitor C_t . When the external clock is used. Input external clock to pin CR and open pins C and R (Figure 1).
 When using the HD66523 during slave mode, the operation clock will not be needed; therefore, connect pin CR to V_{CC} and open pins C and R (Figure 2).
- 2. Liquid Crystal Timing Generator:** The liquid crystal timing generator creates various signals for the LCD. During master mode ($M/\overline{S} = V_{CC}$), the generator operates the HD66523's internal circuitry as a common internal driver using the generated LCD signals. In addition, signals CL1, FLM and \overline{DOC} created by this generator can synchronously display data on a liquid crystal display by inputting them into the RAM-provided segment driver HD66522 used together with HD66523. During slave mode ($M/\overline{S} = GND$), this generator stops; the slave HD66523 operates based on signals CL1, \overline{DOC} and FLM generated by the master HD66523.

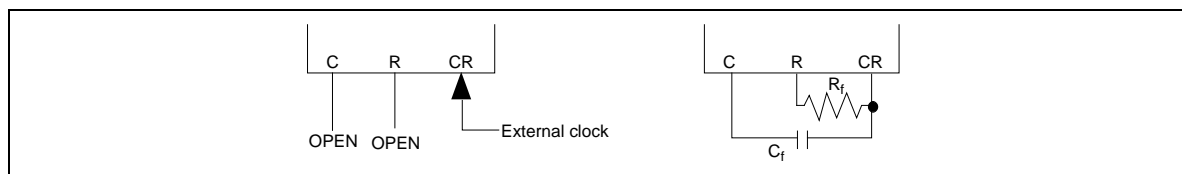


Figure 1 Oscillator Connection in Master Mode

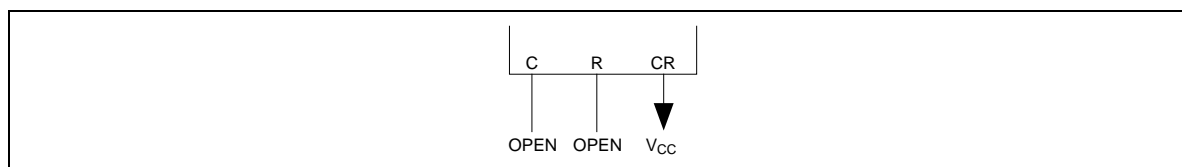


Figure 2 Oscillator Connection in Slave Mode

3. **Scanning Function Generator:** During master mode, this circuit generates the scanning function signals. During slave mode, this circuit stops working and FX1 and FX0 must be supplied from master HD66523.
4. **Selector:** The selector generates signals which select two lines of LCD driver.
5. **Decoder:** Outputs data according to scanning function signals and data.
6. **LCD driver:** Outputs one of three levels according to outputs from decoder.

Internal Function Description

- 1. Generation of Signals CL1 and FLM:** Signal CL1 shifts the scanning signal of the common driver. It is a 50% duty-ratio clock that changes level synchronously with the rising edge of oscillator clock CR.
FLM is a clock signal that goes high once every frame. One frame consists of display lines, 240 lines if DUTY is high and 200 lines if DUTY is low, and vertical retrace period which is set with BP4 to BP0.
- 2. Auto Display-off Control:** This functions prevents incorrect display after reset release. The display is turned off four frames following after reset release. In addition, the display off control signal shown in Figure 4 is output by pin $\overline{\text{DOC}}$. This pin is connected to pin $\overline{\text{DISPOFF}}$ of the HD66522.

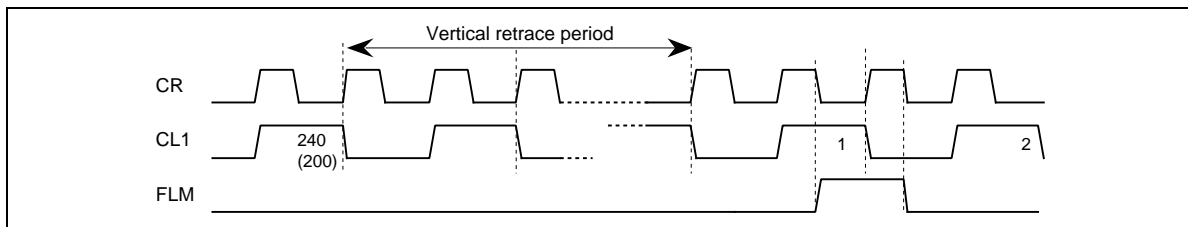


Figure 3 Generation of Signals CL1 and FLM

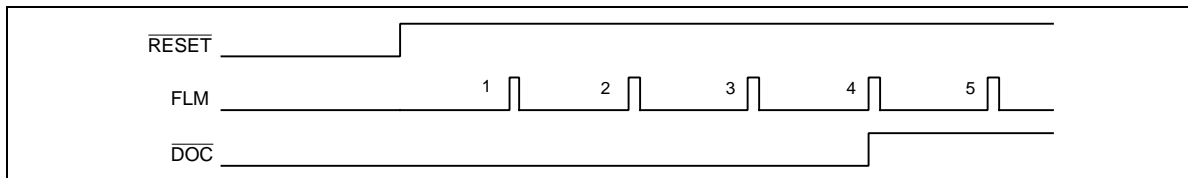


Figure 4 Automatic Display-off Control Function

Application Examples

Outline of HD66523 System Configuration

The HD66523 system configuration is outlined in Figure 5 and 6. Refer to the connection list (Table 4) for connection details.

- When a signal HD66523 is used to configure a small display (Figure 5)
- When two HD66523s are used to configure a large display (Figure 6)

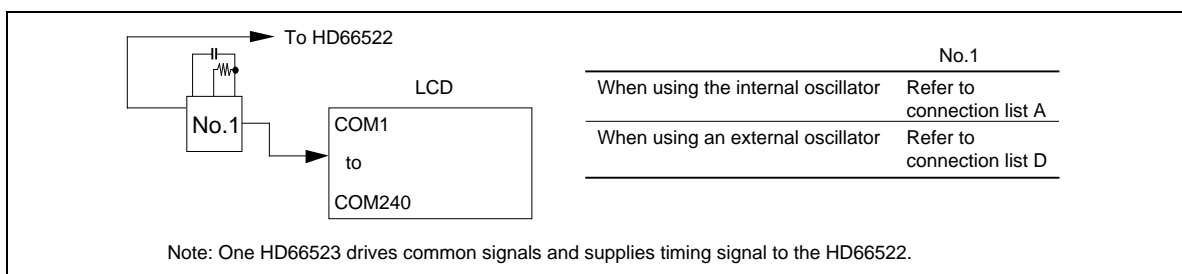


Figure 5 System Configuration When Using a Single HD66523

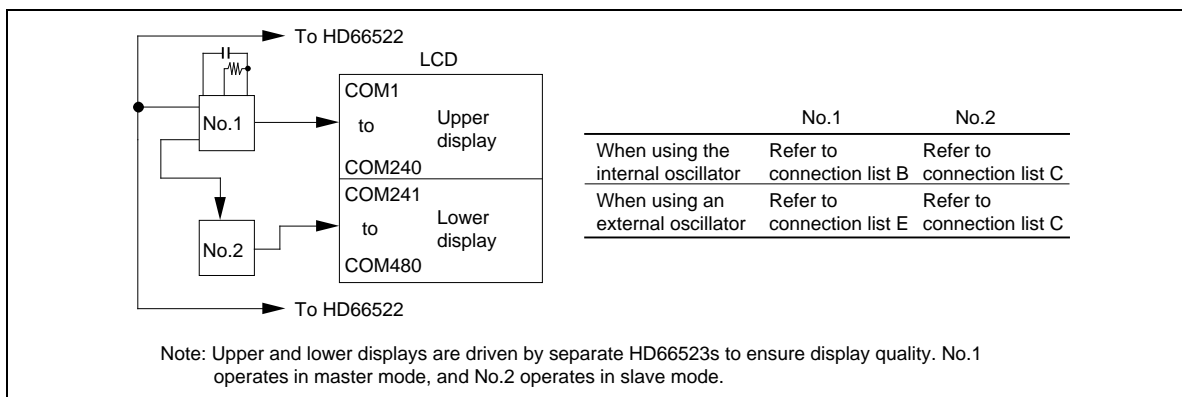


Figure 6 System Configuration When Using a Two HD66523

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Table 4 HD66523 Connection List

Connection Example	M/S	DUTY	BP4 to BP0	RESET	DISPOFF	CR	R	C	CL1	FLM	DOC	FX1 and FX0	SHL X1 to X240
A	H	H	Sets the number of lines for retrace period	From MPU or external reset circuit	From controller	R _f	R _f	C _f	To CL1 of HD66522	To FLM of HD66522	To DISPOFF of HD66522	To FX1 and FX0 of HD66522	H COM1 to COM240 L COM240 to COM1
B	H	H	Sets the number of lines for retrace period	From MPU or external reset circuit	From controller	R _f	R _f	C _f	To CL1 of HD66522, HD66523	To FLM of HD66522, HD66523	To DISPOFF of HD66522, To DOC of HD66523	To FX1 and FX0 of HD66522, HD66523	H COM1 to COM240 L COM240 to COM1
C	L	H	Sets the number of lines for retrace period	From MPU or external reset circuit	H	—	—	—	From CL1 of HD66523	From FLM of HD66523	From DOC of HD66523	To FX1 and FX0 of HD66523	H COM241 to COM480 L COM480 to COM241
D	H	H	Sets the number of lines for retrace period	From MPU or external reset circuit	From controller	External Clock	—	—	To CL1 of HD66522	To FLM of HD66522	To DISPOFF of HD66522	To FX1 and FX0 of HD66522	H COM1 to COM240 L COM240 to COM1
E	H	H	Sets the number of lines for retrace period	From MPU or external reset circuit	From controller	External Clock	—	—	To CL1 of HD66522, HD66523	To FLM of HD66522, HD66523	To DISPOFF of HD66522, To DOC of HD66523	To FX1 and FX0 of HD66522, HD66523	H COM1 to COM240 L COM240 to COM1

Notes: H = V_{CC} (Fixed)
L = GND (Fixed)
"—" means "open"
R_f: Oscillation resistor
C_f: Oscillation capacitor

Example of System Configuration (1)

Figure 7 shows system configuration for a 240 * 160 dots LCD panel using segment driver HD66522 with internal bit-mapped RAM. All required functions can be prepared for liquid crystal display with just two LSIs except for liquid crystal display power supply circuit functions.

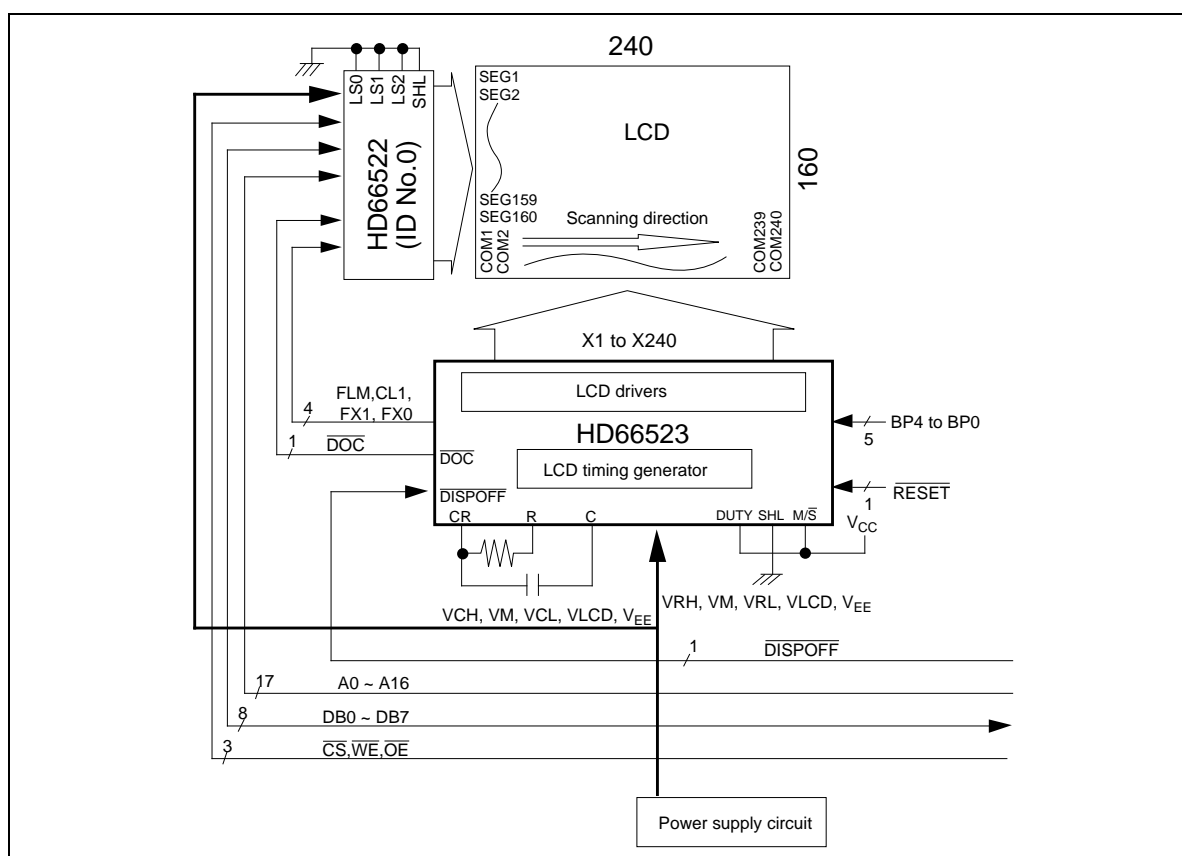


Figure 7 System Configuration (1)

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Example of System Configuration (2)

Figure 8 shows a system configuration for a 240 * 320 dots LCD panel using segment driver HD66522 with internal bit-mapped RAM.

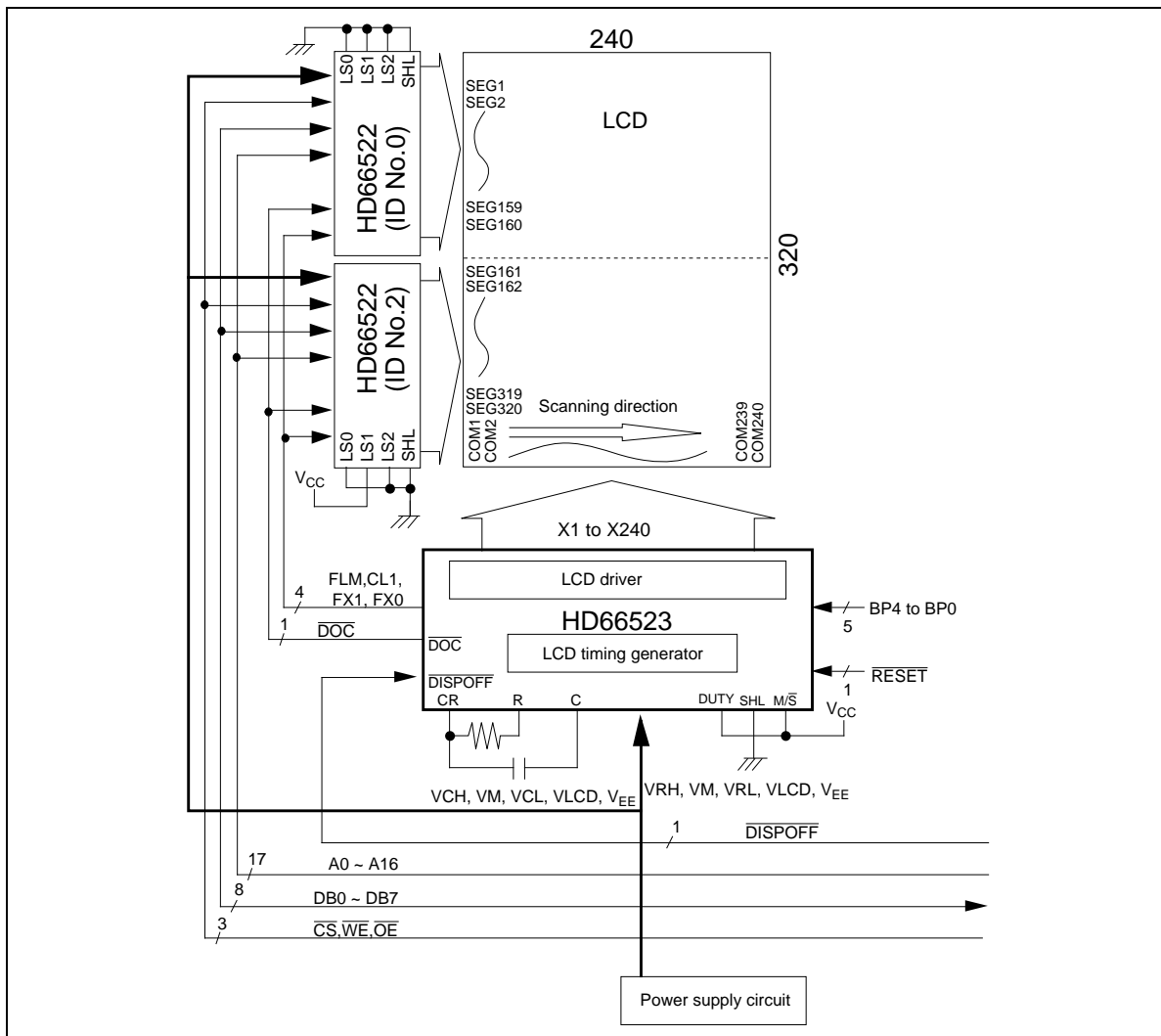


Figure 8 System Configuration (2)

Example of System Configuration (3)

Figure 9 shows a system configuration for a 320 * 480 dots LCD panel using segment driver HD66522 with internal bit-mapped RAM.

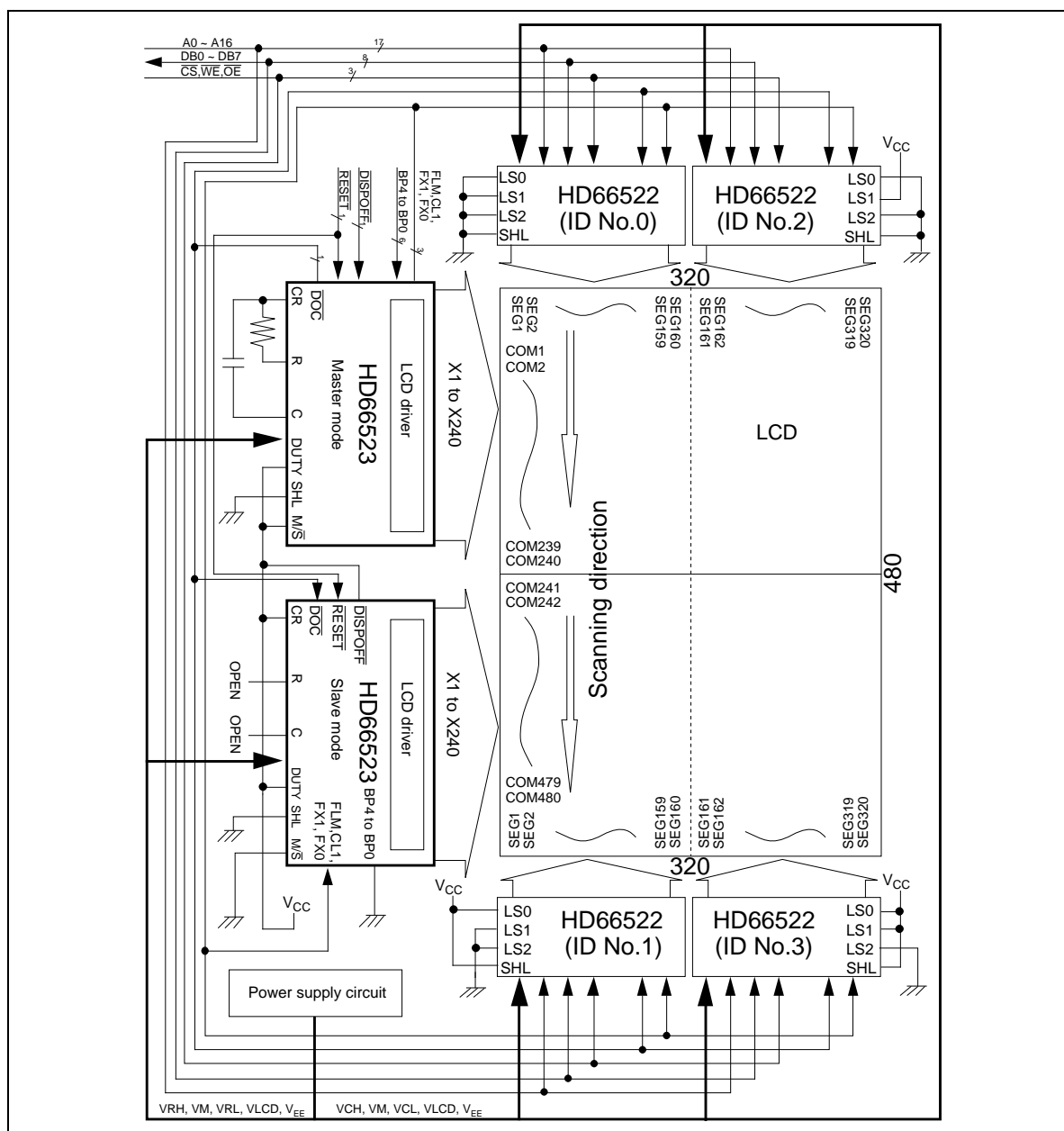


Figure 9 System Configuration (3)

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LCD Drive Output

HD66523 outputs one of three levels, VRH, VM and VRL. VM is unselected level, VRH is high select level and VRL is low select level. Either VRH or VRL level is selected depending on the number of flames and lines. Output timings are showed in Figure 10 to 12.

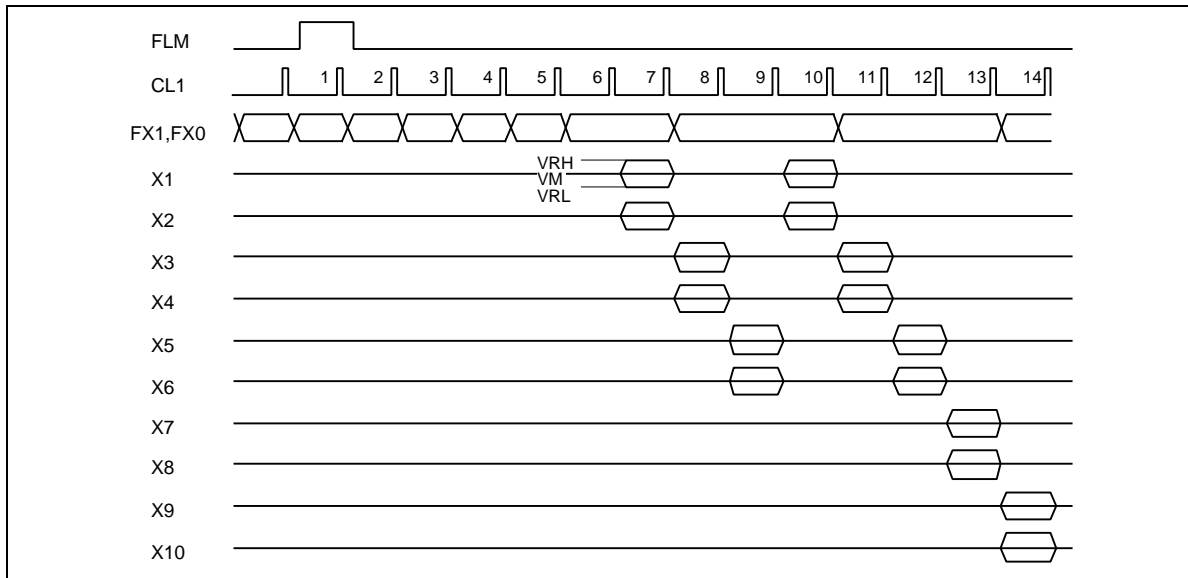


Figure 10 LCD Drive Output Timing at $3n + 1$'s frame ($n = 1, 2, 3, \dots$)

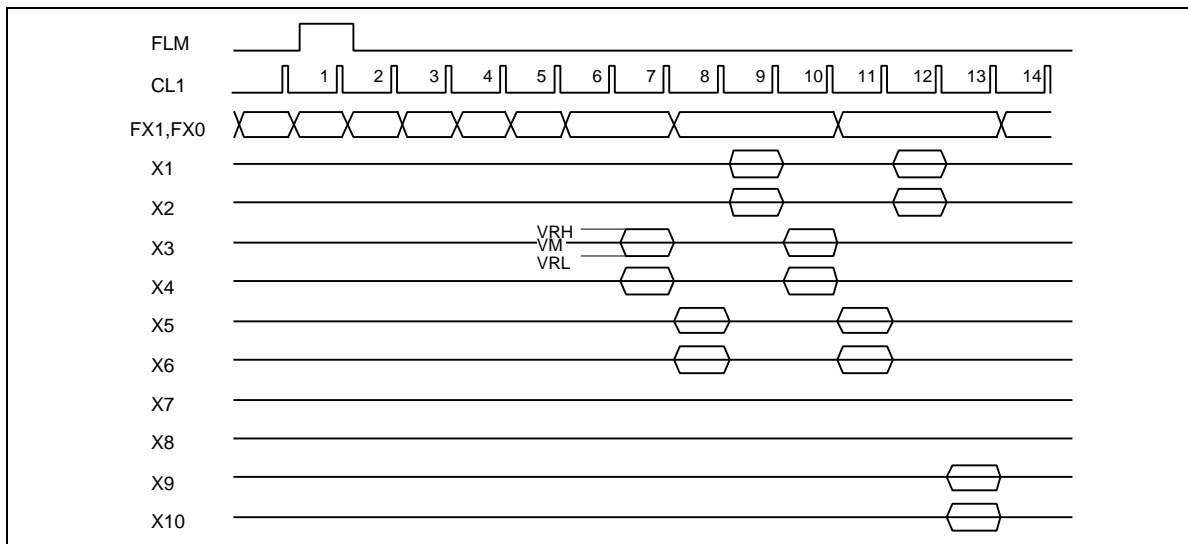


Figure 11 LCD Drive Output Timing at $3n + 2$'s frame ($n = 1, 2, 3, \dots$)

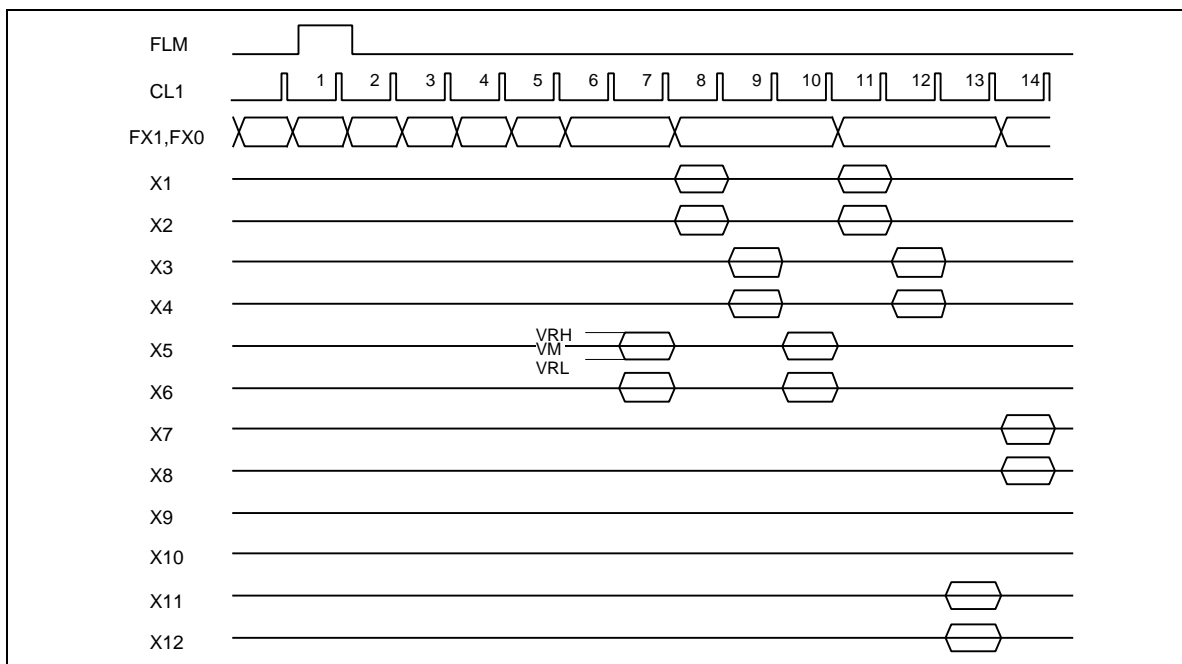


Figure 12 LCD Drive Output Timing at $3n + 3$'s frame ($n = 1, 2, 3, \dots$)

Power Supply Circuit

The example of power circuit is shown in Figure 13. When you want to change contrast, both levels, VRH and VRL must be changed.

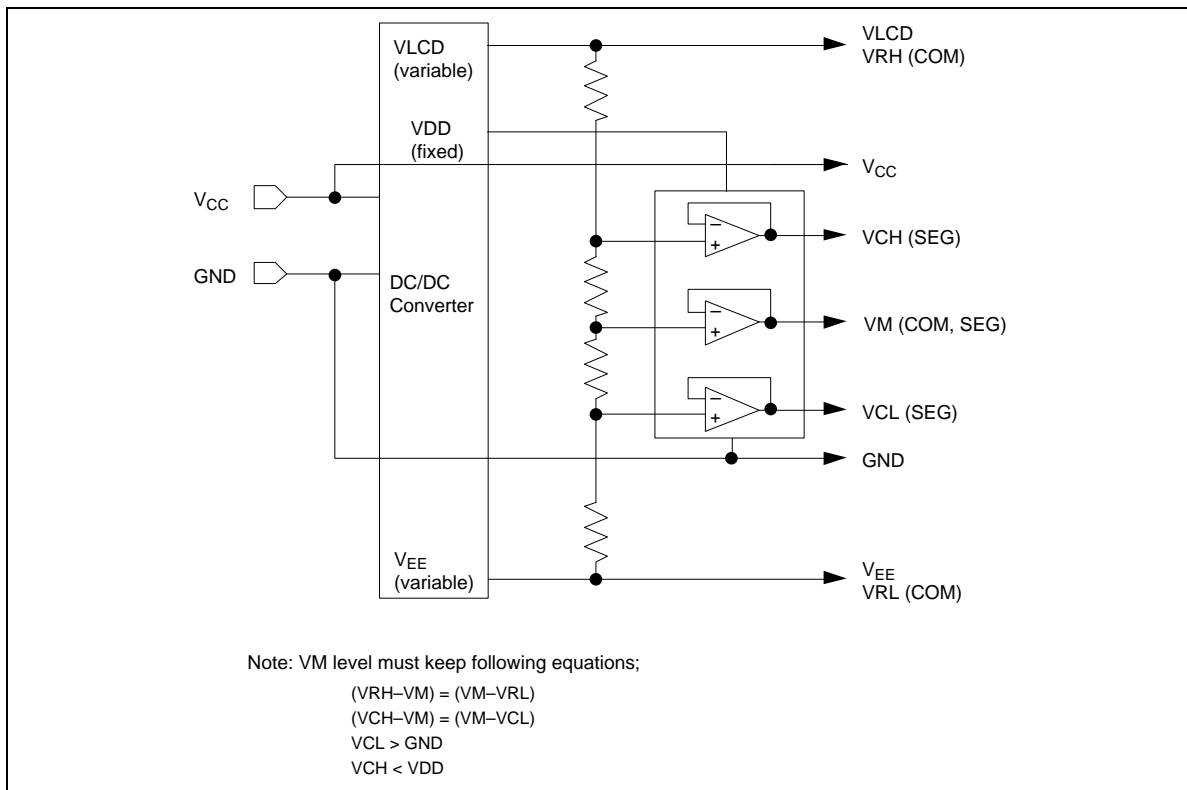


Figure 13 Example of Power Supply Circuit

Absolute Maximum Ratings

Item		Symbol	Rating	Unit	Note
Power voltage	Logic circuit	V_{CC}	-0.3 to + 7.0	V	1
	LCD drive circuit	VRH	-0.3 to +25.0	V	
		VRL	-20.0 to +0.3	V	
Input voltage (1)		VT1	-0.3 to $V_{CC} + 0.3$	V	1, 2
Input voltage (2)		VT2	$V_{EE} - 0.3$ to VLCD + 0.3	V	1, 3
Operating temperature		T_{opr}	-20 to + 75	°C	
Storage temperature		T_{stg}	-40 to + 125	°C	

- Notes:
1. The reference point is GND (0V)
 2. Applies to pins M/\bar{S} , DUTY, BP4 to BP0, \overline{DOC} , $\overline{DISPOFF}$, SHL, \overline{RESET} , CR, CL1, FLM, FX0 to FX1, and TEST1 to TEST0.
 3. Applies to pins VM1 and VM2.
Supply the same voltage to pairs VRH1 and VRH2, VM1 and VM2, VRL1 and VRL2.
 4. If the LSI is used beyond its absolute maximum rating, it may be permanently damaged. It should always be used within the limits of its electrical characteristics in order to prevent malfunction or unreliability.

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Electrical Characteristics

DC Characteristics ($V_{CC} = 2.4$ to $3.6V$, $GND = 0V$, $VLCD = 18$ to $23V$, $V_{EE} = -12$ to $-17V$, $T_a = -20$ to $+75^{\circ}C$)

Item	Symbol	Applicable Pins	min.	typ.	max.	Unit	Measurement Condition	Notes
Input high level voltage	V_{IH1}		$0.8 \times V_{CC}$	—	V_{CC}	V		1
Input low level voltage	V_{IL1}		0	—	$0.2 \times V_{CC}$	V		1
Output high level voltage	V_{OH}		$0.9 \times V_{CC}$	—	—	V	$I_{OH} = -50 \mu A$	2
Output low level voltage	V_{OL}		—	—	$0.1 \times V_{CC}$	V	$I_{OL} = 50 \mu A$	2
Input leakage current (1)	I_{IL1}		-2.5	—	2.5	μA	$V_{IN} = V_{CC}$ to GND	1
Input leakage current (2)	I_{IL2}	VRH1, VRH2, VM1, VM2, VRL1, VRL2	-25	—	25	μA	$V_{IN} = VLCD$ to V_{EE}	1
Vi-Vj ON resistance	R_{ON}	X1 to X240	—	1.0	2.0	k Ω	$I_{ON} = 100 \mu A$	3
Current consumption (1)	I_{MS}		—	—	T.B.D.	μA	Master mode 1/240 duty cycle, $C_i = 100pF$ $R_i = 180k\Omega$ $V_{CC} = 3.0V$	4
Current consumption (2)	I_{SL}		—	—	T.B.D.	μA	Slave mode 1/240 duty cycle, $f_{CL} = 16.8 kHz$, $V_{CC} = 3.0V$	4
Current consumption (3)	I_{LCD}		—	—	T.B.D.	μA	Master mode 1/240 duty cycle, $C_i = 100pF$ $R_i = 180k\Omega$ $V_{CC} = 3.0V$ $VLCD = 23V$ $V_{EE} = -17V$	4

- Notes: 1. Applied to input pins M/\bar{S} , DUTY, BP4 to BP0, $\bar{DISPOFF}$, SHL, \bar{RESET} , TEST1, TEST0 and CR, and I/O pins, \bar{DOC} , CL1 and FLM during input state.
2. Applied to output pins, FX1 and FX0, and I/O pins, \bar{DOC} , CL1 and FLM, during output stage.
3. Indicates the resistance between on pin from X1 to X240 and another pin from the V pins, VRH1/VRH2, VM1/VM2 and VRL1/VRL2, when load current is applied to the X pin; defined under the following conditions:
 $VRH = +23V$, $VRL = -17V$
 $VM = 1/2 * (VRH - VRL)$
4. Input and Output currents are excluded. When a CMOS input is floating, excess current flows from the power supply to the input circuit. To avoid this, V_{IH} and V_{IL} must be held to V_{CC} and GND levels, respectively.

Item	Symbol	min.	typ.	max.	Unit.	Measurement Condition	Notes
Operating frequency (1)	f_{opr1}	10	—	200	kHz	Master mode (External clock operation)	1
Operating frequency (2)	f_{opr2}	5	—	100	kHz	Slave mode frequency of CL1	2
Oscillation frequency	f_{osc}	30	36	42	kHz	$C_i = 100\text{pF}$ $R_i = 180\text{k}\Omega$	
External clock duty	Duty	45	50	55	%	Master mode	3
External clock rising time	t_r	—	—	100	ns	Master mode	3
External clock falling time	t_f	—	—	100	ns	Master mode	3

- Notes: 1. External clock is supplied to CR pin during master mode, and C and R pins must be left open.
2. Applies to the clock which is supplied to CL1 during slave mode. CR must be connected to GND, and C and R pins must be left open.
3. Applies to the external clock which is supplied to CR during a master mode.

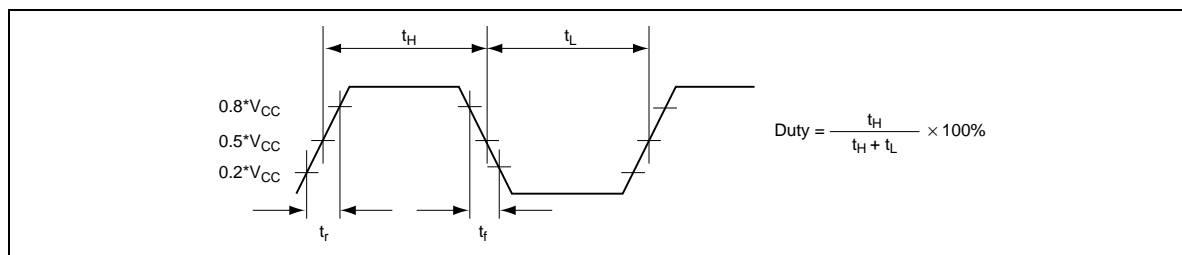


Figure 14 External Clock

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AC Characteristic ($V_{CC} = 2.4$ to $3.6V$, $GND = 0V$, $T_a = -20$ to $75^{\circ}C$)

No.	Item	Symbol	Applicable Pins	min.	max.	Units	Notes
(1)	CL1 high-level width	t_{CWH}	CL1	1.0	—	μs	1
(2)	CL1 low-level width	t_{CWL}	CL1	1.0	—	μs	1
(3)	CL1 rise time	t_r	CL1	—	100	ns	1
(4)	CL1 fall time	t_f	CL1	—	100	ns	1
(5)	FLM setup time	t_{FS}	FLM, CL1	2.0	—	μs	1
(6)	FLM hold time	t_{FH}	FLM, CL1	1.0	—	μs	1
(7)	CL1 delay time	t_{CL1}	CL1	1.0	—	μs	2
(8)	FLM delay time	t_{DFLM}	FLM	1.0	—	μs	2

Notes: 1. Applies during slave mode
2. Applies during master mode

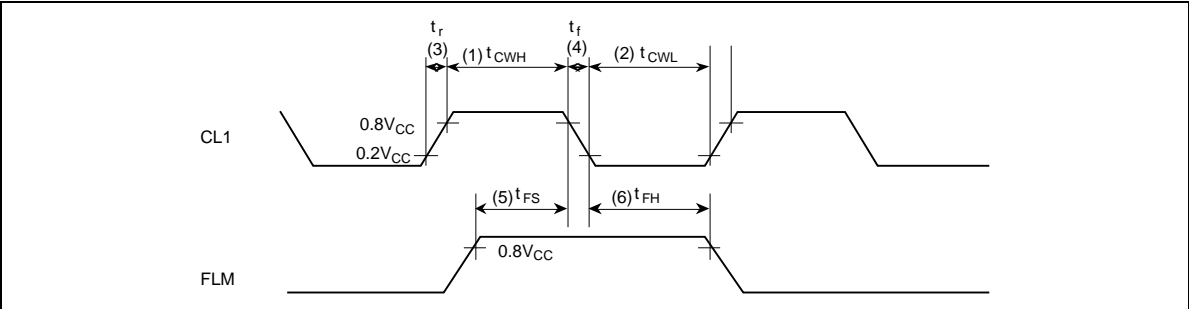


Figure 15 Slave Mode Timing

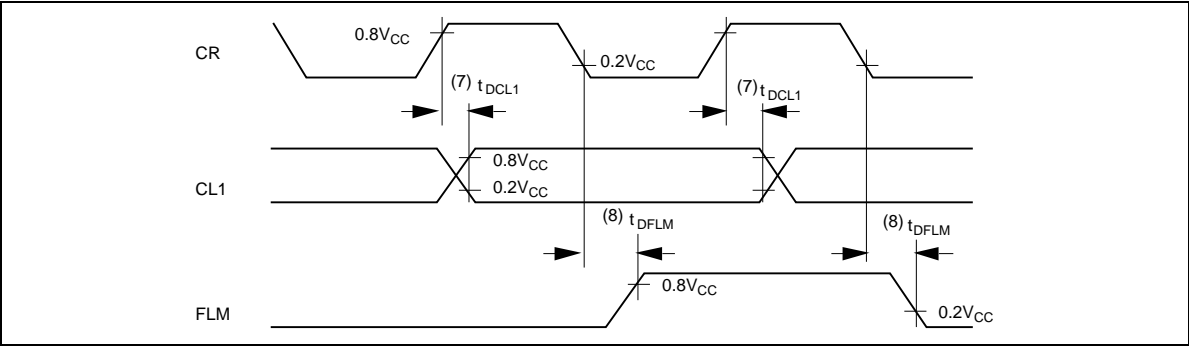


Figure 16 Master Mode Timing