HD66520T

(160-Channel 4-Level Grayscale Display Column Driver with Internal Bit-Map RAM)

HITACHI

Description

The HD66520 is a column driver for liquid crystal dot-matrix graphic display systems. This LSI incorporates 160 liquid crystal drive circuits and a 160 × 240 × 2-bit bit-map RAM, which is suitable for LCDs in portable information devices. It also includes a general-purpose SRAM interface so that draw access can be easily implemented from a general-purpose CPU. The HD66520 also has a new arbitration method which prevents flicker when the CPU performs draw access asynchronously. The on-chip display RAM greatly decreases power consumption compared to previous liquid crystal display systems because there is no need for high-speed data transfer. The chip also incorporates a four-level grayscale controller for enhanced graphics capabilities, such as icons on a screen.

Features

- Duty cycle: 1/64 to 1/240
- Liquid crystal drive circuits: 160
- Low-voltage logic circuit: 3.0 to 5.5-V operation power supply voltage
- High-voltage liquid crystal drive circuit: 8 to 28-V liquid crystal drive voltage
- Grayscale display: FRC four-level grayscale display
- Grayscale memory management: Packed pixel
- Internal bit-map display RAM: 76800 bits (160 × 240 lines × two planes)
- CPU interface
  - SRAM interface
  - Address bus: 16 bits, data bus: 8 bits

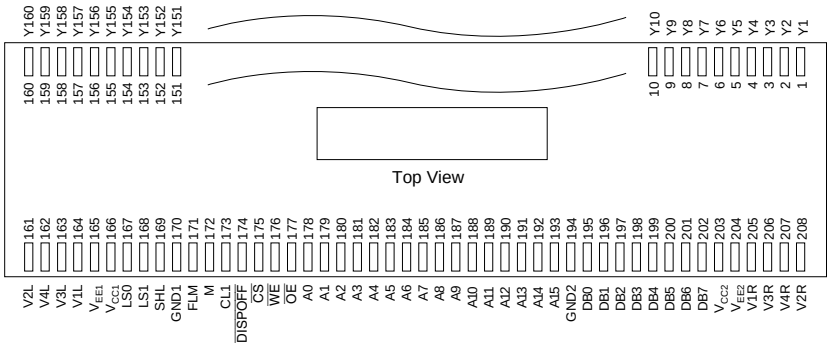
- High-speed draw function: Supports burst transfer mode
- Arbitration function: Implemented internally (draw access has priority)
- Access time
  - 180 ns (V_{CC} = 5V operation)
  - 240 ns (V_{CC} = 3V operation)
- Low power consumption:
  V_{CC} = 3.3-V operation
  - 360 µA during display (logic circuit, liquid crystal drive circuit)
  - 10 mA during RAM access (logic circuit)

  V_{CC} = 5.5-V operation
  - 400 µA during display (logic circuit, liquid crystal drive circuit)
  - 16 mA during RAM access (logic circuit)
- On-chip address management function
- Refresh unnecessary
- Internal display off function
- Package: 208-pin TCP

Ordering Information

Type No.	TCP	Outer Lead Pitch (µm)
HD66520TA0	Straight TCP	200
HD66520TB0	Folding TCP	200

Pin Arrangement



Note : This figure does not specify the TCP dimensions.

Pin Description

Classi-fication	Symbol	Pin No.	Pin Name	I/O	Number of Pins	Function
Power supply	V_{CC1} V_{CC2}		V_{CC} V_{CC}	— —		V_{CC}–GND: logic power supply
	GND1 GND2		GND GND	— —		
	V_{EE1} V_{EE2}		LCD drive circuit power supply	— —		V_{CC}–V_{EE}: LCD drive circuit power supply
	V1L, V1R		LCD select high-level voltage	Input	2	LCD drive level power supplies See Figure 1. The user should apply the same potential to the L and R side.
	V2L, V2R		LCD select low-level voltage	Input	2	
	V3L, V3R		LCD deselect high-level voltage	Input	2	
	V4L, V4R		LCD deselect low- level voltage	Input	2	
Control	LS0, LS1		LSI ID select switch pin0 and 1	Input	2	Pins for setting LSI ID no (refer to signals **Pin Functions** for details).
	SHL		Shift direction control signal	Input	1	Reverses the relationship between LCD drive output pins Y and addresses.
	FLM		First line marker	Input	1	First line select signal.
	CL1		Data transfer clock	Input	1	Clock signal to transfer the line data to an LCD display driver block.
	M		AC switching signal	Input	1	Switching signal to convert LCD drive output to AC.
	$\overline{DISPOF}$ $\overline{F}$		Display off signal	Input	1	Control signal to fix LCD driver outputs to LCD select high level. When low, LCD drive outputs Y1 to Y160 are set to V1, or LCD select high level. Display can be turned off by setting a common driver to V1.

Classi-fication	Symbol	Pin No.	Pin Name	I/O	Number of Pins	Function
Bus interface	A0 to A15		Address input	Input	16	Upper 9 bits (A15–A7) are used for the duty-directional addresses, and lower 7 bits (A6–A0) for the output-pin directional addresses (refer to **Pin Functions** for details).
	DB0 to DB7		Data input/ output	I/O	8	Packed-pixel 2-bit/pixel display data transfer (refer to **Pin Functions** for details).
	$\overline{CS}$		Chip select signal	Input	1	LSI select signal during draw access (refer to **Pin Functions** for details).
	$\overline{WE}$		Write signal	Input	1	Write-enable signal during draw access (refer to **Pin Functions** for details).
	$\overline{OE}$		Output enable signal	Input	1	Output-enable signal during draw access (refer to **Pin Functions** for details).
LCD drive output	Y1 to Y160		LCD drive output	Output	160	Each Y outputs one of the four voltage levels V1, V2, V3, or V4, depending on the combination of the M signal and data levels

Note: The number of input outer leads: 48

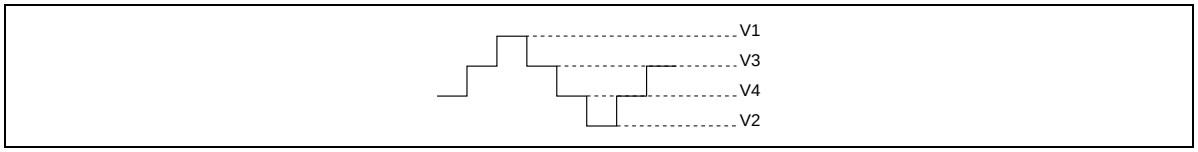


Figure 1 LCD Drive Levels

Pin Functions

Control Signals

LS0 and LS1 (Input): The LS pins can assign four (0 to 3) ID numbers to four LSIs, thus making it possible to connect a maximum of four HD66520s sharing the same $\overline{CS}$ pin to the same bus (Figure 2.)

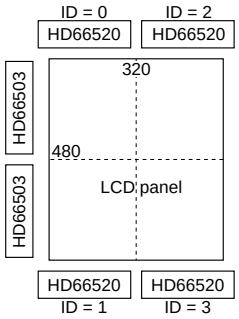
SHL (Input): This pin reverses the relationship between LCD drive output pins Y1 to Y160 and addresses. There is no need to change the address assignment for the display regardless of whether the HD66520 is mounted from the back or the front of the LCD panel. Refer to Driver Layout and Address Management for details.

FLM (Input): When the pin is high, it resets the display line counter, returns the display line to the start line, and synchronizes common signals with frame timing.

CL1 (Input): At each falling edge of data-transfer clock pulses input to this pin, the latch circuits latch display data and output it to the liquid crystal display driver section.

M (Input): AC voltage needs to be applied to liquid crystals to prevent deterioration due to DC voltage application. The M pin is a switch signal for liquid crystal drive voltage and determines the AC cycle.

$\overline{DISPOFF}$ (Input): A control signal to fix liquid crystal driver output to liquid crystal select high level. When this pin is low, liquid crystal drive outputs Y1 to Y160 are set to liquid crystal select high level V1. The display can be turned off by setting the outputs of the common driver to level V1. In this case, display RAM data will be retained. Therefore, if signal $\overline{DISPOFF}$ returns to high level, liquid crystal drive outputs will return to normal display state. Draw access can be executed when signal $\overline{DISPOFF}$ is either in high or low state.



LS1	LS0	ID No.	RAM Address Arrangement
L	L	0	Upper-left of LCD panel
L	H	1	Lower-left of LCD panel
H	L	2	Upper-right of LCD panel
H	H	3	Lower-right of LCD panel

L: Low level
H: High level

Figure 2 LS Pins and Address Assignment

Power Supply Pins

V_{CC1-2} and GND1–2: These pins supply power to the logic circuit.

V_{CC1-2} and V_{EE1-2}: These pins supply power to the liquid crystal circuits.

V1L, V1R, V2L, V2R, V3L, V3R, V4L, V4R: These pins are used to input the level power supply to drive the liquid crystal.

Bus Interface

$\overline{CS}$ (Input): A basic signal of the RAM area. When $\overline{CS}$ is low (active), the system can access the on-chip RAM of the LSI whose address space, set by LS0, LS1, and SHL pins, contains the input address. When $\overline{CS}$ is high, it is prohibited to access the RAM.

In addition, this signal is used for arbitration control when draw access from the CPU competes with display access that is used to transfer line data to the liquid crystal panel. Note that there are restraints for the pulse width, as shown in Figure 3. The example shown here is when V_{CC} = 3V for a write operation.

A0 to A15 (Input): A bus to transfer addresses during RAM access. Upper nine bits (A15 to A7) are duty-direction addresses, and lower seven bits (A6 to A0) are output pin-direction addresses.

$\overline{WE}$ (Input): When $\overline{WE}$ is during low level, the RAM is in active mode, and during high level, it is prohibited to access the RAM. This is used to write display data to the RAM. Only the LSI whose address space, set by pins LS0, LS1, and SHL, contains the input address can be written to when $\overline{CS}$ is low.

$\overline{OE}$ (Input): When $\overline{OE}$ is during low level the RAM is in active mode, and during high level, it is prohibited to access the RAM. This is used to read display data from the RAM. Only the LSI whose address space, set by pins LS0, LS1, and SHL, contains the input address can be read from when $\overline{CS}$ is low.

DB0 to DB7 (Input/Output): The pins function as data input/output pins. They can accommodate to a data format with 2 bits/pixel, which implement packed-pixel four-level grayscale display.

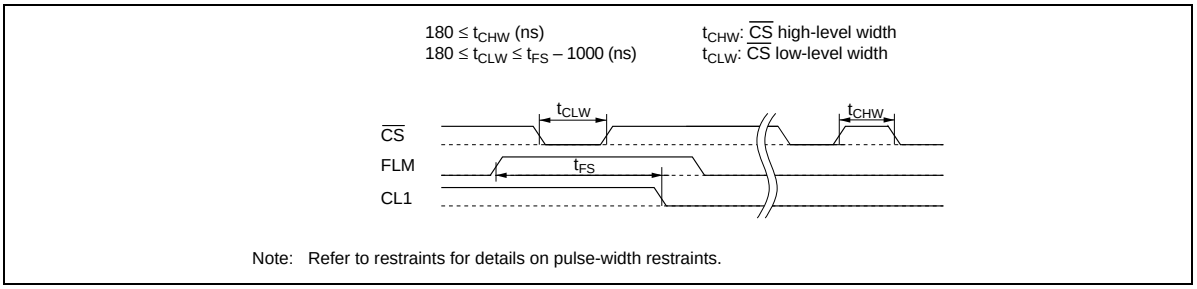


Figure 3 $\overline{CS}$ (Input)

Block Diagram

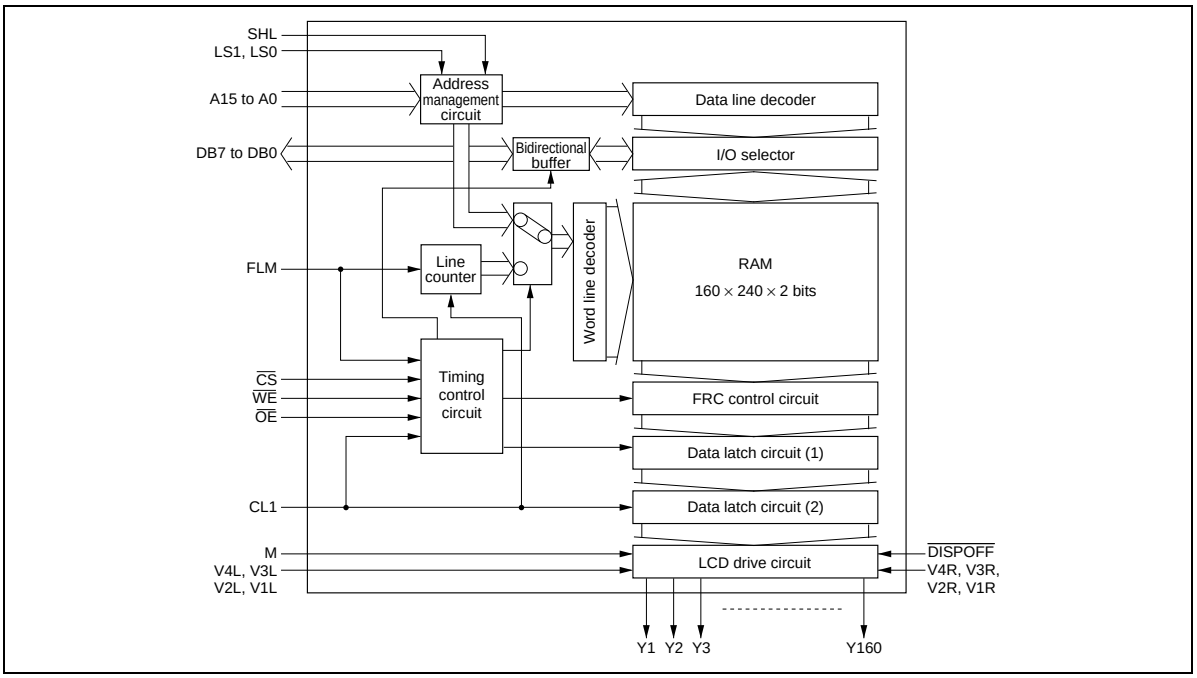


Figure 4 Block Diagram

Address Management Circuit: Converts the addresses input via A15–A0 from the system to the addresses for a memory map of the on-chip RAM. When several LSIs (HD66520s) are used, only the LSI whose address space, set by pins LS0, LS1, and SHL, contains the input address, accepts the access from the system, and enables the inside. The address management circuit enables configuration of the LCD display system with memory addresses not affected by the connection direction, and reduces burdens of software and hardware in the system. Refer to the How to Use the LS1 and LS0 Pins to set pins LS0, LS1, and SHL.

Timing Control Circuit: This circuit controls arbitration between display access and draw access. Specifically, it controls access timing while receiving signals FLM, CL1, $\overline{CS}$, $\overline{WE}$, and $\overline{OE}$ as input. FLM and CL1 are used to perform refresh (display access), that is, to transfer line data to the liquid crystal circuit. $\overline{CS}$, $\overline{WE}$, and $\overline{OE}$ are used for the CPU to perform draw operation (draw access), that is, to read and write display data from and to the internal RAM. This circuit also generates a timing signal for the FRC control circuit to implement four-level grayscale display.

Line Counter: Operates refresh functions. When FLM is high, the counter clears the count value and generates an address to select the first line in the RAM section. The counter increments its value whenever CL1 is valid and generates an address to select subsequent lines in the RAM section.

Bidirectional Buffer: Controls the transfer direction of the display data according to signals from pins $\overline{WE}$ and $\overline{OE}$ in draw operation from the system.

Word Line Decoder: Decodes duty addresses (A15 to A7) and selects one of 240 lines in the display RAM section, and activates one-line memory cells in the display RAM section.

Data Line Decoder: Decodes pin addresses (A6 to A0) and selects a data line in the display RAM section for the 7-bit memory cells in one-line memory cells activated by the word line decoder.

I/O Selector: Reads and writes 8-bit display data for the memory cells in the RAM section.

Display RAM: $160 \times 240 \times 2$-bit memory cell array. Since the memory is static, display data can be held without refresh operation during power supply.

FRC Circuit: Implements FRC (frame rate control) function for four-level grayscale display. For details, refer to Half Tone Display.

Data Latch Circuit (1): Latches 160-pixel grayscale display data processed by the FRC control circuit after being read from the display RAM section by refresh operation. This circuit is needed to arbitrate between display access for performing liquid crystal display and draw access from the CPU.

Data Latch Circuit (2): This circuit again outputs the data in data latch circuit (1) synchronously with signal CL1.

LCD Drive Circuit: Selects one of LCD select/deselect power levels V4R to V1R and V4L to V1L according to the grayscale display data, AC signal M, and display-off signal $\overline{DISPOFF}$. The circuit is configured with 160 circuits each generating LCD voltage to turn on/off the display.

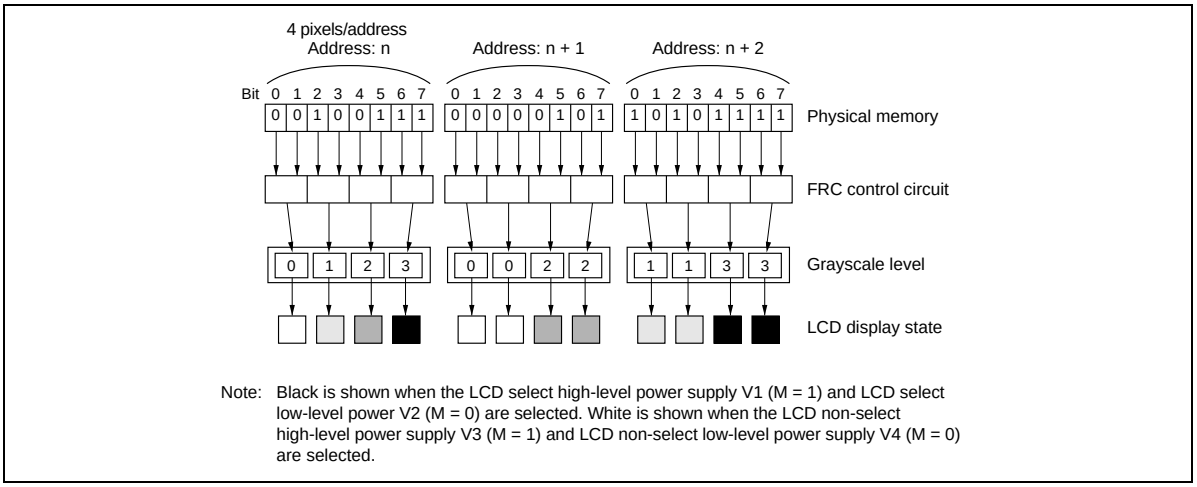
Configuration of Display Data Bit

Packed Pixel Method

For grayscale display, multiple bits are needed for one pixel. In the HD66520, two bits are assigned to one pixel, enabling a four-level grayscale display.

One address (eight bits) specifies four pixels, and pixel bits 0 and 1 are managed as consecutive bits. When grayscale display data is manipulated in bit units, one memory access is sufficient, which enables smooth high-speed data rewriting.

The bit data to input to pin DB7, DB5, DB3, and DB1 becomes MSB and the bit data to input via pin DB6, DB4, DB2, and DB0 is LSB.



Note: Black is shown when the LCD select high-level power supply V1 (M = 1) and LCD select low-level power V2 (M = 0) are selected. White is shown when the LCD non-select high-level power supply V3 (M = 1) and LCD non-select low-level power supply V4 (M = 0) are selected.

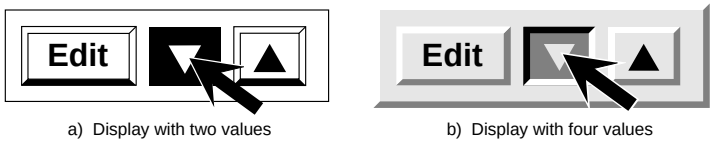
Figure 5 Packed Pixel System

Half Tone Display (FRC: Frame Rate Control Function)

The HD66520 incorporates an FRC function to display four-level grayscale half tone.

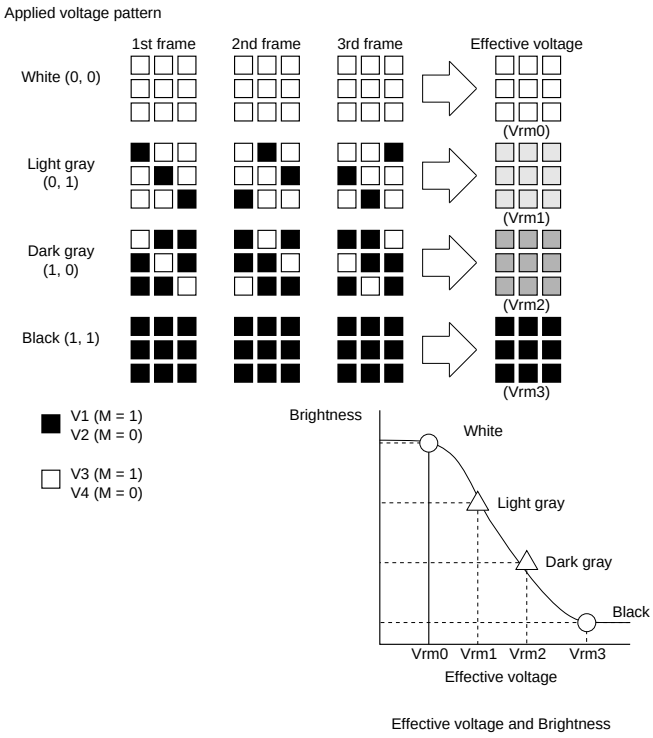
The FRC function utilizes liquid crystal characteristics whose brightness is changed by an effective value of applied voltage. Different voltages are applied to each frame and half brightness is expressed in addition to display on/off.

Since the HD66520 has two-bit grayscale data per one pixel, it can display four-level grayscale and improve user interface (Figure 6). Figure 7 shows the relationships between voltage patterns applied to each frame, the effective voltage value, and brightness obtained.



a) Display with two values b) Display with four values

Figure 6 Example of User Interface Improvement



Note: Black is shown when the LCD select high-level power supply V1 (M = 1) and LCD select low-level power V2 (M = 0) are selected. White is shown when the LCD non-select high-level power supply V3 (M = 1) and LCD non-select low-level power supply V4 (M = 0) are selected.

Figure 7 Effective Voltage Values vs. Brightness

Address Management

The HD66520 has an address management function that corresponds to three display sizes all of which are standard sizes for portable information devices: a 160-dot-wide by 240-dot-long display (small information devices); a 320-dot-wide by 240-dot-long display (quarter VGA size); and a 320-dot-wide by 480-dot-long display (half VGA size). Up to four HD66520s can be connected to at a time to configure easily liquid crystal displays with the resolutions mentioned above.

Driver Layout and Address Management

The Y lines on a liquid crystal panel and memory data in a driver are inverted horizontally depending on the connection side of the liquid crystal panel and the driver. When several drivers are connected, address management is needed for each driver. Although reinverted bit-map plotting or address management by the $\overline{CS}$ pin in each driver are possible by using special write addressing, the load on the software is significantly increased. To avoid this, the HD66520 provides memory addresses independent of connection side, but responds to the setting of pins LS0, LS1, and SHL.

How to Use the LS1 and LS0 Pins

Pins LS1 and LS0 set the LSI position (up to four) as shown in Figure 8 by assigning ID numbers 0 to 3 to each HD66520.

LS1	LS0	ID No.	Address Arrangement
L	L	0	Upper-left side
L	H	1	Lower-left side
H	L	2	Upper-right side
H	H	3	Lower-right side

L: Low level
H: High level

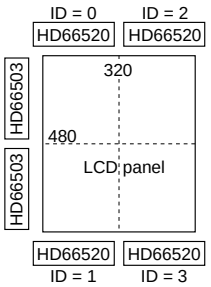


Figure 8 LS0 and LS1 Pin Setting and Internal Memory Map

How to Use the SHL Pin

It is possible to invert the relationship between the addresses and output pins Y1 to Y160 by setting the SHL pin (Figure 9). The upper left section on the screen can be assigned to address H'0000 regardless of which side of the LCD panel the HD66520 is connected to.

The Relationship between the Data Bus and Output Pins

The 8-bit data on the data bus has a 2-bit/pixel configuration for a 4-level grayscale display. In addition, the 8-bit data on the data bus has a relationship as shown in table regardless of the relationship between pins LS0, LS1, and SHL.

Table 1 Data Bus and Output Pins

Data Bus	Output Pins				
DB 0, 1	Y1	Y5	· · · · · · · · ·	Y153	Y157
DB 2, 3	Y2	Y6	· · · · · · · · ·	Y154	Y158
DB 4, 5	Y3	Y7	· · · · · · · · ·	Y155	Y159
DB 6, 7	Y4	Y8	· · · · · · · · ·	Y156	Y160

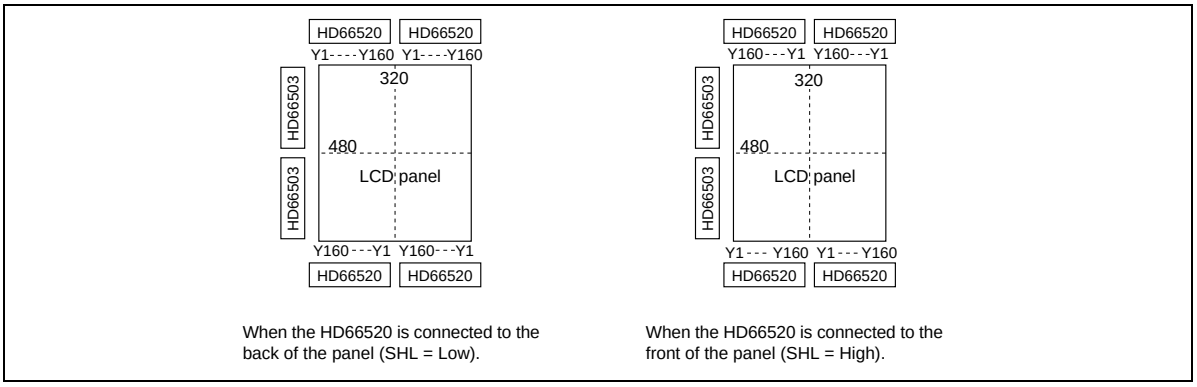


Figure 9 Address Assignment and SHL Pin Setting

Since the relationship between data bus pins DB0 to DB7 and the output pins are fixed, connect the data from the CPU to data bus pins DB0 to DB7 according to the driver arrangement on the panel as shown in Figure 10.

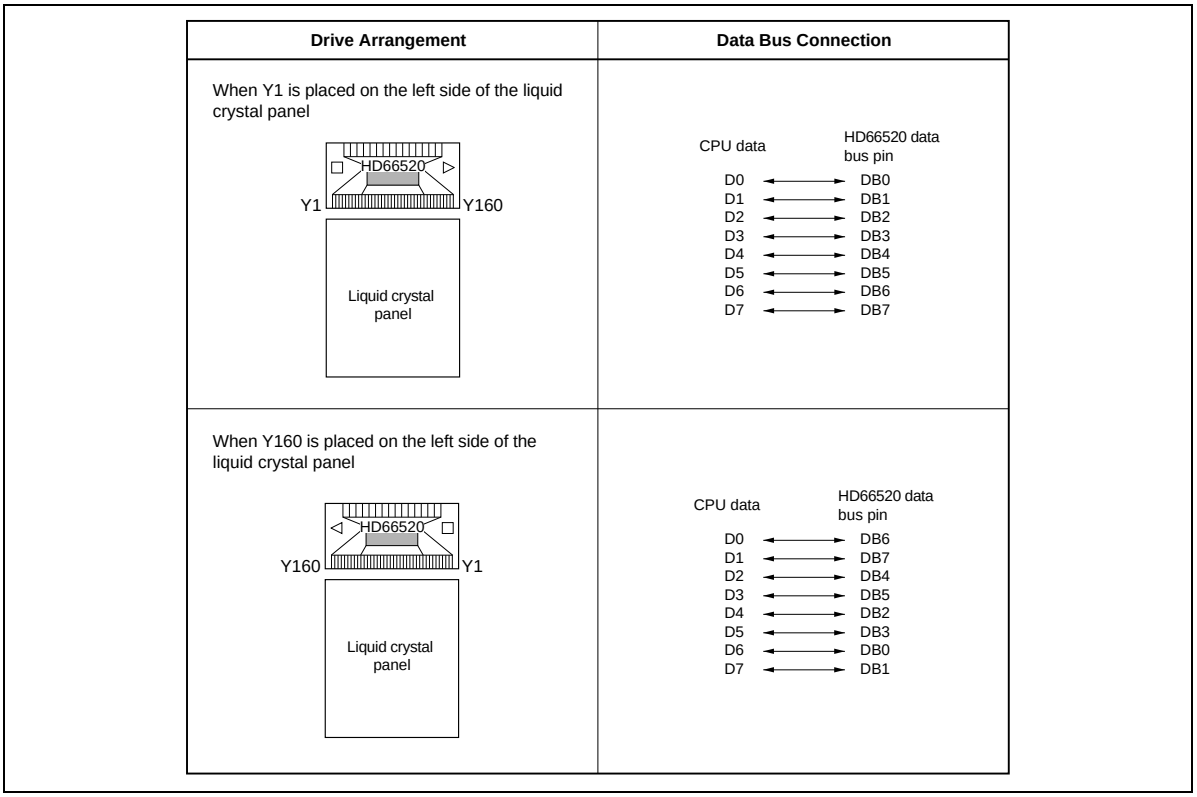


Figure 10 Relationship between Data Bus Pins DB0 to DB7 and Output Pins

Application Example

The HD66520 is suitable for a 160-dot-wide by 240-dot-long display (small information devices); a 320-dot-wide by 240-dot-long display (quarter VGA size); and a 320-dot-wide by 480-dot-long display (half VGA size). All of these are standard sizes for portable information devices. The following shows the system configuration.

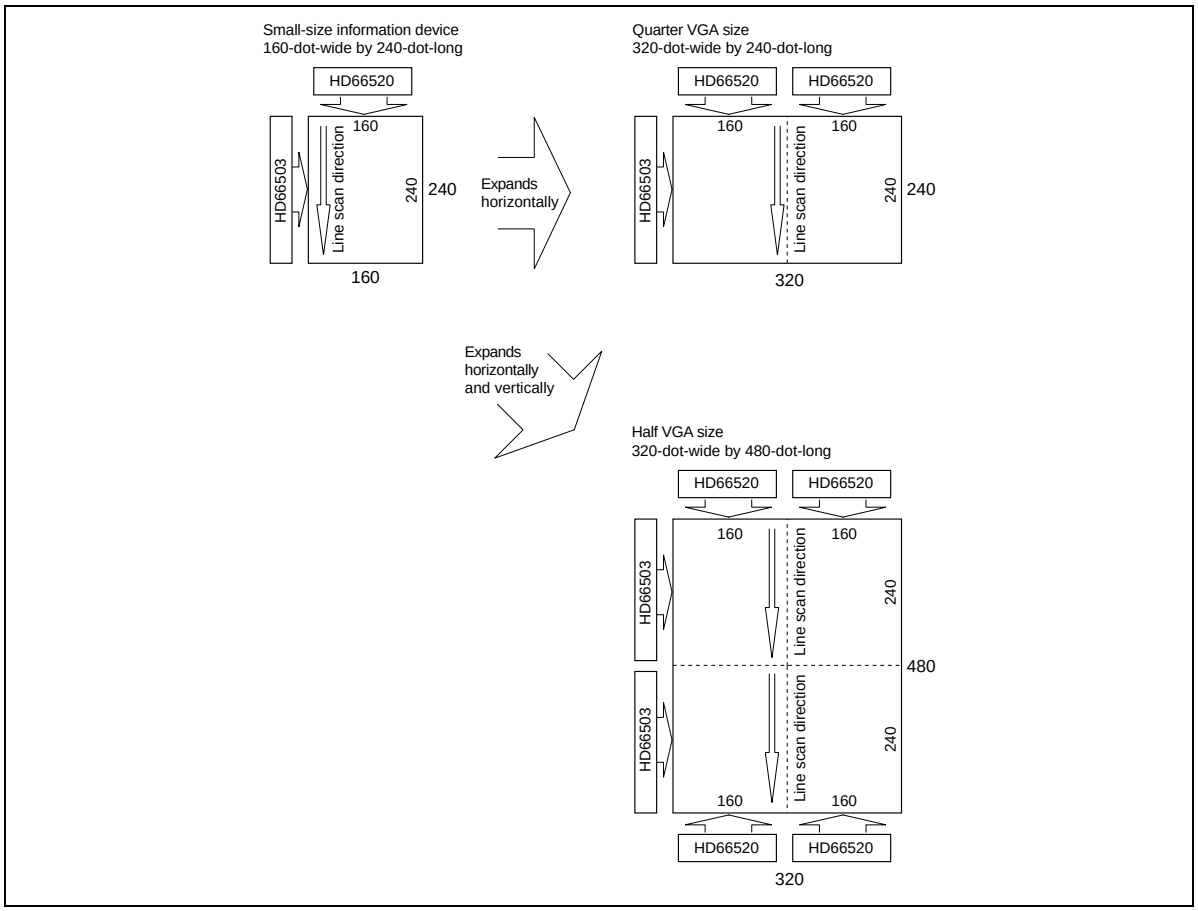


Figure 11 Application Examples

Small Information Device (SHL = Low)

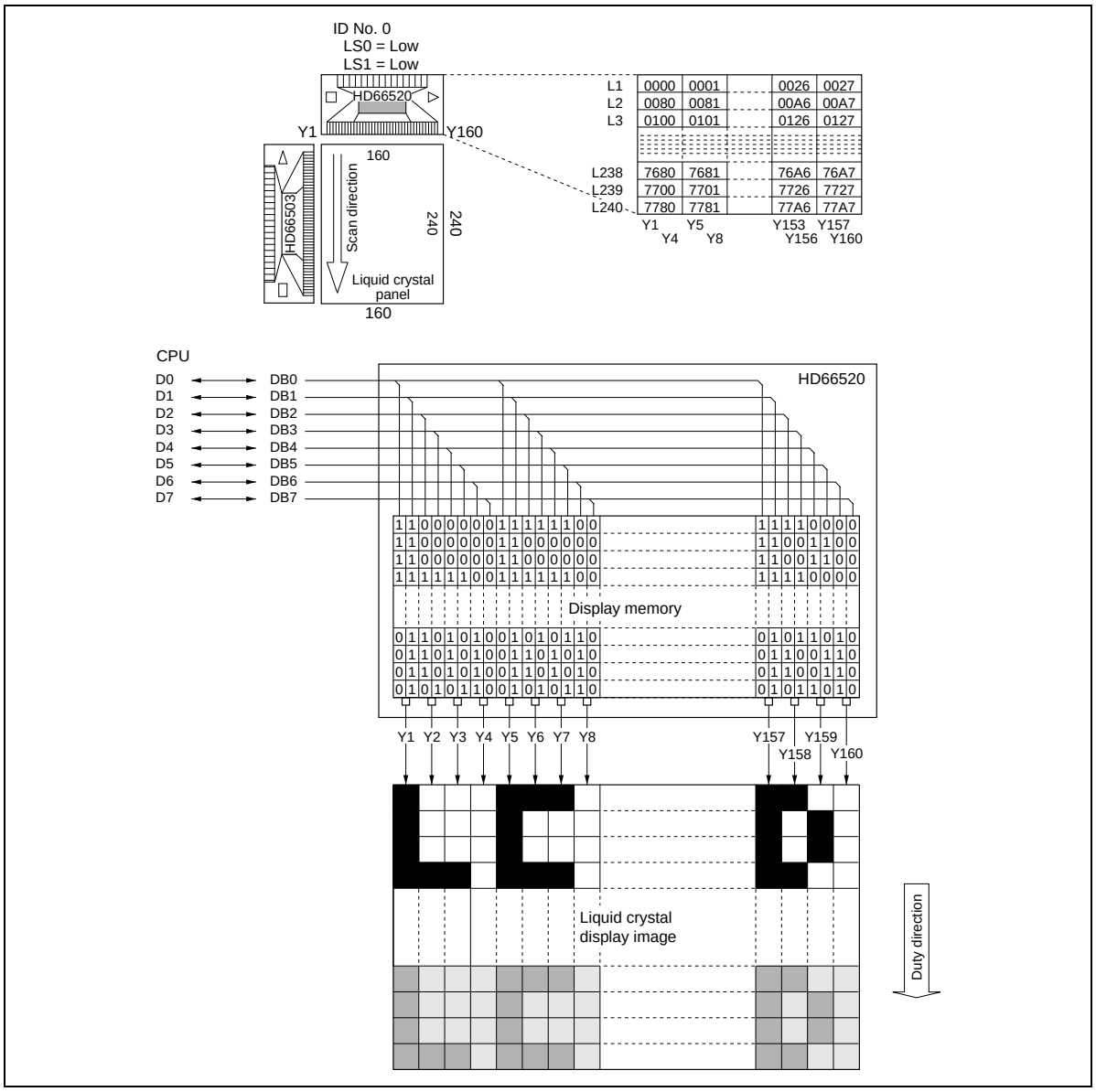


Figure 12 Small Information Device (1)

Small Information Device (SHL = High)

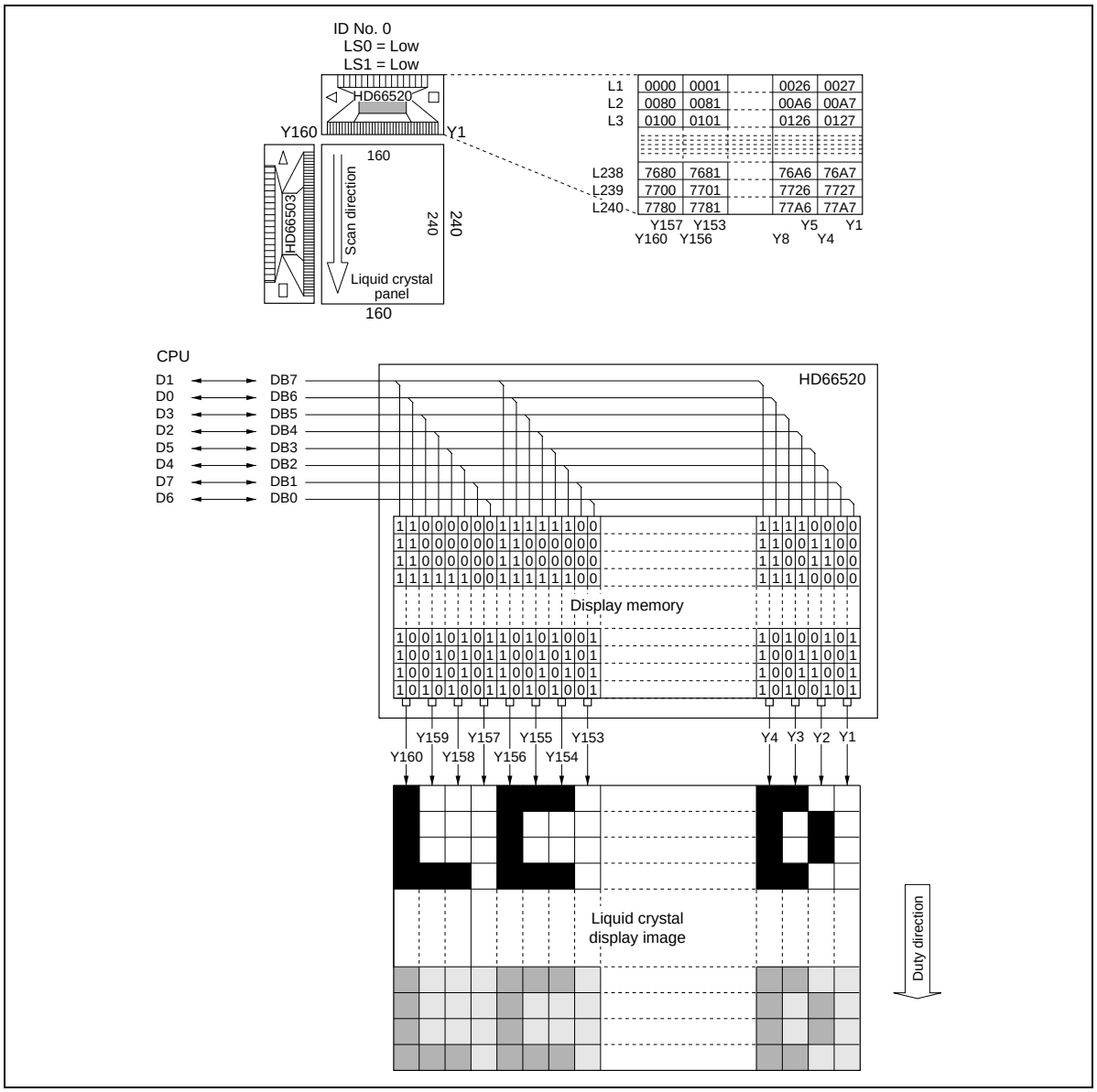


Figure 13 Small Information Device (2)

Quarter VGA Size (SHL = Low)

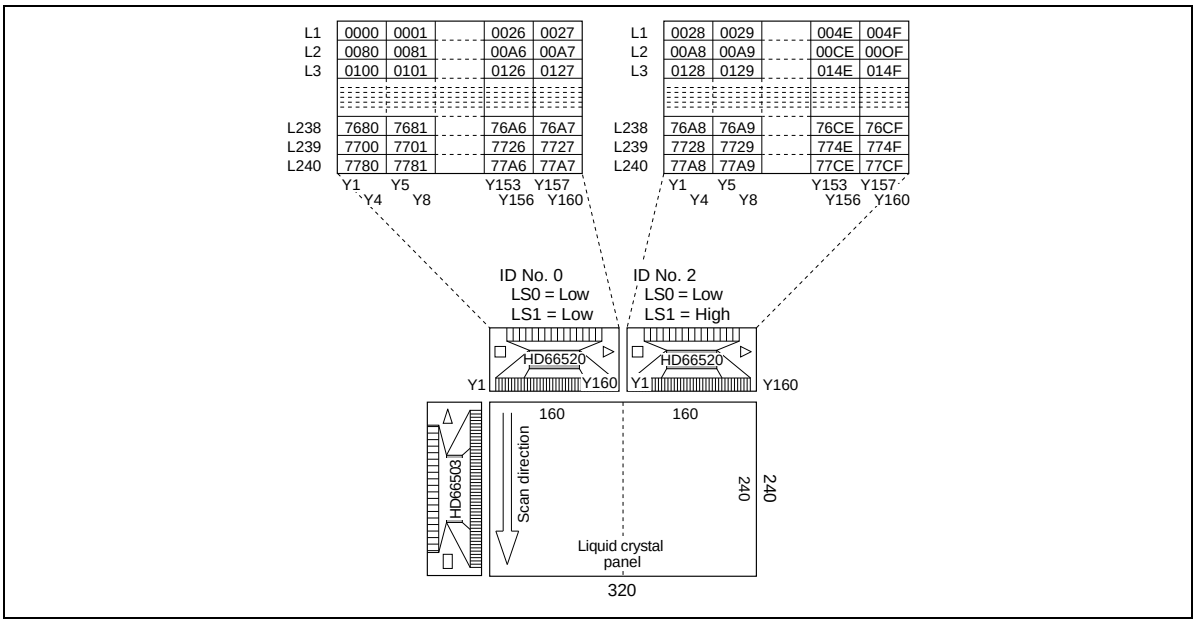


Figure 14 Quarter VGA Size (1)

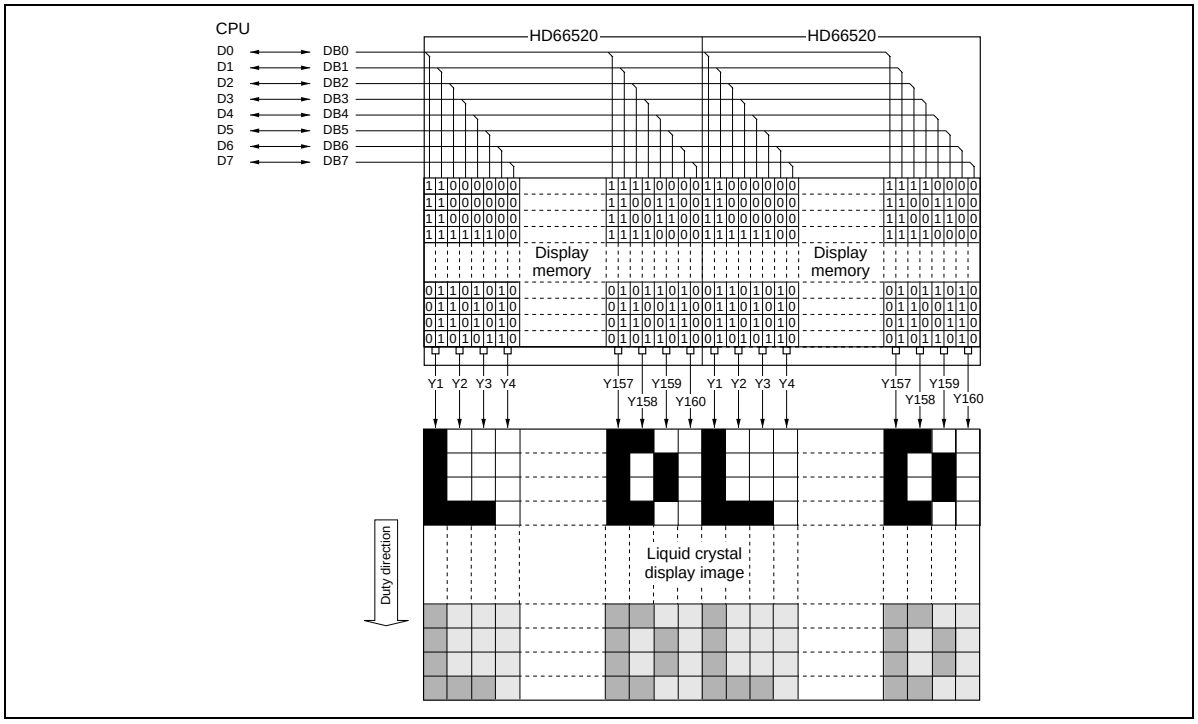


Figure 15 Quarter VGA Size (2)

Quarter VGA Size (SHL = High)

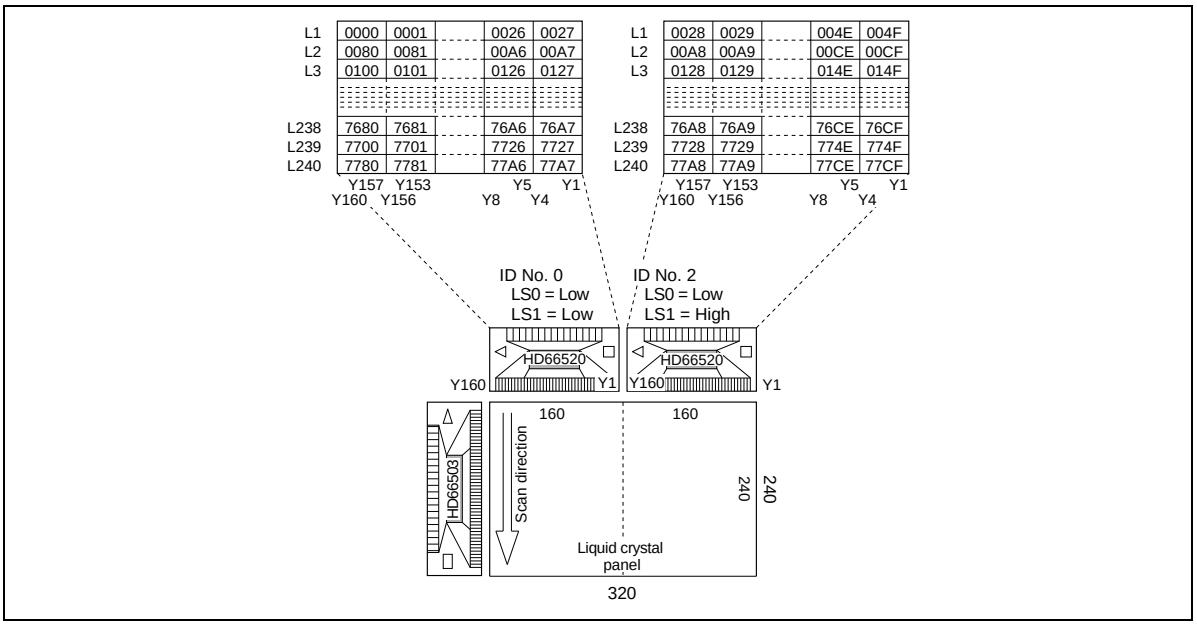


Figure 16 Quarter VGA Size (3)

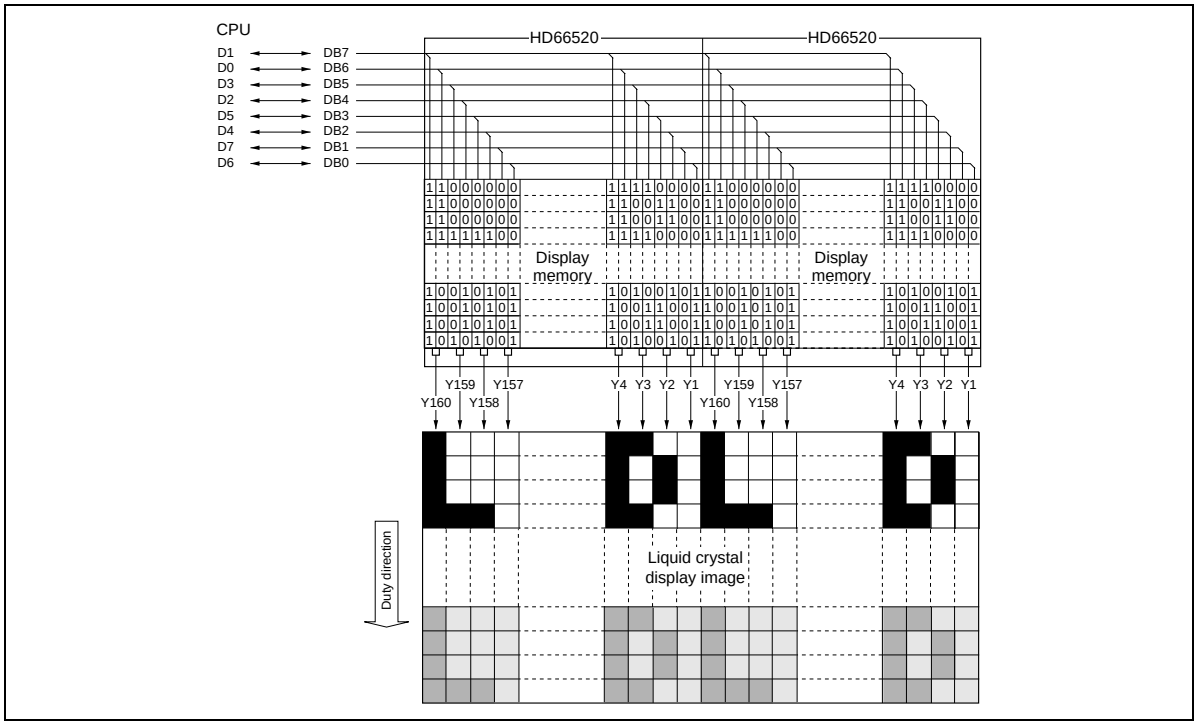


Figure 17 Quarter VGA Size (4)

Half VGA Size (SHL = Low)

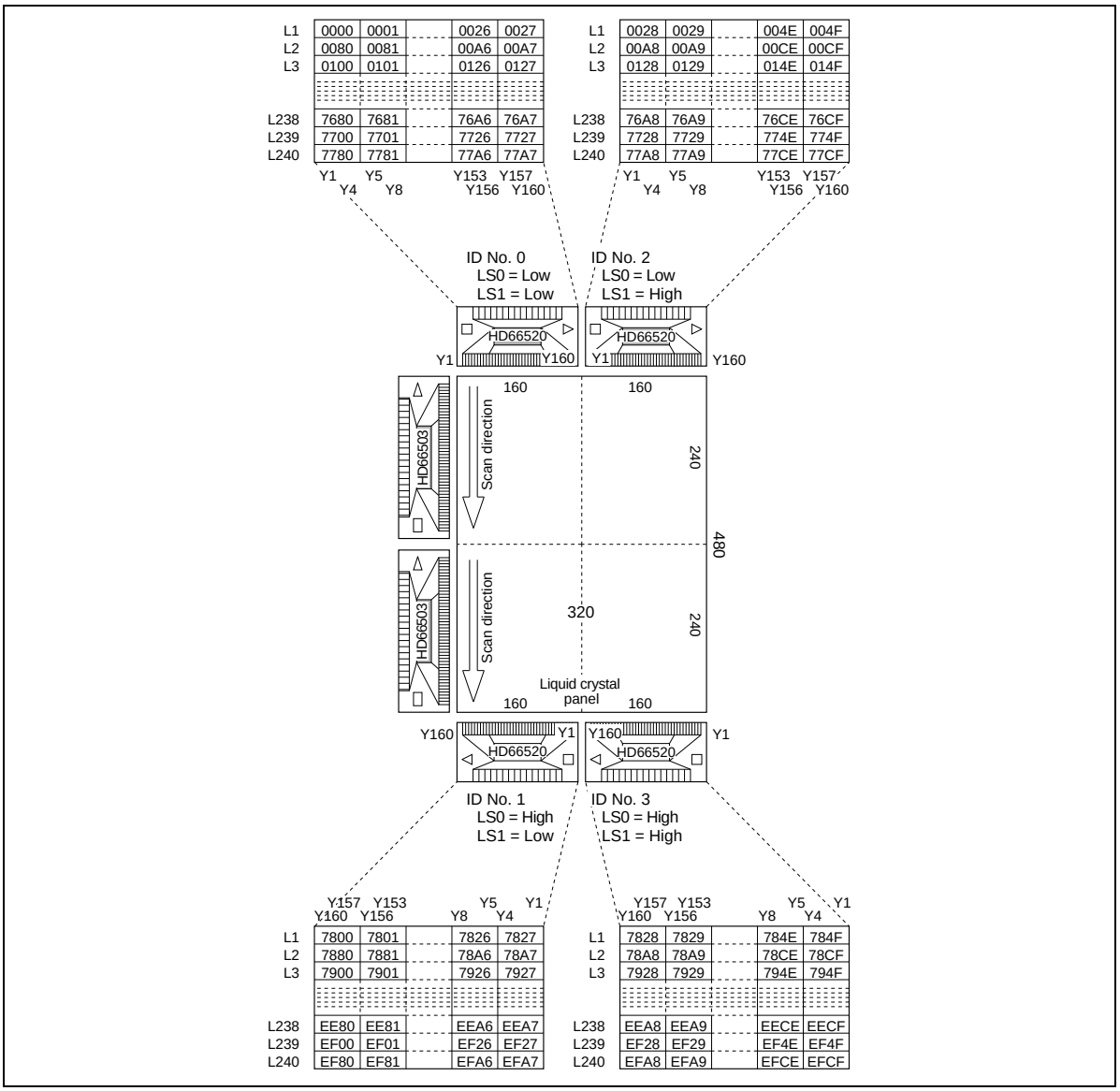


Figure 18 Half VGA Size (1)

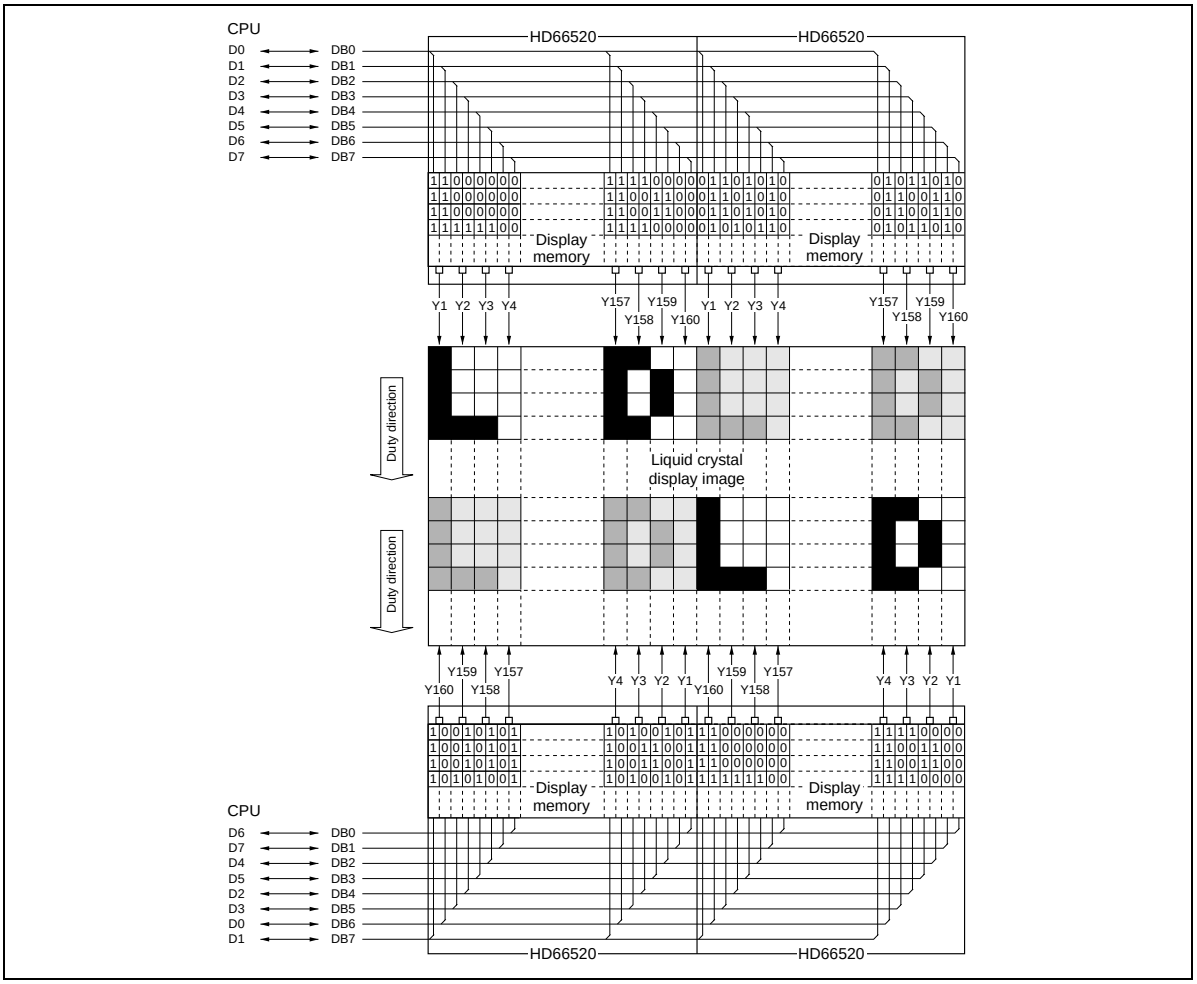


Figure 19 Half VGA Size (2)

Half VGA Size (SHL = High)

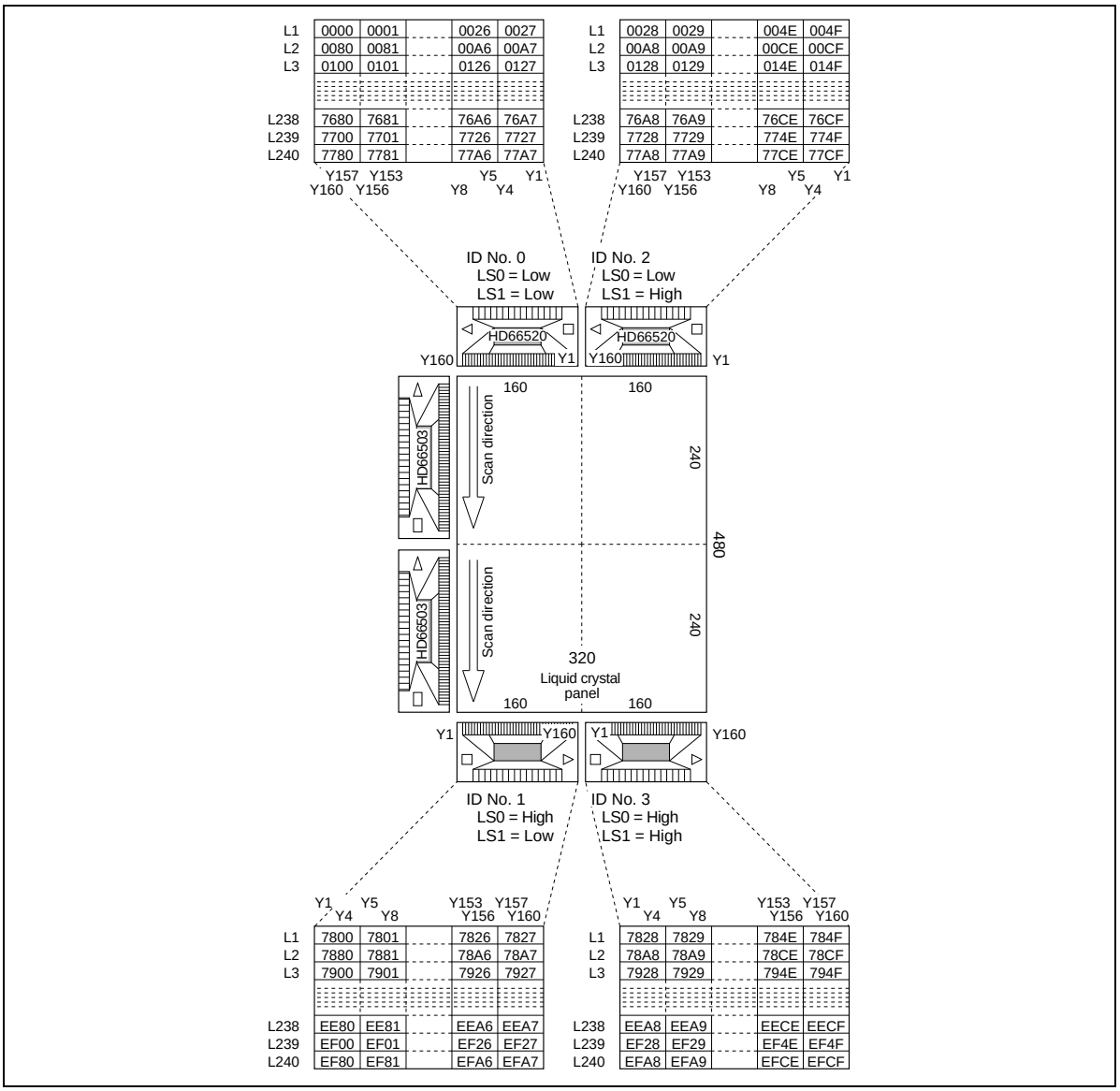


Figure 20 Half VGA Size (3)

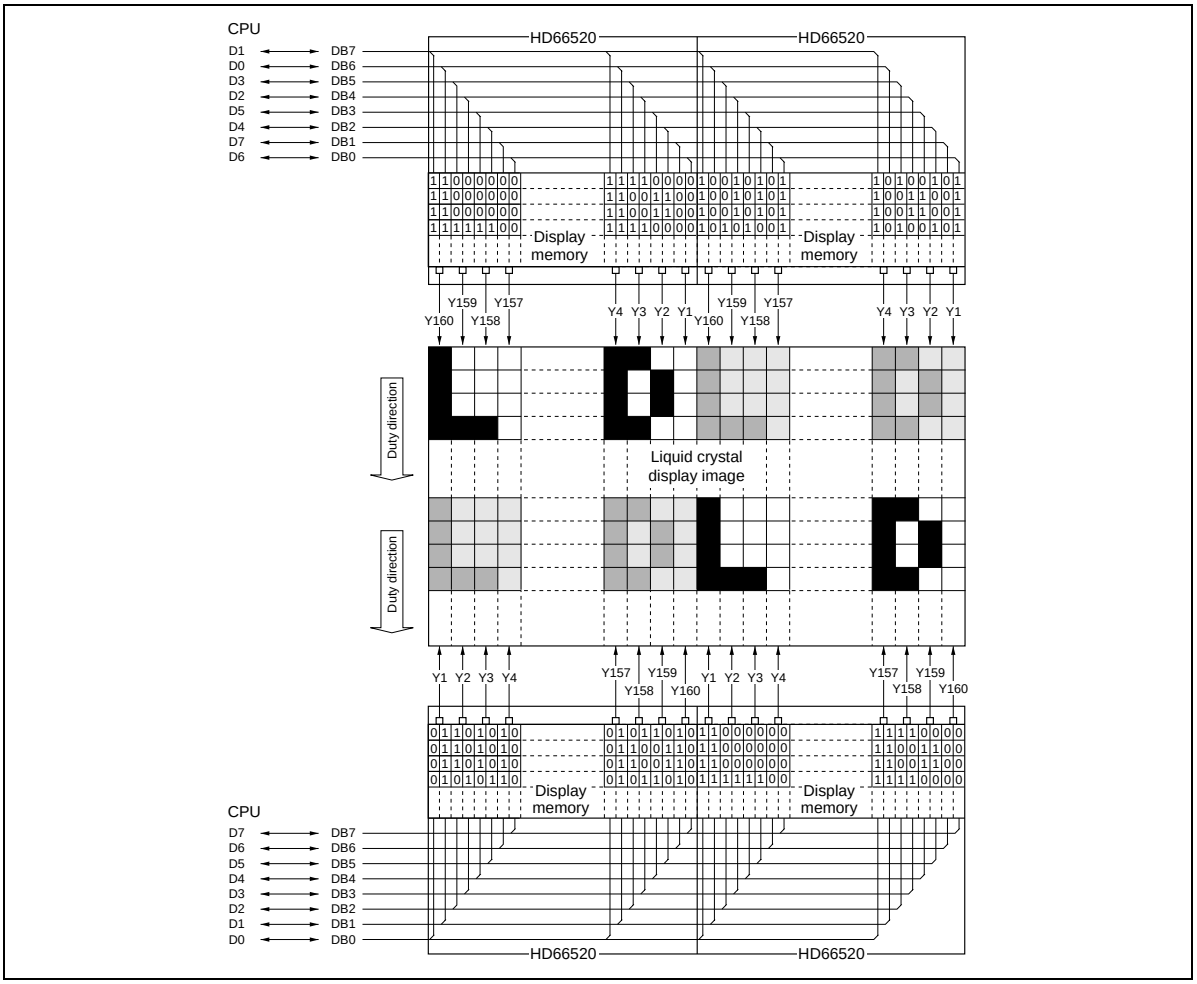


Figure 21 Half VGA Size (4)

Display-Data Transfer

Display RAM data is transferred to 160-bit data latch circuits 1 and 2 at each falling edge of the CL1 clock pulse. Since display data transfer and RAM access to draw data are completely synchronous-separated in the LSI, there will be no draw data loss or display flickering due to display data transfer timing.

The first line data transfer involves the first line marker (FLM), which initializes a line counter, and transfers the first line data to data latch circuits 1 and 2. Subsequent line data transfers involve transferring the second and the subsequent line data to data latch circuits 1 and 2 while incrementing the line counter value.

First Line Data Transfer

The line counter is initialized synchronously with an FLM signal. The first line is transferred to data latch circuits 1 and 2 at the falling edge of the CL1 (Figure 22).

Subsequent Line Data Transfer

The second and the subsequent line data are transferred to data latch circuits 1 and 2 at the falling edge of the CL1 to update the line counter value (Figure 23).

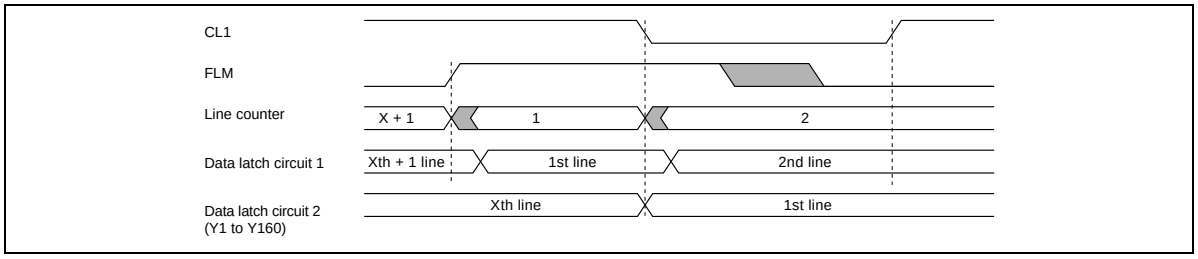


Figure 22 First Line Data Transfer

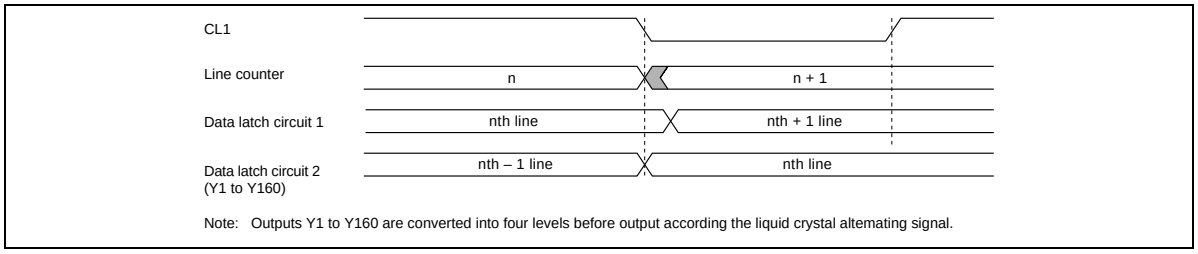


Figure 23 Subsequent Line Data Transfer

Draw Access

Random Cycle

Random cycle sequence is the same as that for the general-purpose SRAM interface (Figures 24 and 25). It can easily be connected to a CPU address bus and data bus.

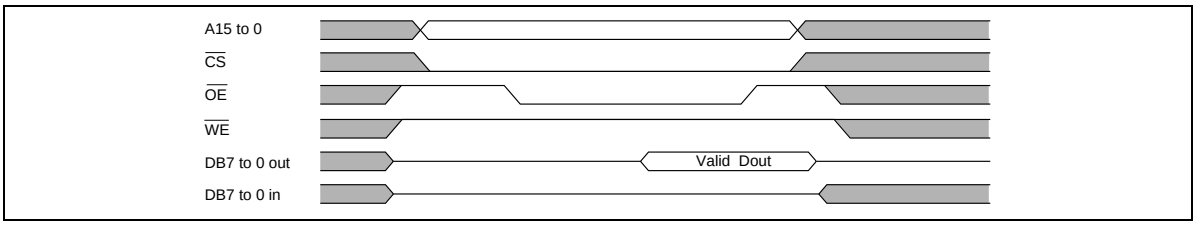


Figure 24 Read Cycle

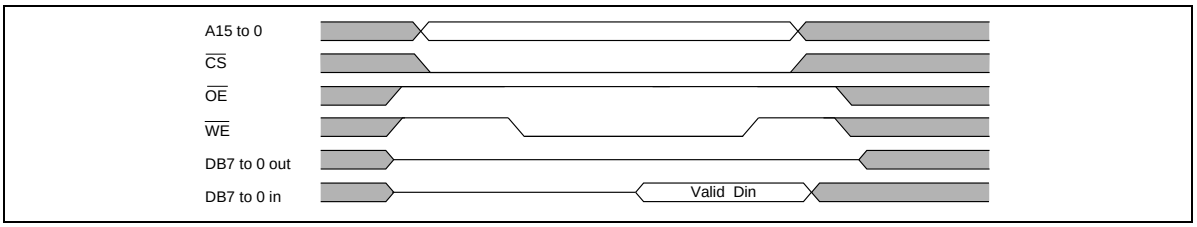


Figure 25 Write Cycle

Burst Cycle

Continuous access (burst cycle) can be performed by enabling addresses and $\overline{OE}$ or $\overline{WE}$ when $\overline{CS}$ is low (Figures 26 and 27). Refer to restraints for the period of continuous transfer.

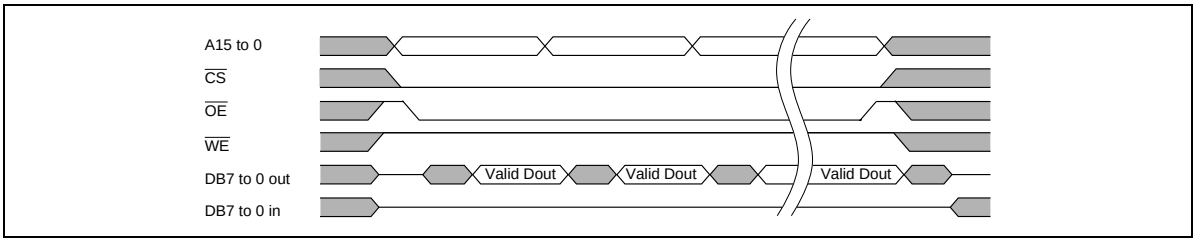


Figure 26 Burst Read Cycle

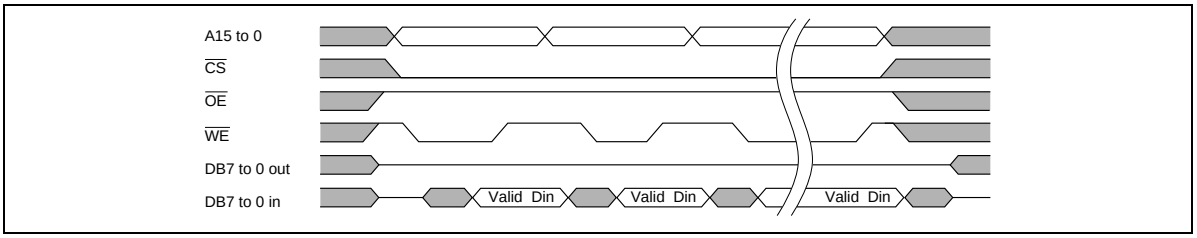


Figure 27 Burst Write Cycle

Arbitration Control

The HD66520 controls the arbitration between draw access and display access. The draw access reads and writes display data of the display memory incorporated in the HD66520. The display access outputs display memory line data to the liquid crystal panel. In this case, draw access is performed before display access, so continuous access is enabled without having the system to wait. For arbitration control, draw access is recognized as valid when signal $\overline{CS}$ is low.

The following describes the typical examples of display memory access state during arbitration control.

Sequence Line Data Transfer Display Access Performed by Subsequent Line Data Transfer

If no draw access is attempted, normal display access is performed when signal CL1 is low (Figure 28).

Draw Access 1

If draw access is attempted when signal CL1 is high, draw access is performed regardless of the display access (Figure 29).

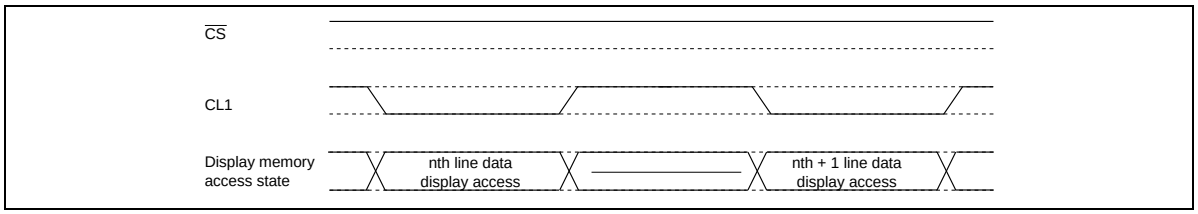


Figure 28 Sequence Line Data Transfer

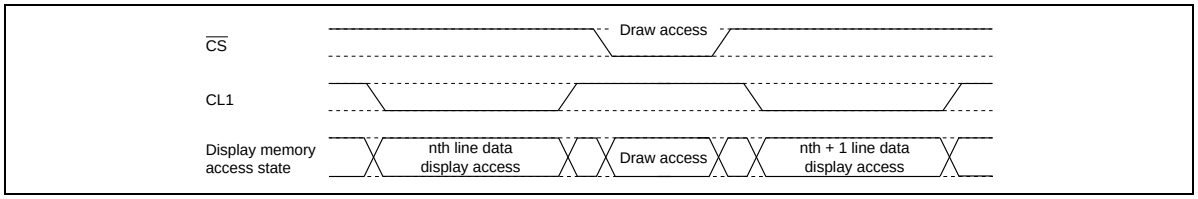


Figure 29 Draw Access (1)

Draw Access 2

If draw access is attempted when signal CL1 is low, the display access is suspended to perform draw access (Figure 30). After the draw access, the display access is performed again. As a result, even if draw access is attempted asynchronously, at least one of the display accesses will be performed.

Display Access by First Line Data Transfer

If no draw access is attempted, display access for the first line is performed when signal FLM is high and CL1 is low. The display access for the second line is performed when signal CL1 is low (Figure 31).

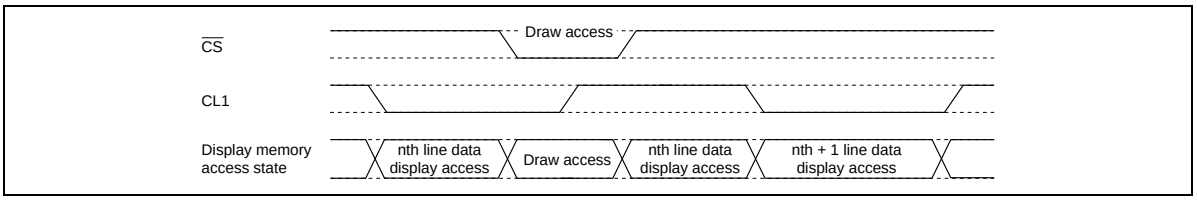


Figure 30 Draw Access (2)

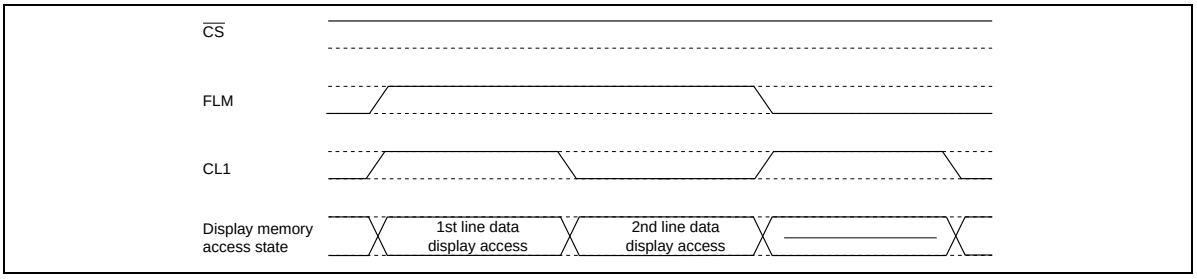


Figure 31 First Line Data Transfer

Draw Access 3

If draw access is attempted when signal FLM is high, stop the display access is suspended to perform the draw access (Figure 32). After the draw access, the display access is performed again. As a result, even if draw access is attempted asynchronously, at least one of the two display accesses will be performed.

Note: In order to satisfy draw access 3 and transfer the first line data, there are restraints for the period when pins FLM and CL1 are both high and for the low level pulse width of pin $\overline{CS}$. Refer to Restraints for details on the restraints for the pulse width.

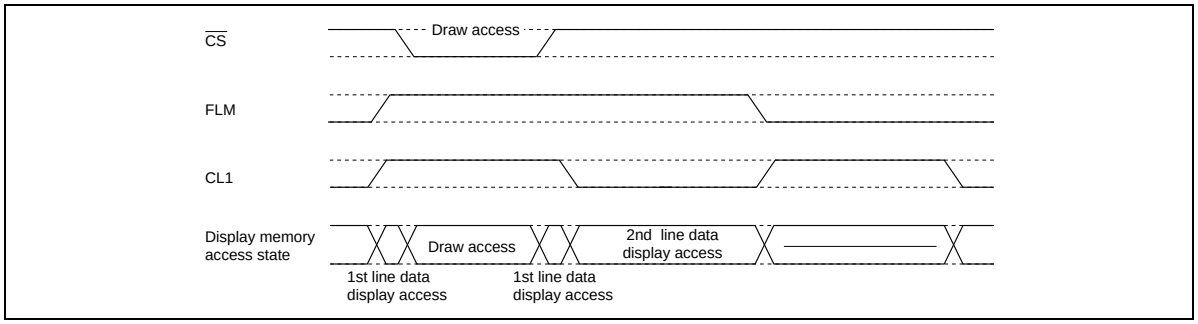


Figure 32 Draw Access (3)

Example of System Configuration

Figure 33 shows a system configuration for a 320-dot-wide by 240-dot-long LCD panel using HD66520s and common driver HD66503 with internal liquid crystal display timing control circuits. All required functions can be prepared for liquid crystal display with just three chips except for liquid crystal display power supply circuit functions.

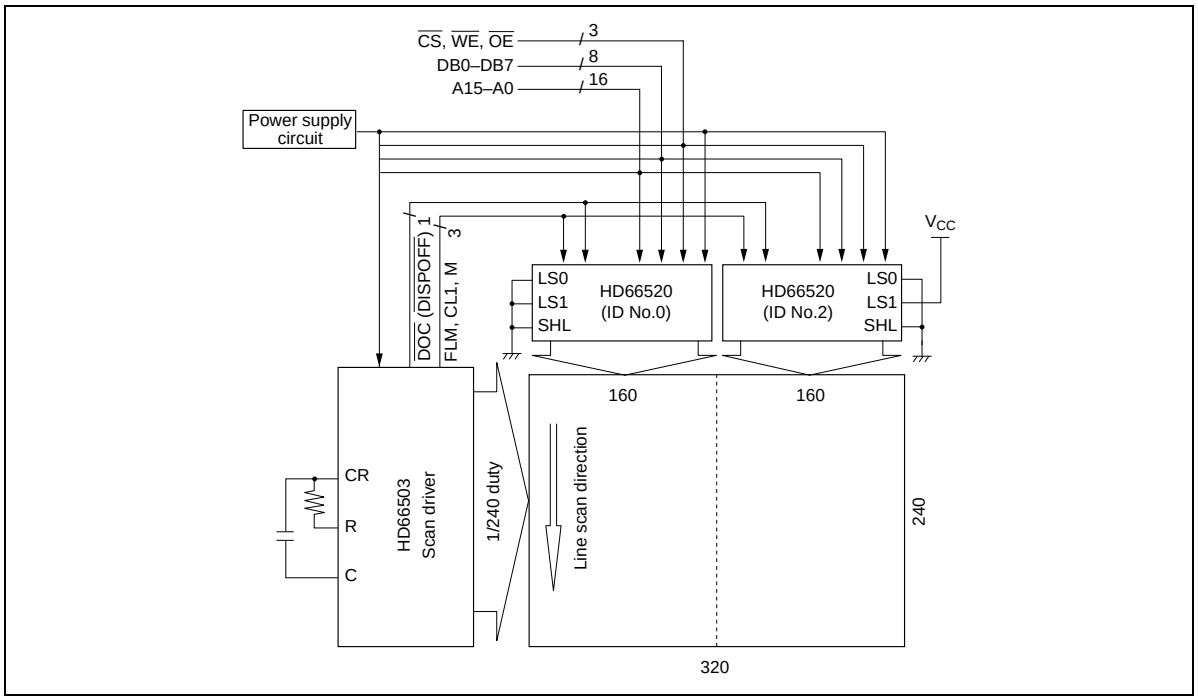


Figure 33 System Configuration

Restraints

The HD66520 can perform continuous draw access (burst access) when signal $\overline{CS}$ is low. As a result, display data can be rewritten at high speed.

However, since signal $\overline{CS}$ is necessary to perform arbitration control between draw access and display access to the display memory, the following restraints exist for the pulse width of signal $\overline{CS}$.

V_{CC} = 3.0 to 4.5V

- Read operation

Item	Symbol	Min	Max	Unit
Chip select high level width	t_{CHR}	180	—	ns
Chip select low level width	t_{CLR}	240	t_{FS} – 1000	ns

- Write operation

Item	Symbol	Min	Max	Unit
Chip select high level width	t_{CHW}	180	—	ns
Chip select low level width	t_{CLW}	180	t_{FS} – 1000	ns

V_{CC} = 4.5 to 5.5V

- Read operation

Item	Symbol	Min	Max	Unit
Chip select high level width	t_{CHR}	120	—	ns
Chip select low level width	t_{CLR}	180	t_{FS} – 1000	ns

- Write operation

Item	Symbol	Min	Max	Unit
Chip select high level width	t_{CHW}	120	—	ns
Chip select low level width	t_{CLW}	120	t_{FS} – 1000	ns

Chip Select High Level Width

Display access is performed when signal $\overline{CS}$ is high during normal draw access. Therefore, only the minimum display access time is necessary for the chip select high level width (Figure 34).

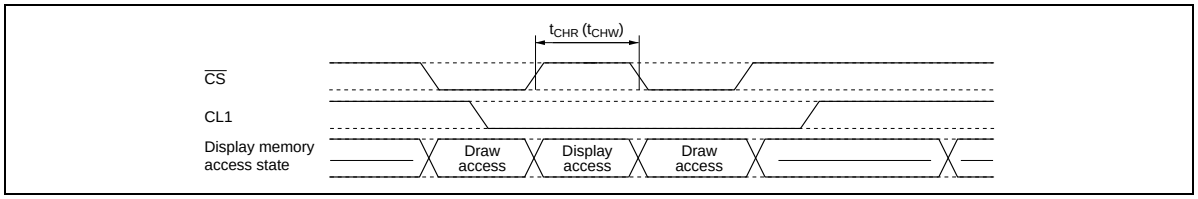


Figure 34 Chip Select High Level Width

Chip Select Low Level Width

When continuous draw access (burst access) is performed when signal $\overline{CS}$ is low, the maximum display access time, that is, t_{FS}–1000 (ns) is necessary for the chip select low level width (Figure 35). This is needed to secure the display access period for the first line.

When common driver HD66503 is used together with the HD66520, t_{FS} can be calculated with the following formula.

$$t_{FS} = \frac{1}{4 \cdot n_{DUTY} \cdot f_{FLM}}$$

f_{FLM}: frame frequency
n_{DUTY}: duty

When write operation is performed with the burst access having a frame frequency of 70 Hz and a duty cycle of 1/240, display data of 77 bytes can be consequtively written in one burst access (write cycle is 180 ns).

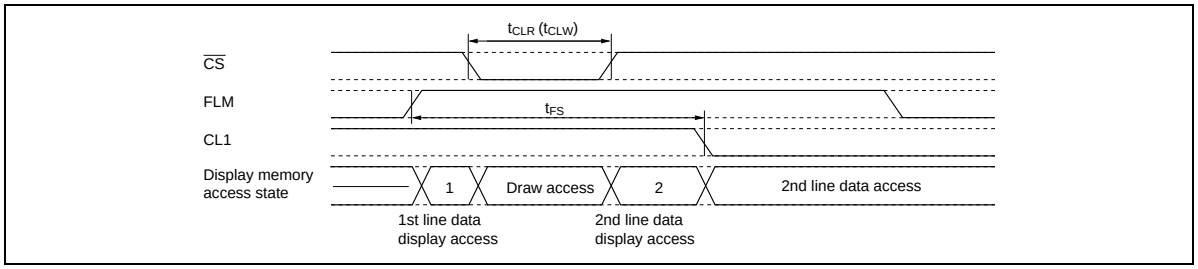


Figure 35 Chip Select Low Level Width

Absolute Maximum Ratings

Item		Symbol	Ratings	Unit	Notes
Power voltage	Logic circuit	V_{CC}	–0.3 to +7.0	V	1
	LCD drive circuit	V_{EE}	V_{CC} – 30.0 to V_{CC} + 0.3	V	
Input voltage (1)		VT1	–0.3 to V_{CC} + 0.3	V	1, 2
Input voltage (2)		VT2	V_{EE} – 0.3 to V_{CC} + 0.3	V	1, 3
Operating temperature		T_{opr}	–20 to +75	°C	
Storage temperature		T_{stg}	–40 to +125	°C	

Notes: 1. The reference point is GND (0V).
2. Applies to pins LS0, LS1, SHL, FLM, CL1, M, A0 to A15, DB0 to DB7, $\overline{\text{DISPOFF}}$, $\overline{\text{CS}}$, $\overline{\text{WE}}$, and $\overline{\text{OE}}$.
3. Applies to pins V1L, V1R, V2L, V2R, V3L, V3R, V4L, V4R.
4. If the LSI is used beyond its absolute maximum rating, it may be permanently damaged. It should always be used within the limits of its electrical characteristics in order to prevent malfunction or unreliability.

Electrical Characteristics

DC Characteristics 1 (V_{CC} = 3.0 to 5.5V, GND = 0V, V_{CC}–V_{EE} = 8 to 28V, Ta = –20 to +75°C)

Item	Symbol	Applicable Pins	Min	Typ	Max	Unit	Measurement Condition	Notes
Input leakage current (1)	I_{IL1}	Except for DB0 to DB7	–2.5	—	2.5	µA	VIN = V_{CC} to GND	
Input leakage current (2)	I_{IL2}	V1L/R, V2L/R, V3L/R, V4L/R	–25	—	25	µA	VIN = V_{CC} to V_{EE}	
Tri-state leakage current	I_{IST}	DB0 to DB7	–10	—	10	µA	VIN = V_{CC} to GND	
Vi-Yj on resistance	R_{ON}	Y1 to Y160	—	1.0	2.0	kΩ	I_{ON} = 100 µA	1

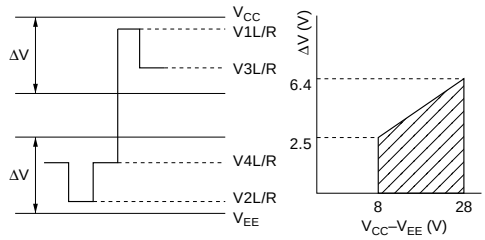
Note: 1. Indicates the resistance between one pin from Y1 to Y160 and another pin from V1L/V1R, V2L/V2R, V3L/V3R, V4L/V4R when load current is applied to the Y pin; defined under the following conditions:

V_{CC}–V_{EE} = 28V

V1L/V1R, V3L/V3R = V_{CC} – 2/10 (V_{CC}–V_{EE})

V4L/V4R, V2L/V2R = V_{EE} + 2/10 (V_{CC}–V_{EE})

V1L/V1R and V3L/V3R should be near the V_{CC} level, and V2L/V2R and V4L/V4R should be near the V_{EE} level. All voltage must be within ÆV. ÆV is the range within which R_{ON}, the LCD drive circuits' output impedance, is stable. Note that ÆV depends on power supply voltage V_{CC}–V_{EE}.



Relationship between Driver Output Waveform and Output Voltage

DC Characteristics 2 (V_{CC} = 3.0 to 4.5V, GND = 0V, V_{CC}–V_{EE} = 8 to 28V, Ta = –20 to +75°C)

Item	Symbol	Applicable Pins	Min	Typ	Max	Unit	Measurement Condition	Notes
Input high level voltage (1)	VIH1	LS0–1, SHL, FLM, CL1, M, $\overline{DISPOFF}$	$0.8 \times V_{CC}$	—	V_{CC}	V		
Input low level voltage (1)	VIL1		0	—	$0.2 \times V_{CC}$	V		
Input high level voltage (2)	VIH2	DB0 to DB7, CS, A0 to A15, $\overline{WE}$, $\overline{OE}$	$0.7 \times V_{CC}$	—	V_{CC}	V		
Input low level voltage (2)	VIL2		0	—	$0.15 \times V_{CC}$	V		
Output high level voltage	VOH	DB0 to DB7	$0.9 \times V_{CC}$	—	—	V	I_{OH} = –50 µA	
Output low level voltage	VOL		—	—	$0.1 \times V_{CC}$	V	I_{OL} = 50 µA	
Current consumption during RAM access	I_{CC}	Measurement pin V_{CC}	—	8	10	mA	Access time 600 ns V_{CC} = 3.3V	2
Current consumption in LCD drive part	I_{EE}	Measurement pin V_{EE}	—	200	300	µA	V_{CC}–V_{EE} = 28V V_{CC} = 3.3V t_{CYC} = 59.5 µs No access	2, 3
Current consumption during display operation	I_{DIS}	Measurement pin GND	—	40	60	µA		

Notes: 2. Input and output currents are excluded. When a CMOS input is floating, excess current flows from the power supply through to the input circuit. To avoid this, VIH and VIL must be held to V_{CC} and GND levels, respectively.

3. Indicates the current when the memory access is stopped and the still image of a zig-zag pattern is displayed in its place.

DC Characteristics 3 (V_{CC} = 4.5 to 5.5V, GND = 0V, V_{CC}–V_{EE} = 8 to 28V, Ta = –20 to +75°C)

Item	Symbol	Applicable Pins	Min	Typ	Max	Unit	Measurement Condition	Notes
Input high level voltage (1)	VIH1	LS0–1, SHL, FLM, CL1, M, $\overline{DISPOFF}$	0.8 × V_{CC}	—	V_{CC}	V		
Input low level voltage (1)	VIL1		0	—	0.2 × V_{CC}	V		
Input high level voltage (2)	VIH2	DB0 to DB7, $\overline{CS}$, A0 to A15, $\overline{WE}$, $\overline{OE}$	2.2	—	V_{CC}	V		
Input low level voltage (2)	VIL2		0	—	0.8	V		
Output high level voltage	VOH	DB0 to DB7	2.4	—	—	V	I_{OH} = –100 µA	
Output low level voltage	VOL		—	—	0.4	V	I_{OL} = 100 µA	
Current consumption during RAM access	I_{CC}	Measurement pin V_{CC}	—	13	16	mA	Access time 600 ns V_{CC} = 5.5V	2
Current consumption in LCD drive part	I_{EE}	Measurement pin V_{EE}	—	200	300	µA	V_{CC}–V_{EE} = 28V, V_{CC} = 5.5V, t_{CYC} = 59.5 µs, no access	2, 3
Current consumption during display operation	I_{DIS}	GND	—	60	100	µA		

Notes: 2. Input and output currents are excluded. When a CMOS input is floating, excess current flows from the power supply through to the input circuit. To avoid this, VIH and VIL must be held to V_{CC} and GND levels, respectively.

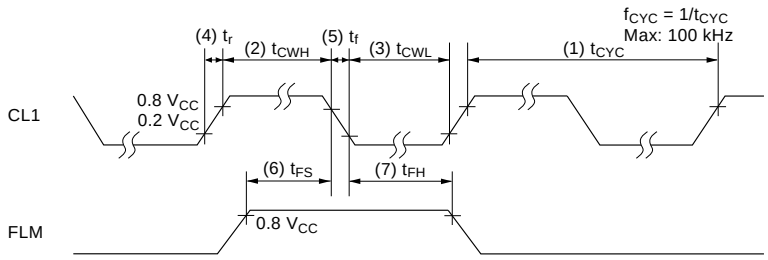
3. Indicates the current when the memory access is stopped and the still image of a zig-zag pattern is displayed in its place.

AC Characteristics 1 (V_{CC} = 3.0 to 5.5V, GND = 0V, V_{CC}–V_{EE} = 8 to 28V, Ta = –20 to +75°C)

- Display-Data Transfer Timing

No.	Item	Symbol	Applicable Pins	Min	Max	Unit	Notes
(1)	Clock cycle time	t_{CYC}	CL1	10	—	µs	1
(2)	CL1 high-level width	t_{CWH}	CL1	1.0	—	µs	
(3)	CL1 low-level width	t_{CWL}	CL1	1.0	—	µs	
(4)	CL1 rise time	t_r	CL1	—	50	ns	
(5)	CL1 fall time	t_f	CL1	—	50	ns	
(6)	FLM setup time	t_{FS}	FLM, CL1	2.0	—	µs	
(7)	FLM hold time	t_{FH}	FLM, CL1	1.0	—	µs	

Notes: 1.



When executing draw access with burst transfer, the period described in the restrains must be satisfied in the relationship with the arbitration control.

AC Characteristics 2 (V_{CC} = 3.0 to 4.5V, GND = 0V, V_{CC}–V_{EE} = 8 to 28V, Ta = –20 to +75°C)

- **Draw Access Timing**

— Read Cycle

Measurement conditions:

Input level: VIH = 2.4V, VIL = 0.8V

Output level: VOH/VOL = 1.5V

Output load: 1 TTL gate + 100 pF capacitor

No.	Item	Symbol	Min	Max	Unit	Note
(8)	Read cycle time	t_{RC}	240	—	ns	
(9)	Address access time	t_{AA}	—	240	ns	
(10)	Chip select access time	t_{CA}	—	240	ns	
(11)	$\overline{CS}$ high level width	t_{CHR}	180	—	ns	
(12)	$\overline{CS}$ low level width	t_{CLR}	240	t_{FS}–1000	ns	
(13)	$\overline{OE}$ delay time	t_{OE}	—	150	ns	
(14)	$\overline{OE}$ delay time (low impedance)	t_{OLZ}	5	—	ns	
(15)	Output-disable delay time	t_{OHZ}	0	35	ns	
(16)	Output hold time	t_{OH}	5	—	ns	

— Write Cycle

Measurement conditions:

Input level: VIH = 2.4V, VIL = 0.8V

No.	Item	Symbol	Min	Max	Unit	Note
(17)	Write cycle time	t_{WC}	180	—	ns	
(18)	Address-to-$\overline{WE}$ setup time	t_{ASW}	30	—	ns	
(19)	$\overline{CS}$ high level width	t_{CHW}	180	—	ns	
(20)	$\overline{CS}$ low level width	t_{CLW}	180	t_{FS}–1000	ns	
(21)	Address-to-$\overline{WE}$ hold time	t_{AHW}	0	—	ns	
(22)	$\overline{CS}$-to-$\overline{WE}$ hold time	t_{CH}	0	—	ns	
(23)	$\overline{WE}$ low level width	t_{WLW}	100	—	ns	
(24)	$\overline{WE}$ high level width	t_{WHW}	30	—	ns	
(25)	Data-to-$\overline{WE}$ setup time	t_{DS}	80	—	ns	
(26)	Data-to-$\overline{WE}$ hold time	t_{DH}	30	—	ns	

AC Characteristics 3 (V_{CC} = 4.5 to 5.5V, GND = 0V, V_{CC}–V_{EE} = 8 to 28V, Ta = –20 to +75°C)

- Access Timing
  - — Read Cycle

    Regulation terms:

    Input level: VIH = 2.4V, VIL = 0.8V

    Output judge-level: VOH/VOL = 1.5V

    Output load: 1 TTL gate + capa. 100 pF

No.	Item	Symbol	Min	Max	Unit	Note
(8)	Read cycle time	t_{RC}	180	—	ns	
(9)	Address access time	t_{AA}	—	180	ns	
(10)	Chip select access time	t_{CA}	—	180	ns	
(11)	$\overline{CS}$ high level width	t_{CHR}	120	—	ns	
(12)	$\overline{CS}$ low level width	t_{CLR}	180	t_{FS}–1000	ns	
(13)	$\overline{OE}$ delay time	t_{OE}	—	100	ns	
(14)	$\overline{OE}$ delay time (low impedance)	t_{OLZ}	5	—	ns	
(15)	Output-disable delay time	t_{OHZ}	0	35	ns	
(16)	Output hold time	t_{OH}	5	—	ns	

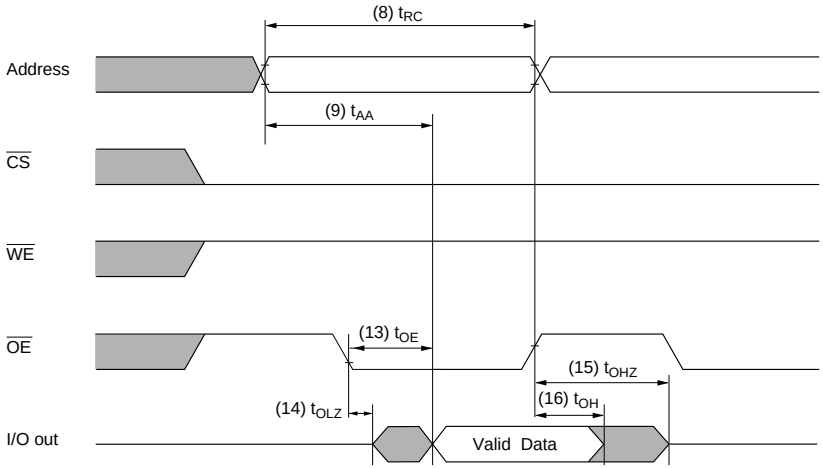
  - — Write Cycle

    Regulation terms:

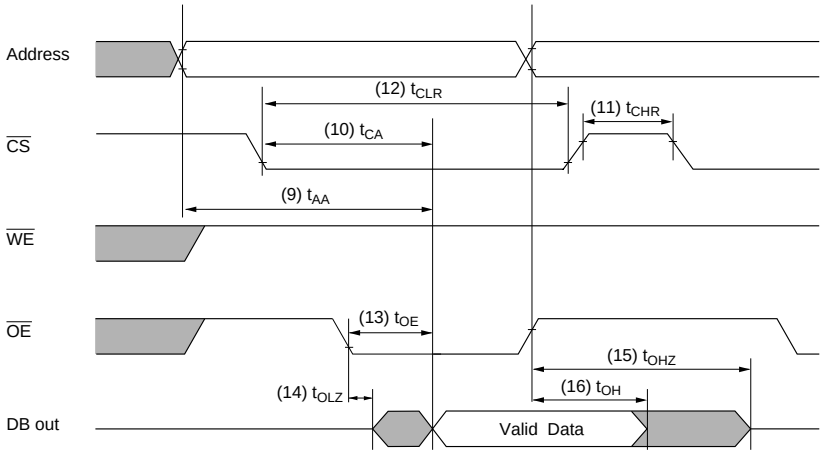
    Input level: VIH = 2.4V, VIL = 0.8V

No.	Item	Symbol	Min	Max	Unit	Note
(17)	Write cycle time	t_{WC}	120	—	ns	
(18)	Address-to-$\overline{WE}$ setup time	t_{ASW}	20	—	ns	
(19)	$\overline{CS}$ high level width	t_{CHW}	120	—	ns	
(20)	$\overline{CS}$ low level width	t_{CLW}	120	t_{FS}–1000	ns	
(21)	Address-to-$\overline{WE}$ hold time	t_{AHW}	0	—	ns	
(22)	$\overline{CS}$-to-$\overline{WE}$ hold time	t_{CH}	0	—	ns	
(23)	$\overline{WE}$ low level width	t_{WLW}	80	—	ns	
(24)	$\overline{WE}$ high level width	t_{WHW}	30	—	ns	
(25)	Data-to-$\overline{WE}$ setup time	t_{DS}	60	—	ns	
(26)	Data-to-$\overline{WE}$ hold time	t_{DH}	20	—	ns	

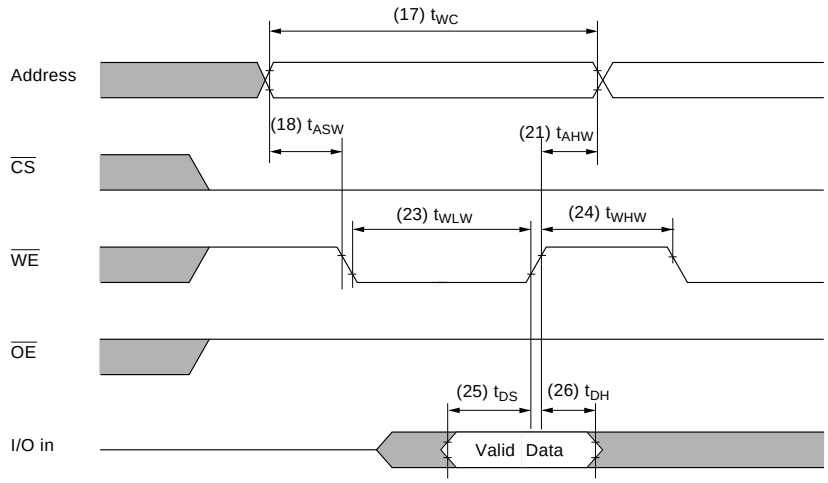
Read Cycle 1



Read Cycle 2



Write Cycle 1



Write Cycle 2