HD66137T

High-Voltage Durable 240-Channel Common Driver
for Dot-Matrix STN LCD

HITACHI

ADE-207-291(Z)
Rev. 2
Aug. 03, 1999

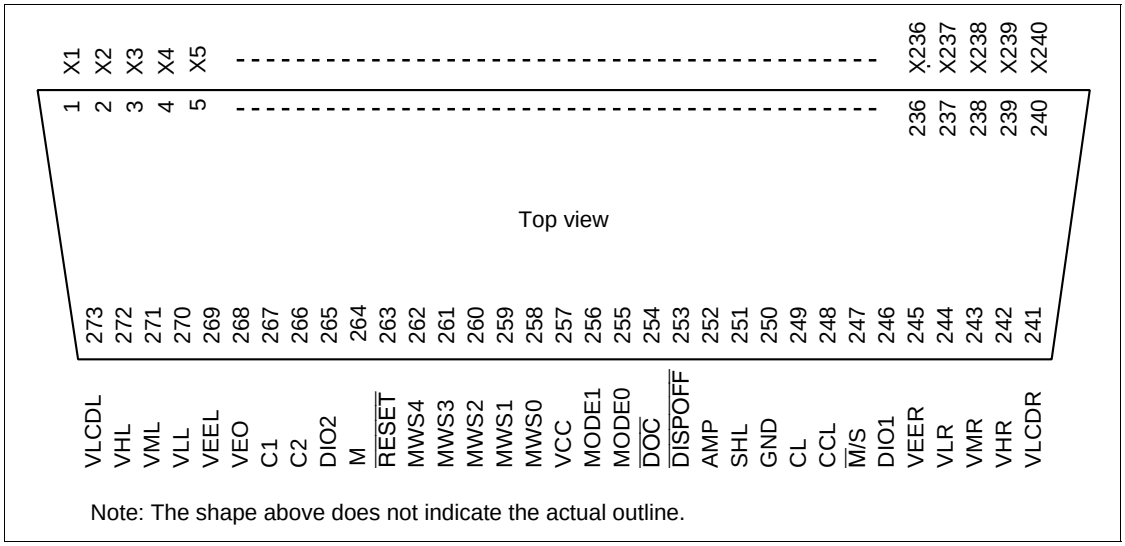
Description

The HD 66137T is a 240-channel common driver which drives a dot matrix STN LCD panel. By changing the mode, this can be applied to 240- and 200- and 160- channel output. Through the use of a 43-V high-voltage CMOS process technology, a high-voltage drive of +21.5 V and –21.5 V, centering on VM is possible. –21.5V generated from +21.5 V with built-in switching circuit and external capacity. Low logic-drive voltage (3 V) is used. This device is used together with the segment driver HD66130, HD66134ST or HD66136.

Features

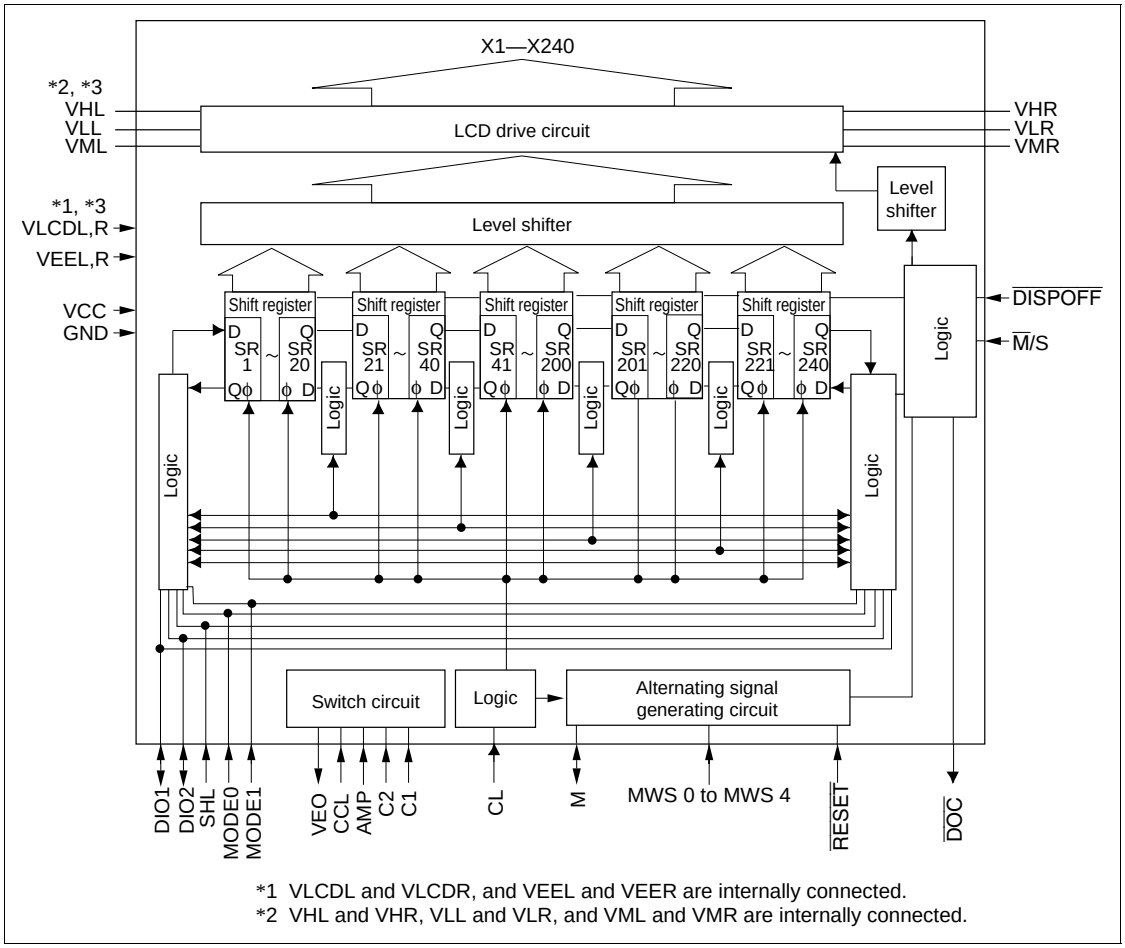
- Display duty: Up to 1/240
- LCD drive voltage: 43 V max
- Built-in switching circuit (to generate –21.5 V)
- Number of LCD drive circuit: 240
- Operating voltage: 2.5 to 5.5 V
- Intermediate voltage I/F
- Built-in alternating signal generation circuit Pin programmable
- Output mode change: 240-output mode
  200-output mode
  160-output mode
- Built-in display-off function
- Flex TCP

Pin Arrangement



Note: The shape above does not indicate the actual outline.

Block Diagram



*1 VLCDL and VLCDR, and VEEL and VEER are internally connected.
*2 VHL and VHR, VLL and VLR, and VML and VMR are internally connected.

Internal Block Diagram

1. LCD drive Circuit

This circuit selects and outputs the three level signals for the LCD drive. By a combination of the data in the shift register and M, either VH, VL, or VM is selected and transmitted to the output circuit.

2. Level shifter

This boosts a 5-V signal to a high-voltage signal for LCD drive.

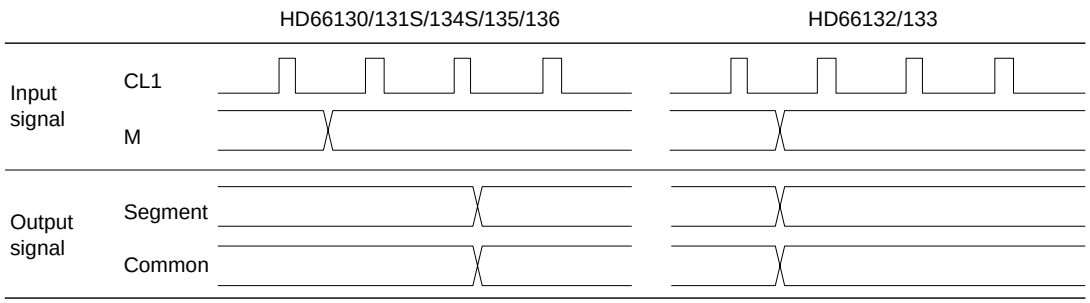
3. Shift register

This is a 240-bit bidirectional shift register circuit. The first line marker signal output from the DIO1 pin and DIO2 pin is sequentially shifted by shift clock CL. The shift direction is determined by the SHL pin.

4. Alternating signal generating circuit

This circuit generates an alternating signal (M signal) for LCD display. To suppress cross-talk, the signal is alternated in a unit from several lines to several tens of lines. By connecting MWS0 to MWS4 pins to V_{CC} or GND, the desired number of signals can be alternated. When alternating signals are externally input, all pins (MWS0 to MWS4) are connected to GND.

HIFAS Family timing Comparison

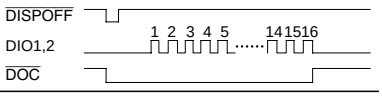


Pin Function

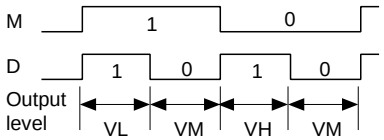
Classification	Symbol	Pin No.	Connected to	I/O	Functions
Power supply	VLCDL, R VEEL, R V_{CC}, GND	273, 241 269, 245 257 250	Power supply	—	VLCDL, R–VEEL, R : Power supply for LCD drive VLCDL, R : Power supply for switch circuit V_{CC}–GND : Power supply for logic circuit
	VHL, R VLL, R VML, R	272, 242 270, 244 271, 243	Power supply	Input	Power supply for LCD drive level VHL, R : Selected level (Set to the same voltage as VLCDL, R.) VLL, R : Selected level (Set to the same voltage as VEEL, R.) VML, R : Non-selected level and Power supply for switch circuit
	VEO	268	VEEL, R	output	When use built -in switching circuit and generate VEE, VEO pin connect to VEEL, R pins. VM voltage is point of reference and reversed and output the voltage input to the voltage between VLCD and VM. If built-in switching circuit is not used, don't connect any lines to this pin.
	C1, C2	267, 266	Capacitance	—	External capacitance should be connected here when using the switch circuit for generate VEE. If built-in switching circuit is not used, don't connect any lines to this pin.
Control signal	CL	249	MPU	Input	Shift clock input. Data is shifted at the falling edge of shift clock CL of the shift register.
	M	264	Extension driver or MPU	I/O	Inputs or outputs the alternating current for LCD drive output.
	MWS0 MWS1 MWS2 MWS3 MWS4	258 259 260 261 262	—	Input	This pin specifies the cycle of the alternating signal (M signal) in the unit of the number of lines. The number of lines, which is an integer from 2 to 31, is specified as follows. Usually, specify the number of lines within a range from 10 to 31. When the HD66131T is driven by an external alternating signal, specify the number of lines as zero.

Number of lines	MWS4	MWS3	MWS2	MWS1	MWS0	Line alternating waveform	M-pin status
0	0	0	0	0	0	——	Input
1	0	0	0	0	1	Prohibited	Output
2	0	0	0	1	0	2 lines alternated	
3	0	0	0	1	1	3 lines alternated	
:	:	:	:	:	:	:	
31	1	1	1	1	1	31 lines alternated	

Pin Functions (cont)

Classification	Symbol	Pin No.	Connected to	I/O	Function
Control signal	MODE0 MODE1	256 256	—	Input	Switch terminals for the number of LCD drive output pins. **MODE0 / MODE1 / Shift direction** "H" / "H" / 240 - output (X1, X2, X3.....X238, X239, X240) "H" / "L" / 200 - output (X21, X22, X23.....X218, X219, X220) "L" / "H" / 160 - output (X41, X42, X43.....X198, X199, X200) "L" / "L" / Prohibited
	DIO1 DIO2	246 265	Extension driver or MPU	I/O	Serial data input output pin **SHL / DIO1 / DIO2** "H" level / serial output pin / serial input pin "L" level / seiral input pin / seiral output pin
	CCL	248	MPU	Input	Built-in switching circuit clock input. When use built-in switching circuit and generate V_{EE}, this pin connect CL pin. If built-in switching circuit is not used, CCL must be fixed to GND
	AMP	252	—	Input	Built-in swiching circuit on-off control. When use built-in switching circuit, this pin must be fixed to V_{CC}. If built-in switching circuit is not used, this pin must be fixed to GND
	$\overline{\text{RESET}}$	263	MPU or V_{CC}	Input	Setting this pin to GND sets initializes the alternating signal (M signal) circuit. A V_{CC} level RESET is normally used.
	$\overline{\text{DISPOFF}}$	253	MPU	Input	Setting this pin to GND sets LCD drive output X1 to X240 to the VM level.
	$\overline{\text{M}}$/S	247	—	Input	Controls the display-off function, and display-off signal output from $\overline{\text{DOC}}$ pin. **$\overline{\text{M}}$/S / $\overline{\text{DISPOFF}}$ pin state and functions** "H" level / When $\overline{\text{DISPOFF}}$ is Low level, X1-240 set VM level "L" level / Until serial data input 16 times X1-X240 set VM level
	$\overline{\text{DOC}}$	254	—	Output	**$\overline{\text{M}}$/S / $\overline{\text{DOC}}$** "H" level / When $\overline{\text{DISPOFF}}$ is Low level, output low level When $\overline{\text{DISPOFF}}$ is High level, output High level "L" level / Until serial data input 16 times output low level from $\overline{\text{DOC}}$ pin  When using M/S is low level, DOC pin should be connect to SEG LSI Dispoff control pin.

Pin Functions (cont)

<table>
<tr><th>Classification</th><th>Symbol</th><th>Pin No.</th><th>Connected to</th><th>I/O</th><th>Function</th></tr>
<tr><td>Control signal</td><td>SHL</td><td>251</td><td>—</td><td>Input</td><td>This pin switches shift directions.
<table>
<tr><th>SHL</th><th>MODE0</th><th>MODE1</th><th>Shift direction</th></tr>
<tr><td>"H" level</td><td colspan="3">Right shift</td></tr>
<tr><td></td><td>"H"</td><td>"H"</td><td>DIO2→SR1·····SR240→DIO1</td></tr>
<tr><td></td><td>"H"</td><td>"L"</td><td>DIO2→SR21·····SR220→DIO1</td></tr>
<tr><td></td><td>"L"</td><td>"H"</td><td>DIO2→SR41·····SR200→DIO1</td></tr>
<tr><td>"L" level</td><td colspan="3">Left shift</td></tr>
<tr><td></td><td>"H"</td><td>"H"</td><td>DIO1→SR240·····SR1→DIO2</td></tr>
<tr><td></td><td>"H"</td><td>"L"</td><td>DIO1→SR220·····SR21→DIO2</td></tr>
<tr><td></td><td>"L"</td><td>"H"</td><td>DIO1→SR200·····SR41→DIO2</td></tr>
</table>
SR1, SR2•••SR240 correspond to X1, X2•••X240.
Note: The 40 or 80 pins invalidated at the 200-output or 160-output mode output the non-selected level synchronized every time; release these pins.</td></tr>
<tr><td>LCD drive output</td><td>X1 to X240</td><td>1 to 240</td><td>LCD</td><td>Output</td><td>LCD drive output
By a combination of the display data and the M signal, when $\overline{\text{DISPOFF}}$ is set to V_{CC}, either VH, VL, or VM is selected and transmitted to the output circuit.
 
</td></tr>
</table>

Note: Configuring the LCD panel using the HD66137 when using the select SEGMENT driver.

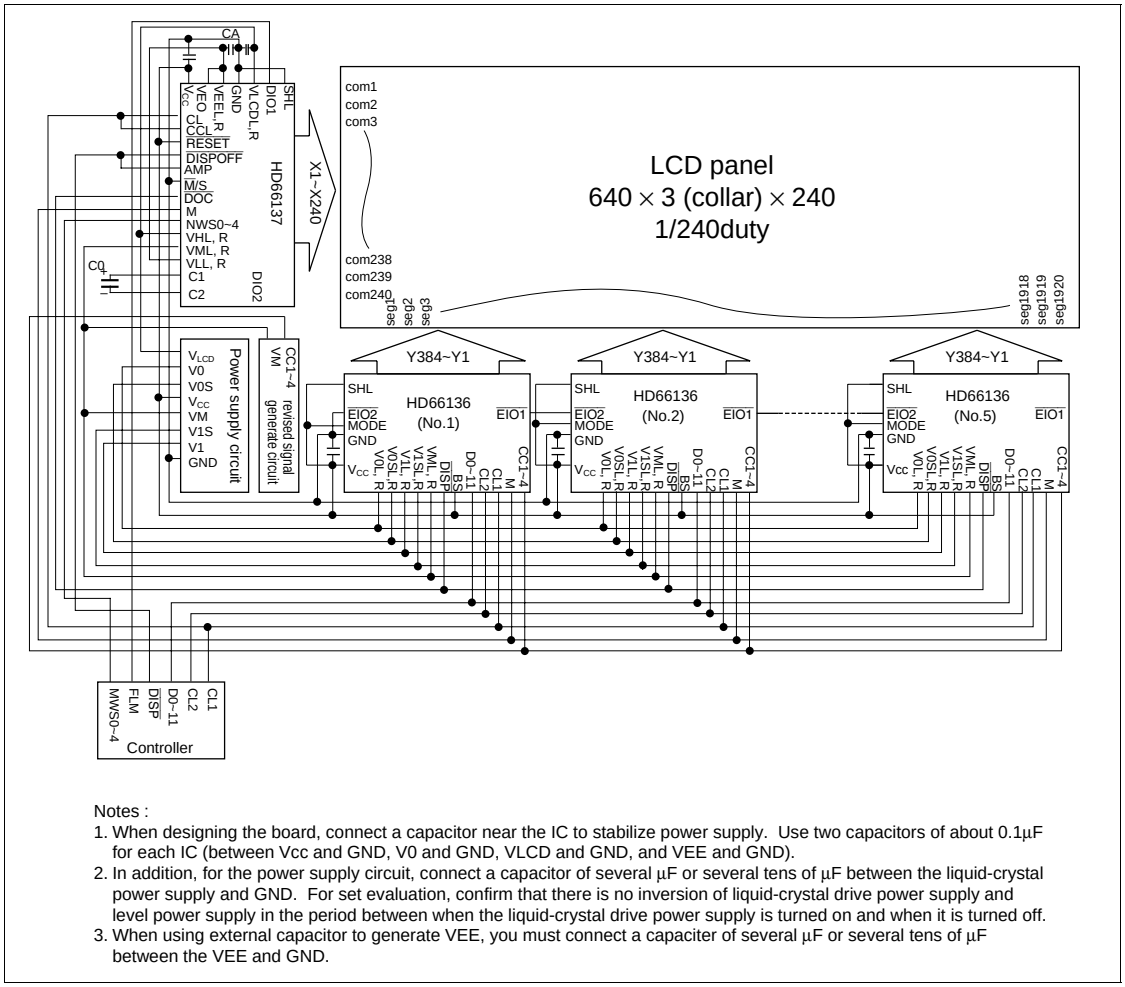
The Select SEGMENT driver

SEGMENT driver	Select
HD66130 (320 OUT)	○
HD66132 (240 OUT)	×
HD66134S (240 OUT)	○
HD66136 (400 OUT)	○

Application Example

Application Example (1)

Figure 1 shows an application example 640 × 3 (collar) × 240 dot Half VGA Size STN color panel.
This panel configured HD66137 × 1 piece and HD66136 × 5 pieces.
HD66137 generates M signal and DOC signal. M signal pin is connected M signal pin of HD66136 and DOC signal pin is connected DISP signal pin of HD66136.
HD66137 is able to generates - voltage by external capacitor.
VEO pin is connected VEE pin and VL pin.

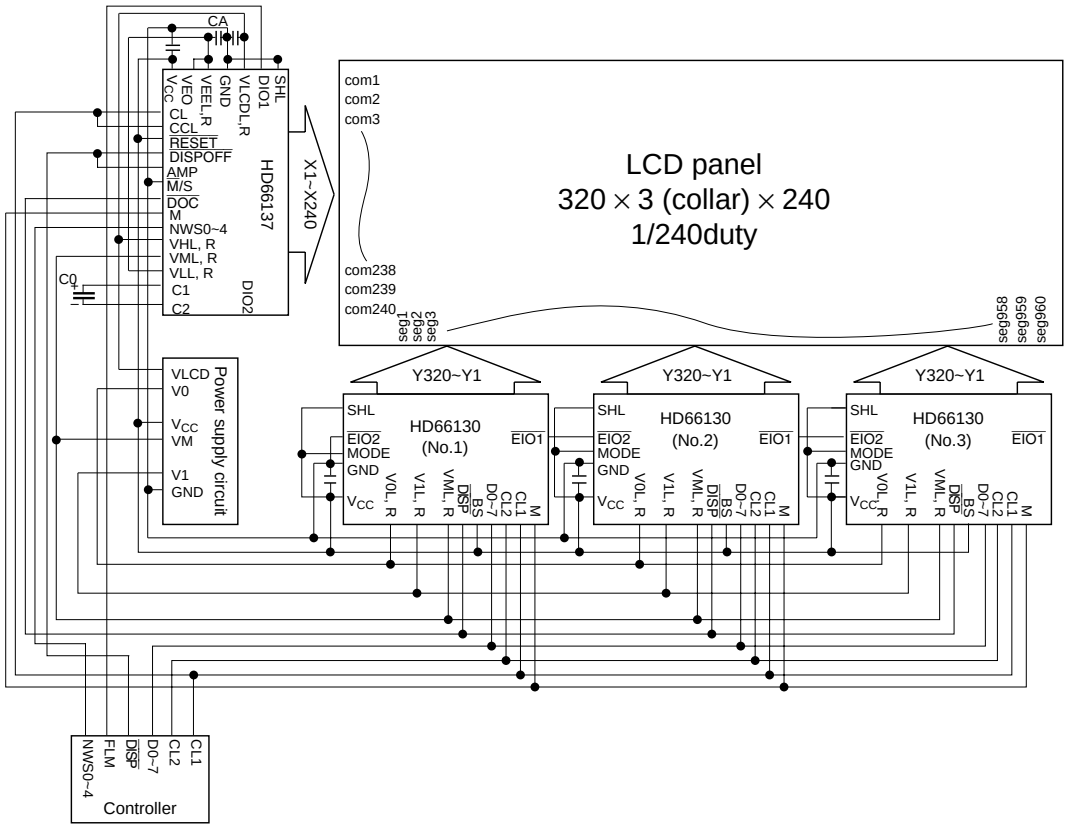


Notes :
1. When designing the board, connect a capacitor near the IC to stabilize power supply. Use two capacitors of about 0.1µF for each IC (between Vcc and GND, V0 and GND, VLCD and GND, and VEE and GND).
2. In addition, for the power supply circuit, connect a capacitor of several µF or several tens of µF between the liquid-crystal power supply and GND. For set evaluation, confirm that there is no inversion of liquid-crystal drive power supply and level power supply in the period between when the liquid-crystal drive power supply is turned on and when it is turned off.
3. When using external capacitor to generate VEE, you must connect a capaciter of several µF or several tens of µF between the VEE and GND.

Figure 1 Application Example (1)

Application Example (2)

Figure 2 shows an application example 320 × 3 (collar) × 240 dot Quarter VGA Size STN color panel.
This panel configured HD66137 × 1 piece and HD66130 × 3 pieces.
HD66137 generates M signal and DOC signal. M signal pin is connected M signal pin of HD66130 and DOC signal pin is connected DISP signal pin of HD66136.
HD66137 is able to generates - voltage by external capacitor.
VEO pin is connected VEE pin and VL pin.



Notes :
1. When designing the board, connect a capacitor near the IC to stabilize power supply. Use two capacitors of about 0.1µF for each IC (between Vcc and GND, V0 and GND, VLCD and GND, and VEE and GND).
2. In addition, for the power supply circuit, connect a capacitor of several µF or several tens of µF between the liquid-crystal power supply and GND. For set evaluation, confirm that there is no inversion of liquid-crystal drive power supply and level power supply in the period between when the liquid-crystal drive power supply is turned on and when it is turned off.
3. When useing external capacitor to generate VEE, you must connect a capacitor of several µF or several tens of µF between the VEE and GND.

Figure 2 Application Example (2)

Power Supply Circuit Example

Figure 3 shows a power supply circuit example.

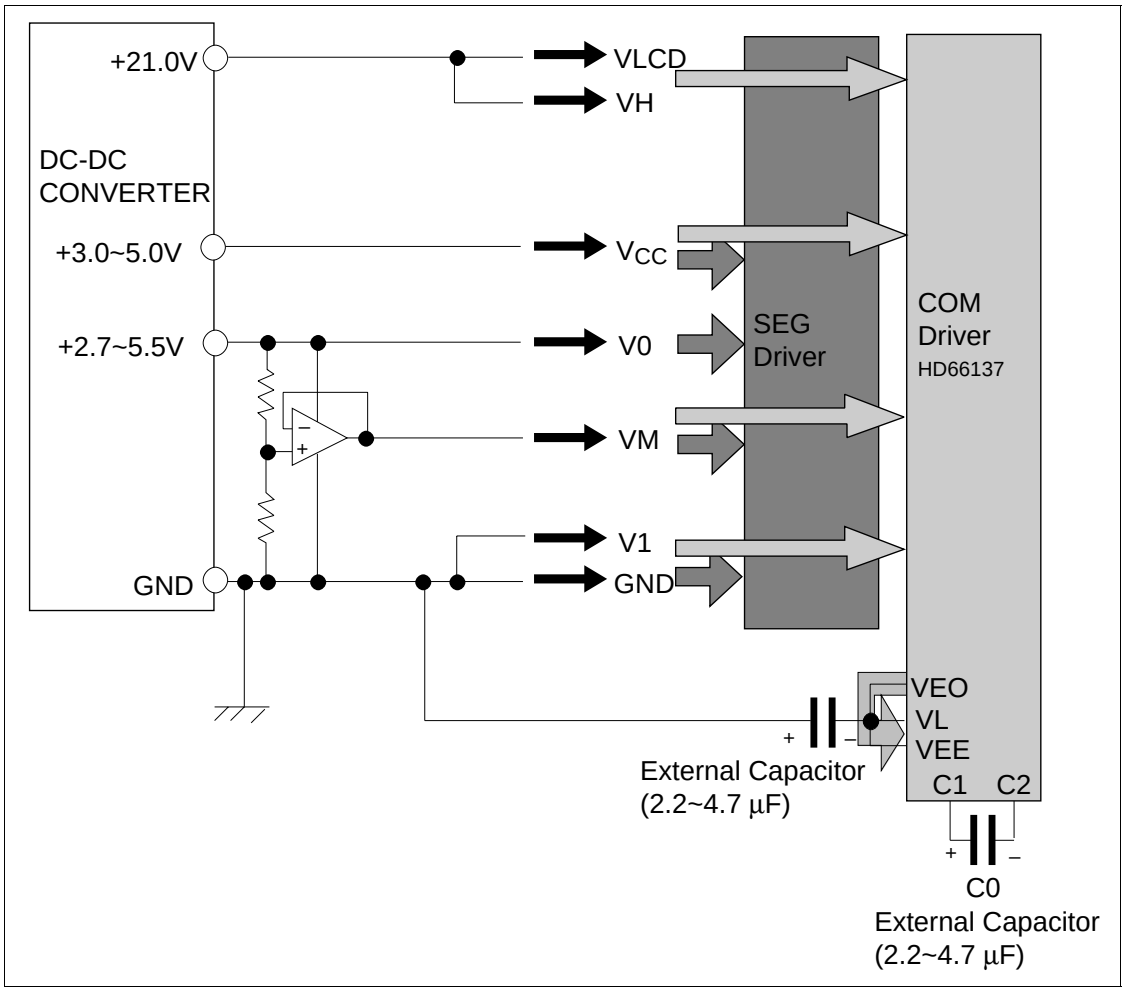


Figure 3 Power Supply Circuit Example

Absolute Maximum Rating

Item		Symbol	Ratings	Unit	Notes
Power supply	Logic circuit	V_{CC}	–0.3 to +7.0	V	1, 8
voltage	LCD drive circuit	V_{LCD}	–0.3 to +25.0	V	1, 3, 8
		V_{EE}	–20.0 to +0.3	V	1, 4, 8
Input voltage (1)		VT1	–0.3 to V_{CC} + 0.3	V	1, 2
Input voltage (2)		VH	–0.3 to V_{LCD}	V	1, 5, 8
Input voltage (3)		VL	+0.3 to V_{EE}	V	1, 6, 8
Input voltage (4)		VM	–0.3 to + 5.0	V	1, 7, 8
Operating temperature		Topr	–30 to +75	°C	
Storage temperature		Tstg	–55 to +110	°C	

Notes: 1. Voltage from GND.

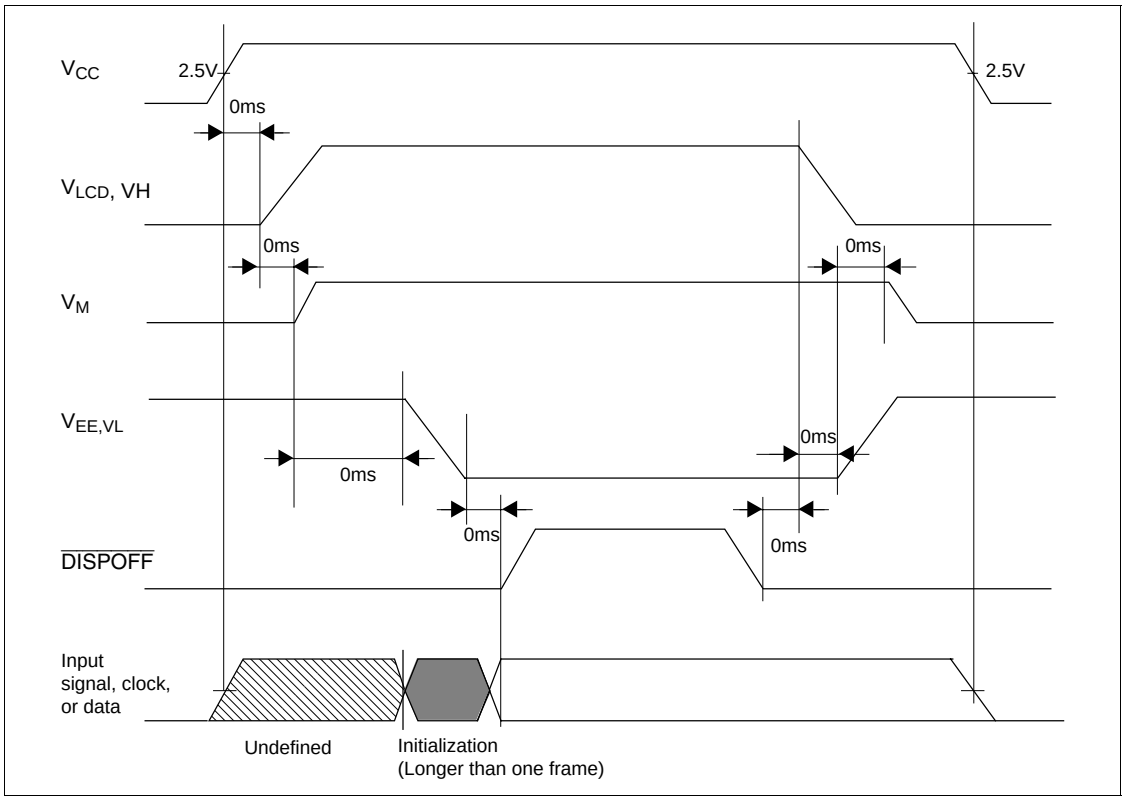
2. Applicable to DIO1, $\overline{\text{DISPOFF}}$, SHL, M, NWS0, NWS1, NWS2, NWS3, NWS4, $\overline{\text{RESET}}$, MODE0, MODE1, CL, $\overline{\text{M}}$/S, AMP, CCL, DIO2.
3. Applicable to V_{LCDL}, R pins.
4. Applicable to V_{EEL}, R pins.
5. Applicable to V_{HL}, R pins.
6. Applicable to V_{LL}, R pins.
7. Applicable to V_{ML}, R pins.

   (Caution)

   Operating the LSI in excess of the absolute maximum rating will result in permanent damage. Use the LSI observing electrical characteristic conditions in normal operation. Exceeding the conditions will cause malfunctions or will affect LSI reliability.
8. Observe the sequence of activation and inactivation for the following power supplies and signals.

   And this sequence apply to use built - in switching circuit.

   If the sequence is not observed, it may cause LSI malfunction, permanent damage, or adverse effects.



8.1 Power on

(1) Turn on the power supply in the order of GND- V_{CC}, GND-VLCD (VH), and VM. VM-VEE is generated automatically. In this case, input GND to the $\overline{DISPOFF}$ pin.

(2) The LCD level forcibely outputs the VM level by the DISPOFF function.

(3) The DISPOFF function has a priority even if input signal distortion occurs immediately after V_{CC} input.

(4) Then input the predetermined signals to initialize the driver registers. In this case, assure a period for more than one frame.

(5) Preparation for normal display is thus completed. Cancel the DISPOFF function by setting the $\overline{DISPOFF}$ pin to V_{CC}. At this point, the levels of VEE (VL), VLCD (VH) and VM must have reached the predetermined respective voltage.

8.2 Shut down

As a rule, shut down in order opposite to that used for power on.

(1) Set the $\overline{DISPOFF}$ pin to GND.

(2) At first shut off the LCD power supply GND-VLCD (VH), at same time GND-VEE (VL) get to VM. Next shut off the VM.

(3) Set V_{CC} and the input signal to GND.

At this point, VEE (VL), VLCD (VH) and VM pin input must completely drop to 0 V.

Since the DISPOFF function is inactivated when the V_{CC} level drops to GND, the LCD output may output a level other than VM. Therefore, an incorrect display may appear at shut down or power on.

Electrical Characteristics

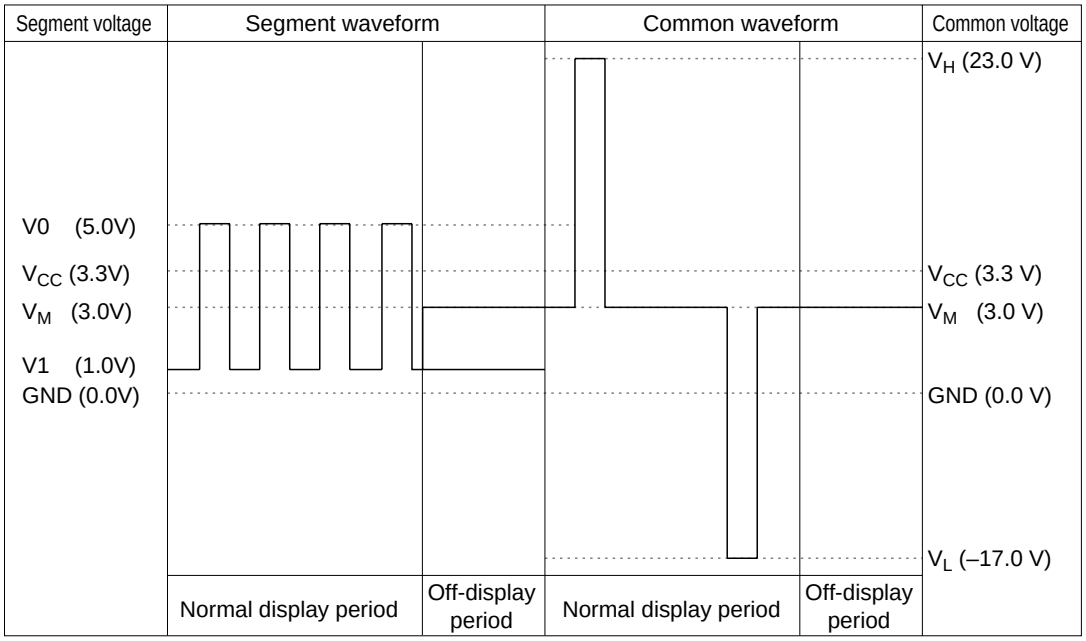
DC Characteristics (V_{CC} = 2.5 to 5.5 V, GND = 0 V, V_{LCD}–V_{EE} = 15 to 43 V, Ta = –30 to +75 °C)

Item	Symbol	Applicable Pins	Min.	Typ.	Max.	Unit	Measurement Conditions	Notes
Input high-level voltage	V_{IH}	DIO1, $\overline{DISPOFF}$, SHL, M, $\overline{M}$/S, MWS0~4, $\overline{RESET}$,	0.7 × V_{CC}	—	V_{CC}	V		
Input low-level voltage	V_{IL}	CL, MODE0, MODE1, $\overline{DOC}$, AMP, CCL, DIO2	0	—	0.3 × V_{CC}	V		
Output high-level voltage	V_{OH}	M, $\overline{DOC}$, DIO1, DIO2	V_{CC} – 0.4	—	—	V	I_{OH} = –0.4 mA	
Output low-level voltage	V_{OL}	M, $\overline{DOC}$, DIO1, DIO2	—	—	0.4	V	I_{OL} = 0.4 mA	
ON resistance between Vi–Yj	RON	X1 to X240, V pin	—	0.7	2.0	kΩ	I_{ON} = 150 µA	1
Input leak current (1)	$I_{IL}1$	DIO1, $\overline{DISPOFF}$, SHL, M, $\overline{M}$/S, MWS0~4, $\overline{RESET}$, CL, MODE0, MODE1, $\overline{DOC}$, AMP, CCL, DIO2	–5	—	5	µA	V_{IN} = V_{CC} to GND	
Input leak current (2)	$I_{IL}2$	VH, VL, VM, C1, C2	–25	—	25	µA		
Current consumption (1)	$I_{CC}1$	V_{CC}	—	10	40	µA	V_{CC} = 3.3 V, V_{LCD}–V_{EE} = 40 V, f_{CL} = 19.2 kHz, f_M = 1.5 kHz	2
Current consumption (2)	$I_{CC}2$	V_{CC}	—	20	50	µA	V_{CC} = 5.0 V, V_{LCD}–V_{EE} = 40 V, f_{CL} = 19.2 kHz, f_M = 1.5 kHz	
Current consumption (3)	I_{LCD}	V_{LCD}	—	25	50	µA	V_{CC} = 3.3 V, V_{LCD}–V_{EE} = 40 V, f_{CL} = 19.2 kHz, f_M = 1.5 kHz	

Notes: 1. This is a resistance value between the X and V pins (either of VH, VL, or VM) when a load current is applied to one of x1 to x240 pins. These values are regulated under the conditions of VLCD = VH = 21.75 V, VEE = VL = –18.5 V, VM = 1.75 V, GND = 0 V, Use VH, VL, and VM in the range of VLCD – VM≥VH – VM = 21.5 to 7.5 V, VEE – VM≤VL – VM = –21.5 to –7.5 V, with the relation of VH > VM > VL.

2. The current applied between the input and output is excluded. When an input to a CMOS gate is at an intermediate level, through current flows between the power supplies, and the power supply current increases. Therefore, use V_{IH} = V_{CC} and V_{IL} = GND.

3. The voltage relationship of each signal is as follows :



AC Characteristics (1) (V_{CC} = 2.5 to 5.5 V, GND = 0 V, V_{LCD}–V_{EE} = 15 to 43 V, Ta = –30 to +75 °C)

Item	Symbol	Pin Name	min.	max.	Dimensions	Note
Clock cycle time	t_{CYC}	CL	400	—	ns	
CL high-level width	t_{CWH}	CL	25	—	ns	
CL low-level width	t_{CWL}	CL	370	—	ns	
CL rising time	t_r	CL	—	30	ns	
CL falling time	t_f	CL	—	30	ns	
Data set-up time	t_{DS}	DIO1, DIO2, CL	100	—	ns	
Data hold time	t_{DH}	DIO1, DIO2, CL	10	—	ns	
Data output delay time	t_{DD}	DIO1, DIO2, CL	—	200	ns	1
M output delay time	t_{MD}	M, CL	—	200	ns	1
M set-up time	t_{MS}	M, CL	20	—	ns	
M Hold time	t_{MH}	M, CL	20	—	ns	
DOC delay time 1	t_{DOC1}	$\overline{\text{DISPOFF}}$, $\overline{\text{DOC}}$	—	300	ns	2
DOC delay time 2	t_{DOC2}	DIO1, DIO2, $\overline{\text{DOC}}$	—	300	ns	2

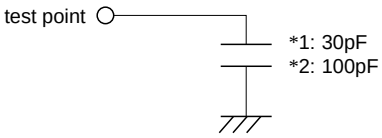
AC Characteristics (2) (V_{CC} = 2.5 to 4.5 V, GND = 0 V, V_{LCD}–V_{EE} = 43 V, Ta = –30 to +75 °C)

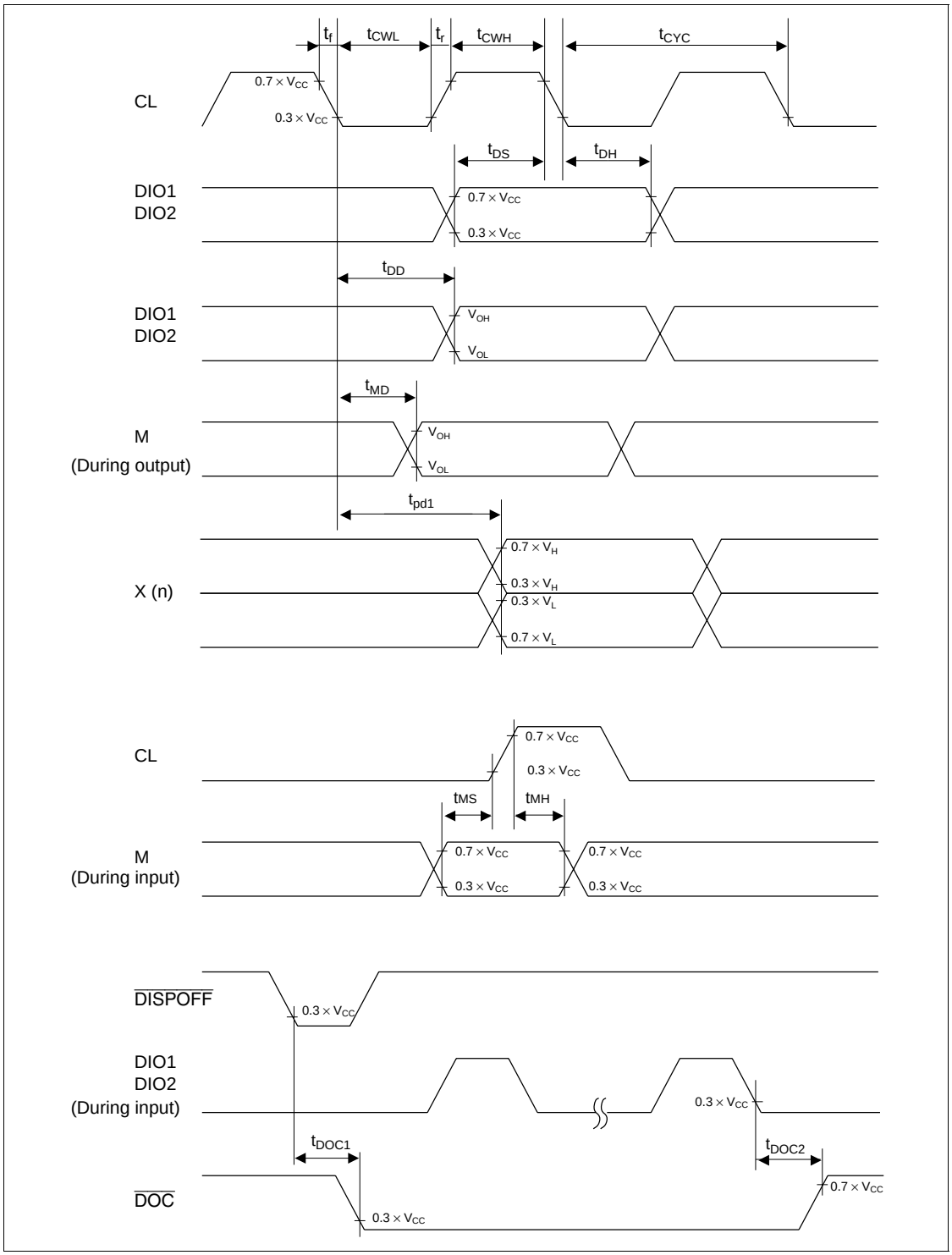
Item	Symbol	Pin Name	min.	max.	Dimensions	Note
Output delay time1	t_{pd1}	X(n), M	—	1.2	µs	2

AC Characteristics (3) (V_{CC} = 4.5 to 5.5 V, GND = 0 V, V_{LCD}–V_{EE} = 43 V, Ta = –30 to +75 °C)

Item	Symbol	Pin Name	min.	max.	Dimensions	Note
Output delay time1	t_{pd1}	X(n), M	—	0.7	µs	2

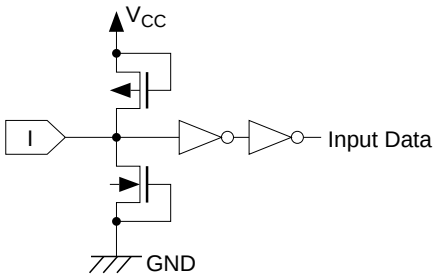
*1, *2. The following timing is regulated with the circuit at the right connected.



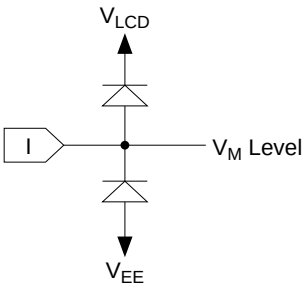


Terminal Configuration

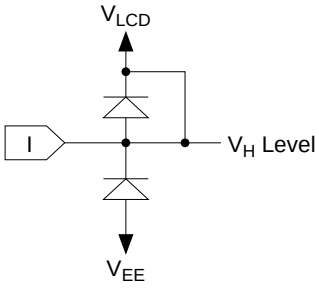
Terminal Configuration (1)



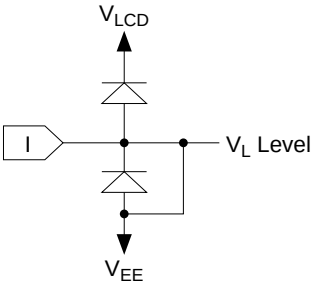
Input Terminal 1
Applicable terminals :
CL, CCL, SHL, MODE0,1, AMP
$\overline{DISPOFF}$, $\overline{RESET}$, MWS0~4, $\overline{M}$/S



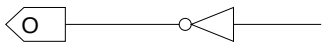
Input Terminal 2
Applicable terminals : $V_{MR, L}$
* V_{MR} terminal connect with V_{ML} terminal in LSI.



Input Terminal 3
Applicable terminals : $V_{HR, L}$
* V_{HR} terminal connect with V_{HL} terminal in LSI.

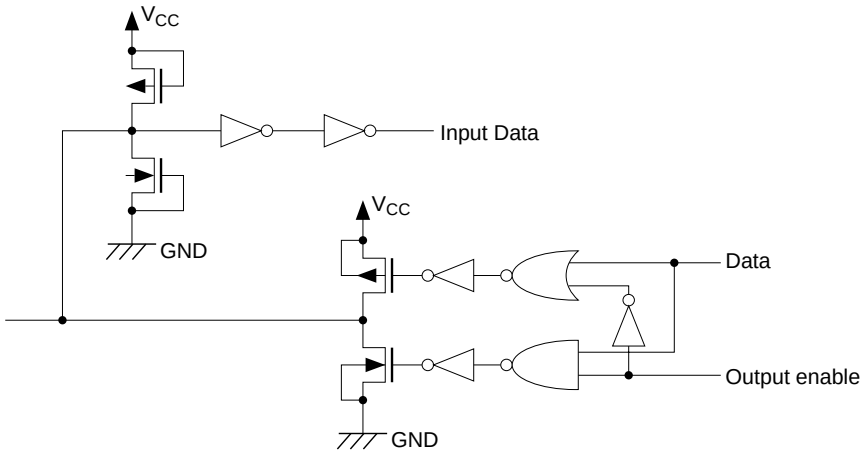


Input Terminal 4
Applicable terminals : $V_{LR, L}$
* V_{LR} terminal connect with V_{LL} terminal in SLI.

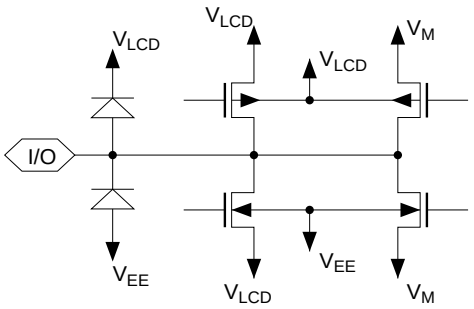


Output Terminal 1
Applicable terminals : $\overline{DOC}$

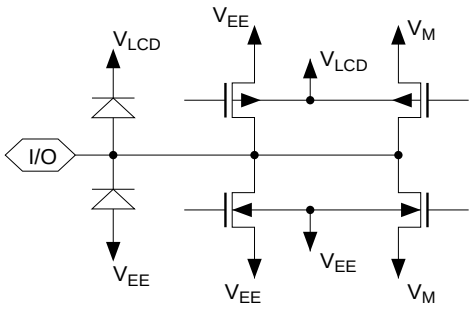
Terminal Configuration (2)



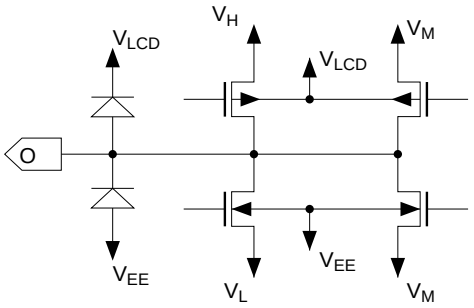
I/O Terminal 1
Applicable terminals : DIO1, DIO2, M,



I/O Terminal 2
Applicable terminals : C1



I/O Terminal 3
Applicable terminals : C2



LCD drive Output Terminal
Applicable terminals : X1 to X240

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