

---

# HD66130T

320-channel Low-voltage Segment Driver for Dot-Matrix STN  
Liquid Crystal Display

# HITACHI

---

## Description

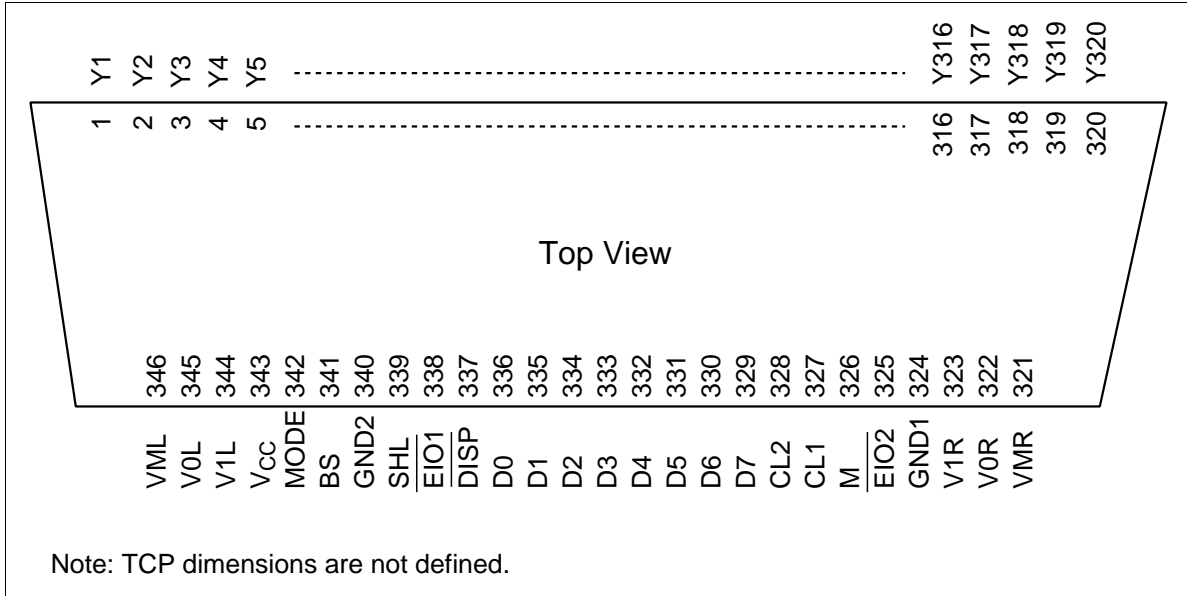
The HD66130T is a 320-channel segment driver for driving a dot-matrix STN liquid-crystal panel at a low voltage. The driver can also correspond to 240-channel output by switching mode. It operates at a low voltage: a liquid-crystal drive voltage of 5 V and a logic drive voltage of 3 V, and is used together with common driver HD66131T or HD66135T. The package, which adopts a flexible TCP, can be applied to various liquid crystal panels.

## Features

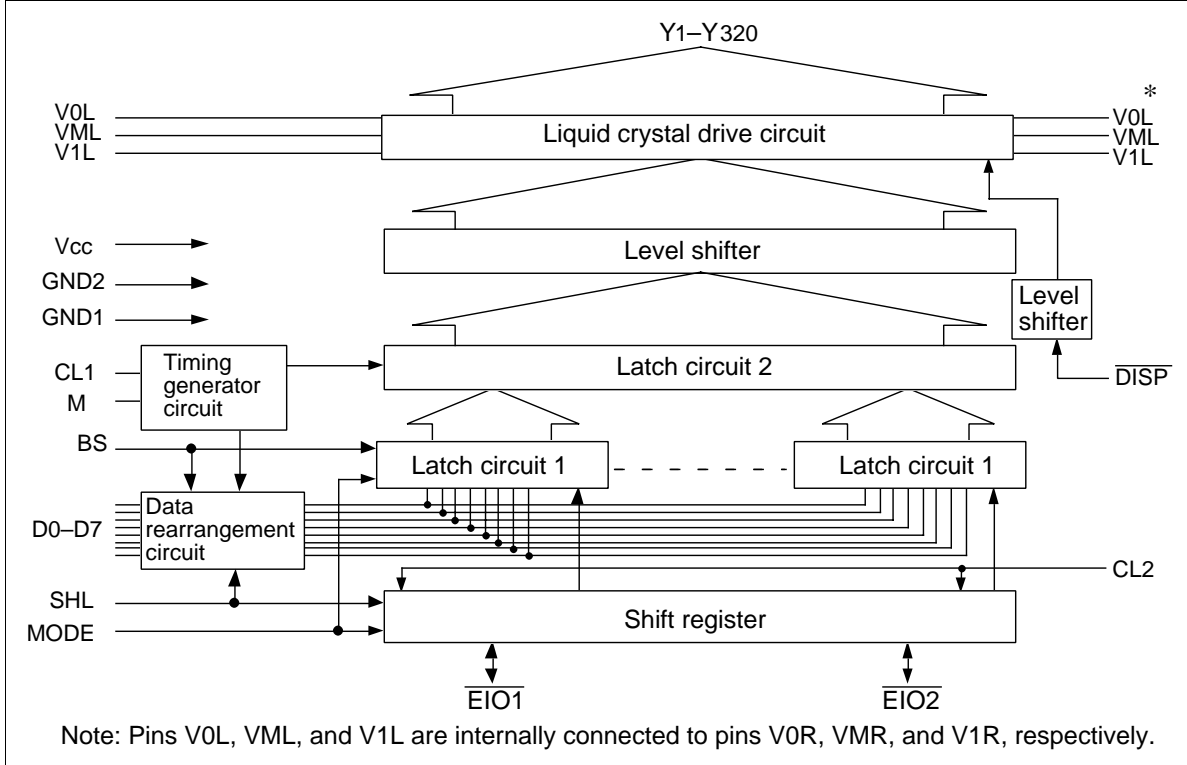
- Display duty: Up to 1/240
- Liquid crystal drive voltage: 2.6 to 5.5 V
- Number of liquid crystal drive circuits: 320 circuits
- Operating voltage: 2.5 to 5.5 V
- Number of data bits: 4 or 8 bits
- Shift clock speed: 8 MHz max/5V  
6.5 MHz max/3V
- Together with the common drivers  
HD66131T , HD66135T
- Low power consumption
- Switching output mode: 320 output mode  
240 output mode
- Display-off function
- Flexible TCP
- Automatic generation of chip-enable signals
- Standby function

# HD66130T

## Pin Arrangement

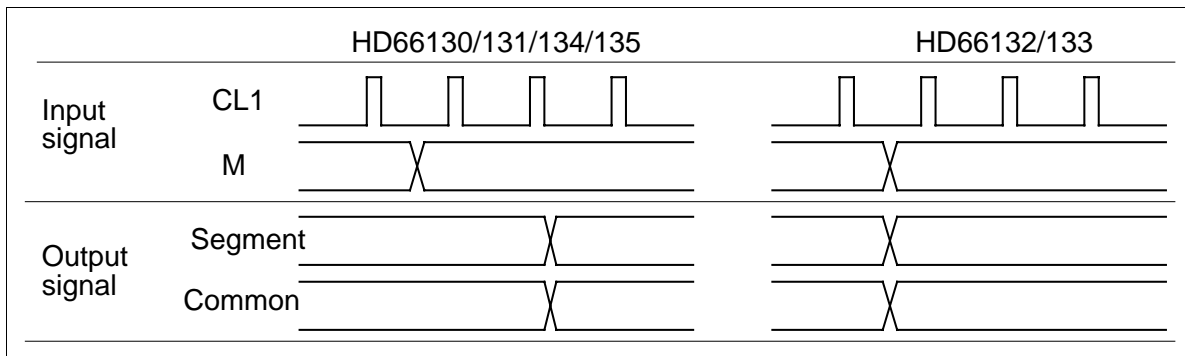


## Internal Block Diagram



1. Liquid crystal drive circuit  
Selects and outputs the liquid crystal drive level V0, VM, or V1 by  $\overline{\text{DISP}}$  and a combination of data for latch circuit 2 and signal M.
2. Level shifter  
Converts logic signals to liquid crystal drive signals.
3. Latch circuit 2  
320-bit latch circuit, which latches the data of latch circuits 1 at the fall of CL1 and outputs the data to the level shifter.
4. Latch circuit 1  
4/8-bit parallel data latch circuit, which latches display data D0 to D7 according to signals transmitted from the shift register.
5. Shift register  
80-bit shift register, which generates data-capture signals for latch circuits 1 at the fall of CL2.
6. Data rearrangement circuit  
Inverts the order of data output crosswise.
7. Timing generator circuit  
The timing generator circuit generates data latch pulses for latch circuit2 and changes pulse the LCD drive outputs to AC.

**HIFAS Family timing Comparision**



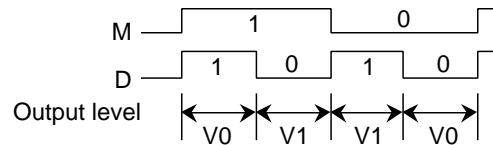
# HD66130T

## Pin Functions

Class	Symbol	Pin Number	Pin Name	I/O	Functions									
Power supply	V <sub>CC</sub>	343	V <sub>CC</sub>	—	V <sub>CC</sub> -GND: Power supply for logic.									
	GND1	324	GND											
	GND2	340												
	V0L, R	345, 322	V0L, R	Input	Liquid crystal drive level power supply									
	VML, R	346, 321	VML, R											
	V1L, R	344, 323	V1L, R											
Control signal	CL1	327	Clock 1	Input	Latch signal of display data: A liquid crystal drive signal corresponding to display data is output at the fall of CL1.									
	CL2	328	Clock 2	Input	Capture signal of display data: Display data is captured at the fall of CL2.									
	M	326	M	Input	A.C. signal of liquid crystal drive output									
	D0 to D7	336 to 329	DATA 0 to DATA 7	Input	<table border="1"> <thead> <tr> <th>Display data</th> <th>Liquid crystal drive output</th> <th>Liquid crystal display</th> </tr> </thead> <tbody> <tr> <td>1 (V<sub>CC</sub> level)</td> <td>Selected level</td> <td>ON</td> </tr> <tr> <td>0 (GND level)</td> <td>Not-selected level</td> <td>OFF</td> </tr> </tbody> </table>	Display data	Liquid crystal drive output	Liquid crystal display	1 (V <sub>CC</sub> level)	Selected level	ON	0 (GND level)	Not-selected level	OFF
	Display data	Liquid crystal drive output	Liquid crystal display											
	1 (V <sub>CC</sub> level)	Selected level	ON											
	0 (GND level)	Not-selected level	OFF											
	SHL	339	Shift Left	Input	Control signal for inverting the order of data output (see the following page)									
	$\overline{\text{EIO1}}$	338	Enable IO1	I/O	<table border="1"> <thead> <tr> <th>SHL</th> <th><math>\overline{\text{EIO1}}</math></th> <th><math>\overline{\text{EIO2}}</math></th> </tr> </thead> <tbody> <tr> <td>GND</td> <td>Enable input</td> <td>Enable output</td> </tr> <tr> <td>V<sub>CC</sub></td> <td>Enable output</td> <td>Enable input</td> </tr> </tbody> </table>	SHL	$\overline{\text{EIO1}}$	$\overline{\text{EIO2}}$	GND	Enable input	Enable output	V <sub>CC</sub>	Enable output	Enable input
	SHL	$\overline{\text{EIO1}}$	$\overline{\text{EIO2}}$											
GND	Enable input	Enable output												
V <sub>CC</sub>	Enable output	Enable input												
$\overline{\text{EIO2}}$	325	Enable IO2	I/O	Enable input: The enable input of the first IC is connected to the GND and another is connected to the enable output of the second IC. Enable output: Connected to the enable input of the second IC at cascade output.										
$\overline{\text{DISP}}$	337	Disp off	Input	Grounding $\overline{\text{DISP}}$ sets liquid crystal drive output Y1–Y320 to the VM level.										
BS	341	Bus Select	Input	Switches the number of input bits for the display data. <b>V<sub>CC</sub> 8-bit input mode</b> GND 4-bit input mode (Captures data from D0–D3. At this time, connect D4–D7 to the GND.)										
MODE	342	MODE	Input	Switches the number of input bits for the display data. <b>V<sub>CC</sub> 320 output mode</b> GND 240 output mode (Y41–Y280 are valid output. The other 80 pins output the not-selected-level signals synchronized every time; release these pins.)										

**Pin Functions (cont)**

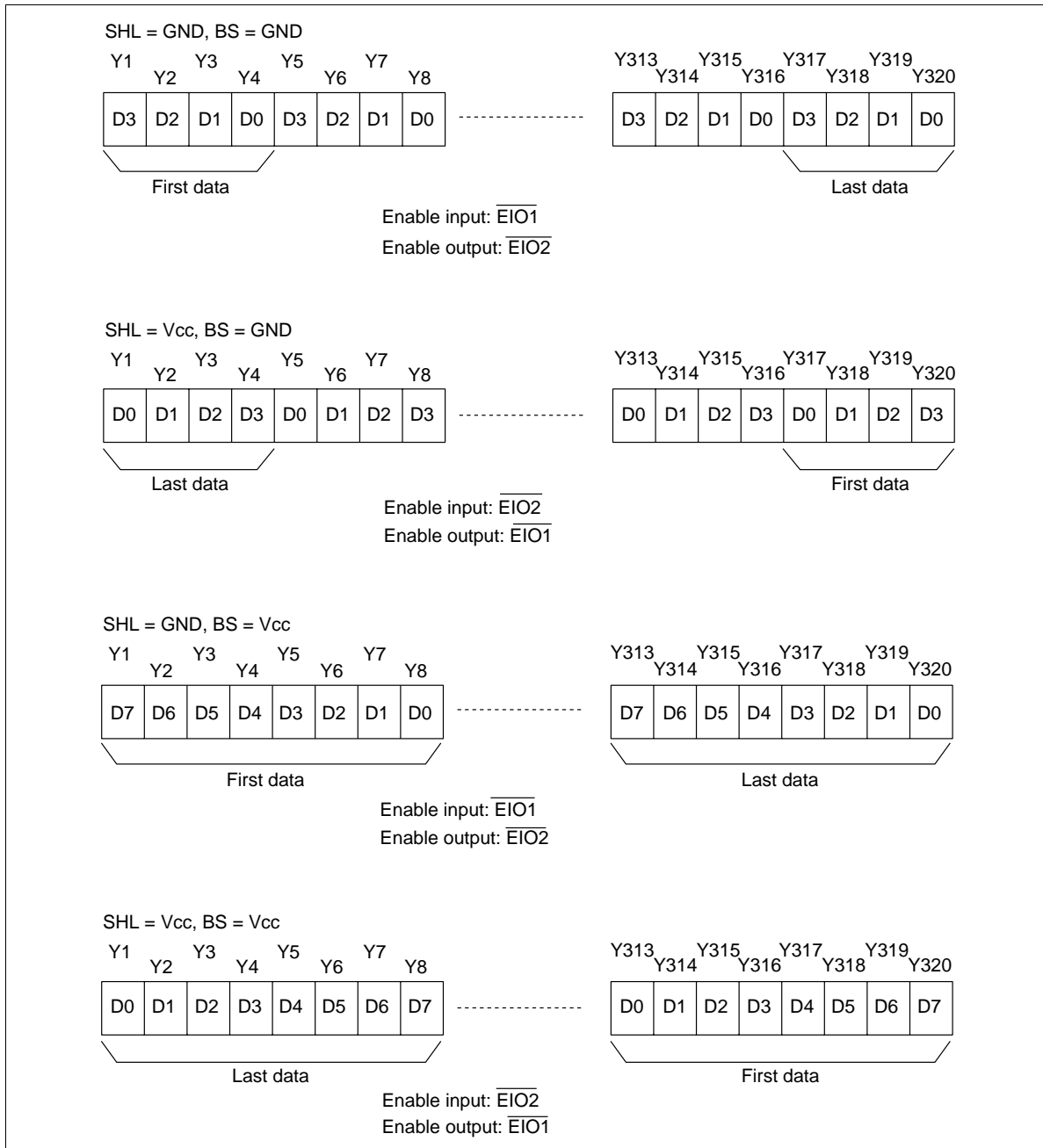
Class	Symbol	Pin Number	Pin Name	I/O	Function
Liquid crystal drive output	Y1 to Y320	1 to 320	Y1 to Y320	Output	Liquid crystal drive output: Selects and outputs level V0 or V1 according to the combination of the M signal and display data when $\overline{\text{DISP}}$ is connected to Vcc.



# HD66130T

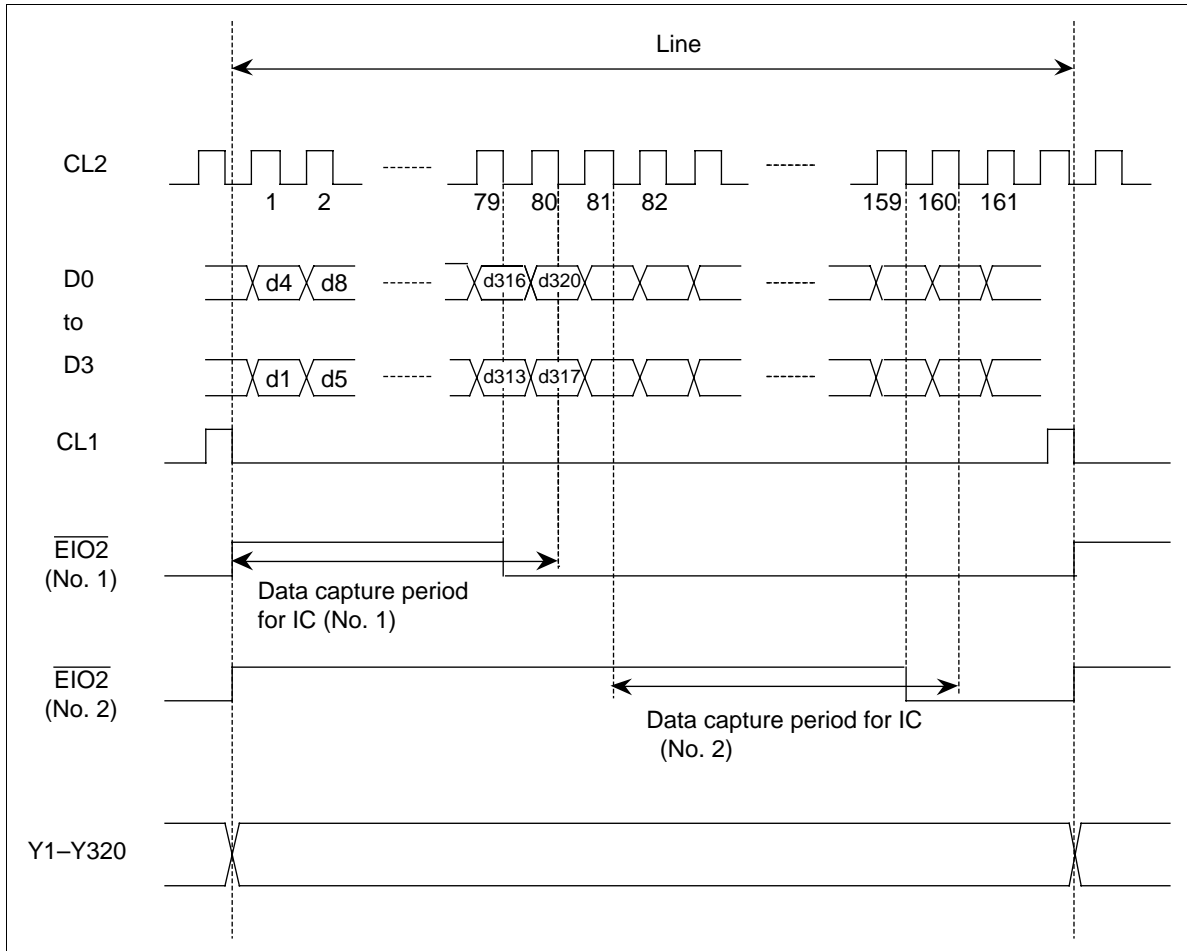
## Rearranging Output Data (SHL)

The order for the output of captured data is inverted crosswise according to the SHL signal. At this time, the input/output pin of the enable signal can be switched.



Operation Timing

(1) 4-bit capture mode (1 line, 640 dots)



**BS = GND (4-bit capture mode)**

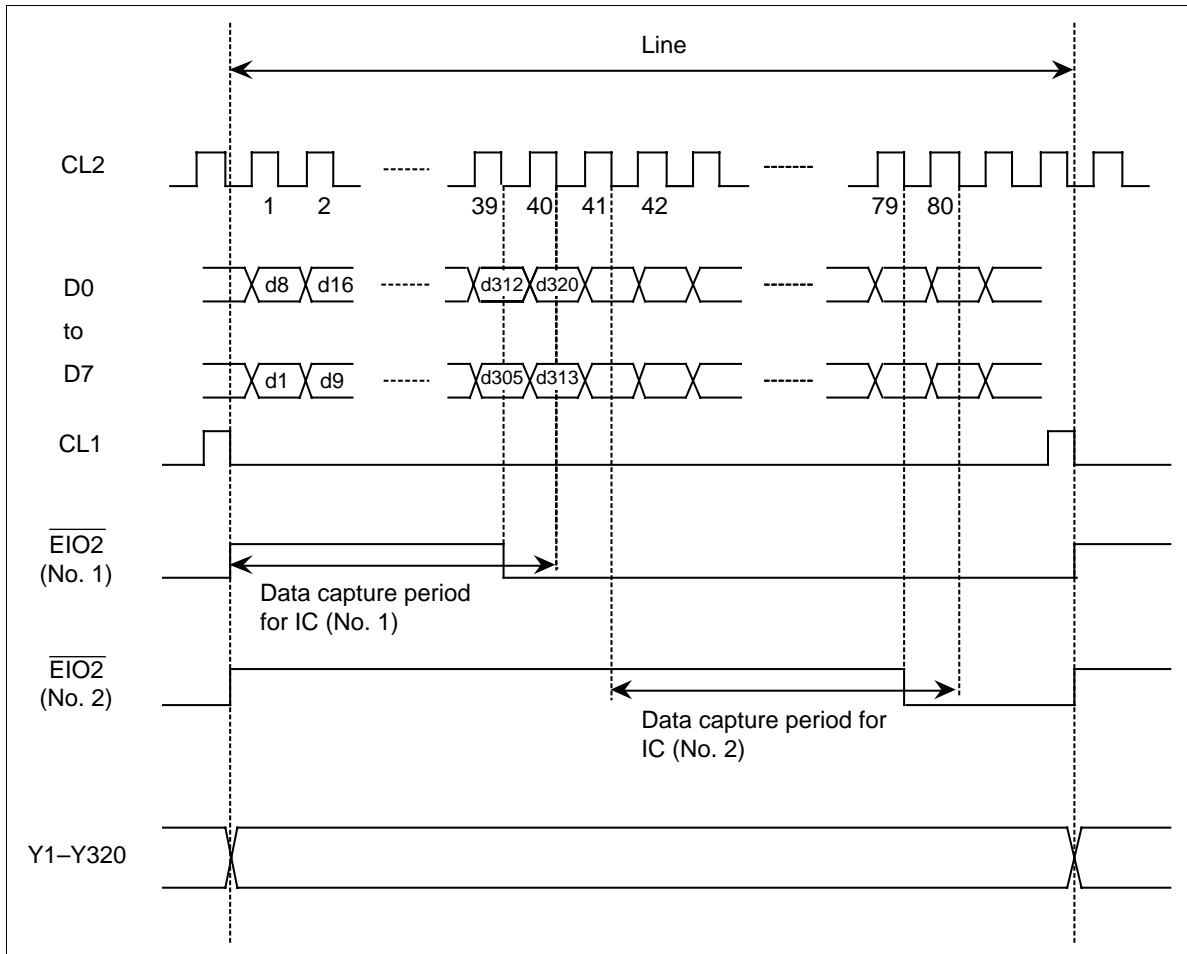
During the data standby state when the data capture operation enable signal is low (SHL = GND:  $\overline{\text{EIO1}}$ ), the next data capture clock (CL2) cancels the standby state. The 4-bit data is captured at the fall of CL2. When 316 bits are captured, the enable signal becomes the GND level (SHL = GND:  $\overline{\text{EIO2}}$ ). When 320 bits are captured, the operation automatically stops (the standby state is entered). The second IC is then activated when pin  $\overline{\text{EIO2}}$  is connected to pin  $\overline{\text{EIO1}}$  of the second IC.

Data output changes at the fall of CL1.

During SHL = GND, captured data d1 and d320 are output to Y1 and Y320, respectively. During SHL = Vcc, data d1 and d320 are output to Y320 and Y1, respectively.

# HD66130T

## (2) 8-bit capture mode (1 line, 640 dots)

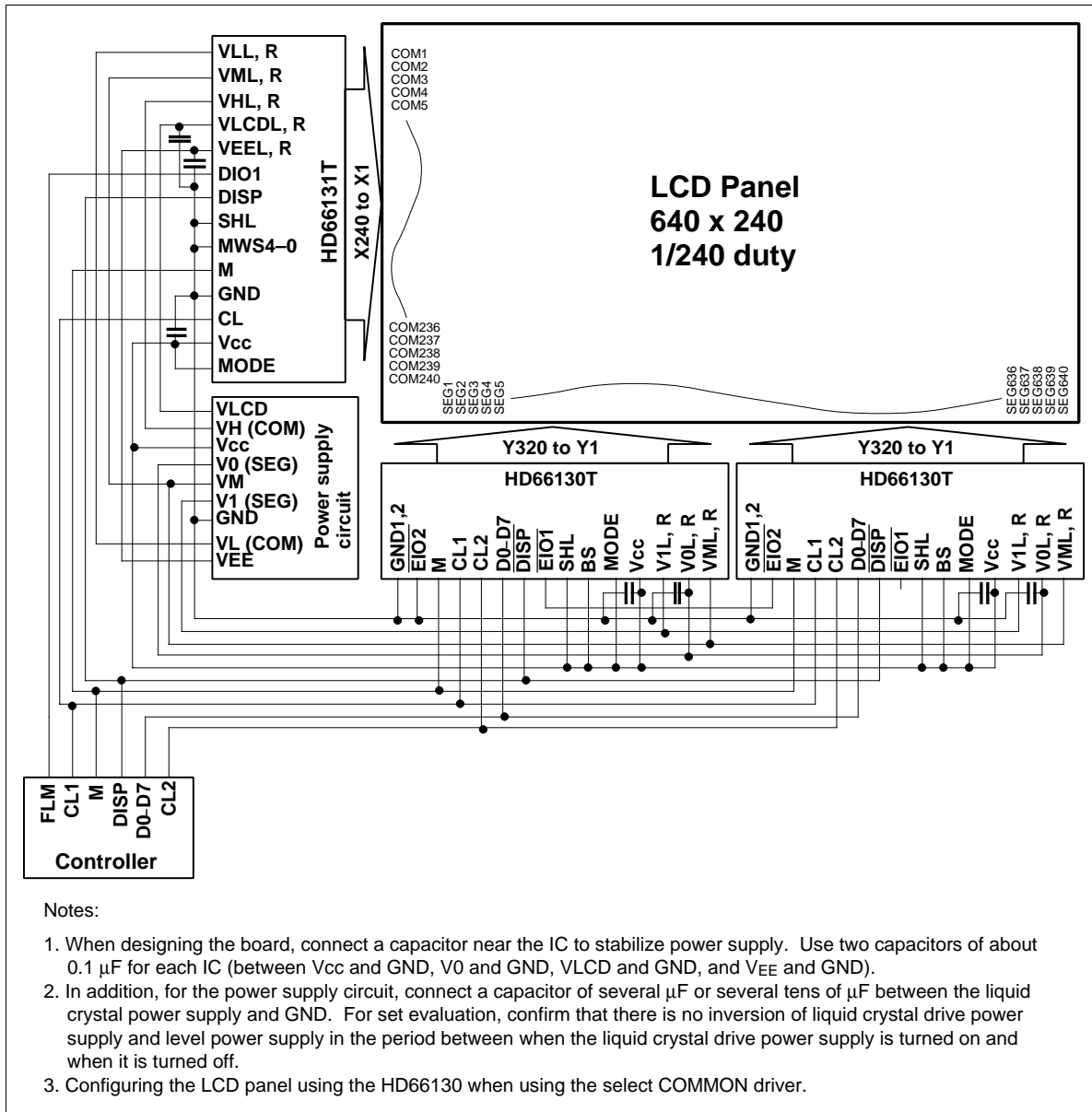


### BS = Vcc (8-bit capture mode)

The 8-bit display data is captured at the fall of CL2. Other basic operations are the same as those of the 4-bit capture mode.



Application Example



The select COMMON driver

COMMON driver	select
HD66131 (240OUT)	<input type="radio"/>
HD66133 (120OUT)	<input checked="" type="radio"/>
HD66135 (120OUT)	<input type="radio"/>

# HD66130T

## Absolute Maximum Ratings

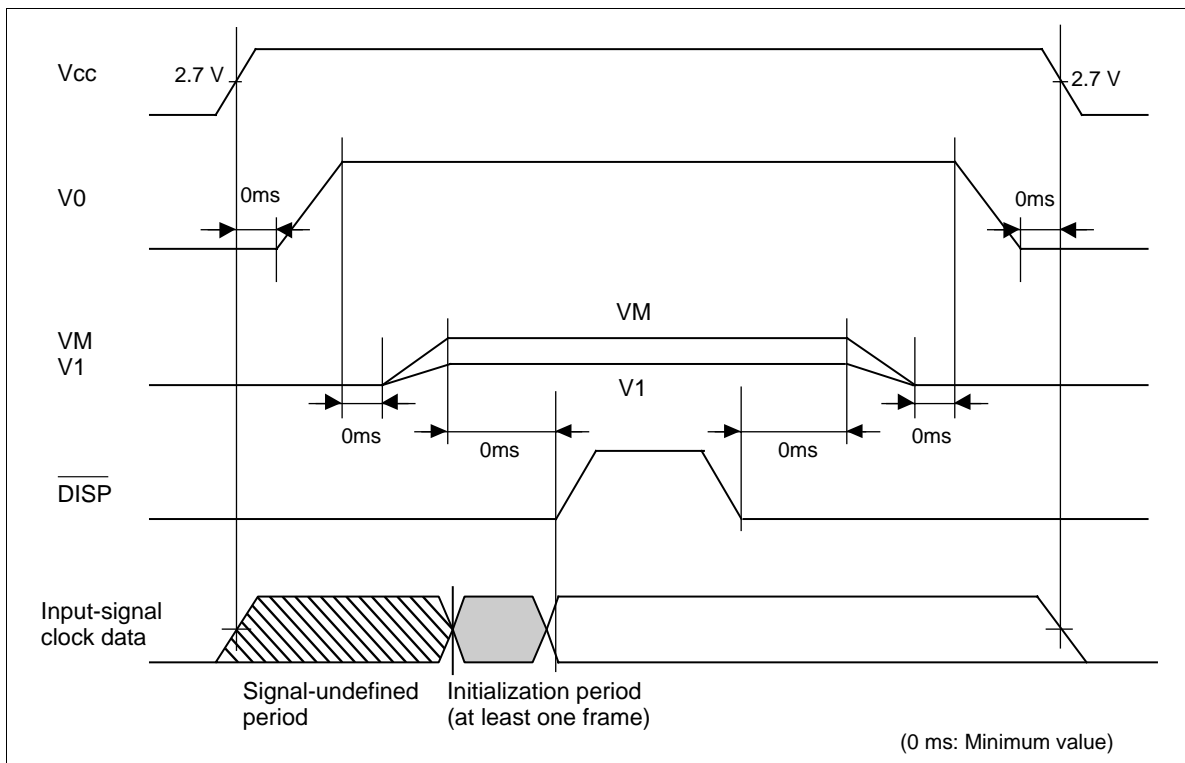
Item	Symbol	Rating	Unit	Notes
Power supply voltage for logic circuits	$V_{CC}$	-0.3 to +7.0	V	1, 4
Power supply voltage for LCD drive circuits	$V_0$	-0.3 to +7.0	V	1, 4
Input voltage 1	$V_{T1}$	-0.3 to $V_{CC} + 0.3$	V	1, 2
Input voltage 2	$V_{T2}$	-0.3 to $V_0 + 0.3$	V	1, 3, 4
Operating temperature	$T_{opr}$	-30 to +75	°C	
Storage temperature	$T_{stg}$	-55 to +110	°C	

Notes: 1. Potential from the GND

- Applied to pins SHL,  $\overline{EIO1}$ ,  $\overline{EIO2}$ ,  $\overline{DISP}$ , D0 to D7, CL1, CL2, M, BS, and MODE.
- Applied to VML, VMR, V1L, and VMR.

Operating the LSI in excess of the absolute maximum rating will result in permanent damage. Use the LSI observing electrical characteristic conditions in normal operation. Exceeding the conditions will cause malfunctions or will affect LSI reliability.

- Conform to the following turn-on/off sequence of the power and signals. Otherwise, the LSI will malfunction or will be permanently damaged. In addition, LSI reliability will be affected.



#### 4.1 Turning on the power

- 1) Turn on the power in the order of GND-  $V_{CC}$ , GND-V0, and VM/V1. Then, ground the  $\overline{DISP}$  pin.
- 2) The LCD forcibly outputs the VM level by the DISPOFF function.
- 3) Even if an input signal is disturbed immediately after  $V_{CC}$  is applied, the DISPOFF function has priority.
- 4) Input the specific signal to initialize registers in the driver. The initialization period must be at least one frame.
- 5) The preparation of normal display is completed. Input the  $V_{CC}$  level to the  $\overline{DISP}$  pin to cancel the DISPOFF function. At this time, the level of pins V0, VM, and V1 must rise to the specific potential.

#### 4.2 Turning off the power

The procedure is basically the reverse for turning on the power.

- 1) Ground the  $\overline{DISP}$  pin.
- 2) Turn off the liquid crystal power in the order of VM/V1 and GND-V0.
- 3) Ground  $V_{CC}$  and an input signal.

At this time, the level of pins V0, VM, and V1 must fall to 0 V. Since the DISPOFF function stops when  $V_{CC}$  falls to 0 V, the LCD may output a level other than VM. Therefore, a display failure may occur when the power is turned off or on.

# HD66130T

## Electrical Characteristics

DC Characteristics 1 ( $V_{CC} = 2.5$  to  $4.5V$ ,  $V_0-GND = 2.6$  to  $5.5V$ ,  $T_a = -30$  to  $+75^\circ C$ )

Item	Symbol	Pins	Min	Typ	Max	Unit	Test Condition	Notes
Input high voltage	$V_{IH}$	CL1, CL2, SHL, M, $\overline{EIO1}$ , $\overline{EIO2}$ ,	$0.8 \times V_{CC}$	—	$V_{CC}$	V		
Input low voltage	$V_{IL}$	MODE, 0, $\overline{DISP}$ , D0 to D7, BS	0	—	$0.2 \times V_{CC}$	V		
Output high voltage	$V_{OH}$	$\overline{EIO1}$ , $\overline{EIO2}$	$V_{CC} - 0.4$	—	—	V	$I_{OH} = -0.4$ mA	
Output low voltage	$V_{OL}$	$\overline{EIO1}$ , $\overline{EIO2}$	—	—	0.4	V	$I_{OL} = 0.4$ mA	
Vi–Yj on resistance	$R_{ON}$	Y1 to Y320, V0L, R	—	0.7	2.0	k $\Omega$	$I_{ON} = 150$ $\mu$ A	1
		Y1 to Y320, VML, R	—	2.0	3.0	k $\Omega$		
		Y1 to Y320, V1L, R	—	0.7	2.0	k $\Omega$		
Input leakage current 1	$I_{IL1}$	CL1, CL2, SHL, M, $\overline{EIO1}$ , $\overline{EIO2}$ , MODE, $\overline{DISP}$ , D0 to D7, BS	–5.0		5.0	$\mu$ A	$V_{IN} = V_{CC}$ to GND	
Input leakage current 2	$I_{IL2}$	VML, R, V1L, R	–25		25	$\mu$ A	$V_{IN} = V_0$ to GND	
Current consumption 1	$I_{CC}$	$V_{CC}$	—	150	300	$\mu$ A	$V_{CC} = 3.3$ V $V_0 = 2.7$ V	2
Current consumption 2	$I_{V0}$	V0L, R	—	60	200	$\mu$ A	$f_{CL2} = 3.5$ MHz $f_{CL1} = 19.2$ kHz	
Current consumption 3	$I_{ST}$	$V_{CC}$	—	50	100	$\mu$ A	$f_M = 1.5$ kHz	2, 3

**DC Characteristics 2 ( $V_{CC} = 4.5$  to  $5.5V$ ,  $V_0-GND = 2.6$  to  $5.5V$ ,  $T_a = -30$  to  $+75^\circ C$ )**

Item	Symbol	Pins	Min	Typ	Max	Unit	Test Condition	Notes
Input high voltage	$V_{IH}$	CL1, CL2, SHL, M, $\overline{EIO1}$ , $\overline{EIO2}$ ,	$0.8 \times V_{CC}$	—	$V_{CC}$	V		
Input low voltage	$V_{IL}$	MODE, 0, DISP, D0 to D7, BS	0	—	$0.2 \times V_{CC}$	V		
Output high voltage	$V_{OH}$	$\overline{EIO1}$ , $\overline{EIO2}$	$V_{CC} - 0.4$	—	—	V	$I_{OH} = -0.4$ mA	
Output low voltage	$V_{OL}$	$\overline{EIO1}$ , $\overline{EIO2}$	—	—	0.4	V	$I_{OL} = 0.4$ mA	
Vi–Yj on resistance	$R_{ON}$	Y1 to Y320, V0L, R	—	0.7	2.0	k $\Omega$	$I_{ON} = 150$ $\mu$ A	1
		Y1 to Y320, VML, R	—	2.0	3.0	k $\Omega$		
		Y1 to Y320, V1L, R	—	0.7	2.0	k $\Omega$		
Input leakage current 1	$I_{IL1}$	CL1, CL2, SHL, M, $\overline{EIO1}$ , $\overline{EIO2}$ , MODE, DISP, D0 to D7, BS	–5.0		5.0	$\mu$ A	$V_{IN} = V_{CC}$ to GND	
Input leakage current 2	$I_{IL2}$	VML, R, V1L, R	–25		25	$\mu$ A	$V_{IN} = V_0$ to GND	
Current consumption 1	$I_{CC}$	$V_{CC}$	—	230	450	$\mu$ A	$V_{CC} = 5.0$ V $V_0 = 2.7$ V	2
Current consumption 2	$I_{V0}$	V0L, R	—	60	200	$\mu$ A	$f_{CL2} = 3.5$ MHz $f_{CL1} = 19.2$ kHz	
Current consumption 3	$I_{ST}$	$V_{CC}$	—	80	150	$\mu$ A	$f_M = 1.5$ kHz	2, 3

Notes: 1. Resistance between pins Y and V when a load current flows to one of the pins from Y1 to Y320.

The following conditions are defined:

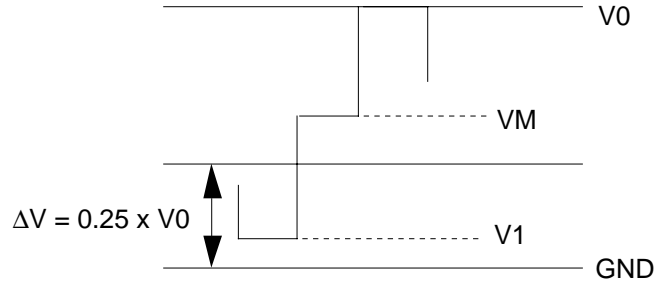
$V_0-GND = 5.5$  V

$V_M = (V_0 + V_1)/2$

## HD66130T

$$V1 = \text{GND} + 1.0$$

The voltage range of the liquid crystal drive level power supply is described. A voltage around the GND is applied to pin V1, and an intermediate voltage of about V0 and V1 is applied to pin VM. Use the V1 in the range of  $\Delta V = 0.25 \times V0$ , in which the impedance Ron of driver output is stable.



Relationship between the driver output waveform and each level voltage

2. A current flowing in the input or output section is excluded. If an input signal is at an intermediate level for the CMOS, a through-current flows in the input circuit and power supply current increases. Therefore, VIH must be at the Vcc level and VIL must be at the GND level.
3. Current at standby
4. The voltage of each signal is shown below.

Segment voltage	Segment waveform		Common waveform		Common voltage
V0 (5.0 V)					VH (23.0 V)
Vcc (3.3 V)					Vcc (3.3 V)
VM (3.0 V)					VM (3.0 V)
V1 (1.0 V)					GND (0.0 V)
GND (0.0 V)					GND (0.0 V)
	Normal display period	Display-off period	Normal display period	Display-off period	VL (-17.0 V)

**AC Characteristics 1 ( $V_{CC} = 2.5$  to  $4.5V$ ,  $V_0-GND = 2.6$  to  $5.5V$ ,  $T_a = -30$  to  $+75^\circ C$ )**

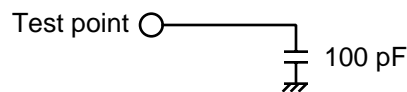
Item	Symbol	Pins	Min	Max	Unit
Clock cycle time	$t_{CYC}$	CL2	152	—	ns
Clock high pulse width 1	$t_{CWH2}$	CL2	65	—	ns
Clock low pulse width 1	$t_{CWL2}$	CL2	65	—	ns
Clock high pulse width 2	$t_{CWH1}$	CL1	65	—	ns
Clock setup time	$t_{SCL}$	CL1, CL2	80	—	ns
Clock hold time	$t_{HCL}$	CL1, CL2	80	—	ns
Clock rise time	$t_r$	CL1, CL2	—	30	ns
Clock fall time	$t_f$	CL1, CL2	—	30	ns
Data setup time	$t_{DS}$	D0 to D7, CL2	50	—	ns
Data hold time	$t_{DH}$	D0 to D7, CL2	50	—	ns
M setup time	$t_{MS}$	M, CL1	20	—	ns
M hold time	$t_{MH}$	M, CL1	20	—	ns
Output delay time 1	$t_{pd1}$	CL1, Y1 to Y320	—	1000	ns

**AC Characteristics 2 ( $V_{CC} = 4.5V$  to  $5.5V$ ,  $V_0-GND = 2.6$  to  $5.5V$ ,  $T_a = -30$  to  $+75^\circ C$ )**

Item	Symbol	Pins	Min	Max	Unit
Clock cycle time	$t_{CYC}$	CL2	125	—	ns
Clock high pulse width 1	$t_{CWH2}$	CL2	45	—	ns
Clock low pulse width 1	$t_{CWL2}$	CL2	45	—	ns
Clock high pulse width 2	$t_{CWH1}$	CL1	45	—	ns
Clock setup time	$t_{SCL}$	CL1, CL2	80	—	ns
Clock hold time	$t_{HCL}$	CL1, CL2	80	—	ns
Clock rise time	$t_r$	CL1, CL2	—	20	ns
Clock fall time	$t_f$	CL1, CL2	—	20	ns
Data setup time	$t_{DS}$	D0 to D7, CL2	20	—	ns
Data hold time	$t_{DH}$	D0 to D7, CL2	20	—	ns
M setup time	$t_{MS}$	M, CL1	20	—	ns
M hold time	$t_{MH}$	M, CL1	20	—	ns
Output delay time 1	$t_{pd1}$	CL1, Y1 to Y320	—	1000	ns

Notes: 1. A load must be 10 pF or less for EI/O connection between drivers.

2. For output delay time 1 and 2, connect the load circuit shown below.



# HD66130T

