HD66765

396-channel Segment Driver with Internal RAM for 4096-color Displays

HITACHI

Target Specification
Rev.0.1
January, 2001

Description

The HD66765, 396-channel segment driver LSI, displays 132RGB-by-176-dot graphics on STN displays in 4096 colors. It is for driving STN color LCD displays to a maximum of 132RGB by 176 dots, in combination with the HD66764 common driver. The HD66765's bit-operation functions, 16-bit high-speed bus interface, and high-speed RAM-write functions enable efficient data transfer and high-speed rewriting of data to the graphics RAM.

The HD66765 and HD66764 have various functions for reducing the power consumption of an LCD system. The HD66765 has a low-voltage operation (1.8 V min.) and an internal RAM to display a maximum of 132RGB-by-176-dot color, and the HD66764 has a step-up circuit to generate the LCD-drive voltage, a bleeder resistor for the drive interface with the LCD, and voltage-followers. Since the HD66765 incorporates a circuit that interfaces with the HD66764, it can set instructions for the HD66764. In addition, precise power control can be achieved by combining these hardware functions with software functions, such as a partial display that only requires a low drive-voltage duty, and standby and sleep modes. This LSI is suitable for any medium-sized or small portable battery-driven product requiring long-term driving capabilities, such as digital cellular phones supporting a WWW browser, bidirectional pagers, and small PDAs.

Features

- 132RGB x 176-dot graphics display LCD controller/driver for 4,096 STN colors (when HD66764 is used)
- Low-voltage drive and flickerless PWM grayscale drive
- 16-/8-bit high-speed bus interface and serial peripheral interface (SPI)
- High-speed burst-RAM write function
- Writing to a window-RAM address area by using a window-address function
- Bit-operation functions for graphics processing:
  - — Write-data mask function in bit units
  - — Logical operation in pixel unit and conditional write function

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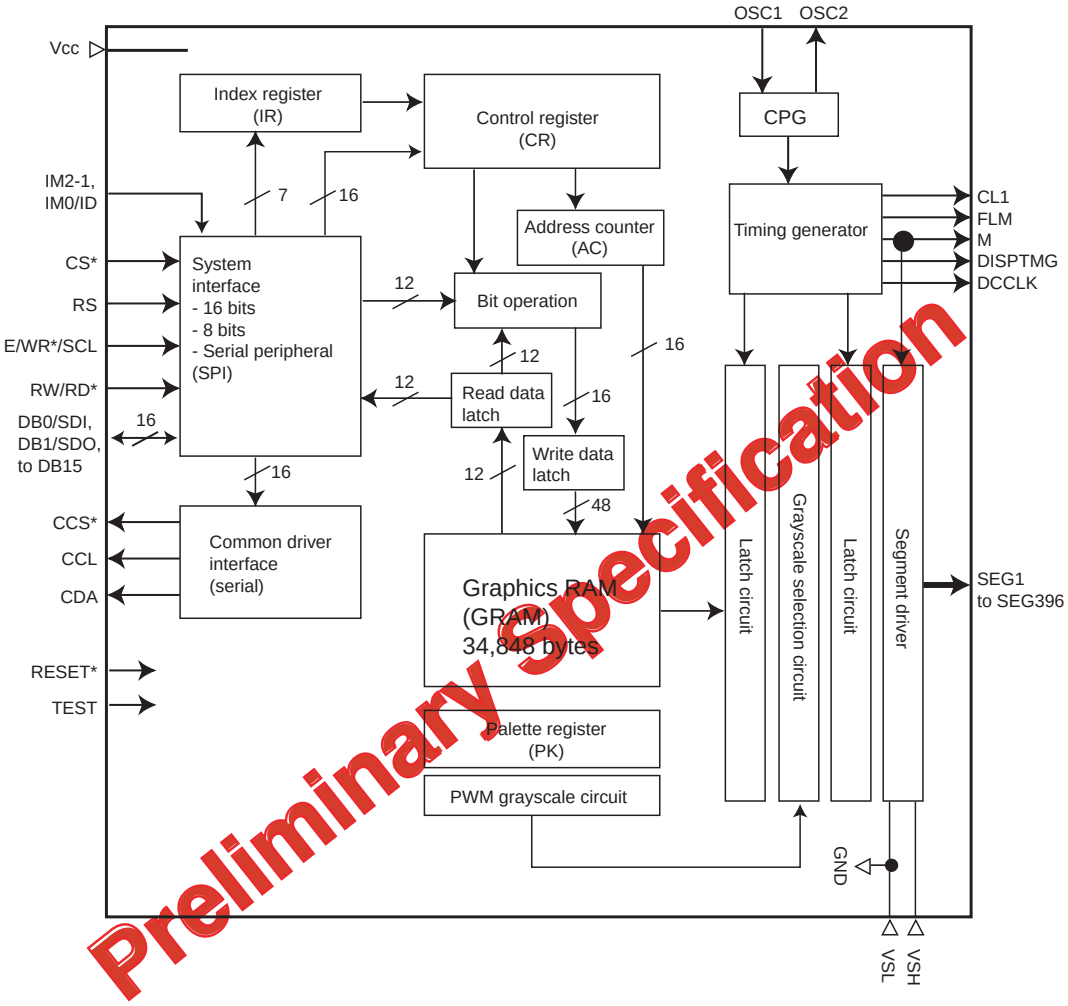
- Various color-display control functions:
  - 4,096 out of 13,824 possible colors can be displayed at the same time (grayscale palette included)
  - Vertical scroll display function in raster-row units
- Low-power operation supports:
  - Vcc = 1.8 to 3.6 V (low-voltage range)
  - VLCD = 2.0 to 4.0 V (liquid crystal drive voltage)
  - Power-save functions such as the standby mode and sleep mode
  - Partial LCD drive of two screens in any position
  - Programmable drive duty ratios (1/16–1/176) and bias values (1/4–1/13) displayed on LCD
  - Maximum 12-times step-up circuit for liquid crystal drive voltage (HD66764)
  - Voltage followers to decrease direct current flow in the LCD drive bleeder-resistors (HD66764)
  - 128-step contrast adjuster (HD66764)
- Built-in circuit for interfacing with the HD66764 common driver
- Maximum 132RGB-by-176-dot display in combination with the HD66764 common driver
- Internal RAM capacity: 34,848 bytes
- 396-segment liquid crystal display driver
- n-raster-row AC liquid-crystal drive (C-pattern waveform drive)
- Internal oscillation and hardware reset
- Shift change of segment driver

Type Number

Type Number	External Appearance
HD66765TB0	Bending TCP
HCD66765BP	Au-bump chip

HD66765 Block Diagram



HD66765 PAD Arrangement

- Chip size : 13.22mm x 3.85mm
- Chip thickness : 550um (typ.)
- PAD coordinate : PAD center
- Coordinate origine : Chip center

- Au bump size :

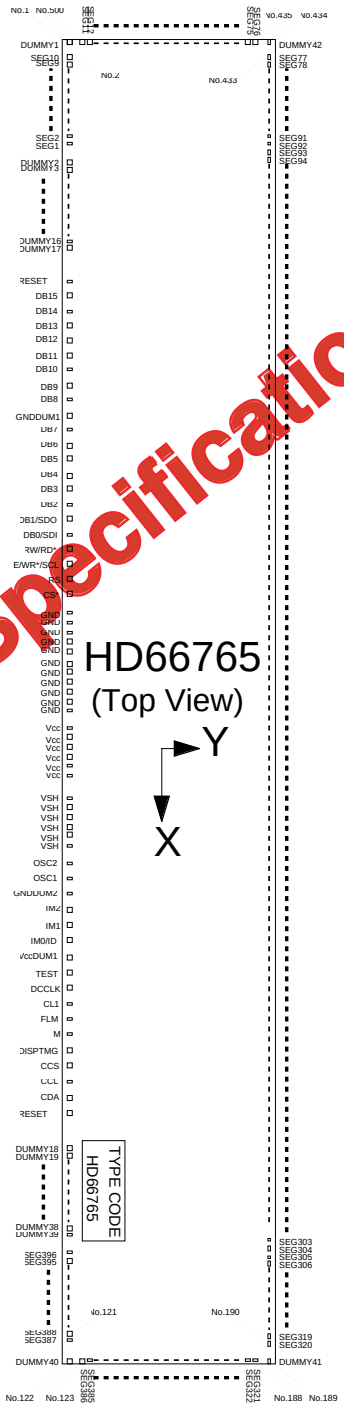
(1) 80um x 80 um
DUMMY1, DUMMY2-DUMMY39,
DUMMY40, DUMMY41, DUMMY42

(2) 35um x 80um
SEG304-SEG93

(3) 80um x 35um
SEG386-SEG321,
SEG76-SEG11

(4) 45um x 80um
SEG10-SEG1, SEG396-SEG387,
SEG320-SEG305, SEG92-SEG77

- Au bump pitch : Refer PAD coordinate
- Au bump height : 15um (typ.)



HD66765 PAD Coordinate

UNIT: μm Rev 0.1

No.	PAD Name	X	Y	No.	PAD Name	X	Y	No.	PAD Name	X	Y	No.	PAD Name	X	Y	No.	PAD Name	X	Y
1	DUMMY1	-6480	-1795	101	DUMMY29	4522	-1795	201	SEG309	5573	1795	301	SEG209	525	1795	401	SEG109	-4477	1795
2	SEG10	-6234	-1795	102	DUMMY30	4623	-1795	202	SEG308	5513	1795	302	SEG208	475	1795	402	SEG108	-4527	1795
3	SEG9	-6174	-1795	103	DUMMY31	4723	-1795	203	SEG307	5453	1795	303	SEG207	425	1795	403	SEG107	-4577	1795
4	SEG8	-6113	-1795	104	DUMMY32	4823	-1795	204	SEG306	5393	1795	304	SEG206	375	1795	404	SEG106	-4627	1795
5	SEG7	-6053	-1795	105	DUMMY33	4923	-1795	205	SEG305	5333	1795	305	SEG205	325	1795	405	SEG105	-4677	1795
6	SEG6	-5993	-1795	106	DUMMY34	5023	-1795	206	SEG304	5278	1795	306	SEG204	275	1795	406	SEG104	-4727	1795
7	SEG5	-5933	-1795	107	DUMMY35	5123	-1795	207	SEG303	5228	1795	307	SEG203	225	1795	407	SEG103	-4777	1795
8	SEG4	-5873	-1795	108	DUMMY36	5223	-1795	208	SEG302	5178	1795	308	SEG202	175	1795	408	SEG102	-4827	1795
9	SEG3	-5813	-1795	109	DUMMY37	5323	-1795	209	SEG301	5128	1795	309	SEG201	125	1795	409	SEG101	-4877	1795
10	SEG2	-5753	-1795	110	DUMMY38	5423	-1795	210	SEG300	5078	1795	310	SEG200	75	1795	410	SEG100	-4928	1795
11	SEG1	-5693	-1795	111	DUMMY39	5523	-1795	211	SEG299	5028	1795	311	SEG199	25	1795	411	SEG99	-4978	1795
12	DUMMY2	-5505	-1795	112	SEG396	5693	-1795	212	SEG298	4978	1795	312	SEG198	-25	1795	412	SEG98	-5028	1795
13	DUMMY3	-5405	-1795	113	SEG395	5753	-1795	213	SEG297	4928	1795	313	SEG197	-75	1795	413	SEG97	-5078	1795
14	DUMMY4	-5305	-1795	114	SEG394	5813	-1795	214	SEG296	4877	1795	314	SEG196	-125	1795	414	SEG96	-5128	1795
15	DUMMY5	-5205	-1795	115	SEG393	5873	-1795	215	SEG295	4827	1795	315	SEG195	-175	1795	415	SEG95	-5178	1795
16	DUMMY6	-5105	-1795	116	SEG392	5933	-1795	216	SEG294	4777	1795	316	SEG194	-225	1795	416	SEG94	-5228	1795
17	DUMMY7	-5005	-1795	117	SEG391	5993	-1795	217	SEG293	4727	1795	317	SEG193	-275	1795	417	SEG93	-5278	1795
18	DUMMY8	-4905	-1795	118	SEG390	6053	-1795	218	SEG292	4677	1795	318	SEG192	-325	1795	418	SEG92	-5333	1795
19	DUMMY9	-4805	-1795	119	SEG389	6113	-1795	219	SEG291	4627	1795	319	SEG191	-375	1795	419	SEG91	-5393	1795
20	DUMMY10	-4705	-1795	120	SEG388	6174	-1795	220	SEG290	4577	1795	320	SEG190	-425	1795	420	SEG90	-5453	1795
21	DUMMY11	-4605	-1795	121	SEG387	6234	-1795	221	SEG289	4527	1795	321	SEG189	-475	1795	421	SEG89	-5513	1795
22	DUMMY12	-4504	-1795	122	DUMMY40	6480	-1795	222	SEG288	4477	1795	322	SEG188	-525	1795	422	SEG88	-5573	1795
23	DUMMY13	-4404	-1795	123	SEG386	6480	-1626	223	SEG287	4427	1795	323	SEG187	-575	1795	423	SEG87	-5633	1795
24	DUMMY14	-4304	-1795	124	SEG385	6480	-1576	224	SEG286	4377	1795	324	SEG186	-625	1795	424	SEG86	-5693	1795
25	DUMMY15	-4204	-1795	125	SEG384	6480	-1526	225	SEG285	4327	1795	325	SEG185	-675	1795	425	SEG85	-5753	1795
26	DUMMY16	-4104	-1795	126	SEG383	6480	-1476	226	SEG284	4277	1795	326	SEG184	-725	1795	426	SEG84	-5813	1795
27	DUMMY17	-4004	-1795	127	SEG382	6480	-1426	227	SEG283	4227	1795	327	SEG183	-775	1795	427	SEG83	-5873	1795
28	RESET*	-3874	-1795	128	SEG381	6480	-1376	228	SEG282	4177	1795	328	SEG182	-825	1795	428	SEG82	-5933	1795
29	DB15	-3743	-1795	129	SEG380	6480	-1326	229	SEG281	4127	1795	329	SEG181	-875	1795	429	SEG81	-5993	1795
30	DB14	-3613	-1795	130	SEG379	6480	-1276	230	SEG280	4077	1795	330	SEG180	-925	1795	430	SEG80	-6053	1795
31	DB13	-3483	-1795	131	SEG378	6480	-1226	231	SEG279	4027	1795	331	SEG179	-975	1795	431	SEG79	-6113	1795
32	DB12	-3352	-1795	132	SEG377	6480	-1176	232	SEG278	3977	1795	332	SEG178	-1026	1795	432	SEG78	-6174	1795
33	DB11	-3222	-1795	133	SEG376	6480	-1126	233	SEG277	3927	1795	333	SEG177	-1076	1795	433	SEG77	-6234	1795
34	DB10	-3091	-1795	134	SEG375	6480	-1076	234	SEG276	3877	1795	334	SEG176	-1126	1795	434	DUMMY42	-6480	1795
35	DB9	-2961	-1795	135	SEG374	6480	-1026	235	SEG275	3827	1795	335	SEG175	-1176	1795	435	SEG76	-6480	1626
36	DB8	-2831	-1795	136	SEG373	6480	-975	236	SEG274	3777	1795	336	SEG174	-1226	1795	436	SEG75	-6480	1576
37	GNDDUM1	-2731	-1795	137	SEG372	6480	-925	237	SEG273	3727	1795	337	SEG173	-1276	1795	437	SEG74	-6480	1526
38	DB7	-2631	-1795	138	SEG371	6480	-875	238	SEG272	3677	1795	338	SEG172	-1326	1795	438	SEG73	-6480	1476
39	DB6	-2500	-1795	139	SEG370	6480	-825	239	SEG271	3627	1795	339	SEG171	-1376	1795	439	SEG72	-6480	1426
40	DB5	-2370	-1795	140	SEG369	6480	-775	240	SEG270	3577	1795	340	SEG170	-1426	1795	440	SEG71	-6480	1376
41	DB4	-2239	-1795	141	SEG368	6480	-725	241	SEG269	3527	1795	341	SEG169	-1476	1795	441	SEG70	-6480	1326
42	DB3	-2109	-1795	142	SEG367	6480	-675	242	SEG268	3477	1795	342	SEG168	-1526	1795	442	SEG69	-6480	1276
43	DB2	-1979	-1795	143	SEG366	6480	-625	243	SEG267	3427	1795	343	SEG167	-1576	1795	443	SEG68	-6480	1226
44	DB1/SDO	-1848	-1795	144	SEG365	6480	-575	244	SEG266	3377	1795	344	SEG166	-1626	1795	444	SEG67	-6480	1176
45	DB0/SDI	-1718	-1795	145	SEG364	6480	-525	245	SEG265	3327	1795	345	SEG165	-1676	1795	445	SEG66	-6480	1126
46	RW/RD*	-1587	-1795	146	SEG363	6480	-475	246	SEG264	3277	1795	346	SEG164	-1726	1795	446	SEG65	-6480	1076
47	E/WR*/SCL	-1457	-1795	147	SEG362	6480	-425	247	SEG263	3227	1795	347	SEG163	-1776	1795	447	SEG64	-6480	1026
48	RS	-1327	-1795	148	SEG361	6480	-375	248	SEG262	3177	1795	348	SEG162	-1826	1795	448	SEG63	-6480	975
49	CS*	-1196	-1795	149	SEG360	6480	-325	249	SEG261	3127	1795	349	SEG161	-1876	1795	449	SEG62	-6480	925
50	GND	-1066	-1795	150	SEG359	6480	-275	250	SEG260	3077	1795	350	SEG160	-1926	1795	450	SEG61	-6480	875
51	GND	-966	-1795	151	SEG358	6480	-225	251	SEG259	3027	1795	351	SEG159	-1976	1795	451	SEG60	-6480	825
52	GND	-866	-1795	152	SEG357	6480	-175	252	SEG258	2977	1795	352	SEG158	-2026	1795	452	SEG59	-6480	775
53	GND	-766	-1795	153	SEG356	6480	-125	253	SEG257	2926	1795	353	SEG157	-2076	1795	453	SEG58	-6480	725
54	GND	-666	-1795	154	SEG355	6480	-75	254	SEG256	2876	1795	354	SEG156	-2126	1795	454	SEG57	-6480	675
55	GND	-565	-1795	155	SEG354	6480	-25	255	SEG255	2826	1795	355	SEG155	-2176	1795	455	SEG56	-6480	625
56	GND	-465	-1795	156	SEG353	6480	25	256	SEG254	2776	1795	356	SEG154	-2226	1795	456	SEG55	-6480	575
57	GND	-365	-1795	157	SEG352	6480	75	257	SEG253	2726	1795	357	SEG153	-2276	1795	457	SEG54	-6480	525
58	GND	-265	-1795	158	SEG351	6480	125	258	SEG252	2676	1795	358	SEG152	-2326	1795	458	SEG53	-6480	475
59	GND	-165	-1795	159	SEG350	6480	175	259	SEG251	2626	1795	359	SEG151	-2376	1795	459	SEG52	-6480	425
60	GND	-65	-1795	160	SEG349	6480	225	260	SEG250	2576	1795	360	SEG150	-2426	1795	460	SEG51	-6480	375
61	VCC	65	-1795	161	SEG348	6480	275	261	SEG249	2526	1795	361	SEG149	-2476	1795	461	SEG50	-6480	325
62	VCC	165	-1795	162	SEG347	6480	325	262	SEG248	2476	1795	362	SEG148	-2526	1795	462	SEG49	-6480	275
63	VCC	265	-1795	163	SEG346	6480	375	263	SEG247	2426	1795	363	SEG147	-2576	1795	463	SEG48	-6480	225
64	VCC	365	-1795	164	SEG345	6480	425	264	SEG246	2376	1795	364	SEG146	-2626	1795	464	SEG47	-6480	175
65	VCC	465	-1795	165	SEG344	6480	475	265	SEG245	2326	1795	365	SEG145	-2676	1795	465	SEG46	-6480	125
66	VCC	565	-1795	166	SEG343	6480	525	266	SEG244	2276	1795	366	SEG144	-2726	1795	466	SEG45	-6480	75
67	VSH	696	-1795	167	SEG342	6480	575	267	SEG243	2226	1795	367	SEG143	-2776	1795	467	SEG44	-6480	25
68	VSH	796	-1795	168	SEG341	6480	625	268	SEG242	2176	1795	368	SEG142	-2826	1795	468	SEG43	-6480	-25
69	VSH	896	-1795	169	SEG340	6480	675	269	SEG241	2126	1795	369	SEG141	-2876	1795	469	SEG42	-6480	-75
70	VSH	996	-1795	170	SEG339	6480	725	270	SEG240	2076	1795	370	SEG140	-2926	1795	470	SEG41	-6480	-125
71	VSH	1096	-1795	171	SEG338	6480	775	271	SEG239	2026	1795	371	SEG139	-2977	1795	471	SEG40	-6480	-175
72	VSH	1196	-1795	172	SEG337	6480	825	272	SEG238	1976	1795	372	SEG138	-3027	1795	472	SEG39	-6480	-225
73	OSC2	1327	-1795	173	SEG336	6480	875	273	SEG237	1926	1795	373	SEG137	-3077	1795	473	SEG38	-6480	-275
74	OSC1	1457	-1795	174	SEG335	6480	925	274	SEG236	1876	1795	374	SEG136	-3127	1795	474	SEG37	-6480	-325
75	GNDDUM2	1557	-1795	175	SEG334	6480	975	275	SEG235	1826	1795	375	SEG135	-3177	1795	475	SEG36	-6480	-375
76	IM2	1657	-1795	176	SEG333	6480	1026	276	SEG234	1776	1795	376	SEG134	-3227	1795	476	SEG35	-6480	-425
77	IM1	1787	-1795	177	SEG332	6480	1076	277	SEG233	1726	1795	377	SEG133	-3277	1795	477	SEG34	-6480	-475
78	IM0/ID	1918	-1795	178	SEG331	6480	1126	278	SEG232	1676	1795	378	SEG132	-3327	1795	478	SEG33	-6480	-525
79	VCCDUM1	2018	-1795	179	SEG330	6480	1176	279	SEG231	1626	1795	379	SEG131	-3377	1795	479	SEG32	-6480	-575
80	TEST	2118	-1795	180	SEG329	6480	1226	280	SEG230	1576	1795	380	SEG130	-3427	1795	480	SEG31	-6480	-625
81	DCCLK	2248	-1795	181	SEG328	6480	1276	281	SEG229	1526	1795	381	SEG129	-3477	1795	481	SEG30	-6480	-675
82	CL1	2379	-1795	182	SEG327	6480	1326	282	SEG228	1476	1795	382	SEG128	-3527	1795	482	SEG29	-6480	-725
83	FLM	2509	-1795	183	SEG326	6480	1376	283	SEG227	1426	1795	383	SEG127	-3577	1795	483	SEG28	-6480	-775
84	M	2640	-1795	184	SEG325	6480	1426	284	SEG226	1376	1795	384	SEG126	-3627	1795	484	SEG27	-6480	-825
85	DISPTMG	2770	-1795	185	SEG324	6480	1476	285	SEG225	1326	1795	385	SEG125	-3677	1795	485	SEG26	-6480	-875
86	CCS	2900	-1795	186	SEG323	6480	1526	286	SEG224	1276	1795	386	SEG124	-3727	1795	486	SEG25	-6480	-925
87	CCL	3031	-1795	187	SEG322	6480	1576	287	SEG223	1226	1795	387	SEG123	-3777	1795	487	SEG24	-6480	-975
88	CDA	3161	-1795	188	SEG321	6480	1626	288	SEG222	1176	1795	388	SEG122	-3827	1795	488	SEG23	-6480	-1026
89	RESET*	3292	-1795	189	DUMMY41	6480	1795	289	SEG221	1126	1795	389	SEG121	-3877	1795	489	SEG22	-6480	-1076
90	DUMMY18	3422	-1795	190	SEG320	6234	1795	290	SEG220	1076	1795	390	SEG120	-3927	1795	490	SEG21	-6480	-1126
91	DUMMY19	3522	-1795	191	SEG319	6174	1795	291	SEG219	1026	1795	391	SEG119	-3977	1795	491	SEG20	-6480	-1176
92	DUMMY20	3622	-1795	192	SEG318	6113	1795	292	SEG218	975	1795	392	SEG118	-4027	1795	492	SEG19	-6480	-1226
93	DUMMY21	3722	-1795	193	SEG317	6053	1795	293	SEG217	925	1795	393	SEG117	-4077	1795	493	SEG18	-6480	-1276
94	DUMMY22	3822	-1795	194	SEG316	5993	1795	294	SEG216	875	1795	394	SEG116	-4127	1795	494	SEG17	-6480	-1326
95	DUMMY23	3922	-1795	195	SEG315	5933	1795	295	SEG215	825	1795	395	SEG115	-4177	1795	495	SEG16	-6480	-1376
96	DUMMY24	4022	-1795	196	SEG314	5873	1795	296	SEG214	775	1795	396	SEG114	-4227	1795	496	SEG15	-6480	-1426
97	DUMMY25	4122	-1795	197	SEG313	5813	1795	297	SEG213	725	1795	397	SEG113	-4277	1795	497	SEG14	-6480	-1476
98	DUMMY26	4222	-1795	198	SEG312	5753	1795	298	SEG212	675	1795	398	SEG112	-4327	1795	498	SEG13	-6480	-1526
99	DUMMY27	4322	-1795	199	SEG311	5693	1795	299	SEG211	625	1795	399	SEG111	-4377	1795	499	SEG12	-6480	-1576
100	DUMMY28	4422	-1795	200	SEG310	5633	1795	300	SEG210	575	1795	400	SEG110	-4427	1795	500	SEG11	-6480	-1626

Pin Functions

Table 1 Pin Functional Description

Signals	Number of Pins	I/O	Connected to	Functions
IM2-1, IM0/ID	3	I	GND or V_{CC}	Selects the MPU interface mode: IM2 IM1 IM0/ID MPU interface mode GND GND GND 68-system 16-bit bus interface GND GND Vcc 68-system 8-bit bus interface GND Vcc GND 80-system 16-bit bus interface GND Vcc Vcc 80-system 8-bit bus interface Vcc GND ID Serial peripheral interface (SPI) When a serial interface is selected, the IM0 pin is used as the ID setting for a device code.
CS*	1	I	MPU	Selects the HD66765: Low: HD66765 is selected and can be accessed High: HD66765 is not selected and cannot be accessed Must be fixed at GND level when not in use.
RS	1	I	MPU	Selects the register. Low: Index/status High: Control
E/WR*/SCL	1	I	MPU	For a 68-system bus interface, serves as an enable signal to activate data read/write operation. For an 80-system bus interface, serves as a write strobe signal and writes data at the low level. For a synchronous clock interface, serves as the synchronous clock signal.
RW/RD*	1	I	MPU	For a 68-system bus interface, serves as a signal to select data read/write operation. Low: Write High: Read For an 80-system bus interface, serves as a read strobe signal and reads data at the low level.
DB0/SDI	1	I/O	MPU	Serves as a 16-bit bidirectional data bus. For an 8-bit bus interface, data transfer uses DB15-DB8; fix unused DB7-DB0 to the Vcc or GND level. For a clock-synchronous serial interface, serves as the serial data input pin (SDI). The input level is read on the rising edge of the SCL signal.

Table 1 Pin Functional Description (cont)

Signals	Number of Pins	I/O	Connected to	Functions
DB1/SDO	1	I/O	MCU	Serves as a 16-bit bidirectional data bus. For an 8-bit bus interface, data transfer uses DB15-DB8; fix unused DB7-DB0 to the Vcc or GND level. For a clock-synchronous serial interface, serves as a serial data output pin (SDO). Successive bit values are output on the falling edge of the SCL signal.
DB2-DB15	14	I/O	MPU	Serves as a 16-bit bidirectional data bus. For an 8-bit bus interface, data transfer uses DB15-DB8; fix unused DB7-DB0 to the Vcc or GND level.
SEG1–SEG396	396	O	LCD	Output signals for segment drive. In the display-off period (D1–0 = 00, 01) or standby mode (STB = 1), all pins output GND level. The SGS bit can change the shift direction of the segment signal. For example, if SGS = 0, RAM address 0000 is output from SEG1. If SGS = 1, it is output from SEG396. SEG1, SEG4, SEG7, ... display red (R), SEG2, SEG5, SEG8, ... display green (G), and SEG3, SEG6, SEG9, ... display blue (B) (SGS = 0).
CL1	1	O	HD66764	The one-raster-row-cycle pulse is output.
M	1	O	HD66764	The AC-cycle signal is output.
FLM	1	O	HD66764	The frame-start pulse is output.
DISPTMG	1	O	HD66764	Outputs the display period signal.
DCCLK	1	O	HD66764	Outputs clocks for the step-up.
CCL	1	O	HD66764	Clock signal for a serial transfer of register setting values to the common driver. Data is output on the falling edge of this clock.
CDA	1	O	HD66764	Data signal for serial transfer as register setting values to the common driver.
CCS*	1	O	HD66764	Chip-select for the HD66764. Low: the HD66764 is selected and can receive a serial transfer. High: the HD66764 is not selected and cannot receive a serial transfer.
VSH	1	I	HD66764	Input for the LCD-drive voltage for the segment driver, which can be provided by the HD66764's on-chip power supply. VSH ≤ 4.0 V
V_{CC}, GND	2	—	Power supply	V_{CC}: + 1.8 V to + 3.6 V; GND (logic): 0

Table 1 Pin Functional Description (cont)

Signals	Number of Pins	I/O	Connected to	Functions
OSC1, OSC2	2	I or O	Oscillation-resistor	Connect an external resistor for R-C oscillation. When providing clocks from outside, open OSC2.
RESET*	1	I	MPU or external R-C circuit	Reset pin. Initializes the LSI when low. Must be reset after power-on.
VccDUM		O	Input pins	Outputs the internal V_{CC} level; shorting this pin sets the adjacent input pin to the V_{CC} level.
GNDDUM		O	Input pins	Outputs the internal GND level; shorting this pin sets the adjacent input pin to the GND level.
Dummy		—	—	Dummy pad. Must be left disconnected.
TEST	1	I	GND	Test pin. Must be fixed at GND level.

Block Function Description

System Interface

The HD66765 has five high-speed system interfaces: an 80-system 16-bit/8-bit bus, a 68-system 16-bit/8-bit bus, and a serial peripheral (SPI: Serial Peripheral Interface port). The interface mode is selected by the IM2-0 pins.

The HD66765 has three 16-bit registers: an index register (IR), a write data register (WDR), and a read data register (RDR). The IR stores index information from the control registers and the GRAM. The WDR temporarily stores data to be written into control registers and the GRAM, and the RDR temporarily stores data read from the GRAM. Data written into the GRAM from the MPU is first written into the WDR and then is automatically written into the GRAM by internal operation. Data is read through the RDR when reading from the GRAM, and the first read data is invalid and the second and the following data are normal. When a logic operation is performed inside of the HD66765 by using the display data set in the GRAM and the data written from the MPU, the data read through the RDR is used. Accordingly, the MPU does not need to read data twice nor to fetch the read data into the MPU. This enables high-speed processing.

Execution time for instruction excluding oscillation start is 0 clock cycle and instructions can be written in succession.

Table 2 Register Selection (8/16 Parallel Interface)

80-system Bus		68-system Bus		
WR	**RD**	**R/W**	**RS**	**Operations**
0	1	0	0	Writes indexes into IR
1	0	1	0	Reads internal status
0	1	0	1	Writes into control registers and GRAM through WDR
1	0	1	1	Reads from GRAM through RDR

Table 3 Register Selection (Serial Peripheral Interface)

Start bytes		
R/W Bits	**RS Bits**	**Operations**
0	0	Writes indexes into IR
1	0	Reads internal status
0	1	Writes into control registers and GRAM through WDR
1	1	Reads from GRAM through RDR

Bit Operation

The HD66765 supports the following functions: a write data mask function that selects and writes data into the GRAM in bit units, and a logic operation function that performs logic operations or conditional determination on the display data set in the GRAM and writes into the GRAM. With the 16-bit bus interface, these functions can greatly reduce the processing loads of the MPU graphics software and can rewrite the display data in the GRAM at high speed. For details, see the Graphics Operation Function section.

Address Counter (AC)

The address counter (AC) assigns addresses to the GRAM. When an address set instruction is written into the IR, the address information is sent from the IR to the AC.

After writing into the GRAM, the AC is automatically incremented by 1 (or decremented by 1). After reading from the data, the AC is not updated. A window address function allows for data to be written only to a window area specified by GRAM.

Graphics RAM (GRAM)

The graphics RAM (GRAM) has eight bits/pixel and stores the bit-pattern data of 132 x 176 bytes.

PWM Grayscale Circuit

The PWM grayscale circuit generates a PWM signal that corresponds to the grayscale levels as specified in the grayscale palette register. Any 4096 out of 13,824 possible colors can be displayed at the same time. For details, see the Grayscale Palette section.

Grayscale Selection Circuit

The grayscale selection circuit reads data from the GRAM and controls the signal generated in the PWM grayscale circuit. PWM (pulse width modulation) is used to control each color in the display. For details, see the Grayscale Palette section.

Timing Generator

The timing generator generates timing signals for the operation of internal circuits such as the GRAM. The RAM read timing for display and internal operation timing by MPU access are generated separately to avoid interference with one another. The timing generator generates the interface signals (M, FLM, CL1, DISPTMG, and DCCLK) for the common driver.

Oscillation Circuit (OSC)

The HD66765 can provide R-C oscillation simply through the addition of an external oscillation-resistor between the OSC1 and OSC2 pins. The appropriate oscillation frequency for operating voltage, display size, and frame frequency can be obtained by adjusting the external-resistor value. Clock pulses can also be supplied externally. Since R-C oscillation stops during the standby mode, current consumption can be reduced. For details, see the Oscillation Circuit section.

Liquid Crystal Display Driver Circuit

The liquid crystal display driver circuit consists of 396 segment signal drivers (SEG1 to SEG396).

Display pattern data is latched when 396-bit data has arrived. The latched data then enables the segment signal drivers to generate drive waveform outputs. The shift direction of 396-bit data can be changed by the SGS bit by selecting an appropriate direction for the device mounting configuration.

When multiplexing drive is not used, or during standby mode, all of the common and segment signal drivers listed above, and the common drivers from the HD66764, output the GND level, halting the display.

Interface with Common Driver

A serial interface circuit provides an interface with the HD66764 common driver. When sending an instruction setting from the HD66765 to a common driver, a register setting value from within the HD66765 is transferred via the serial interface circuit. A transfer is started by setting a serial transfer enable in the HD66765. However, transfer to and reading from the common driver are not possible during standby. For details, see the Common Serial Transfer section.

Table Relationship between GRAM address and display position (SGS=0)

SEG/COM pins		SEG1	SEG2	SEG3	SEG4	SEG5	SEG6	• • • • •	SEG391	SEG392	SEG393	SEG394	SEG395	SEG396
CMS=0	CMS=1	DB 11 • • • • • • DB 0			DB 11 • • • • • • DB 0				DB 11 • • • • • • DB 0			DB 11 • • • • • • DB 0		
COM1	COM176	"0000"H			"0001"H			• • • • •	"0082"H			"0083"H		
COM2	COM175	"0100"H			"0101"H			• • • • •	"0182"H			"0183"H		
COM3	COM174	"0200"H			"0201"H			• • • • •	"0282"H			"0283"H		
COM4	COM173	"0300"H			"0301"H			• • • • •	"0382"H			"0383"H		
COM5	COM172	"0400"H			"0401"H			• • • • •	"0482"H			"0483"H		
COM6	COM171	"0500"H			"0501"H			• • • • •	"0582"H			"0583"H		
COM7	COM170	"0600"H			"0601"H			• • • • •	"0682"H			"0683"H		
COM8	COM169	"0700"H			"0701"H			• • • • •	"0782"H			"0783"H		
COM9	COM168	"0800"H			"0801"H			• • • • •	"0882"H			"0883"H		
COM10	COM167	"0900"H			"0901"H			• • • • •	"0982"H			"0983"H		
COM11	COM166	"0A00"H			"0A01"H			• • • • •	"0A82"H			"0A83"H		
COM12	COM165	"0B00"H			"0B01"H			• • • • •	"0B82"H			"0B83"H		
COM13	COM164	"0C00"H			"0C01"H			• • • • •	"0C82"H			"0C83"H		
COM14	COM163	"0D00"H			"0D01"H			• • • • •	"0D82"H			"0D83"H		
COM15	COM162	"0E00"H			"0E01"H			• • • • •	"0E82"H			"0E83"H		
COM16	COM161	"0F00"H			"0F01"H			• • • • •	"0F82"H			"0F83"H		
COM17	COM160	"1000"H			"1001"H			• • • • •	"1082"H			"1083"H		
COM18	COM159	"1100"H			"1101"H			• • • • •	"1182"H			"1183"H		
COM19	COM158	"1200"H			"1201"H			• • • • •	"1282"H			"1283"H		
COM20	COM157	"1300"H			"1301"H			• • • • •	"1382"H			"1383"H		
⋮	⋮	⋮			⋮				⋮			⋮		
COM169	COM8	"A800"H			"A801"H			• • • • •	"A882"H			"A883"H		
COM170	COM7	"A900"H			"A901"H			• • • • •	"A982"H			"A983"H		
COM171	COM6	"AA00"H			"AA01"H			• • • • •	"AA82"H			"AA83"H		
COM172	COM5	"AB00"H			"AB01"H			• • • • •	"AB82"H			"AB83"H		
COM173	COM4	"AC00"H			"AC01"H			• • • • •	"AC82"H			"AC83"H		
COM174	COM3	"AD00"H			"AD01"H			• • • • •	"AD82"H			"AD83"H		
COM175	COM2	"AE00"H			"AE01"H			• • • • •	"AE82"H			"AE83"H		
COM176	COM1	"AF00"H			"AF01"H			• • • • •	"AF82"H			"AF83"H		

Table Relationship between GRAM data and output pin (SGS=0)

GRAM data	DB 15	DB 14	DB 13	DB 12	DB 11	DB 10	DB 9	DB 8	DB 7	DB 6	DB 5	DB 4	DB 3	DB 2	DB 1	DB 0
Selected palette	N/A				PK palette				PK palette				PK palette			
Output pin	N/A				SEG (3n+1)				SEG (3n+2)				SEG (3n+3)			

n = Lower 6-bits address (0 to 131)

Table Relationship between GRAM address and display position (SGS=1)

SEG/COM pins		SEG1	SEG2	SEG3	SEG4	SEG5	SEG6	• • • • •	SEG391	SEG392	SEG393	SEG394	SEG395	SEG396
CMS=0	CMS=1	DB 11 • • • DB 0			DB 11 • • • DB 0			• • • • •	DB 11 • • • DB 0			DB 11 • • • DB 0		
COM1	COM176	"0083"H			"0082"H			• • • • •	"0001"H			"0000"H		
COM2	COM175	"0183"H			"0182"H			• • • • •	"0101"H			"0100"H		
COM3	COM174	"0283"H			"0282"H			• • • • •	"0201"H			"0200"H		
COM4	COM173	"0383"H			"0382"H			• • • • •	"0301"H			"0300"H		
COM5	COM172	"0483"H			"0482"H			• • • • •	"0401"H			"0400"H		
COM6	COM171	"0583"H			"0582"H			• • • • •	"0501"H			"0500"H		
COM7	COM170	"0683"H			"0682"H			• • • • •	"0601"H			"0600"H		
COM8	COM169	"0783"H			"0782"H			• • • • •	"0701"H			"0700"H		
COM9	COM168	"0883"H			"0882"H			• • • • •	"0801"H			"0800"H		
COM10	COM167	"0983"H			"0982"H			• • • • •	"0901"H			"0900"H		
COM11	COM166	"0A83"H			"0A82"H			• • • • •	"0A01"H			"0A00"H		
COM12	COM165	"0B83"H			"0B82"H			• • • • •	"0B01"H			"0B00"H		
COM13	COM164	"0C83"H			"0C82"H			• • • • •	"0C01"H			"0C00"H		
COM14	COM163	"0D83"H			"0D82"H			• • • • •	"0D01"H			"0D00"H		
COM15	COM162	"0E83"H			"0E82"H			• • • • •	"0E01"H			"0E00"H		
COM16	COM161	"0F83"H			"0F82"H			• • • • •	"0F01"H			"0F00"H		
COM17	COM160	"1083"H			"1082"H			• • • • •	"1001"H			"1000"H		
COM18	COM159	"1183"H			"1182"H			• • • • •	"1101"H			"1100"H		
COM19	COM158	"1283"H			"1282"H			• • • • •	"1201"H			"1200"H		
COM20	COM157	"1383"H			"1382"H			• • • • •	"1301"H			"1300"H		
⋮	⋮	⋮			⋮				⋮			⋮		
COM169	COM8	"A883"H			"A882"H			• • • • •	"A801"H			"A800"H		
COM170	COM7	"A983"H			"A982"H			• • • • •	"A901"H			"A900"H		
COM171	COM6	"AA83"H			"AA82"H			• • • • •	"AA01"H			"AA00"H		
COM172	COM5	"AB83"H			"AB82"H			• • • • •	"AB01"H			"AB00"H		
COM173	COM4	"AC83"H			"AC82"H			• • • • •	"AC01"H			"AC00"H		
COM174	COM3	"AD83"H			"AD82"H			• • • • •	"AD01"H			"AD00"H		
COM175	COM2	"AE83"H			"AE82"H			• • • • •	"AE01"H			"AE00"H		
COM176	COM1	"AF83"H			"AF82"H			• • • • •	"AF01"H			"AF00"H		

Table Relationship between GRAM data and output pin (SGS=1)

GRAM data	DB 15	DB 14	DB 13	DB 12	DB 11	DB 10	DB 9	DB 8	DB 7	DB 6	DB 5	DB 4	DB 3	DB 2	DB 1	DB 0
Selected palette	N/A				PK palette				PK palette				PK palette			
Output pin	N/A				SEG (396n-3n)				SEG (395-3n)				SEG (394-3n)			

n = Lower 6-bits address (0 to 131)

Instructions

Outline

The HD66765 uses the 16-bit bus architecture. Before the internal operation of the HD66765 starts, control information is temporarily stored in the registers described below to allow high-speed interfacing with a high-performance microcomputer. The internal operation of the HD66765 is determined by signals sent from the microcomputer. These signals, which include the register selection signal (RS), the read/write signal (R/W), and the data bus signals (DB15 to DB0), make up the HD66765 instructions. There are nine categories of instructions that:

- Specify the index
- Read the status
- Control the display
- Control power management
- Process the graphics data
- Set internal GRAM addresses
- Transfer data to and from the internal GRAM
- Set grayscale level for the internal grayscale palette table
- Interface with the common driver

Normally, instructions that write data are used the most. However, an auto-update of internal GRAM addresses after each data write can lighten the microcomputer program load.

Because instructions are executed in 0 cycles, they can be written in succession.

Instruction Descriptions

Index

The index instruction specifies the RAM control indexes (R00h to R37h). It sets the register number in the range of 00000 to 110111 in binary form. However, R40 to R44 are disabled since they are test registers.

R/W	RS	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
W	0	*	*	*	*	*	*	*	*	*	ID6	ID5	ID4	ID3	ID2	ID1	ID0

Figure 1 Index Instruction

Status Read

The status read instruction reads the internal status of the HD66765.

L7–0: Indicate the driving raster-row position where the liquid crystal display is being driven.

C6–0: Read the contrast setting values (CT6–0).

R/W	RS	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
R	0	L7	L6	L5	L4	L3	L2	L1	L0	0	C6	C5	C4	C3	C2	C1	C0

Figure 2 Status Read Instruction

Start Oscillation (R00h)

The start oscillation instruction restarts the oscillator from the halt state in the standby mode. After issuing this instruction, wait at least 10 ms for oscillation to stabilize before issuing the next instruction. (See the Standby Mode section.)

If this register is read forcibly, *765H is read.

R/W	RS	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
W	1	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	1
R	1	0	0	0	0	0	1	1	1	0	1	1	0	0	1	0	1

Figure 3 Start Oscillation Instruction

Driver Output Control (R01h)

R/W	RS	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
W	1	0	0	0	0	0	0	CMS	SGS	0	0	0	NL4	NL3	NL2	NL1	NL0

Figure 4 Driver Output Control Instruction

CMS: Selects the output shift direction of a common driver. When CMS = 0, COM1 shifts to COM176. When CMS = 1, COM176 shifts to COM1.

SGS: Selects the output shift direction of a segment. When SGS = 0, SEG1 shifts to SEG396 and <R><G><B> color is assigned from SEG1. When SGS = 1, SEG396 shifts to SEG1 and <R><G><B> color is assigned from SEG396. Re-write to the RAM when intending to change the SGS bit.

Note: The CMS bit is for setting the common driver. Control according to the bit's value is executed by the common driver. For details, see the data sheet for the common driver.

NL4–0: Specify the LCD drive duty ratio. The duty ratio can be adjusted for every eight raster-rows. GRAM address mapping does not depend on the setting value of the drive duty ratio.

Table 8 NL Bits and Drive Duty

NL4	NL3	NL2	NL1	NL0	Display Size	LCD Drive Duty	Common Driver Used
0	0	0	0	0	Setting disabled	Setting disabled	Setting disabled
0	0	0	0	1	396 x 16 dots	1/16 Duty	COM1–COM16
0	0	0	1	0	396 x 24 dots	1/24 Duty	COM1–COM24
0	0	0	1	1	396 x 32 dots	1/32 Duty	COM1–COM32
0	0	1	0	0	396 x 40 dots	1/40 Duty	COM1–COM40
0	0	1	0	1	396 x 48 dots	1/48 Duty	COM1–COM48
0	0	1	1	0	396 x 56 dots	1/56 Duty	COM1–COM56
0	0	1	1	1	396 x 64 dots	1/64 Duty	COM1–COM64
0	1	0	0	0	396 x 72 dots	1/72 Duty	COM1–COM72
0	1	0	0	1	396 x 80 dots	1/80 Duty	COM1–COM80
0	1	0	1	0	396 x 88 dots	1/88 Duty	COM1–COM88
0	1	0	1	1	396 x 96 dots	1/96 Duty	COM1–COM96
0	1	1	0	0	396 x 104 dots	1/104 Duty	COM1–COM104
0	1	1	0	1	396 x 112 dots	1/112 Duty	COM1–COM112
0	1	1	1	0	396 x 120 dots	1/120 Duty	COM1–COM120
0	1	1	1	1	396 x 128 dots	1/128 Duty	COM1–COM128
1	0	0	0	0	396 x 136 dots	1/136 Duty	COM1–COM136
1	0	0	0	1	396 x 144 dots	1/144 Duty	COM1–COM144
1	0	0	1	0	396 x 152 dots	1/152 Duty	COM1–COM152
1	0	0	1	1	396 x 160 dots	1/160 Duty	COM1–COM160
1	0	1	0	0	396 x 168 dots	1/168 Duty	COM1–COM168
1	0	1	0	1	396 x 176 dots	1/176 Duty	COM1–COM176

LCD-Driving-Waveform Control (R02h)

R/W	RS	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
W	1	0	0	0	0	0	0	B/C	EOR	0	0	NW5	NW4	NW3	NW2	NW1	NW0

Figure 5 LCD-Driving-Waveform Control Instruction

B/C: When B/C = 0, a B-pattern waveform is generated and alternates in every frame for LCD drive. When B/C = 1, a C-pattern waveform is generated and alternates in each raster-row specified by bits EOR and NW4–NW0 in the LCD-driving-waveform control register. For details, see the n-raster-row Reversed AC Drive section.

EOR: When the C-pattern waveform is set (B/C = 1) and EOR = 1, the odd/even frame-select signals and the n-raster-row reversed signals are EORed for alternating drive. EOR is used when the LCD is not alternated by combining the set values of the LCD drive duty ratio and the n raster-row. For details, see the n-raster-row Reversed AC Drive section.

NW5–0: Specify the number of raster-rows n that will alternate at the C-pattern waveform setting (B/C = 1). NW4–NW0 alternate for every set value + 1 raster-row, and the first to the 64th raster-rows can be selected.

Power Control 1 (R03h)

Power Control 2 (R0Ch)

R/W	RS	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
W	1	0	BS2	BS1	BS0	BT3	BT2	BT1	BT0	0	DC2	DC1	DC0	AP1	AP0	SLP	STB
W	1	0	0	0	0	0	0	0	0	0	0	0	0	0	VC2	VC1	VC0

Figure 6 Power Control Instruction

BS2–0: The LCD drive bias value is set. The LCD drive bias value can be selected according to its drive duty ratio and voltage.

BT3–0: The output factor of step-up is switched. The LCD drive voltage level can be selected according to its drive duty ratio and bias. Lower amplification of the step-up circuit consumes less current.

DC2–0: The operating frequency in the step-up circuit is selected. When the step-up operating frequency is high, the driving ability of the step-up circuit and the display quality become high, but the current consumption is increased. Adjust the frequency considering the display quality and the current consumption.

AP1–0: The amount of fixed current from the fixed current source in the operational amplifier for the LCD is adjusted. When the amount of fixed current is large, the LCD driving ability and the display quality become high, but the current consumption is increased. Adjust the fixed current considering the display quality and the current consumption.

During no display, when AP1–0 = 00, the current consumption can be reduced by ending the operational amplifier and step-up circuit operation.

VC2-0: Sets an adjustment factor for the Vci voltage (VC2-0).

SLP: When SLP = 1, the HD66765 enters the sleep mode, where the internal display operations are halted except for the R-C oscillator, thus reducing current consumption. Only the following instructions can be executed during the sleep mode.

Power control (BS2–0, BT3–0, DC2–0, AP1–0, SLP, and STB bits)
Common interface control (TE, IDX)

During the sleep mode, the other GRAM data and instructions cannot be updated although they are retained.

Note: BS2-0, BT3-0, DC2-0, AP1-0, VC2-0 and SLP bits are for setting the common driver. Control according to the bits' values is executed by the common driver. For details, see the data sheet for the common driver.

STB: When STB = 1, the HD66765 enters the standby mode, where display operation completely stops, halting all the internal operations including the internal R-C oscillator. Further, no external clock pulses are supplied. For details, see the Standby Mode section.

Only the following instructions can be executed during the standby mode.

a. Standby mode cancel (STB = 0)
b. Start oscillation

During the standby mode, the GRAM data and instructions may be lost. To prevent this, they must be set again after the standby mode is canceled. Serial transfer to the common driver is not possible when it is in standby mode. Transfer the data again after it has been released from standby mode.

Contrast Control (R04h)

R/W	RS	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
W	1	0	0	0	0	VR3	VR2	VR1	VR0	0	CT6	CT5	CT4	CT3	CT2	CT1	CT0

Figure 7 Contrast Control Instruction

CT6–0: These bits control the LCD drive voltage to adjust 128-step contrast. For details, see the Contrast Adjuster section.

VR3–0: These bits adjust the output voltage in the LCD drive reference generator.

Note: CT6-0 and VR3-0 bits are for setting the common driver. Control according to the bits' values is executed by the common driver. For details, see the data sheet for the common driver.

Entry Mode (R05h)

Compare Register (R06h)

R/W	RS	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
W	1	0	0	0	0	0	0	HWM	0	0	0	I/D1	I/D0	AM	LG2	LG1	LG0
W	1	0	0	0	0	CP11	CP10	CP9	CP8	CP7	CP6	CP5	CP4	CP3	CP2	CP1	CP0

Figure 8 Entry Mode and Compare Register Instruction

The write data sent from the microcomputer is modified in the HD66765 and written to the GRAM. The display data in the GRAM can be quickly rewritten to reduce the load of the microcomputer software processing. For details, see the Graphics Operation Function section.

HWM: When HWM=1, data can be written to the GRAM at high speed. In high-speed write mode, four words of data are written to the GRAM in a single operation after writing to RAM four times. Write to RAM four times, otherwise the four words cannot be written to the GRAM. Thus, set the lower 2 bits to 0 when setting the RAM address. For details, see High-Speed RAM Write Mode section.

I/D1-0: When I/D1-0 = 1, the address counter (AC) is automatically incremented by 1 after the data is written to the GRAM. When I/D1-0 = 0, the AC is automatically decremented by 1 after the data is written to the GRAM. The increment/decrement setting of the address counter by I/D1-0 is done independently for the upper (AD15-8) and lower (AD7-0) addresses. The direction of moving through the addresses when the GRAM is written to is set by the AM bit.

AM: Set the automatic update method of the AC after the data is written to the GRAM. When AM = 0, the data is continuously written in parallel. When AM = 1, the data is continuously written vertically. When window address range is specified, the GRAM in the window address range can be written to according to the I/D1-0 and AM settings.

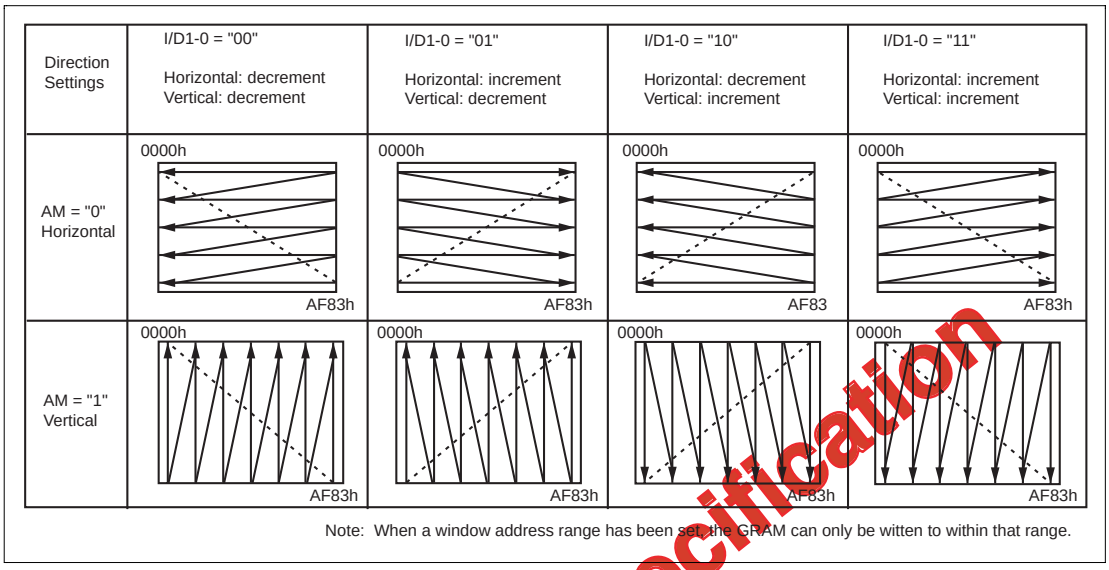


Figure 9 Address Direction Settings

LG2–0: Compare the data read from the GRAM by the microcomputer with the compare registers (CP7–0) by a compare/logical operation and write the results to GRAM. For details, see the Logical/Compare Operation Function.

CP11–0: Set the compare register for the compare operation with the data read from the GRAM or written by the microcomputer.

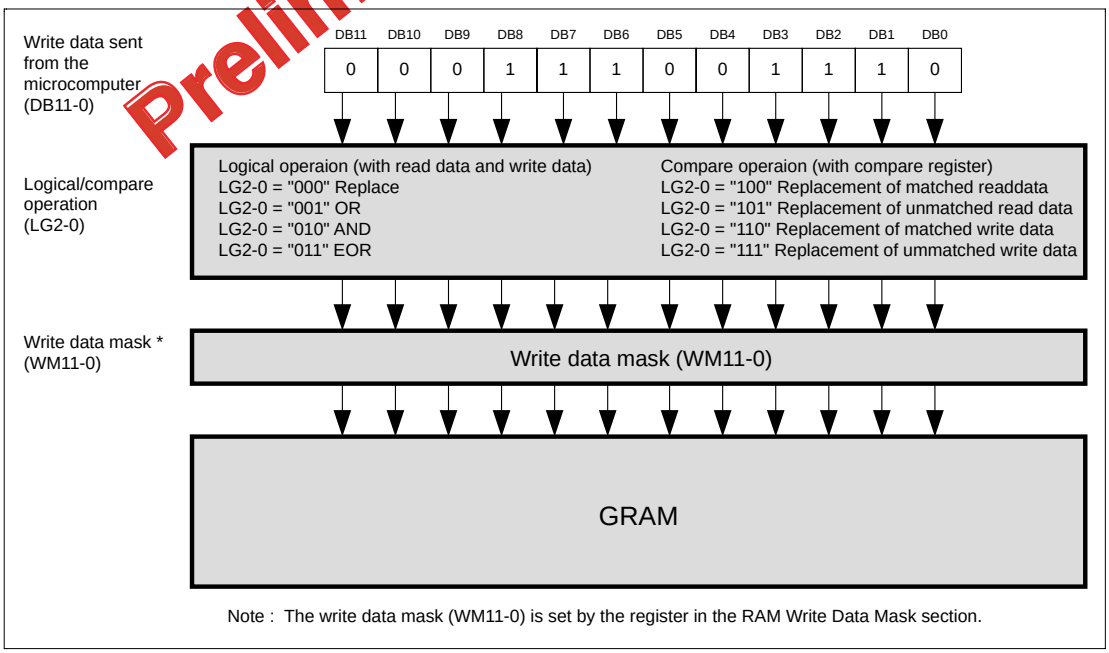


Figure 10 Logical/Compare Operation and Swapping for the GRAM

Display Control (R07h)

R/W	RS	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
W	1	0	0	0	0	0	VLE2	VLE1	SPT	0	0	0	0	0	REV	D1	D0

Figure 11 Display Control Instruction

VLE2–1: When VLE1 = 1, a vertical scroll is performed in the 1st screen. When VLE2 = 1, a vertical scroll is performed in the 2nd screen. Vertical scrolling on the two screens can be independently controlled.

SPT: When SPT = 1, the 2-division LCD drive is performed. For details, see the Screen-division Driving Function section.

REV: Displays all character and graphics display sections with reversal when REV = 1. For details, see the Reversed Display Function section. Since the grayscale level can be reversed, display of the same data is enabled on normally-white and normally-black panels.

D1–0: Display is on when D1 = 1 and off when D1 = 0. When off, the display data remains in the GRAM, and can be displayed instantly by setting D1 = 1. When D1 is 0, the display is off with all of the SEG/COM pin outputs set to the GND level. Because of this, the HD66765 can control the charging current for the LCD with AC driving.

When D1–0 = 01, the internal display of the HD66765 is performed although the display is off. When D1-0 = 00, the internal display operation halts and the display is off.

Table 9 D Bits and Operation

D1	D0	SEG/COM Output	HD66765 Internal Display Operation	Master/Slave Signal (CL1, FLM, M, and DISPTMG)
0	0	GND	Halt	Halt
0	1	GND	Operate	Operate
1	0	Unlit display	Operate	Operate
1	1	Display	Operate	Operate

Notes: 1. Writing from the microcomputer to the GRAM is independent from D1–0.
2. In the sleep and standby modes, D1–0 = 00. However, the register contents of D1–0 are not modified.

Note: SPT and D1 bits are for setting the common driver. Control according to the bits' values is executed by the common driver. For details, see the data sheet for the common driver.

COM Driver Interface Control (R0Ah)

R/W	RS	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
W	1	0	0	0	0	0	0	0	TE	0	0	0	0	0	IDX2	IDX1	IDX0
R	1	0	0	0	0	0	0	0	TE	0	0	0	0	0	IDX2	IDX1	IDX0

Figure 12 COM Driver Interface Control Instruction

IDX2-0: Index bits that select instructions for the common driver. The instruction that corresponds to the setting made here is transferred, with the index, to the common driver via the serial interface. These instructions are transferred in bit rows as shown below. The upper 3 bits correspond to IDX2-0. The IDX2-0 setting at the time of transfer selects the instruction for the common driver as listed below.

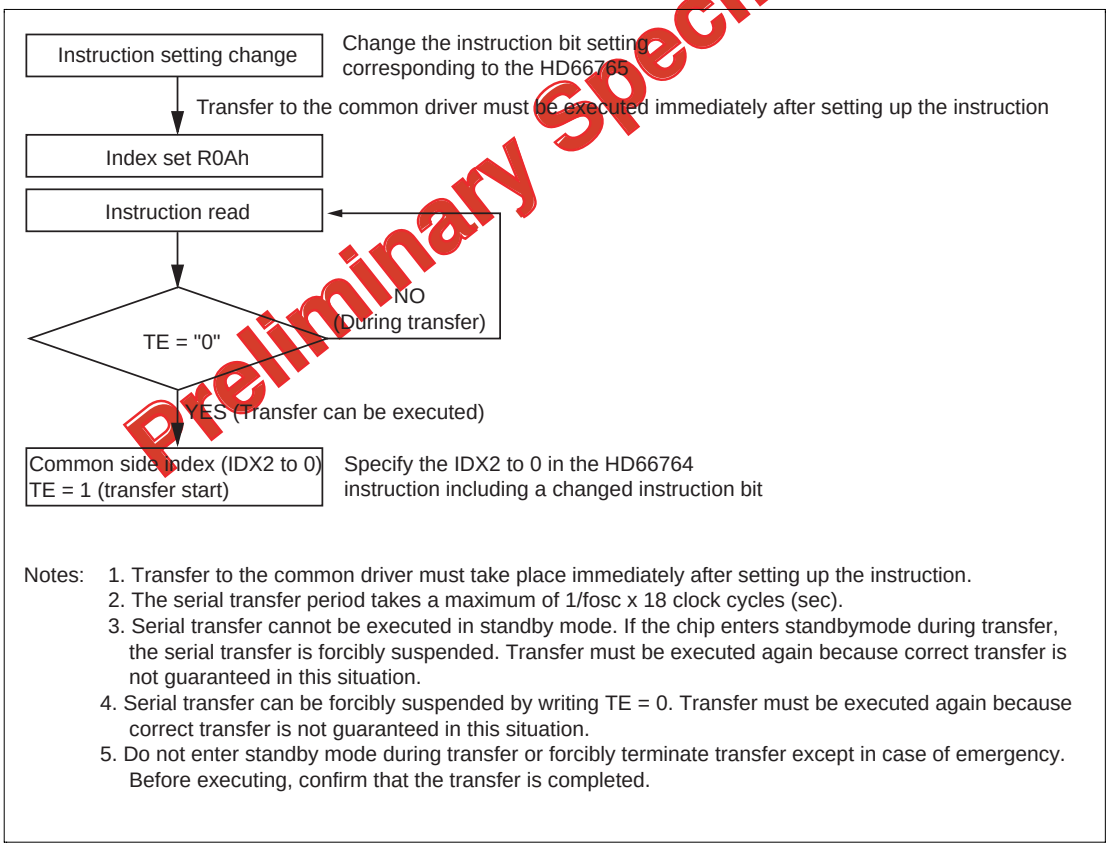
To change an instruction setting on the common driver, first change the instruction bit on the HD66765, select the instruction, which includes the changed instruction bit, from the list below, by setting IDX2-0 as required. The instruction is transferred to the common driver as the transfer starts (TE=1), and is the executed.

TE: Serial transfer enable for the common driver. When TE=0, serial transfer is possible. Do not change the instruction during transfer. When TE=1, transfer starts. TE returning to 0 indicates the end of the transfer. Note that, serial transfer to the common driver requires 18 clock cycles at most. Do not change the instruction during the transfer.

* New instructions should be transferred to the common driver soon after they have been set on the HD66765.

Table of common driver (HD66764) instructions

IDX2	IDX1	IDX0	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	BS2	BS1	BS0	BT3	BT2	BT1	BT0	0	DC1	DC0	AP1	AP0	SLP
0	0	1	0	0	0	0	0	0	0	0	0	0	VC2	VC1	VC0
0	1	0	0	VR3	VR2	VR1	VR0	0	CT6	CT5	CT4	CT3	CT2	CT1	CT0
0	1	1	0	0	D1	CMS	SPT	SS17	SS16	SS15	SS14	SS13	SS12	SS11	SS10
1	0	0	0	0	0	0	0	SE17	SE16	SE15	SE14	SE13	SE12	SE11	SE10
1	0	1	0	0	0	0	0	SS27	SS26	SS125	SS24	SS23	SS22	SS21	SS20
1	1	0	0	0	0	0	0	SE27	SE26	SE25	SE24	SE23	SE22	SE21	SE20



Notes:
1. Transfer to the common driver must take place immediately after setting up the instruction.
2. The serial transfer period takes a maximum of 1/fosc x 18 clock cycles (sec).
3. Serial transfer cannot be executed in standby mode. If the chip enters standbymode during transfer, the serial transfer is forcibly suspended. Transfer must be executed again because correct transfer is not guaranteed in this situation.
4. Serial transfer can be forcibly suspended by writing TE = 0. Transfer must be executed again because correct transfer is not guaranteed in this situation.
5. Do not enter standby mode during transfer or forcibly terminate transfer except in case of emergency. Before executing, confirm that the transfer is completed.

Figure 13 Common Interface: Serial Transfer Sequence

Frame Cycle Control (R0Bh)

R/W	RS	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
W	1	0	0	0	0	0	0	DIV1	DIV0	0	0	0	0	RTN3	RTN2	RTN1	RTN0

Figure 14 Frame Cycle Control Instruction

RTN3-0: Set the line retrace period (RTN3-0) to be added to raster-row cycles. The raster-row cycle becomes longer according to the number of clocks set at RTN3-0.

DIV1-0: Set the division ratio of clocks for internal operation (DIV1-0). Internal operations are driven by clocks which are frequency divided according to the DIV1-0 setting. Frame frequency can be adjusted along with the line retrace period (RTN3-0). When changing the drive-duty cycle, adjust the frame frequency. For details, see the Frame Frequency Adjustment Function section.

Table 10 RTN Bits and Clock Cycles

RTN3	RTN2	RTN1	RTN0	Line Retrace Period (Clock Cycles)	Clock Cycles per Raster-row
0	0	0	0	0	25
0	0	0	1	1	26
0	0	1	0	2	27
0	0	1	1	3	28
:	:	:	:	:	:
1	1	1	0	14	39
1	1	1	1	15	40

Table 11 DIV Bits and Clock Frequency

DIV1	DIV0	Division Ratio	Internal Operation Clock Frequency
0	0	1	fosc / 1
0	1	2	fosc / 2
1	0	4	fosc / 4
1	1	8	fosc / 8

* fosc = R-C oscillation frequency

Formula for the frame frequency

$$\text{Frame frequency} = \frac{\text{fosc}}{\text{Clock cycles per raster-row} \times \text{division ratio} \times 1/\text{duty cycle}} \text{ [Hz]}$$

fosc: R-C oscillation frequency

Duty: drive duty (NL bit)

Division ratio: DIV bit

Clock cycles per raster-row: (RTN + 25) clock cycles

Vertical Scroll Control (R11h)

R/W	RS	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
W	1	VL27	VL26	VL25	VL24	VL23	VL22	VL21	VL20	VL17	VL16	VL15	VL14	VL13	VL12	VL11	VL10

Figure 15 Vertical Scroll Control Instruction

VL17–10: Specify the display-start raster-row at the 1st screen display for vertical smooth scrolling. Any raster-row from the first to 176th can be selected. After the 176th raster-row is displayed, the display restarts from the first raster-row. The display-start raster-row (VL17–10) is valid only when VLE1 = 1. The raster-row display is fixed when VLE1 = 0. (VLE1 is the 1st-screen vertical-scroll enable bit.)

VL27–20: Specify the display-start raster-row at the 2nd screen display. The display-start raster-row (VL27–20) is valid only when VLE2 = 1. The raster-row display is fixed when VLE2 = 0. (VLE2 is the 2nd-screen vertical-scroll enable bit.) The vertical scroll for the 1st and 2nd screens can be independently set.

Table 22 VL Bits and Display-start Raster-row

VL27 VL17	VL26 VL16	VL25 VL15	VL24 VL14	VL23 VL13	VL22 VL12	VL21 VL11	VL20 VL10	Display-start Raster-row
0	0	0	0	0	0	0	0	1st raster-row
0	0	0	0	0	0	0	1	2nd raster-row
0	0	0	0	0	0	1	0	3rd raster-row
:	:	:	:	:	:	:	:	:
1	0	1	0	1	1	1	0	175th raster-row
1	0	1	0	1	1	1	1	176th raster-row

Note: Do not set over the 176th (AFH) raster-row.

1st Screen Driving Position (R14h)

2nd Screen Driving Position (R15h)

R/W	RS	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
W	1	SE17	SE16	SE15	SE14	SE13	SE12	SE11	SE10	SS17	SS16	SS15	SS14	SS13	SS12	SS11	SS10
W	1	SE27	SE26	SE25	SE24	SE23	SE22	SE21	SE20	SS27	SS26	SS25	SS24	SS23	SS22	SS21	SS20

Figure 16 1st Screen Driving Position and 2nd Screen Driving Position Instructions

SS17–0: Specify the driving start position for the first screen in a line unit. The LCD driving starts from the 'set value + 1' common driver.

SE17–0: Specify the driving end position for the first screen in a line unit. The LCD driving is performed to the 'set value + 1' common driver. For instance, when SS17–10 = 07H and SE17–10 = 10H are set, the LCD driving is performed from COM8 to COM17, and non-selection driving is performed for COM1 to COM7, COM18, and others. Ensure that SS17–10 ≤ SE17–10 ≤ AFH. For details, see the Screen-division Driving Function section.

SS27–0: Specify the driving start position for the second screen in a line unit. The LCD driving starts from the 'set value + 1' common driver. The second screen is driven when SPT = 1.

SE27–0: Specify the driving end position for the second screen in a line unit. The LCD driving is performed to the 'set value + 1' common driver. For instance, when SPT = 1, SS27–20 = 20H, and SE27–20 = AFH are set, the LCD driving is performed from COM33 to COM80. Ensure that SS17–10 ≤ SE17–10 ≤ SS27–20 ≤ SE27–20 ≤ 4FH. For details, see the Screen-division Driving Function section.

Horizontal RAM Address Position (R16h)

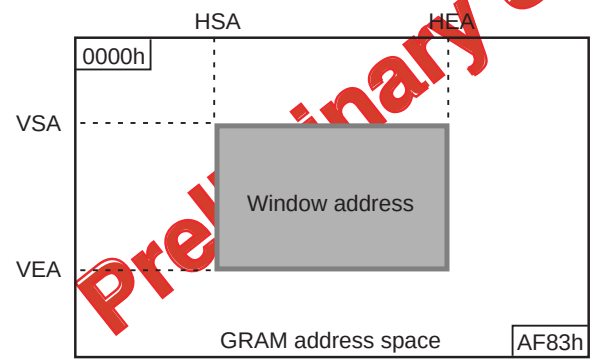
Vertical RAM Address Position (R17h)

R/W	RS	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
W	1	HEA7	HEA6	HEA5	HEA4	HEA3	HEA2	HEA1	HEA0	HSA7	HSA6	HSA5	HSA4	HSA3	HSA2	HSA1	HSA0
W	1	VEA7	VEA6	VEA5	VEA4	VEA3	VEA2	VEA1	VEA0	VSA7	VSA6	VSA5	VSA4	VSA3	VSA2	VSA1	VSA0

Figure 17 Horizontal/Vertical RAM Address Position Instruction

HSA7-0/HEA7-0: Specify the horizontal start/end positions of a window for access in memory. Data can be written to the GRAM from the address specified by HEA7-0 from the address specified by HSA7-0. Note that an address must be set before RAM is written to. Ensure 00h ≤ HSA7-0 ≤ HEA7-0 ≤ 3Fh.

VSA7-0/VEA7-0: Specify the vertical start/end positions of a window for access in memory. Data can be written to the GRAM from the address specified by VEA7-0 from the address specified by VSA7-0. Note that an address must be set before RAM is written to. Ensure 00h ≤ VSA7-0 ≤ VEA7-0 ≤ AFh.



Window address setting range
"00"h ≤ HSA7-0 ≤ HEA7-0 ≤ "83"h
"00"h ≤ VSA7-0 ≤ VEA7-0 ≤ "AF"h

Note: 1. Ensure that the window address area is within the GRAM address space.
2. In high-speed write mode, data are written to GRAM in four-words.
Thus, dummy write operations should be inserted depending on the window address area. For details, see the High-Speed Burst RAM Write Function section.

Figure 18 Window Address Setting Range

RAM Write Data Mask (R20h)

R/W	RS	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
W	1	0	0	0	0	WM 11	WM 10	WM 9	WM 8	WM 7	WM 6	WM 5	WM 4	WM 3	WM 2	WM 1	WM 0

Figure 19 RAM Write Data Mask Instruction

WM11–0: In writing to the GRAM, these bits mask writing in a bit unit. When WM11 = 1, this bit masks the write data of DB11 and does not write to the GRAM. Similarly, the WM10–0 bits mask the write data of DB10–0 in a bit unit. When SWP = 1, the upper and lower bytes in the write data mask are swapped. For details, see the Graphics Operation Function section.

RAM Address Set (R21h)

R/W	RS	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
W	1	AD 15	AD 14	AD 13	AD 12	AD 11	AD 10	AD 9	AD 8	AD 7	AD 6	AD 5	AD 4	AD 3	AD 2	AD 1	AD 0

Figure 20 RAM Address Set Instruction

AD15–0: Initially set GRAM addresses to the address counter (AC). Once the GRAM data is written, the AC is automatically updated according to the AM and I/D bit settings. This allows consecutive accesses without resetting addresses. Once the GRAM data is read, the AC is not automatically updated. GRAM address setting is not allowed in the standby mode. Ensure that the address is set within the specified window address.

Table 13 GRAM Address Range in Eight-grayscale Mode

AD14–AD0	GRAM Setting
"0000"H–"0083"H	Bitmap data for COM1
"0100"H–"0183"H	Bitmap data for COM2
"0200"H–"0283"H	Bitmap data for COM3
"0300"H–"0383"H	Bitmap data for COM4
:	:
"AC00"H–"AC83"H	Bitmap data for COM173
"AD00"H–"AD83"H	Bitmap data for COM174
"AE00"H–"AE83"H	Bitmap data for COM175
"AF00"H–"AF83"H	Bitmap data for COM176

Write Data to GRAM (R22h)

R/W	RS	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
W	1	0	0	0	0	WD 11	WD 10	WD 9	WD 8	WD 7	WD 6	WD 5	WD 4	WD 3	WD 2	WD 1	WD 0

Figure 21 Write Data to GRAM Instruction

WD11–0 : Write 12-bit data to the GRAM. This data calls each grayscale palette. After a write, the address is automatically updated according to the AM and I/D bit settings. During the standby mode, the GRAM cannot be accessed.

	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
GRAM write data	0	0	0	0	WD 11	WD 10	WD 9	WD 8	WD 7	WD 6	WD 5	WD 4	WD 3	WD 2	WD 1	WD 0
					R3	R2	R1	R0	G3	G2	G1	G0	B3	B2	B1	B0
					1 pixel data											

Figure 22 GRAM Write Data Instruction

Table 14 GRAM Data and Grayscale Palette

GRAM Data Setting								
R3	R2	R1	R0					
G3	G2	G1	G0					
B3	B2	B1	B0	Grayscale Palette				
0	0	0	0	PK04	PK03	PK02	PK01	PK00
0	0	0	1	PK14	PK13	PK12	PK11	PK10
0	0	1	0	PK24	PK23	PK22	PK21	PK20
0	0	1	1	PK34	PK33	PK32	PK31	PK30
0	1	0	0	PK44	PK43	PK42	PK41	PK40
0	1	0	1	PK54	PK53	PK52	PK51	PK50
0	1	1	0	PK64	PK63	PK62	PK61	PK60
0	1	1	1	PK74	PK73	PK72	PK71	PK70
1	0	0	0	PK84	PK83	PK82	PK81	PK80
1	0	0	1	PK94	PK93	PK92	PK91	PK90
1	0	1	0	PK104	PK103	PK102	PK101	PK100
1	0	1	1	PK114	PK113	PK112	PK111	PK110
1	1	0	0	PK124	PK123	PK122	PK121	PK120
1	1	0	1	PK134	PK133	PK132	PK131	PK130
1	1	1	0	PK144	PK143	PK142	PK141	PK140
1	1	1	1	PK154	PK153	PK152	PK151	PK150

Read Data from GRAM (R22h)

R/W	RS	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
R	1	0	0	0	0	RD 11	RD 10	RD 9	RD 8	RD 7	RD 6	RD 5	RD 4	RD 3	RD 2	RD 1	RD 0

Figure 23 Read Data from GRAM Instruction

RD11–0: Read 12-bit data from the GRAM. When the data is read to the microcomputer, the first-word read immediately after the GRAM address setting is latched from the GRAM to the internal read-data latch. The data on the data bus (DB11–0) becomes invalid and the second-word read is normal.

When bit processing, such as a logical operation, is performed within the HD66765, only one read can be processed since the latched data in the first word is used.

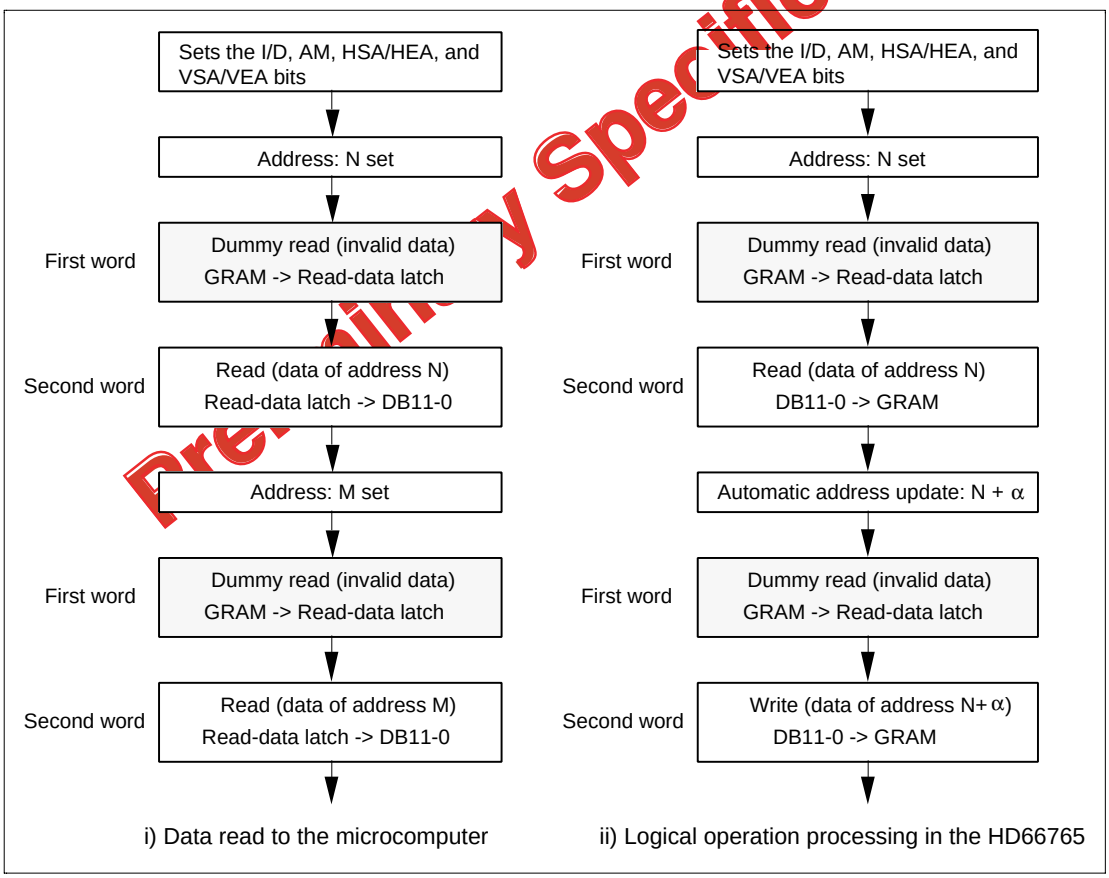


Figure 24 GRAM Read Sequence

Grayscale Palette Control (R30h to R39h)

	R/W	RS	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
R30h	W	1	0	0	0	PK14	PK13	PK12	PK11	PK10	0	0	0	PK04	PK03	PK02	PK01	PK00
R31h	W	1	0	0	0	PK34	PK33	PK32	PK31	PK30	0	0	0	PK24	PK23	PK22	PK21	PK20
R32h	W	1	0	0	0	PK54	PK53	PK52	PK51	PK50	0	0	0	PK44	PK43	PK42	PK41	PK40
R33h	W	1	0	0	0	PK74	PK73	PK72	PK71	PK70	0	0	0	PK64	PK63	PK62	PK61	PK60
R34h	W	1	0	0	0	PK94	PK93	PK92	PK91	PK90	0	0	0	PK84	PK83	PK82	PK81	PK80
R35h	W	1	0	0	0	PK114	PK113	PK112	PK111	PK110	0	0	0	PK104	PK103	PK102	PK101	PK100
R36h	W	1	0	0	0	PK134	PK133	PK132	PK131	PK130	0	0	0	PK124	PK123	PK122	PK121	PK120
R37h	W	1	0	0	0	PK154	PK153	PK152	PK151	PK150	0	0	0	PK144	PK143	PK142	PK141	PK140

Figure 25 Grayscale Palette Control Instruction

RK154–00: Specify the grayscale level for 16-palettes from the 24-grayscale level. For details, see the Grayscale Palette and Grayscale Palette Table sections.

Table 17 Instruction List

Reg. No.	Register Name			Upper Code								Lower Code								Description	Execu-tion Cycle
		R/W	RS	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		
IR	Index	0	0	*	*	*	*	*	*	*	*	*	ID6	ID5	ID4	ID3	ID2	ID1	ID0	Sets the index register value.	0
SR	Status read	1	0	L7	L6	L5	L4	L3	L2	L1	L0	0	C6	C5	C4	C3	C2	C1	C0	Reads the driving raster-row position (L7-0) and contrast setting (C6-0).	0
R00h	Start oscillation	0	1	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	1	Starts the oscillation mode.	10 ms
	Device code read	1	1	0	0	0	0	0	1	1	1	0	1	1	0	0	0	1	1	Reads 0765H.	0
R01h	Driver output control	0	1	0	0	0	0	0	0	CMS	SGS	0	0	0	NL4	NL3	NL2	NL1	NL0	Sets the common driver shift direction (CMS), segment driver shift direction (SGS), and driving duty ratio (NL4-0).	0
R02h	LCD-driving-waveform control	0	1	0	0	0	0	0	0	B/C	EOR	0	0	NW5	NW4	NW3	NW2	NW1	NW0	Sets the LCD drive AC waveform (B/C), EOR output (EOR), and the number of n-raster-rows (NW5-0) at C-pattern AC drive.	0
R03h	Power control 1	0	1	0	BS2	BS1	BS0	BT3	BT2	BT1	BT0	0	DC2	DC1	DC0	AP1	AP0	SLP	STB	Sets the standby mode (STB), LCD power on (AP1-0), sleep mode (SLP), boosting cycle (DC2-0), boosting ouput multiplying factor (BT3-0), and LCD drive bias value (BS2-0).	0
R04h	Contrast control	0	1	0	0	0	0	VR3	VR2	VR1	VR0	0	CT6	CT5	CT4	CT3	CT2	CT1	CT0	Sets the contrast adjustment (CT6-0) and regulator adjustment (VR3-0).	0
R05h	Entry mode	0	1	0	0	0	0	0	0	HWM	0	0	0	I/D1	I/D0	AM	LG2	LG1	LG0	Specifies the logical operation (LG2-0), AC counter mode (AM), increment/ decrement mode (I/D1-0) and high-speed-write mode (HWM).	0
R06h	Compare register	0	1	0	0	0	0	0	0	0	0	CP7	CP6	CP5	CP4	CP3	CP2	CP1	CP0	Sets the compare register (CP7-0).	0
R07h	Display control	0	1	0	0	0	0	0	VLE2	VLE1	SPT	0	0	0	0	0	REV	D1	D0	Specifies display on (D1-0), reversed display (REV), ,screen division driving (SPT), and vertical scroll (VLE2-1).	0
R0Ah	COM driver interface control	0	1	0	0	0	0	0	0	0	TE	0	0	0	0	0	IDX2	IDX1	IDX0	Specifies the serial transfer enable (TE) and index for the COM transfer	0
		1	1	0	0	0	0	0	0	0	TE	0	0	0	0	0	IDX2	IDX1	IDX0	instructions (IDX2-0).	0
R0Bh	Frame cycle control	0	1	0	0	0	0	0	0	DIV1	DIV0	0	0	0	0	RTN3	RTN2	RTN1	RTN0	Sets the line retrace period (RTN3-0) and operating clock frequency-division ratio (DIV1-0)	0
R0Ch	Power control 2	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	VC2	VC1	VC0	Sets an adjustment factor for the Vci voltage (VC2-0).	0
R11h	Vertical scroll control	0	1	VL27	VL26	VL25	VL24	VL23	VL22	VL21	VL20	VL17	VL16	VL15	VL14	VL13	VL12	VL11	VL10	Specifies the 1st-screen display-start raster-row (VL17-10) and 2nd-screen display-start raster-row (VL27-20).	0
R14h	1st screen driving position	0	1	SE17	SE16	SE15	SE14	SE13	SE12	SE11	SE10	SS17	SS16	SS15	SS14	SS13	SS12	SS11	SS10	Sets 1st-screen driving start (SS17-10) and end (SE17-10).	0
R15h	2nd screen driving position	0	1	SE27	SE26	SE25	SE24	SE23	SE22	SE21	SE20	SS27	SS26	SS25	SS24	SS23	SS22	SS21	SS20	Sets 2nd-screen driving start (SS27-20) and end (SE27-20).	0
R16h	Horizontal RAM address position	0	1	HEA7	HEA6	HEA5	HEA4	HEA3	HEA2	HEA1	HEA0	HSA7	HSA6	HSA5	HSA4	HSA3	HSA2	HSA1	HSA0	Sets the start (HSA7-0) and end (HEA7-0) of the horizontal RAM address range.	0
R17h	Vertical RAM address position	0	1	VEA7	VEA6	VEA5	VEA4	VEA3	VEA2	VEA1	VEA0	VSA7	VSA6	VSA5	VSA4	VSA3	VSA2	VSA1	VSA0	Sets the start (VSA7-0) and end (VEA7-0) of the vertical RAM address range.	0
R20h	RAM write data mask	0	1	0	0	0	0	WM 11	WM 10	WM9	WM8	WM7	WM6	WM5	WM4	WM3	WM2	WM1	WM0	Specifies write data mask (WM15-0) at RAM write.	0
R21h	RAM address set	0	1	AD15-8 (upper)								AD7-0 (lower)								Initially sets the RAM address to the address counter (AC).	0
R22h	Write data to GRAM	0	1	Write Data (upper)								Write Data (lower)								Write data to RAM.	0
	Write data from GRAM	1	1	Read Data (upper)								Read Data (lower)								Read data from RAM.	0
R30h	Grayscale palette control (1)	0	1	0	0	0	PK14	PK13	PK12	PK11	PK10	0	0	0	PK04	PK03	PK02	PK01	PK00	Specifies the Grayscale palette.	0
R31h	Grayscale palette control (2)	0	1	0	0	0	PK34	PK33	PK32	PK31	PK30	0	0	0	PK24	PK23	PK22	PK21	PK20	Specifies the Grayscale palette.	0
R32h	Grayscale palette control (3)	0	1	0	0	0	PK54	PK53	PK52	PK51	PK50	0	0	0	PK44	PK43	PK42	PK41	PK40	Specifies the Grayscale palette.	0
R33h	Grayscale palette control (4)	0	1	0	0	0	PK74	PK73	PK72	PK71	PK70	0	0	0	PK64	PK63	PK62	PK61	PK60	Specifies the Grayscale palette.	0
R34h	Grayscale palette control (5)	0	1	0	0	0	PK94	PK93	PK92	PK91	PK90	0	0	0	PK84	PK83	PK82	PK81	PK80	Specifies the Grayscale palette.	0
R35h	Grayscale palette control (6)	0	1	0	0	0	PK114	PK113	PK112	PK111	PK110	0	0	0	PK104	PK103	PK102	PK101	PK100	Specifies the Grayscale palette.	0
R36h	Grayscale palette control (7)	0	1	0	0	0	PK134	PK133	PK132	PK131	PK130	0	0	0	PK124	PK123	PK122	PK121	PK120	Specifies the Grayscale palette.	0
R37h	Grayscale palette control (8)	0	1	0	0	0	PK154	PK153	PK152	PK151	PK150	0	0	0	PK144	PK143	PK142	PK141	PK140	Specifies the Grayscale palette.	0

Note: 1. '*' means 'doesn't matter'.

2. After setting TE = 1, 18 (max.) clock cycles are required for a serial transfer to be completed. During that time, do not change the bits of instructions which are to be transferred.

3. High-speed write mode is available only for the RAM writing.

Reset Function

The HD66765 is internally initialized by RESET input. Reset the common driver as its settings are not automatically reinitialized when the HD66765 is reset. The reset input must be held for at least 1 ms. Do not access the GRAM or initially set the instructions until the R-C oscillation frequency is stable after power has been supplied (10 ms).

Instruction Set Initialization:

1. Start oscillation executed
2. Driver output control (NL4–0 = 10101, SGS = 0, CMS = 0)
3. B-pattern waveform AC drive (B/C = 0, ECR = 0, NW5–0 = 00000)
4. Power control 1 (DC2–0 = 000, AP1–0 = 00: LCD power off, STB = 0: Standby mode off, SLP = 0, BS2-0 = 000, BT2-0 = 000)
5. Contrast control (Weak contrast (VR3-0 = 0000, CT6–0 = 0000000))
6. Entry mode set (HWM = 0, I/D1-0 = 11: Increment by 1, AM = 0: Horizontal move, LG2–0 = 000: Replace mode)
7. Compare register (CP7–0: 00000000)
8. Display control (VLE2–1 = 00: No vertical scroll, SPT = 0, REV = 0, D1–0 = 00: Display off)
9. COM driver interface control (TE = 0, IDX2-0 = 000)
10. Frame cycle control (DIV1-0 = 00: 1-divided clock, RTN2-0: No retrace line period)
11. Power control 2 (VC2-0 = 000)
12. Vertical scroll (VL27–20 = 00000000, VL17–10 = 00000000)
13. 1st screen division (SE17-10 = 11111111, SS17-10 = 00000000)
14. 2nd screen division (SE27-20 = 11111111, SS27-20 = 00000000)
15. Horizontal RAM address position (HEA7-0 = 00111111, HSA7-0 = 000000)
16. Vertical RAM address position (VEA7-0 = 10101111, VSA7-0 = 00000000)
17. RAM write data mask (WM11–0 = 000H: No mask)
18. RAM address set (AD15–0 = 0000H)
19. Grayscale palette
    PK04–00 = 00000, PK14–10 = 00010, PK24–20 = 00100, PK34–30 = 00110,
    PK44–40 = 00111, PK54–50 = 01000, PK64–60 = 01001, PK74–70 = 01010,
    PK84–80 = 01011, PK94–90 = 01100, PK104–100 = 01101, PK114–110 = 01110,
    PK124–120 = 10000, PK134–130 = 10010, PK144–140 = 10101, PK154–150 = 10111

GRAM Data Initialization:

This is not automatically initialized by reset input but must be initialized by software while display is off (D1–0 = 00).

Output Pin Initialization:

1. LCD driver output pins (SEG/COM): Output GND level
2. Oscillator output pin (OSC2): Outputs oscillation signal
3. Common interface signals (CCS*, CCL, and CDA): Halt
4. Timing signals (CL1, M, FLM, DISPTMG, and DCCLK): Halt

Parallel Data Transfer

16-bit Bus Interface

Setting the IM2/1/0 (interface mode) to the GND/GND/GND level allows 68-system E-clock-synchronized 16-bit parallel data transfer. Setting the IM2/1/0 to the GND/Vcc/GND level allows 80-system 16-bit parallel data transfer. When the number of buses or the mounting area is limited, use an 8-bit bus interface.

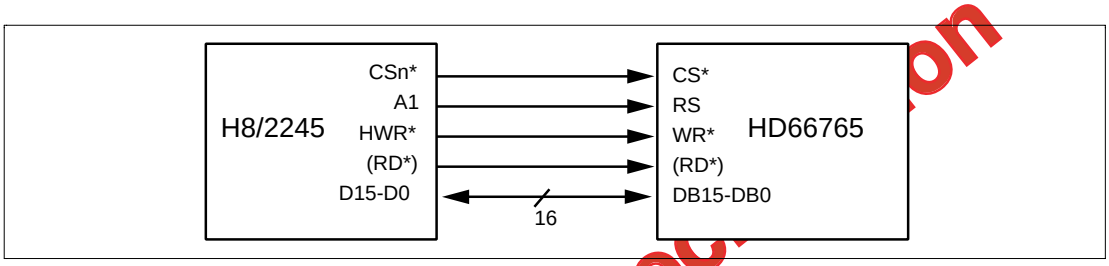


Figure 26 Interface to 16-bit Microcomputer

8-bit Bus Interface

Setting the IM2/1/0 (interface mode) to the GND/GND/Vcc level allows 68-system E-clock-synchronized 8-bit parallel data transfer using pins DB15–DB8. Setting the IM1/0 to the Vcc/Vcc level allows 80-system 8-bit parallel data transfer. The 16-bit instructions and RAM data are divided into eight upper/lower bits and the transfer starts from the upper eight bits. Fix unused pins DB7–DB0 to the Vcc or GND level. Note that the upper bytes must also be written when the index register is written to.

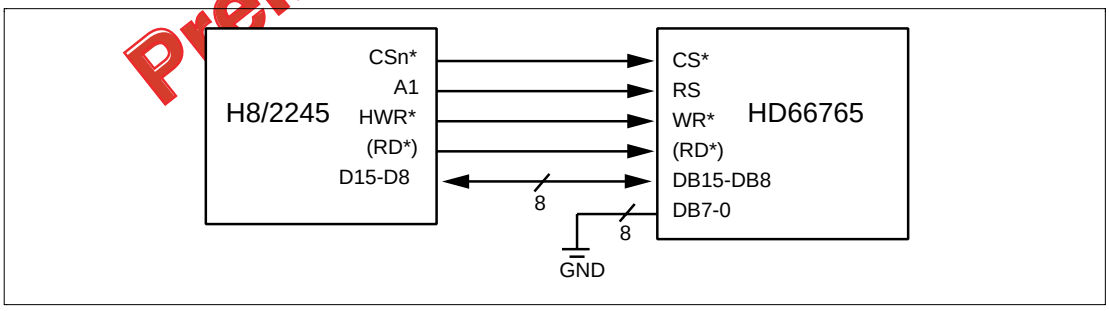


Figure 27 Interface to 8-bit Microcomputer

Note: Transfer synchronization function for an 8-bit bus interface
The HD66765 supports the transfer synchronization function which resets the upper/lower counter to count upper/lower 8-bit data transfer in the 8-bit bus interface. Noise causing transfer mismatch between the eight upper and lower bits can be corrected by a reset triggered by consecutively writing a 00H instruction four times. The next transfer starts from the upper eight bits. Executing synchronization function periodically can recover any runaway in the display system.

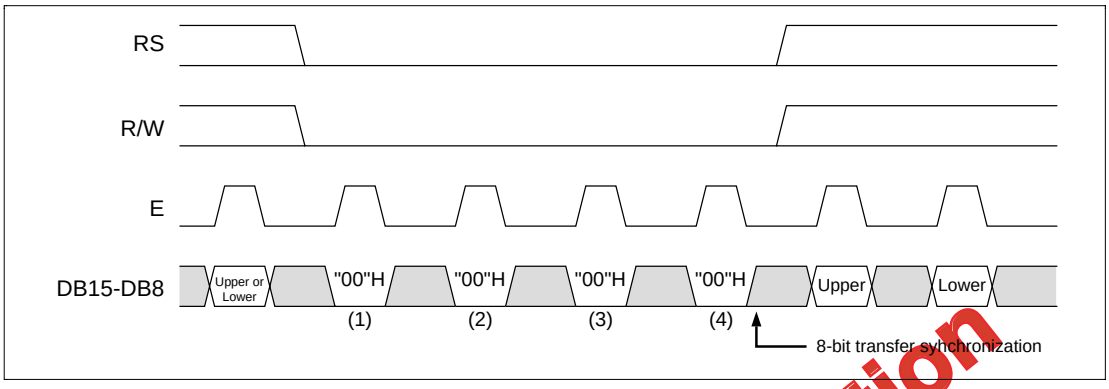


Figure 28 8-bit Transfer Synchronization

Serial Data Transfer

Setting the IM1 pin to the GND level and the IM2 pin to the Vcc level allows standard clock-synchronized serial data (SPI) transfer, using the chip select line (CS*), serial transfer clock line (SCL), serial input data (SDI), and serial output data (SDO). For a serial interface, the IM0/ID pin function uses an ID pin. If the chip is set up for serial interface, the DB15-2 pins which are not used must be fixed at Vcc or GND.

The HD66765 initiates serial data transfer by transferring the start byte at the falling edge of CS* input. It ends serial data transfer at the rising edge of CS* input.

The HD66765 is selected when the 6-bit chip address in the start byte transferred from the transmitting device matches the 6-bit device identification code assigned to the HD66765. The HD66765, when selected, receives the subsequent data string. The least significant bit of the identification code can be determined by the ID pin. The five upper bits must be 01110. Two different chip addresses must be assigned to a single HD66765 because the seventh bit of the start byte is used as a register select bit (RS): that is, when RS = 0, data can be written to the index register or status can be read, and when RS = 1, an instruction can be issued or data can be written to or read from RAM. Read or write is selected according to the eighth bit of the start byte (R/W bit). The data is received when the R/W bit is 0, and is transmitted when the R/W bit is 1.

After receiving the start byte, the HD66765 receives or transmits the subsequent data byte-by-byte. The data is transferred with the MSB first. All HD66765 instructions are 16 bits. Two bytes are received with the MSB first (DB15 to 0), then the instructions are internally executed. After the start byte has been received, the first byte is fetched internally as the upper eight bits of the instruction and the second byte is fetched internally as the lower eight bits of the instruction.

Four bytes of RAM read data after the start byte are invalid. The HD66765 starts to read correct RAM data from the fifth byte.

Table 18 Start Byte Format

Transfer Bit	S	1	2	3	4	5	6	7	8
Start byte format	Transfer start	Device ID code						RS	R/W
		0	1	1	1	0	ID		

Note: ID bit is selected by the IM0/ID pin.

Table 19 RS and R/W Bit Function

RS	R/W	Function
0	0	Sets index register
0	1	Reads status
1	0	Writes instruction or RAM data
1	1	Reads instruction or RAM data

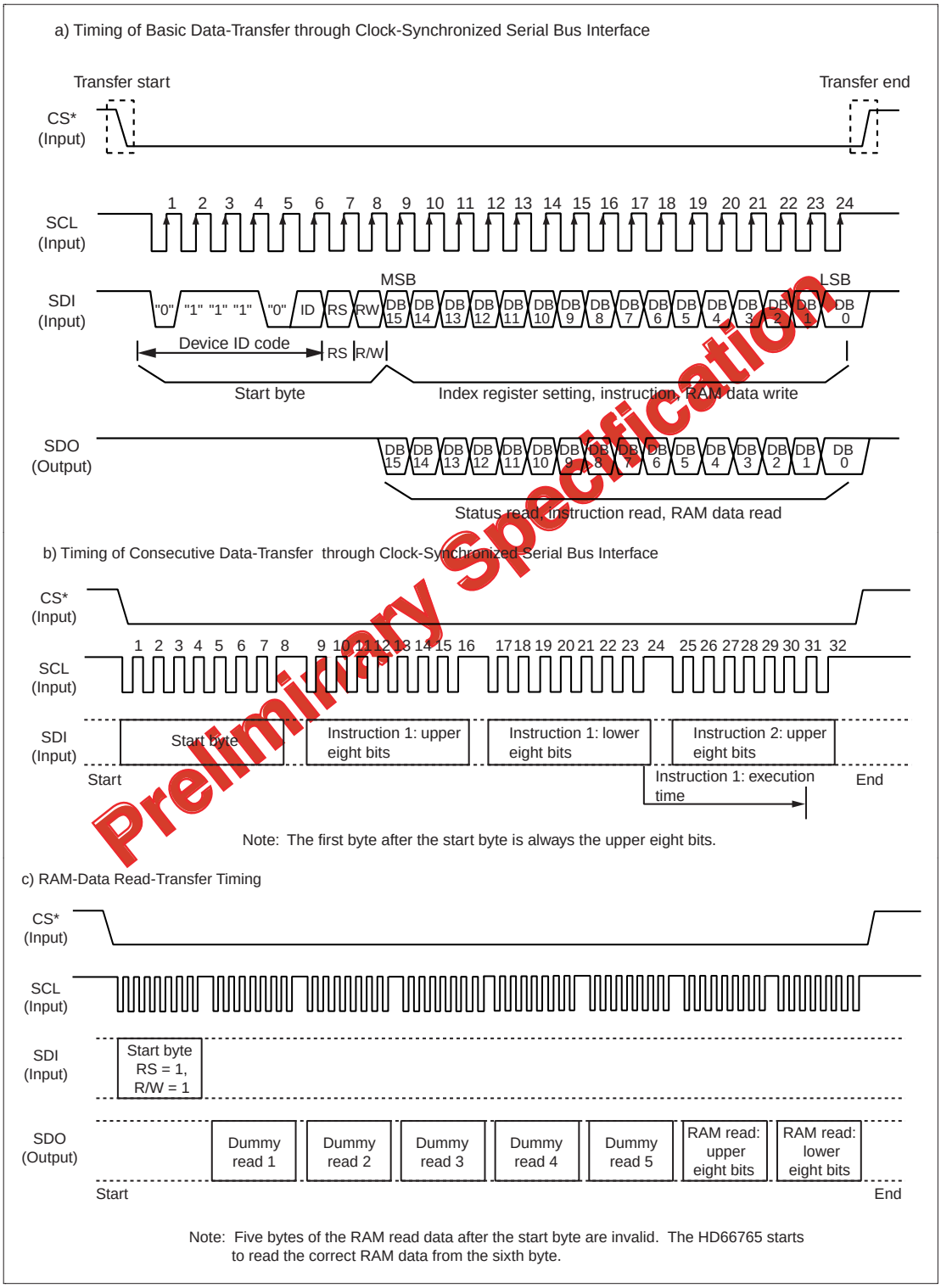


Figure 29 Procedure for Transfer on Clock-Synchronized Serial Bus Interface

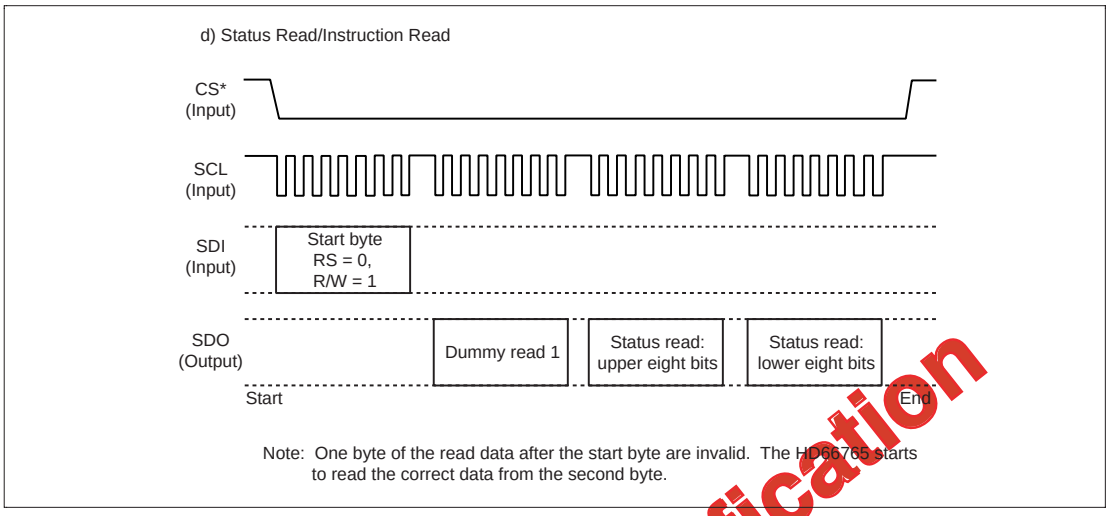


Figure 29 Procedure for Transfer on Clock-Synchronized Serial Bus Interface (cont)

High-Speed Burst RAM Write Function

The HD66765 has a high-speed burst RAM-write function that can be used to write data to RAM in one-fourth the access time required for an equivalent standard RAM-write operation. This function is especially suitable for applications which require the high-speed rewriting of the display data, for example, display of color animations, etc.

When the high-speed RAM-write mode (HWM) is selected, data for writing to RAM is once stored to the HD66765 internal register. When data is selected four times per word, all data is written to the on-chip RAM. While this is taking place, the next data can be written to an internal register so that high-speed and consecutive RAM writing can be executed for animated displays, etc.

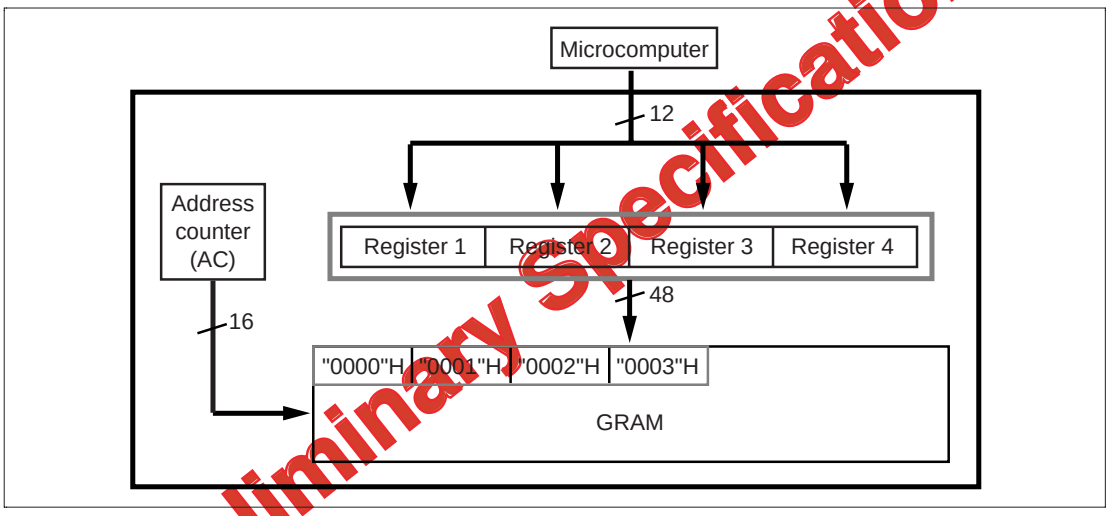


Figure 30 Flow of Operation in High-Speed Consecutive Writing to RAM

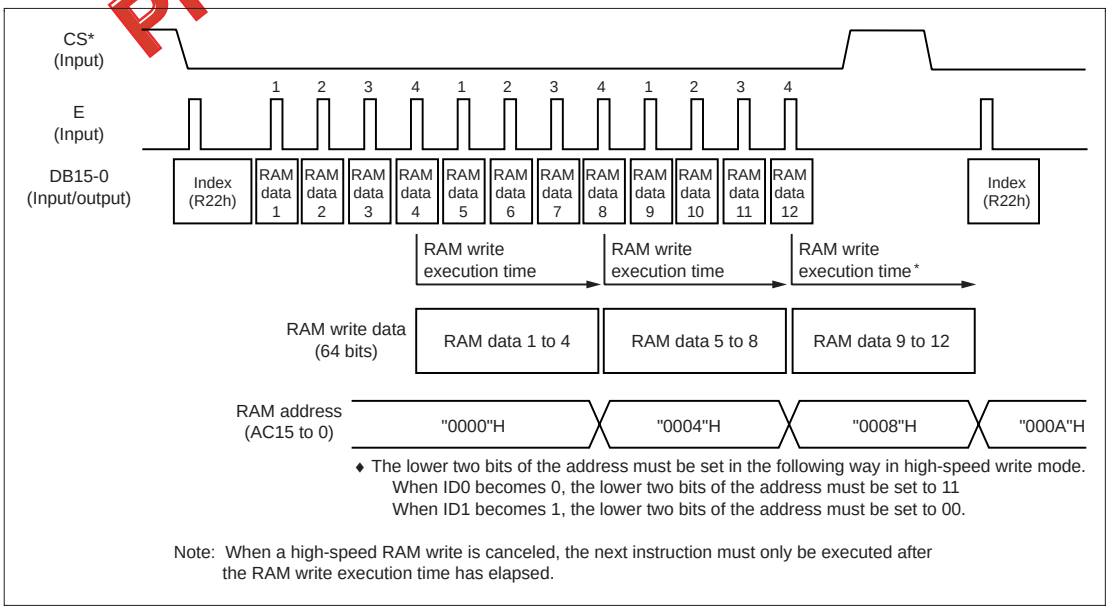


Figure 31 Example of the Operation of High-Speed Consecutive Writing to RAM

When high-speed RAM write mode is used, note the following.

Notes: 1. The logical and compare operations cannot be used.

2. Data is written to RAM each four words. When an address is set, the lower two bits in the address must be set to the following values.

   *When ID0=0, the lower two bits in the address must be set to 11 and be written to RAM.

   *When ID0=1, the lower two bits in the address must be set to 00 and be written to RAM.

3. Data is written to RAM each four words. If less than four words of data is written to RAM, the last data will not be written to RAM.

4. When the index register and RAM data write (R22h) have been selected, the data is always written first. RAM cannot be written to and read from at the same time. HWM must be set to 0 while RAM is being read.

5. High-speed and normal RAM write operations cannot be executed at the same time. The mode must be switched and the address must then be set.

6. When high-speed RAM write is used with a window address-range specified, dummy write operation may be required to suit the window address range-specification. Refer to the High-Speed RAM Write in the Window Address section.

Table 20 Comparison between Normal and High-Speed RAM Write Operations

	Normal RAM Write (HWM=0)	High-Speed RAM Write (HWM=1)
Logical operation function	Can be used	Cannot be used
Compare operation function	Can be used	Cannot be used
Swap function	Can be used	Can be used
Write mask function	Can be used	Can be used
RAM address set	Can be specified by word	ID0 bit=0: Set the lower two bits to 11 ID0 bit=1: Set the lower two bits to 00
RAM read	Can be read by word	Cannot be used
RAM write	Can be written by word	Dummy write operations may have to be inserted according to a window address-range specification
Window address	Can be set by word	Can be set by word

High-Speed RAM Write in the Window Address

When a window address range is specified, RAM data which is in an optional window area can be rewritten consecutively and quickly by inserting dummy write operations so that RAM access counts become 4N as shown in the tables below.

Dummy write operations may have to be inserted as the first or last operations for a row of data, depending on the horizontal window-address range specification bits (HSA1 to 0, HEA1 to 0). Number of dummy write operations of a row must be 4N.

Table 21 Number of Dummy Write Operations in High-Speed RAM Write (HSA Bits)

HSA1	HSA0	Number of Dummy Write Operations to be Inserted at the Start of a Row
0	0	0
0	1	1
1	0	2
1	1	3

Table 22 Number of Dummy Write Operations in High-Speed RAM Write (HEA Bits)

HEA1	HEA0	Number of Dummy Write Operations to be Inserted at the End of a Row
0	0	3
0	1	2
1	0	1
1	1	0

Each row of access must consist of $4 \times N$ operations, including the dummy writes.

Horizontal access count =

$$\text{first dummy write count} + \text{write data count} + \text{last dummy write count} = 4 \times N$$

An example of high-speed RAM write with a window address-range specified is shown below.

The window address-range can be rewritten to consecutively and quickly by inserting two dummy writes at the start of a row and three dummy writes at the end of a row, as determined by using the window address-range specification bits (HSA1 to 0=10, HEA1 to 0=00).

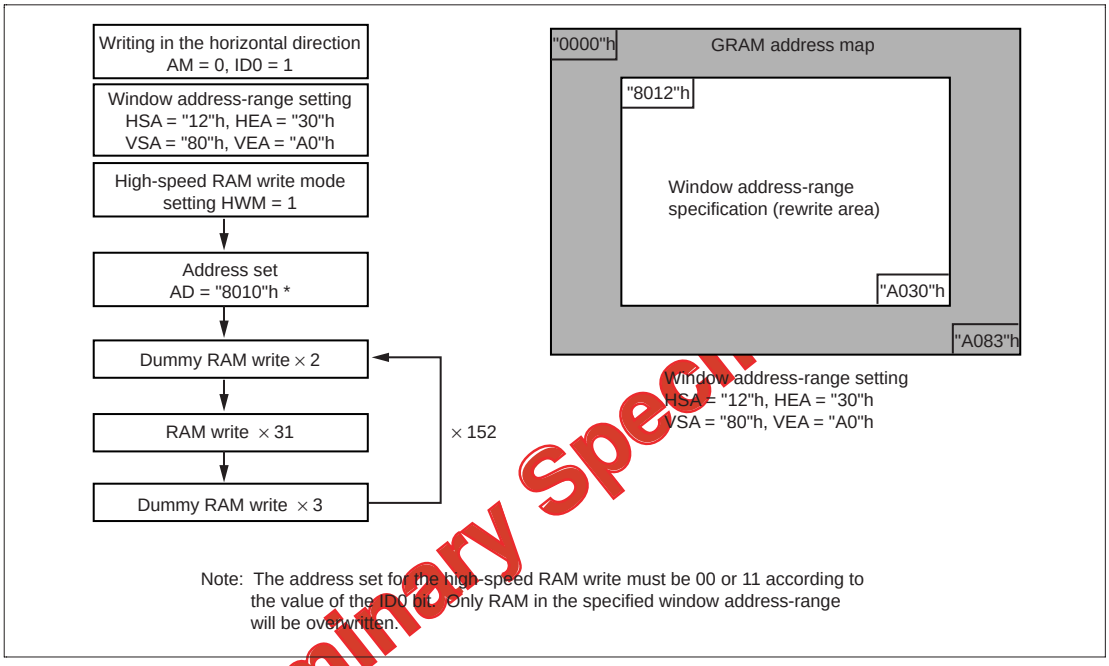


Figure 32 Example of the High-Speed RAM Write with a Window Address-Range Specification

Window Address Function

When data is written to the on-chip GRAM, a window address-range which is specified by the horizontal address register (start: HSA7-0, end: HEA7-0) or the vertical address register (start: VSA7-0, end: VEA7-0) can be written to consecutively.

Data is written to addresses in the direction specified by the AM bit (increment/decrement). When image data, etc. is being written, data can be written consecutively without thinking a data wrap by doing this.

The window must be specified to be within the GRAM address area described below. Addresses must be set within the window address.

[Restriction on window address-range settings]

(horizontal direction) 00H ≤ HSA7-0 ≤ HEA7-0 ≤ 3FH

(vertical direction) 00H ≤ VSA7-0 ≤ VEA7-0 ≤ AFH

[Restriction on address settings during the window address]

(RAM address) HSA5 to 0 ≤ AD7-0 ≤ HEA7-0

VSA7-0 ≤ AD15-8 ≤ VEA7-0

Note: In high-speed RAM-write mode, the lower two bits of the address must be set as shown below according to the value of the ID0 bit.

ID0=0: The lower two bits of the address must be set to 11.

ID0=1: The lower two bits of the address must be set to 00.

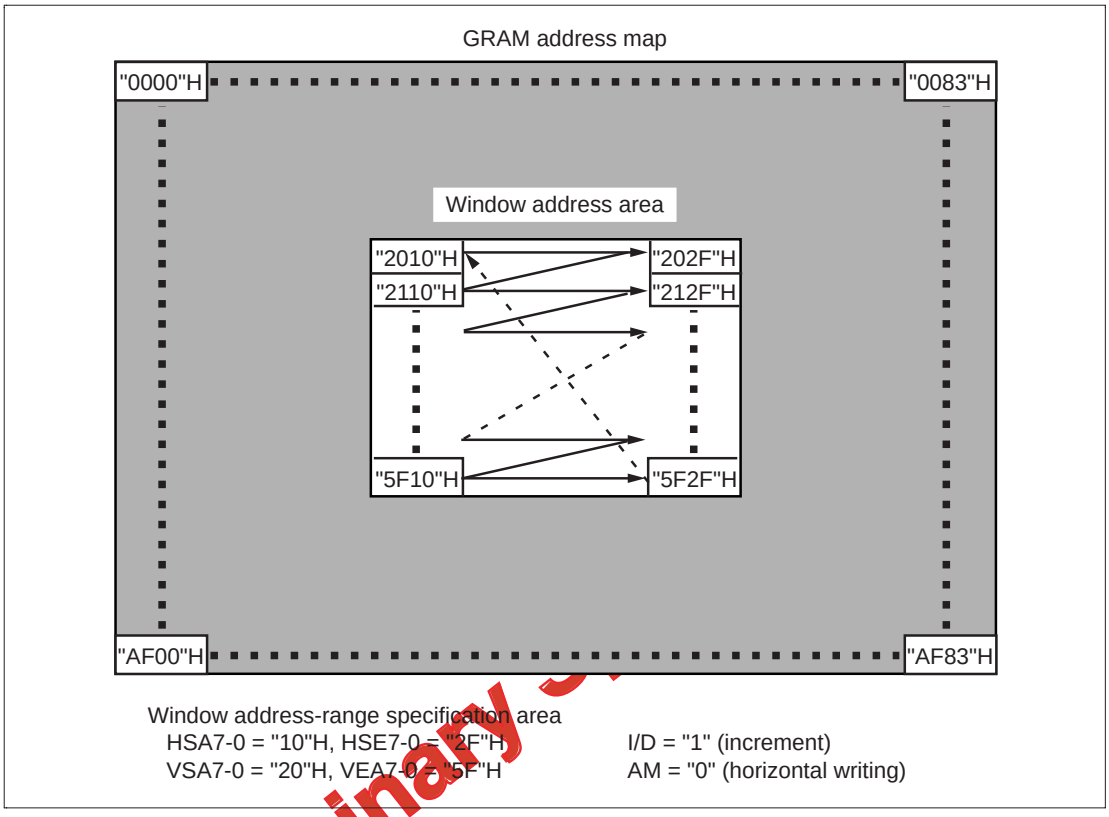


Figure 33 Example of Address Operation in the Window Address Specification

Graphics Operation Function

The HD66765 can greatly reduce the load of the microcomputer graphics software processing through the 16-bit bus architecture and internal graphics-bit operation function. This function supports the following:

1. A write data mask function that selectively rewrites some of the bits in the 12-bit write data.
2. A logical operation write function that writes the data sent from the microcomputer and the original RAM data by a logical operation.
3. A conditional write function that compares the original RAM data or write data and the compare-bit data and writes the data sent from the microcomputer only when the conditions match.

Even if the display size is large, the display data in the graphics RAM (GRAM) can be quickly rewritten.

The graphics bit operation can be controlled by combining the entry mode register, the bit set value of the RAM-write-data mask register, and the read/write from the microcomputer.

Table 23 Graphics Operation

	Bit Setting			
Operation Mode	**I/D**	**AM**	**LG2–0**	**Operation and Usage**
Write mode 1	0/1	0	000	Horizontal data replacement, horizontal-border drawing
Write mode 2	0/1	1	000	Vertical data replacement, vertical-border drawing
Write mode 3	0/1	0	110 111	Conditional horizontal data replacement, horizontal-border drawing
Write mode 4	0/1	1	110 111	Conditional vertical data replacement, vertical-border drawing
Read/write mode 1	0/1	0	001 010 011	Horizontal data write with logical operation, horizontal-border drawing
Read/write mode 2	0/1	1	001 010 011	Vertical data write with logical operation, vertical-border drawing
Read/write mode 3	0/1	0	100 101	Conditional horizontal data replacement, horizontal-border drawing
Read/write mode 4	0/1	1	100 101	Conditional vertical data replacement, vertical-border drawing

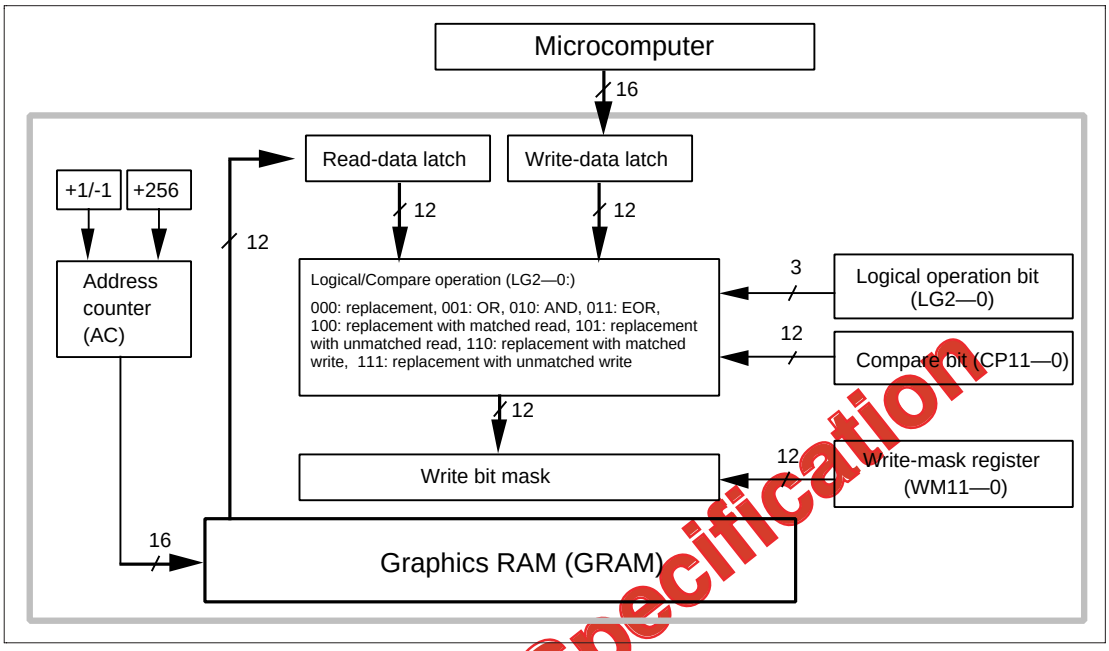


Figure 34 Data Processing Flow of the Graphics Operation

Write-data Mask Function

The HD66765 has a bit-wise write-data mask function that controls writing the two-byte data from the microcomputer to the GRAM. Bits that are 0 in the write-data mask register (WM11–0) cause the corresponding DB bit to be written to the GRAM. Bits that are 1 prevent writing to the corresponding GRAM bit to the GRAM; the data in the GRAM is retained. This function can be used when only one-pixel data is rewritten or the particular display color is selectively rewritten.

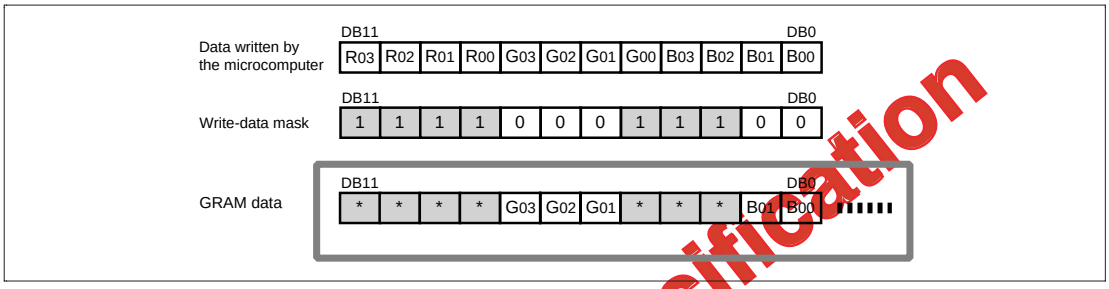


Figure 35 Example of Write-data Mask Function Operation

Logical/Compare Operation Function

The HD66765 performs a logical operation or conditional replacement between the two-byte write data sent from the microcomputer and the read data from the GRAM. The logical operation function has four types: replacement, OR, AND, and EOR. The conditional replacement performs a compare operation for the set value of the compare register (CP11–0) and the read data value from the GRAM, and rewrites only the pixel data in the GRAM that satisfies the conditions (in a byte unit). This function can be used when a particular color is selectively rewritten. The swap function or write-data mask function can be effectively used.

Table 24 Logical/Compare Operation

Bit Setting			
LG2	**LG1**	**LG0**	**Description of Logical/Compare Operation Function**
0	0	0	Writes the data written from the microcomputer directly to the GRAM. Only write processing is performed since the data in the read-data latch is not used.
0	0	1	ORs the data in the read-data latch and the data written by the microcomputer. Writes the result to GRAM. Read, modify, or write processing is performed.
0	1	0	ANDs the data in the read-data latch and the data written by the microcomputer. Writes the result to GRAM.
0	1	1	EORs the data in the read-data latch and the data written by the microcomputer. Writes the result to GRAM.
1	0	0	Compares the data in the read-data latch and the set value of the compare register (CP11–0). When the read data matches CP11–0, the data from the microcomputer is written to the GRAM. Only the particular color specified in the compare register can be rewritten. Read, modify, or write processing is performed.
1	0	1	Compares the data in the read-data latch and the set value of the compare register (CP11–0). When the read data does not match CP11–0, the data from the microcomputer is written to the GRAM. Colors other than the particular one specified in the compare register can be rewritten. Read, modify, or write processing is performed.
1	1	0	Compares the data written to the GRAM by the microcomputer and the set value of the compare register (CP11–0). When the write data matches CP11–0, the data from the microcomputer is written to the GRAM. Only write processing is performed.
1	1	1	Compares the data written to the GRAM by the microcomputer and the set value of the compare register (CP11–0). When the write data does not match CP11–0, the data from the microcomputer is written to the GRAM. Only write processing is performed.

Graphics Operation Processing

1. Write mode 1: AM = 0, LG2–0 = 000

   This mode is used when the data is horizontally written at high speed. It can also be used to initialize the graphics RAM (GRAM) or to draw borders. The write-data mask function (WM11–0) is also enabled in these operations. After writing, the address counter (AC) automatically increments by 1 (I/D = 1) or decrements by 1 (I/D = 0), and automatically jumps to the counter edge one-raster-row below after it has reached the left or right edge of the GRAM.

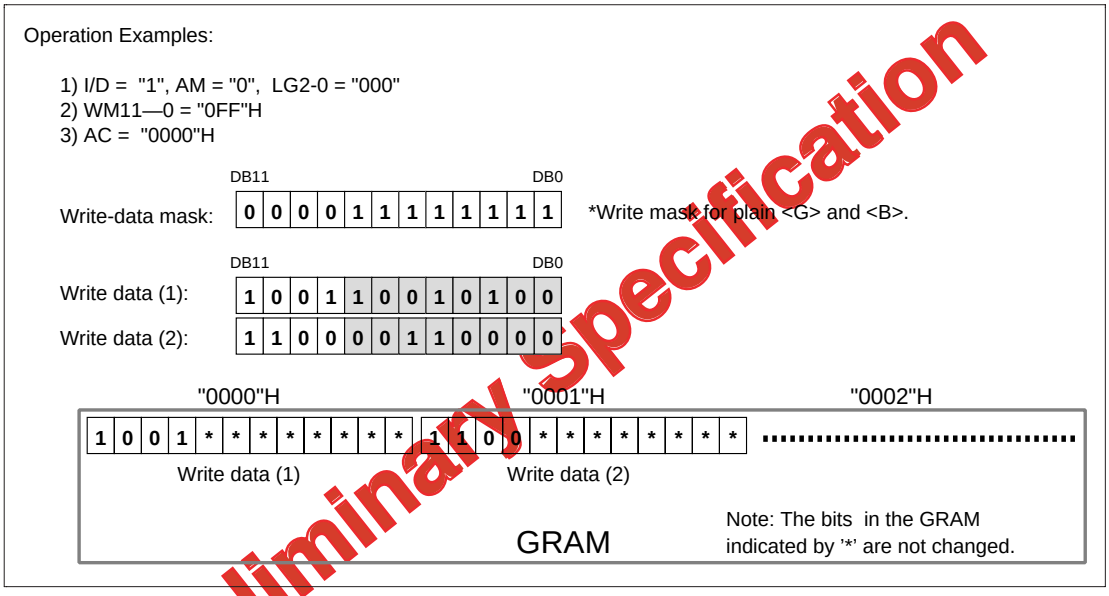


Figure 36 Writing Operation of Write Mode 1

2. Write mode 2: AM = 1, LG2–0 = 000

This mode is used when the data is vertically written at high speed. It can also be used to initialize the GRAM, develop the font pattern in the vertical direction, or draw borders. The write-data mask function (WM11–0) is also enabled in these operations. After writing, the address counter (AC) automatically increments by 256, and automatically jumps to the upper-right edge (I/D = 1) or upper-left edge (I/D = 0) following the I/D bit after it has reached the lower edge of the GRAM.

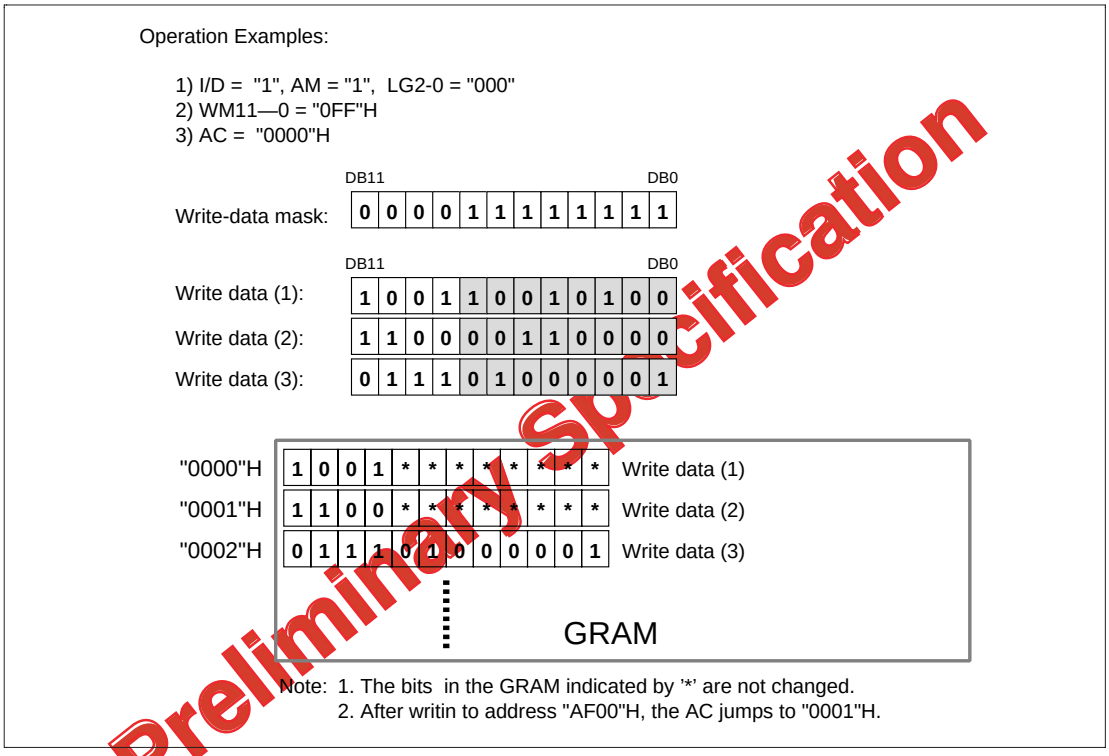


Figure 37 Writing Operation of Write Mode 2

3. Write mode 3: AM = 0, LG2–0 = 110/111

This mode is used when the data is horizontally written by comparing the write data and the set value of the compare register (CP11–0). When the result of the comparison in a byte unit satisfies the condition, the write data sent from the microcomputer is written to the GRAM. In this operation, the write-data mask function (WM11–0) is also enabled. After writing, the address counter (AC) automatically increments by 1 (I/D = 1) or decrements by 1 (I/D = 0), and automatically jumps to the counter edge one-raster-row below after it has reached the left or right edge of the GRAM.

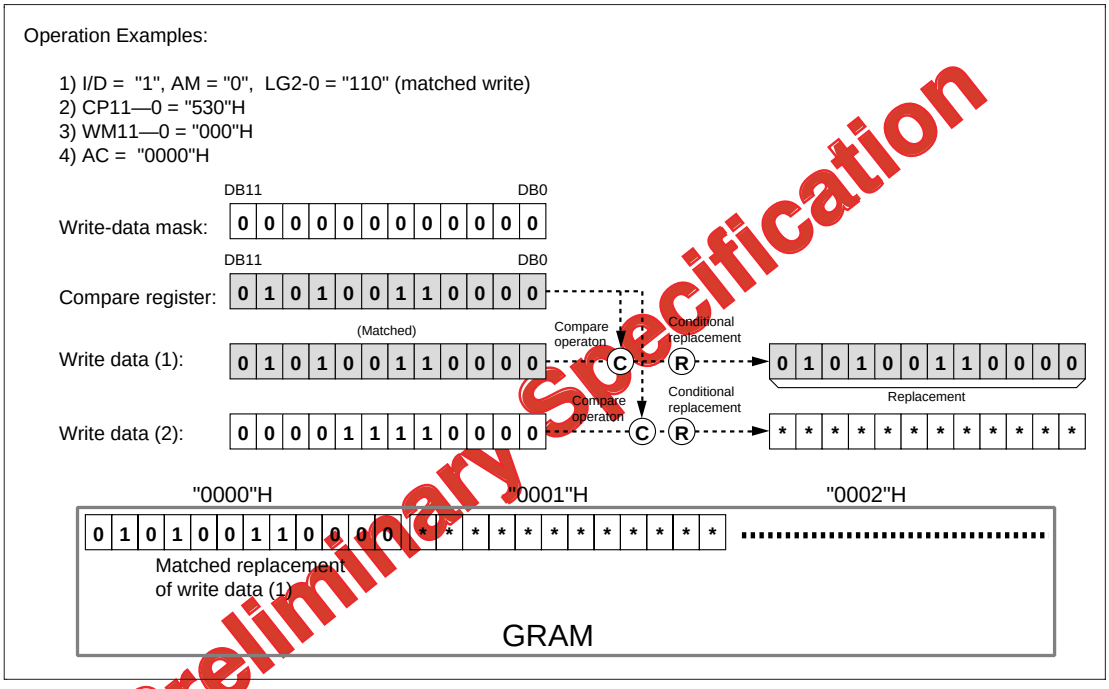


Figure 38 Writing Operation of Write Mode 3

4. Write mode 4: AM = 1, LG2–0 = 110/111

This mode is used when a vertical comparison is performed between the write data and the set value of the compare register (CP11–0) to write the data. When the result by the comparison in a byte unit satisfies the condition, the write data sent from the microcomputer is written to the GRAM. In this operation, the write-data mask function (WM11–0) are also enabled. After writing, the address counter (AC) automatically increments by 256, and automatically jumps to the upper-right edge (I/D = 1) or upper-left edge (I/D = 0) following the I/D bit after it has reached the lower edge of the GRAM.

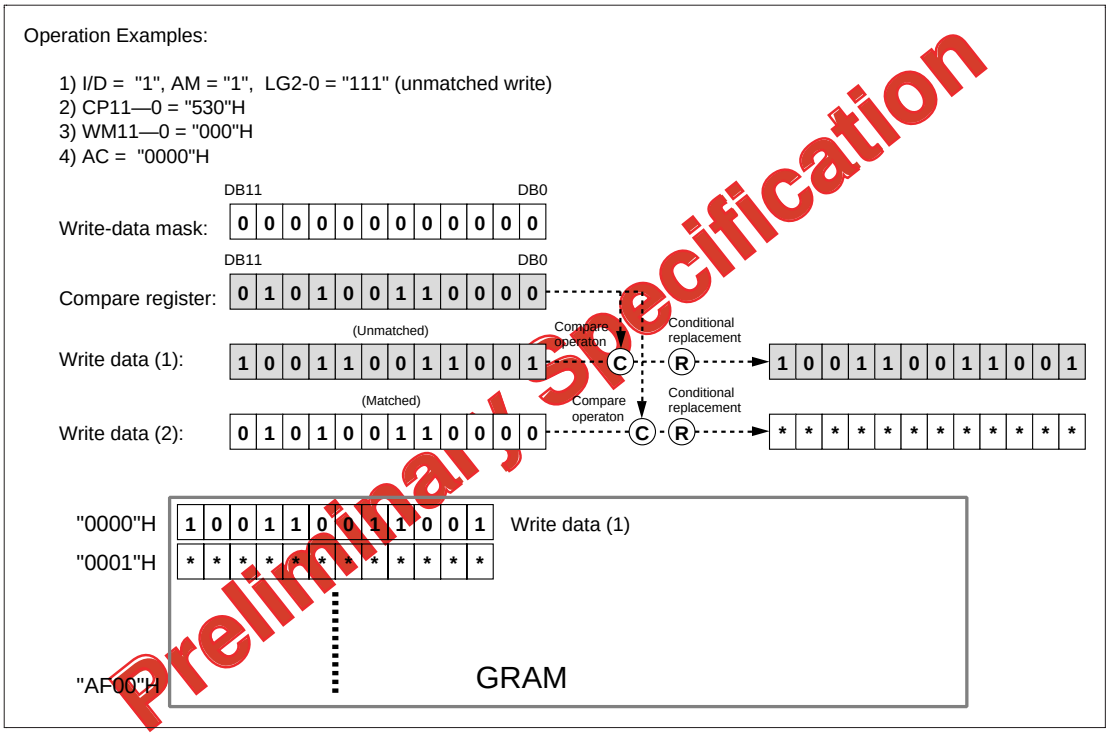


Figure 39 Writing Operation of Write Mode 4

5. Read/Write mode 1: AM = 0, LG2–0 = 001/010/011

This mode is used when the data is horizontally written at high speed by performing a logical operation with the original data. It reads the display data (original data), which has already been written in the GRAM, performs a logical operation with the write data sent from the microcomputer, and rewrites the data to the GRAM. This mode reads the data during the same access-pulse width (68-system: enabled high level, 80-system: RD* low level) as the write operation since reading the original data does not latch the read data into the microcomputer but temporarily holds it in the read-data latch. However, the bus cycle requires the same time as the read operation. The write-data mask function (WM11–0) is also enabled in these operations. After writing, the address counter (AC) automatically increments by 1 (I/D = 1) or decrements by 1 (I/D = 0), and automatically jumps to the counter edge one-raster-row below after it has reached the left or right edges of the GRAM.

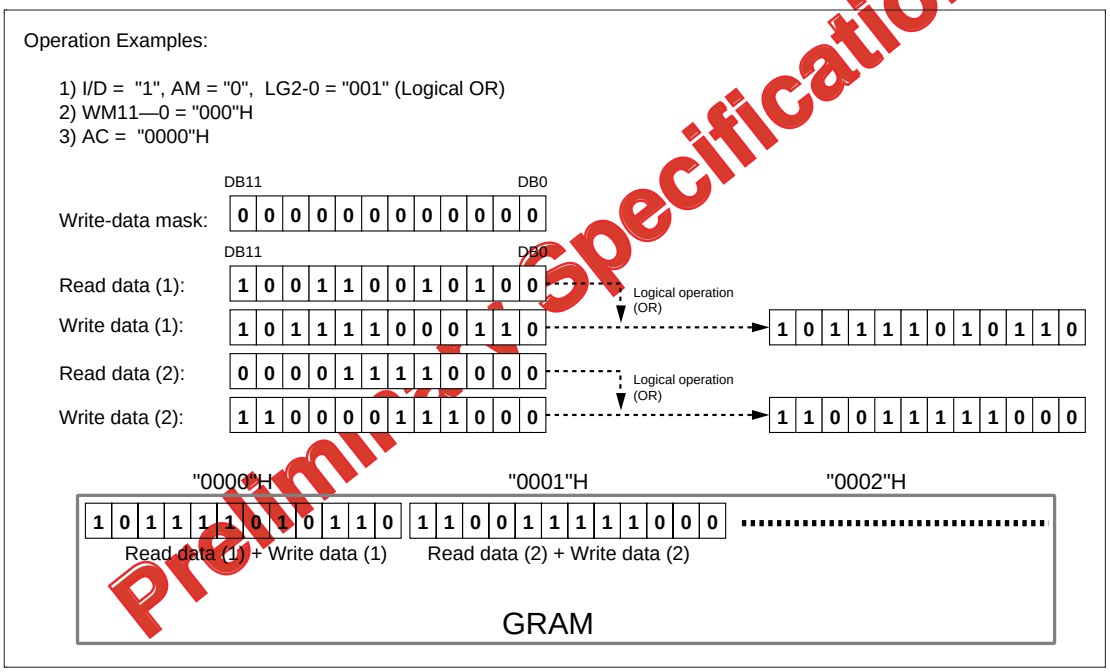


Figure 40 Writing Operation of Read/Write Mode 1

6. Read/Write mode 2: AM = 1, LG1–0 = 001/010/011

This mode is used when the data is vertically written at high speed by performing a logical operation with the original data. It reads the display data (original data), which has already been written in the GRAM, performs a logical operation with the write data sent from the microcomputer, and rewrites the data to the GRAM. This mode can read the data during the same access-pulse width (68-system: enabled high level, 80-system: RD* low level) as for the write operation since the read operation of the original data does not latch the read data into the microcomputer and temporarily holds it in the read-data latch. However, the bus cycle requires the same time as the read operation. The write-data mask function (WM11–0) is also enabled in these operations. After writing, the address counter (AC) automatically increments by 256, and automatically jumps to the upper-right edge (I/D = 1) or upper-left edge (I/D = 0) following the I/D bit after it has reached the lower edge of the GRAM.

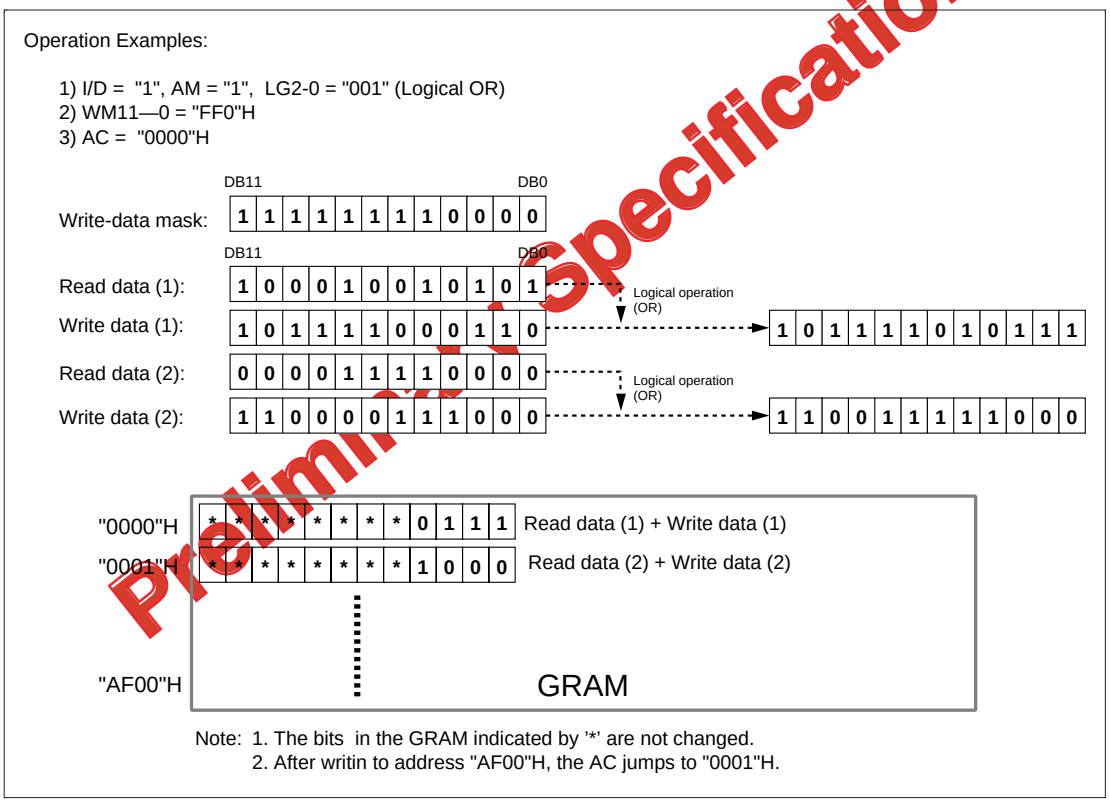


Figure 41 Writing Operation of Read/Write Mode 2

7. Read/Write mode 3: AM = 0, LG2–0 = 100/101

This mode is used when the data is horizontally written by comparing the original data and the set value of compare register (CP11–0). It reads the display data (original data), which has already been written in the GRAM, compares the original data and the set value of the compare register in byte units, and writes the data sent from the microcomputer to the GRAM only when the result of the comparison satisfies the condition. This mode reads the data during the same access-pulse width (68-system: enabled high level, 80-system: RD* low level) as write operation since reading the original data does not latch the read data into the microcomputer but temporarily holds it in the read-data latch. However, the bus cycle requires the same time as the read operation. The write-data mask function (WM11–0) is also enabled in these operations. After writing, the address counter (AC) automatically increments by 1 (I/D = 1) or decrements by 1 (I/D = 0), and automatically jumps to the counter edge one-raster-row below after it has reached the left or right edges of the GRAM.

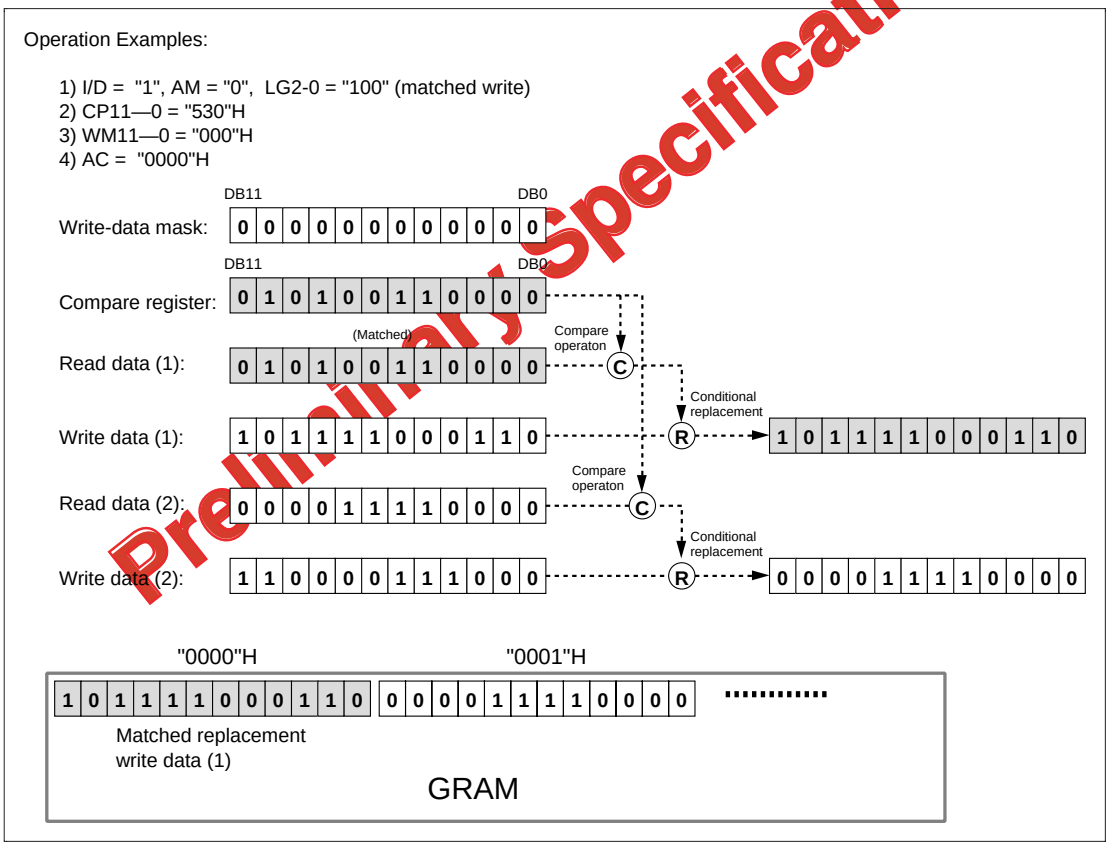


Figure 42 Writing Operation of Read/Write Mode 3

8. Read/Write mode 4: AM = 1, LG2–0 = 100/101

This mode is used when the data is vertically written by comparing the original data and the set value of the compare register (CP11–0). It reads the display data (original data), which has already been written in the GRAM, compares the original data and the set value of the compare register in byte units, and writes the data sent from the microcomputer to the GRAM only when the result of the compare operation satisfies the condition. This mode reads the data during the same access-pulse width (68-system: enabled high level, 80-system: RD* low level) as the write operation since reading the original data does not latch the read data into the microcomputer but temporarily holds it in the read-data latch. However, the bus cycle requires the same time as the read operation. The write-data mask function (WM11–0) is also enabled in these operations. After writing, the address counter (AC) automatically increments by 256, and automatically jumps to the upper-right edge (I/D = 1) or upper-left edge (I/D = 0) following the I/D bit after it has reached the lower edge of the GRAM.

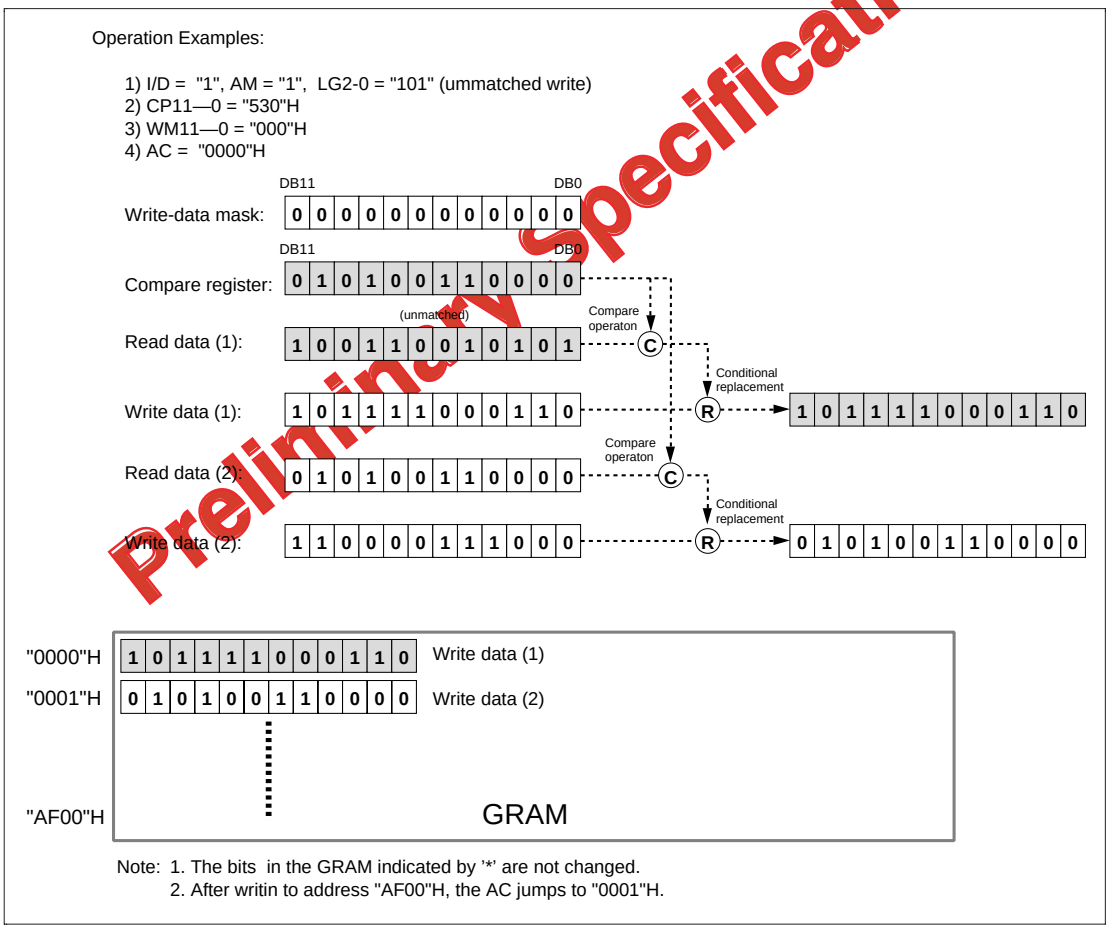


Figure 43 Writing Operation of Read/Write Mode 4

Grayscale Palette

The HD66765 incorporates a grayscale palette to simultaneously display 4,096 out of 13,824 possible colors. The grayscales consist of sixteen five-bit palettes. The 24-stage grayscale levels can be selected from the five-bit palette data.

In this palette, a pulse-width control system (PWM) is used to eliminate flicker in the LCD display. The time over which the LCDs are switched on is adjusted according to the level and grayscales are displayed so that flicker is reduced and grayscales are clearly displayed.

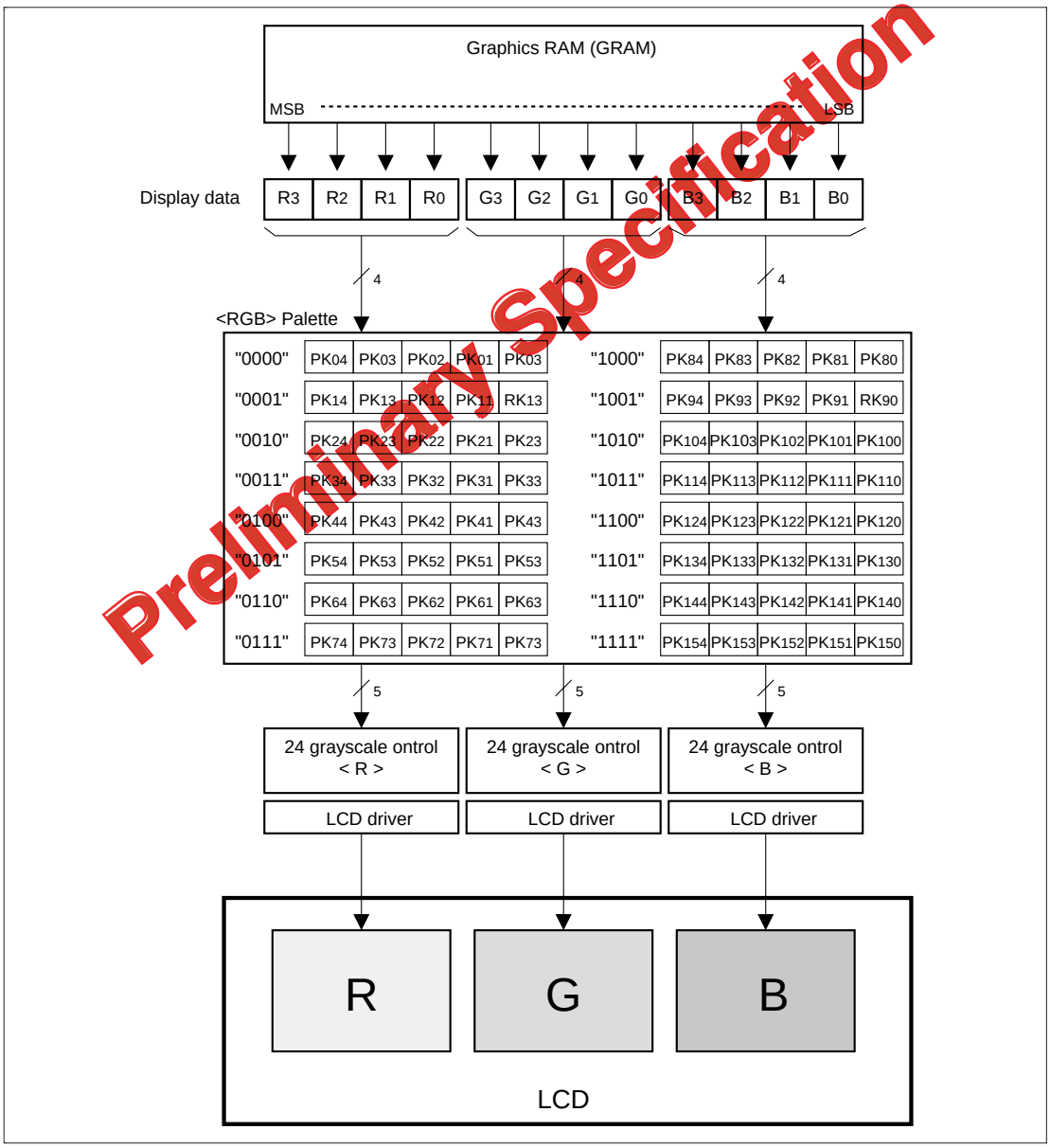


Figure 44 Grayscale Palette Control

Grayscale Palette Table

The grayscale register that is set for the RGB palette register (PK) can be set to any level. 24-grayscale lighting levels can be set according to palette values (00000 to 10111).

Table 25 Grayscale Control Level

Palette Register Value (PK)					Grayscale Control Level
0	0	0	0	0	Unlit level*1
0	0	0	0	1	2/24 level
0	0	0	1	0	3/24 level
0	0	0	1	1	4/24 level
0	0	1	0	0	5/24 level
0	0	1	0	1	6/24 level
0	0	1	1	0	7/24 level
0	0	1	1	1	8/24 level
0	1	0	0	0	9/24 level
0	1	0	0	1	10/24 level
0	1	0	1	0	11/24 level
0	1	0	1	1	12/24 level
0	1	1	0	0	13/24 level
0	1	1	0	1	14/24 level
0	1	1	1	0	15/24 level
0	1	1	1	1	16/24 level
1	0	0	0	0	17/24 level
1	0	0	0	1	18/24 level
1	0	0	1	0	19/24 level
1	0	0	1	1	20/24 level
1	0	1	0	0	21/24 level
1	0	1	0	1	22/24 level
1	0	1	1	0	23/24 level
1	0	1	1	1	All-lit level*2

Notes: 1. The unlit level corresponds to a black display when a normally-black color-LCD panel is used, and a white display when a normally-white color-LCD panel is used.

2. The all-lit level corresponds to a white display when a normally-black color-LCD panel is used, and a black display when a normally-white color-LCD panel is used.

Common Driver Interface

The HD66765 and the HD66764 common driver can drive displays of up to 132 (RGB) × 176 dots in size. Signals to set instructions for CR oscillation, the display timing signal, and the common driver are supplied from the HD66765 to the common driver. The LCD drive voltage is generated by the common driver. The LCD segment drive level (VSH) is also supplied from the common driver. On/off control of the display is required to be controlled by both the common and segment driver. Follow the on/off sequence of the display.

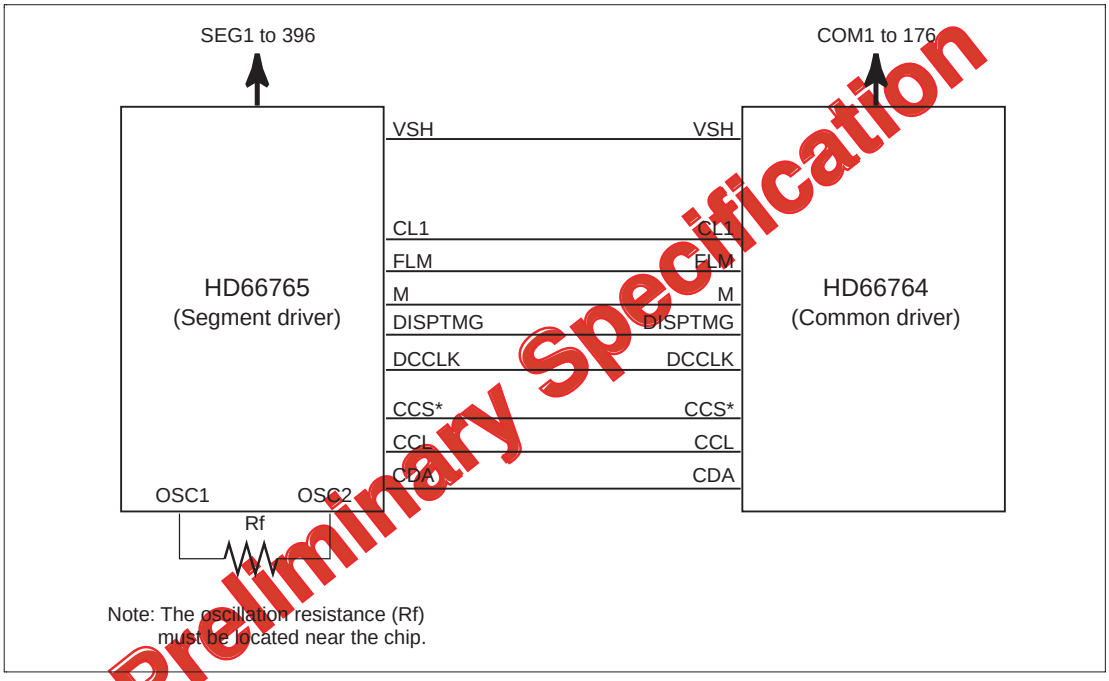


Figure 45 Connection to the Common Driver

Common Driver Serial Transfer

The HD66765 has an on-chip serial circuit to interface with the common driver (HD66764). Registers of the common driver can be set by transferring register settings from the HD66765. The serial interface consists of the serial chip select (CCS*), serial transfer clock (CCL), and serial transfer data (CDA) lines. The HD66765 serial interface circuit is only for transmitting, and cannot be used for receiving data from the common driver.

Serial transfer is started by setting the serial transfer register (TE) in the HD66765 to 1. After TE has been set to 1, CDA will be output in synchronization with CCS*, CCL, and CCL. Transfer is in 16-bit blocks. The data transferred consists of a common driver index register (IDX2 to 0) and an instruction for a register selected by IDX2 to 0. For more information on the common driver indices and instructions, refer to the common-driver data sheet. Serial transfer is independent of the HD66765's internal operation, so other instructions can be executed during transfer. Serial transfer to the common driver requires a maximum of 18 clock cycles.

When the serial transfer is finished, TE is automatically cleared to 0. After reading the register to confirm that TE=0, serial transfer of the next instruction may be started.

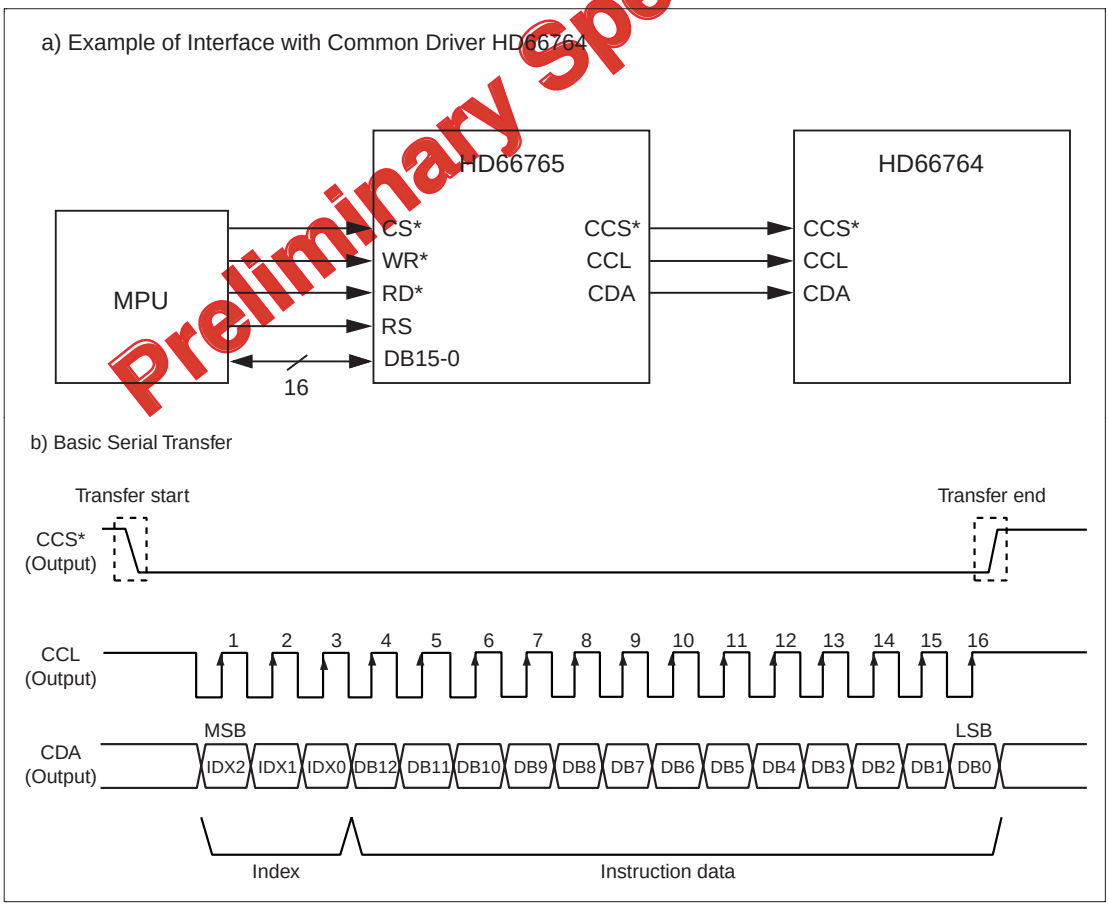


Figure 46 Common Driver Serial Transfer

c) Serial Transfer Sequence

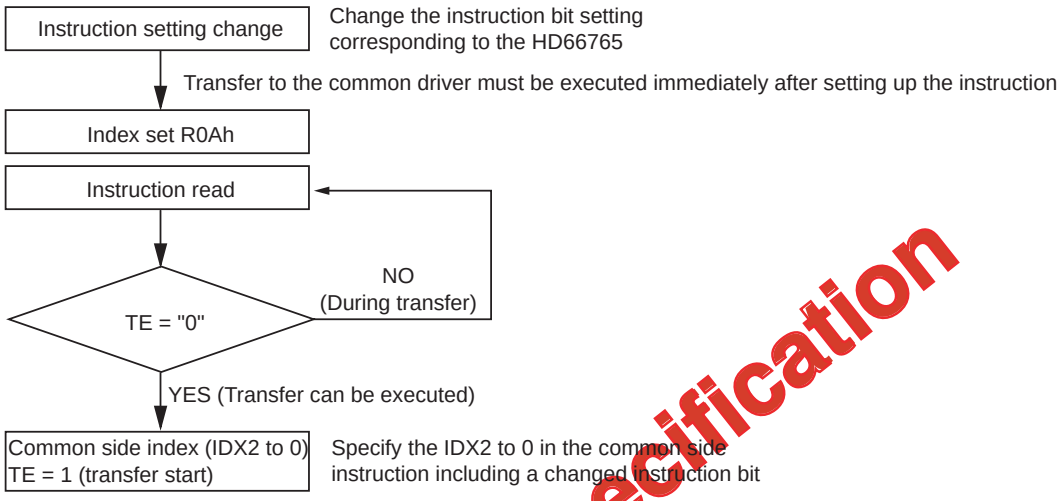


Figure 46 Common Driver Serial Transfer (cont)

Notes:
1. Transfer to the common driver must take place immediately after setting up the instruction.
2. The serial transfer period takes a maximum of 1/fosc × 18 clock cycles (sec).
3. Serial transfer cannot be executed in standby mode. If the chip enters standby mode during transfer, the serial transfer is forcibly suspended. Transfer must be executed again after standby has been canceled because correct transfer is not guaranteed in this situation.
4. Serial transfer can be forcibly suspended by writing TE=0. Transfer must be executed again because correct transfer is not guaranteed in this situation.
5. The instruction bit for the common driver is not executed when it is not transferred to the common driver. When the setting is changed, transfer must be executed again.

When transfer to the common driver is executed, the transfer is executed by using one of the following common driver (HD66764) instructions, corresponding to the value set by the IDX2 to 0.

Table 26 Common Driver (HD66764) Instructions

IDX2	IDX1	IDX0	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	BS2	BS1	BS0	BT3	BT2	BT1	BT0	0	DC1	DC0	AP1	AP0	SLP
0	0	1	0	0	0	0	0	0	0	0	0	0	VC2	VC1	VC0
0	1	0	0	VR3	VR2	VR1	VR0	0	CT6	CT5	CT4	CT3	CT2	CT1	CT0
0	1	1	0	0	D1	CMS	SPT	SS17	SS16	SS15	SS14	SS13	SS12	SS11	SS10
1	0	0	0	0	0	0	0	SE17	SE16	SE15	SE14	SE13	SE12	SE11	SE10
1	0	1	0	0	0	0	0	SS27	SS26	SS125	SS24	SS23	SS22	SS21	SS20
1	1	0	0	0	0	0	0	SE27	SE26	SE25	SE24	SE23	SE22	SE21	SE20

Instruction Setting Flow

When the common driver HD66764 is used, follow the below about each instruction setting. The instruction setting for the common driver is executed by the serial interface. When the instruction for the common driver is set, the serial transfer must be executed to the common driver. The transfer to the common driver must be executed immediately after the instruction set.

Follow the below serial transfer flow about each setting and then transfer must be executed.

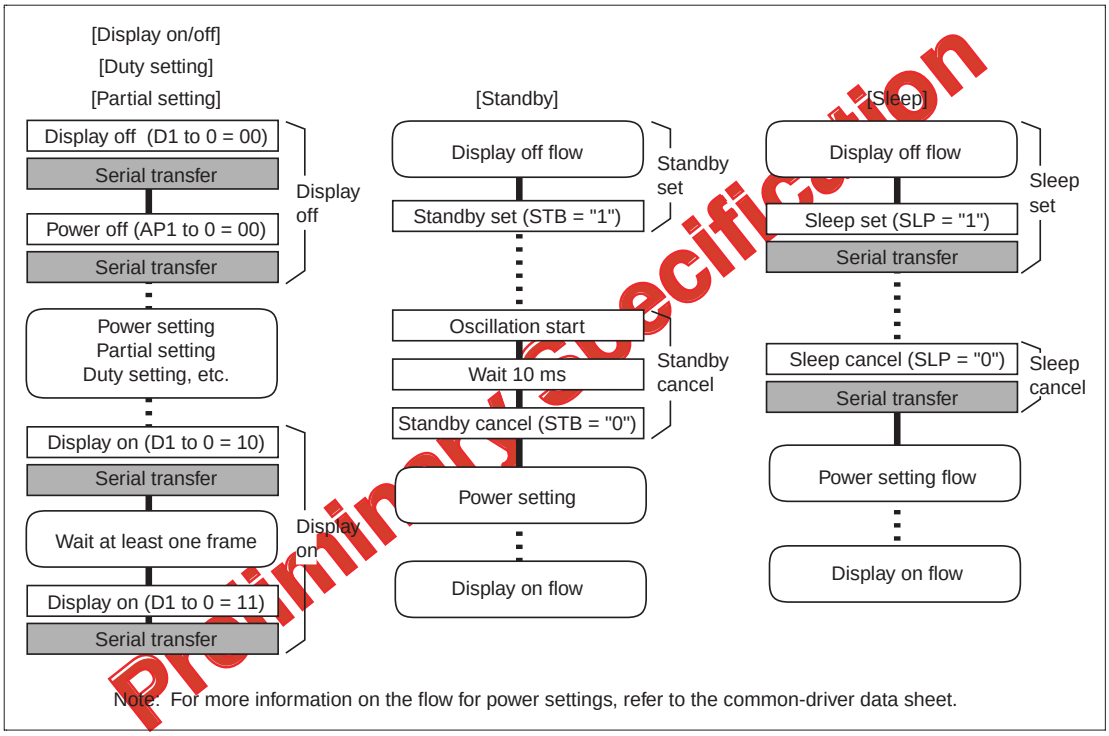


Figure 47 Instruction Setting Flow

Oscillation Circuit

The HD66765 can oscillate between the OSC1 and OSC2 pins using an internal R-C oscillator with an external oscillation resistor. Note that in R-C oscillation, the oscillation frequency is changed according to the external resistance value, wiring length, or operating power-supply voltage. If Rf is increased or power supply voltage is decrease, the oscillation frequency decreases. For the relationship between Rf resistor value and oscillation frequency, see the Electric Characteristics Notes section.

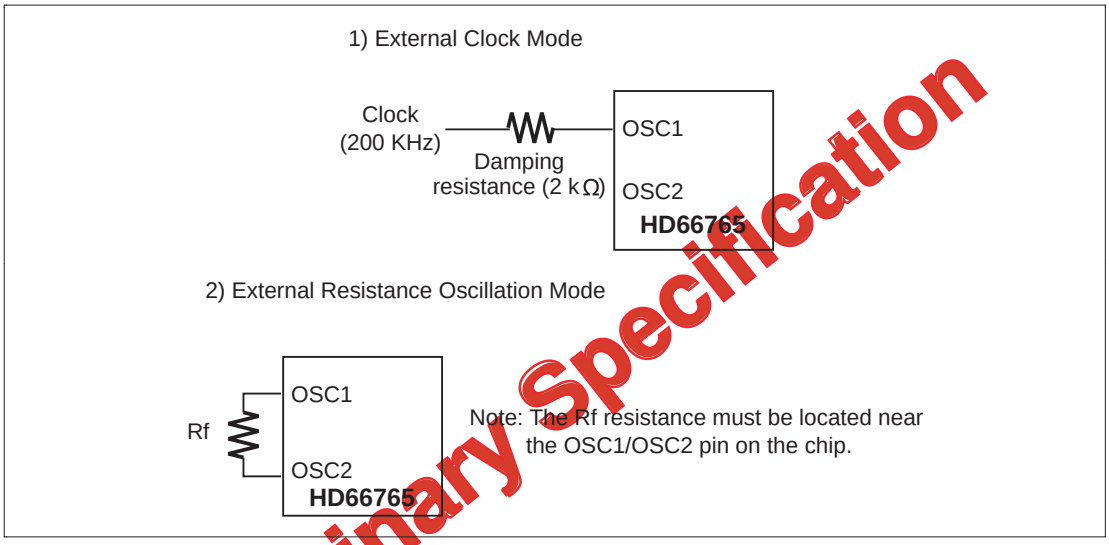


Figure 48 Oscillation Circuits

When using the HD66765 with the HD66764 common driver, the relationship between the SEG and COM output levels is as shown in the following figure. The LCD drive level (VSH, VSL) which is used by the HD66765 is supplied from the HD66764 common driver. While the display is off, SEG and COM outputs go to GND level.

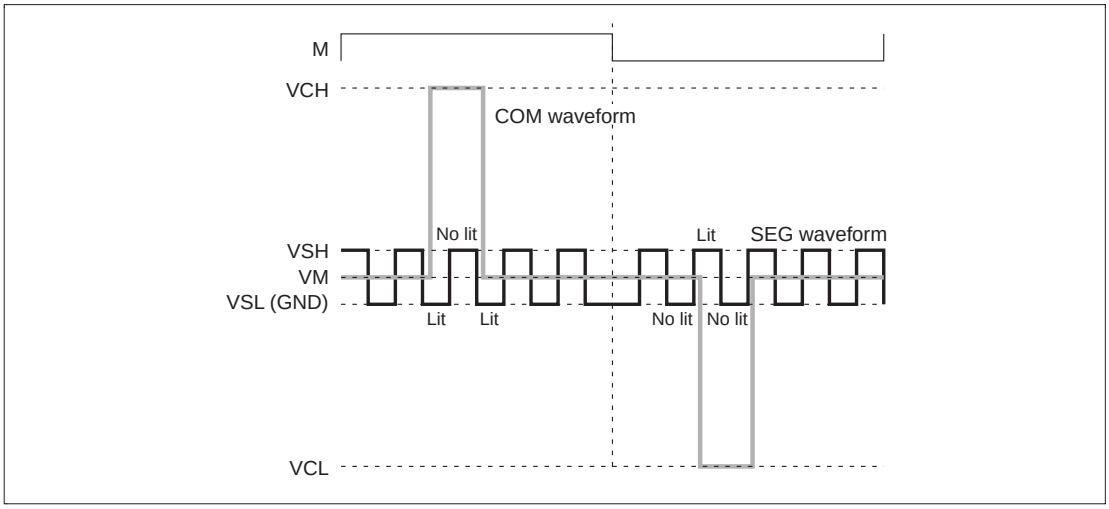


Figure 49 Relationship with SEG/COM Output Level

Frame-Frequency Adjustment Function

The HD66765 has an on-chip frame-frequency adjustment function. The frame frequency can be adjusted by the instruction setting (DIV, RTN) during the LCD drive as the oscillation frequency is always same. When the display duty is changed, the frame frequency can be adjusted to be the same.

If the oscillation frequency is set to high, an animation or a static image can be displayed in suitable ways by changing the frame frequency. When a static image is displayed, the frame frequency can be set low and the low-power consumption mode can be entered. When high-speed screen switching, for an animated display, etc. is required, the frame frequency can be set high.

Relationship between LCD Drive Duty and Frame Frequency

The relationship between the LCD drive duty and the frame frequency is calculated by the following expression. The frame frequency can be adjusted in the retrace-line period bit (RTN) and in the operation clock division bit (DIV) by the instruction.

(Formula for the frame frequency)

$$\text{Frame frequency} = \frac{fosc}{\text{Clock cycles per raster-row} \times \text{division ratio} \times 1/\text{duty cycle}} \quad [\text{Hz}]$$

fosc: R-C oscillation frequency

Duty: drive duty (NL bit)

Division ratio: DIV bit

Clock cycles per raster-row: (RTN + 25) clock cycles

Example Calculation 1 To set the maximum frame frequency to 60 Hz

Display duty: 1/176

Retrace-line period: 0 clock (RTN3 to 0 = 0000)

Operation clock division ratio: 1 division

fosc = 60 Hz × (0 + 25) clock × 1 division × 176 lines = 264 (kHz)

In this case, the CR oscillation frequency becomes 264 kHz. The external resistance value of the CR oscillator must be adjusted to be 264 kHz. The display duty can be changed by the partial display, etc. and the frame frequency can be the same by setting the RNT bit and DIV bit to achieve the following.

Partial display

Display duty: 1/40

Retrace-line period: 3 clock (RTN3 to 0 = 0011)

Operation clock division ratio: 4 division

Frame frequency = 264 kHz/ ((3 + 25) clock × 4 division × 40 lines) = 58.9 (Hz)

Example Calculation 2 Switching the frame frequency to suit animation/static image display

(Animation display)

Frame frequency: 90 Hz

Display duty: 1/176

Retrace-line period: 0 clock (RTN3 to 0 = 0000)

Operation clock division ratio: 1 division

fosc = 90 Hz × (0 + 25) clock × 1 division × 176 lines = 396 (kHz)

(Static image display)

Frame frequency: 60 Hz

Display duty: 1/176

Retrace-line period: 13 clock (RTN3 to 0 = 1101)

Operation clock division ratio: 1 division

Frame frequency: 396 kHz/ ((13 + 25) clock × 2 division × 176 lines) = 59.2 (Hz)

n-raster-row Reversed AC Drive

The HD66765 supports not only the LCD reversed AC drive in a one-frame unit (B-pattern waveform) but also the n-raster-row reversed AC drive which alternates in an n-raster-row unit from one to 64 raster-rows (C-pattern waveform). When a problem affecting display quality occurs, such as crosstalk at high-duty driving of more than 1/64 duty, the n-raster-row reversed AC drive (C-pattern waveform) can improve the quality.

Determine the number of raster-rows n (NW bit set value + 1) for alternating after confirmation of the display quality with the actual LCD panel. However, if the number of AC raster-rows is reduced, the LCD alternating frequency becomes high. Because of this, the charge or discharge current is increased in the LCD cells.

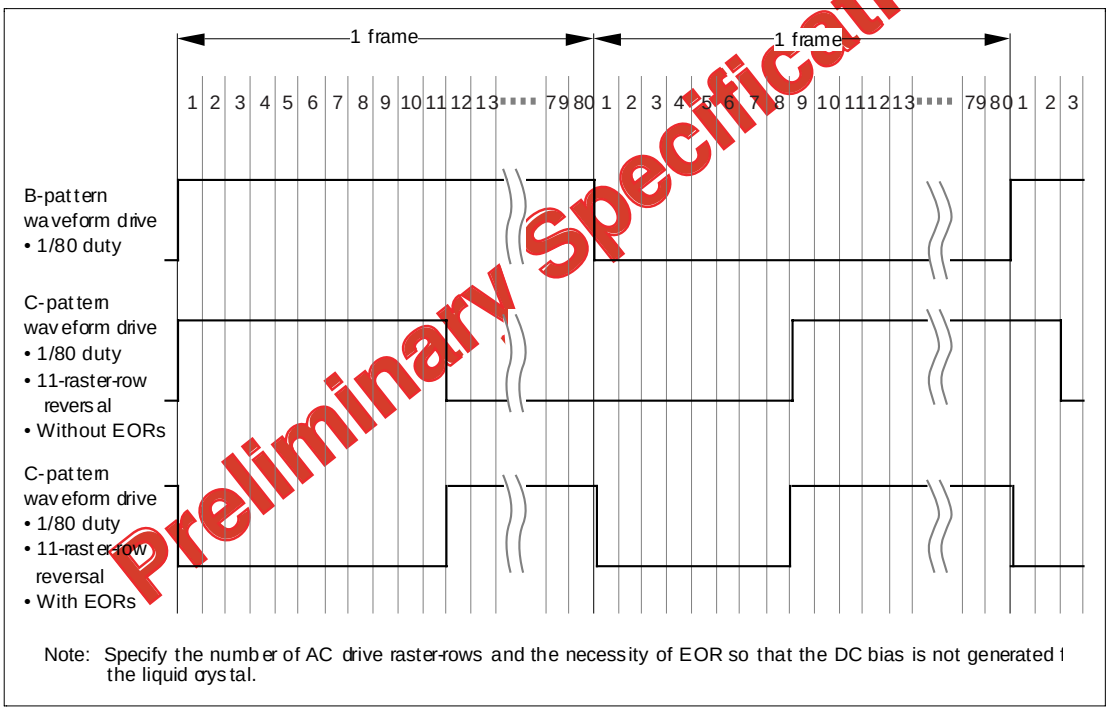


Figure 50 Example of an AC Signal under n-raster-row Reversed AC Drive

Screen-division Driving Function

The HD66765 can select and drive two screens at any position with the screen-driving position registers (R14h and R15h). Any two screens required for display are selectively driven and a duty ratio is lowered by LCD-driving duty setting (NL4-0), thus reducing LCD-driving voltage and power consumption.

For the 1st division screen, start line (SS17-10) and end line (SE17-10) are specified by the 1st screen-driving position register (R14h). For the 2nd division screen, start line (SS27-20) and end line (SE27-20) are specified by the 2nd screen-driving position register (R15h). The 2nd screen control is effective when the SPT bit is 1. The total count of selection-driving lines for the 1st and 2nd screens must correspond to the LCD-driving duty set value.

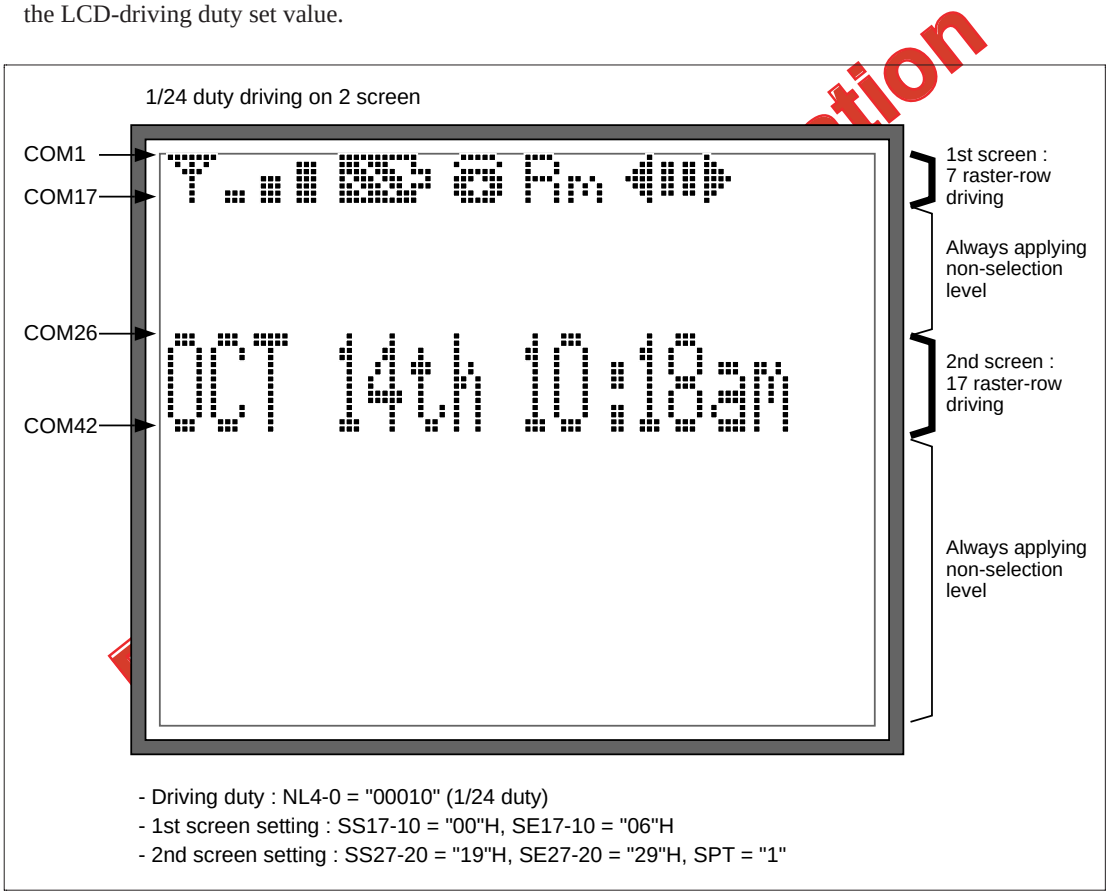


Figure 51 Display example in 2-screen division driving

Restrictions on the 1st/2nd Screen Driving Position Register Settings

The following restrictions must be satisfied when setting the start line (SS17-10) and end line (SE17-10) of the 1st screen driving position register (R14) and the start line (SS27-20) and end line (SE27-20) of the 2nd screen driving position register (R15) for the HD66765. Note that incorrect display may occur if the restrictions are not satisfied.

Table 27 Restrictions on the 1st/2nd Screen Driving Position Register Settings

	1st Screen Driving (SPT = 0)	2nd Screen Driving (SPT = 1)
Register setting	SS17-10 ≤ SE17-0 ≤ AFH	SS17-10 ≤ SE17-10 < SS27-20 ≤ SE27-20 ≤ AFH
Display operation	• Time-sharing driving for COM pins (SS1+1) to (SE1+1) • Non-selection level driving for others	• Time-sharing driving for COM pins (SS1+1) to (SE1+1) and (SS2+1) to (SE2+1) • Non-selection level driving for others

Notes:
1. When the total line count in screen division driving settings is less than the duty setting, non-selection level driving is performed without the screen division driving setting range.
2. When the total line count in screen division driving settings is larger than the duty setting, the start line, the duty-setting line, and the lines between them are displayed and non-selection level driving is performed for other lines.
3. For the 1st screen driving, the SS27-20 and SE27-20 settings are ignored.

Modification history

Revision 0.1

- First release

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