HD66760

104 × 80-dot Graphics LCD Controller/Driver for 256 Colors

HITACHI

ADE-207-335A(Z)
Rev.2.0
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Description

The HD66760, color-graphics LCD controller and driver LSI, displays 104-by-80-dot graphics for 256 STN colors. The HD66760's bit-operation functions and a 16-bit high-speed bus interface enable efficient data transfer and high-speed rewriting of data to the graphics RAM.

The HD66760 has various functions for reducing the power consumption of an LCD system, such as low-voltage operation of 2.2 V/min., a step-up circuit to generate a maximum of six-times the LCD drive voltage from the supplied voltage, and voltage-followers to decrease the direct current flow in the LCD drive bleeder-resistors. Combining these hardware functions with software functions, such as a partial display with low-duty drive and standby and sleep modes, allows precise power control. The HD66760 is suitable for any mid-sized or small portable battery-driven product requiring long-term driving capabilities, such as digital cellular phones supporting a WWW browser, bidirectional pagers, and small PDAs.

Features

- 104 × 80-dot graphics display LCD controller/driver for 256 STN colors
- Display mode change between 256 colors (8 bits per pixel) and four colors (2-bit per pixel)
- 16/8-bit high-speed bus interface
- I2C bus interface
- Clock synchronized serial interface
- Bit-operation functions for graphics processing:
  - — Write-data mask function in bit units
  - — Swap function of upper and lower bytes
  - — Logical operation in pixel unit and conditional write function
- Various color-display control functions:
  - — 256 of the 4,096 possible colors can be displayed at the same time (grayscale palette incorporated)
  - — Vertical scroll display function in raster-row units
  - — Color window cursor display supported by hardware
- Low-power operation supports:

Preliminary: The specifications of this device are subject to change without notice. Please contact your nearest Hitachi's Sales Dept. regarding specification.

Hitachi semiconductor

  - — Vcc = 2.2 to 3.6 V (low voltage)
  - — V_{LCD} (= V_{LPS} – GND) = 5 to 15.5 V (liquid crystal drive voltage)
  - — Three-, four-, five-, or six-times step-up circuit for liquid crystal drive voltage
  - — 128-step contrast adjuster and voltage followers to decrease direct current flow in the LCD drive bleeder-resistors
  - — Power-save functions such as the standby mode and sleep mode
  - — Partial LCD drive of two screens in any position
  - — Programmable drive duty ratios (1/16-1/80) and bias values (1/4-1/10) displayed on LCD
- Internal RAM capacity: 8,320 bytes
- 312-segment × 80-common liquid crystal display driver
- n-raster-row AC liquid-crystal drive (C-pattern waveform drive)
- Internal oscillation, hardware reset and software reset
- Shift change of segment and common drivers

Total Current Consumption Characteristics (Vcc = 3.0 V, TYP Conditions, LCD Drive Power Current Included)

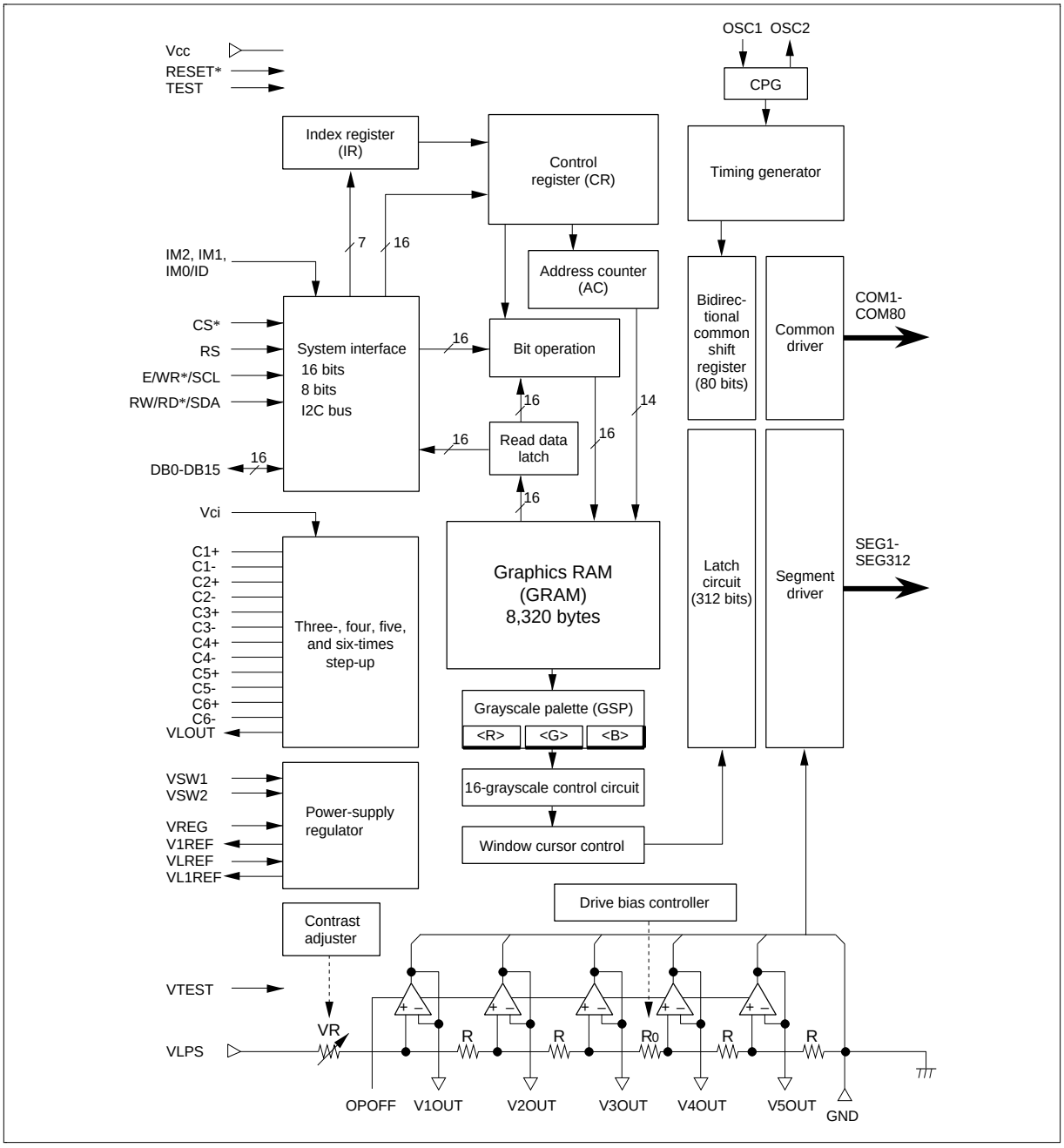
				Total Power Consumption			
				Normal Display Operation			
Character Display Dot Size	Duty Ratio	R-C Oscillation Frequency	Frame Frequency	Internal Logic	LCD Power	Total*	Standby Mode
104 × 16 dots	1/16	180 kHz	70 Hz	(50 µA)	(25 µA)	Four-times (150 µA)	0.2 µA
104 × 24 dots	1/24	180 kHz	70 Hz	(60 µA)	(25 µA)	Four-times (160 µA)	
104 × 56 dots	1/56	180 kHz	70 Hz	(100 µA)	(25 µA)	Five-times (225 µA)	
104 × 64 dots	1/64	180 kHz	70 Hz	(110 µA)	(25 µA)	Five-times (235 µA)	
104 × 72 dots	1/72	180 kHz	70 Hz	(120 µA)	(25 µA)	Six-times (270 µA)	
104 × 80 dots	1/80	180 kHz	70 Hz	(130 µA)	(25 µA)	Six-times (280 µA)	

Note : When a three-, four-, five-, or six-times step-up is used:
the total power consumption = internal logic current + LCD power current x 3 (three-times step-up),
the total power consumption = internal logic current + LCD power current x 4 (four-times step-up),
the total power consumption = internal logic current + LCD power current x 5 (five-times step-up), and
the total power consumption = internal logic current + LCD power current x 6 (six-times step-up)

Type Name

Types	External Dimensions	Interface
HD66760TB0	Bending TCP	Parallel and clock synchronized serial interface
HD66760WTxx	Bending TCP	Parallel and I2C interface
HCD66760BP	Au-bumped chip	Parallel and clock synchronized serial interface
HCD66760WBP	Au-bumped chip	Parallel and I2C interface

HD66760 Block Diagram



HD66760 Pad Arrangement

- Chip size: 14.4 mm × 3.1 mm
- Chip thickness: 550 µm (typ.)
- PAD coordinates: PAD center
- Coordinate origin: Chip center
- Au bump size (pin number is shown in the blacket)

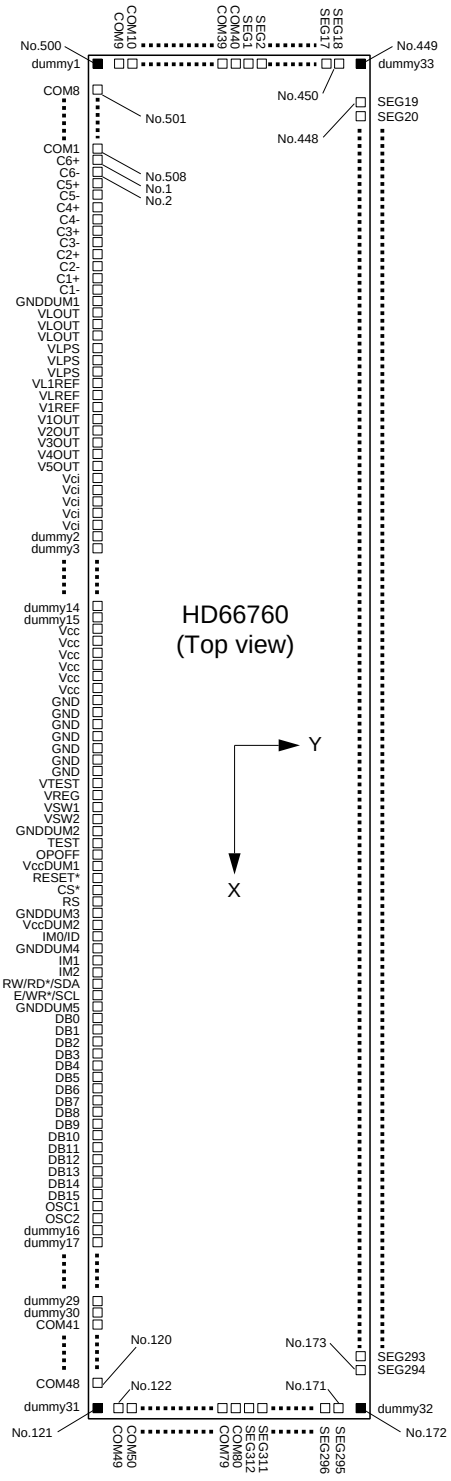
(1) 80 µm × 80 µm
dummy1 (500), dummy31 (121), dummy32 (172) and dummy33 (449)
from C6 + (1) to dummy30 (112)

(2) 35 µm × 80 µm
from SEG294 (173) to SEG19 (448)

(3) 80 µm × 35 µm
from COM49 (122) to SEG295 (171)
from SEG18 (450) to COM9 (499)

(4) 45 µm × 80 µm
from COM8 (501) to COM1 (508)
from COM41 (113) to COM48 (120)

- Au bump pitch: Refer PAD coordinate
- Au bump height: 15 µm (typ.)



HD66760 Pad Coordinates

(Unit : um)

No.	PAD NAME	X	Y
1	C6+	-6285	-1387
2	C6-	-6185	-1387
3	C5+	-6085	-1387
4	C5-	-5985	-1387
5	C4+	-5885	-1387
6	C4-	-5785	-1387
7	C3+	-5685	-1387
8	C3-	-5585	-1387
9	C2+	-5485	-1387
10	C2-	-5385	-1387
11	C1+	-5285	-1387
12	C1-	-5185	-1387
13	GNDDUM1	-5078	-1387
14	VLOUT	-4971	-1387
15	VLOUT	-4871	-1387
16	VLOUT	-4771	-1387
17	VLPS	-4671	-1387
18	VLPS	-4571	-1387
19	VLPS	-4471	-1387
20	VL1REF	-4329	-1387
21	VLREF	-4229	-1387
22	V1REF	-4129	-1387
23	V1OUT	-4029	-1387
24	V2OUT	-3929	-1387
25	V3OUT	-3829	-1387
26	V4OUT	-3729	-1387
27	V5OUT	-3629	-1387
28	VCI	-3486	-1387
29	VCI	-3386	-1387
30	VCI	-3286	-1387
31	VCI	-3186	-1387
32	VCI	-3086	-1387
33	dummy2	-2908	-1387
34	dummy3	-2808	-1387
35	dummy4	-2708	-1387
36	dummy5	-2608	-1387
37	dummy6	-2508	-1387
38	dummy7	-2408	-1387
39	dummy8	-2308	-1387
40	dummy9	-2208	-1387
41	dummy10	-2108	-1387
42	dummy11	-2008	-1387
43	dummy12	-1908	-1387
44	dummy13	-1808	-1387
45	dummy14	-1708	-1387
46	dummy15	-1608	-1387
47	VCC	-1465	-1387
48	VCC	-1365	-1387
49	VCC	-1265	-1387
50	VCC	-1165	-1387
51	VCC	-1065	-1387
52	VCC	-965	-1387
53	GND	-822	-1387
54	GND	-722	-1387
55	GND	-622	-1387
56	GND	-522	-1387
57	GND	-422	-1387
58	GND	-322	-1387
59	GND	-222	-1387
60	VTEST	-80	-1387
61	VREG	65	-1387
62	VSW1	210	-1387
63	VSW2	355	-1387
64	GNDDUM2	455	-1387
65	TEST	555	-1387
66	OPOFF	655	-1387
67	VCCDUM1	755	-1387
68	RESET*	855	-1387
69	CS*	1000	-1387
70	RS	1144	-1387
71	GNDDUM3	1244	-1387
72	VCCDUM2	1344	-1387
73	IM0/ID	1444	-1387
74	GNDDUM4	1544	-1387
75	IM1	1644	-1387
76	IM2	1789	-1387
77	RW/RD*/SDA	1934	-1387
78	E/WR*/SCL	2079	-1387
79	GNDDUM5	2179	-1387
80	DB0	2279	-1387
81	DB1	2424	-1387
82	DB2	2568	-1387
83	DB3	2713	-1387
84	DB4	2858	-1387
85	DB5	3003	-1387
86	DB6	3148	-1387
87	DB7	3292	-1387
88	DB8	3437	-1387
89	DB9	3582	-1387
90	DB10	3727	-1387
91	DB11	3872	-1387
92	DB12	4016	-1387
93	DB13	4161	-1387
94	DB14	4306	-1387
95	DB15	4451	-1387
96	OSC1	4596	-1387
97	OSC2	4740	-1387
98	dummy16	4885	-1387
99	dummy17	4985	-1387
100	dummy18	5085	-1387
101	dummy19	5185	-1387
102	dummy20	5285	-1387
103	dummy21	5385	-1387
104	dummy22	5485	-1387
105	dummy23	5585	-1387
106	dummy24	5685	-1387
107	dummy25	5785	-1387
108	dummy26	5885	-1387
109	dummy27	5985	-1387
110	dummy28	6085	-1387
111	dummy29	6185	-1387
112	dummy30	6285	-1387
113	COM41	6475	-1387
114	COM42	6536	-1387
115	COM43	6596	-1387
116	COM44	6656	-1387
117	COM45	6716	-1387
118	COM46	6776	-1387
119	COM47	6837	-1387
120	COM48	6897	-1387
121	dummy31	7066	-1387
122	COM49	7066	-1215
123	COM50	7066	-1165
124	COM51	7066	-1115
125	COM52	7066	-1064
126	COM53	7066	-1014
127	COM54	7066	-964
128	COM55	7066	-914
129	COM56	7066	-864
130	COM57	7066	-813
131	COM58	7066	-763
132	COM59	7066	-713
133	COM60	7066	-663
134	COM61	7066	-613
135	COM62	7066	-562
136	COM63	7066	-512
137	COM64	7066	-462
138	COM65	7066	-412
139	COM66	7066	-362
140	COM67	7066	-311
141	COM68	7066	-261
142	COM69	7066	-211
143	COM70	7066	-161
144	COM71	7066	-111
145	COM72	7066	-60
146	COM73	7066	-10
147	COM74	7066	40
148	COM75	7066	90
149	COM76	7066	140
150	COM77	7066	191
151	COM78	7066	241
152	COM79	7066	291
153	COM80	7066	341
154	SEG312	7066	391
155	SEG311	7066	442
156	SEG310	7066	492
157	SEG309	7066	542
158	SEG308	7066	592
159	SEG307	7066	642
160	SEG306	7066	692
161	SEG305	7066	743
162	SEG304	7066	793
163	SEG303	7066	843
164	SEG302	7066	893
165	SEG301	7066	943
166	SEG300	7066	994
167	SEG299	7066	1044
168	SEG298	7066	1094
169	SEG297	7066	1144
170	SEG296	7066	1194
171	SEG295	7066	1245
172	dummy32	7066	1416
173	SEG294	6902	1416
174	SEG293	6852	1416
175	SEG292	6801	1416
176	SEG291	6751	1416
177	SEG290	6701	1416
178	SEG289	6651	1416
179	SEG288	6601	1416
180	SEG287	6550	1416
181	SEG286	6500	1416
182	SEG285	6450	1416
183	SEG284	6400	1416
184	SEG283	6350	1416
185	SEG282	6299	1416
186	SEG281	6249	1416
187	SEG280	6199	1416
188	SEG279	6149	1416
189	SEG278	6099	1416
190	SEG277	6048	1416
191	SEG276	5998	1416
192	SEG275	5948	1416
193	SEG274	5898	1416
194	SEG273	5848	1416
195	SEG272	5797	1416
196	SEG271	5747	1416
197	SEG270	5697	1416
198	SEG269	5647	1416
199	SEG268	5597	1416
200	SEG267	5546	1416
201	SEG266	5496	1416
202	SEG265	5446	1416
203	SEG264	5396	1416
204	SEG263	5346	1416
205	SEG262	5295	1416
206	SEG261	5245	1416
207	SEG260	5195	1416
208	SEG259	5145	1416
209	SEG258	5095	1416
210	SEG257	5045	1416
211	SEG256	4994	1416
212	SEG255	4944	1416
213	SEG254	4894	1416
214	SEG253	4844	1416
215	SEG252	4794	1416
216	SEG251	4743	1416
217	SEG250	4693	1416
218	SEG249	4643	1416
219	SEG248	4593	1416
220	SEG247	4543	1416
221	SEG246	4492	1416
222	SEG245	4442	1416
223	SEG244	4392	1416
224	SEG243	4342	1416
225	SEG242	4292	1416
226	SEG241	4241	1416
227	SEG240	4191	1416
228	SEG239	4141	1416
229	SEG238	4091	1416
230	SEG237	4041	1416
231	SEG236	3990	1416
232	SEG235	3940	1416
233	SEG234	3890	1416
234	SEG233	3840	1416
235	SEG232	3790	1416
236	SEG231	3739	1416
237	SEG230	3689	1416
238	SEG229	3639	1416
239	SEG228	3589	1416
240	SEG227	3539	1416
241	SEG226	3488	1416
242	SEG225	3438	1416
243	SEG224	3388	1416
244	SEG223	3339	1416
245	SEG222	3288	1416
246	SEG221	3238	1416
247	SEG220	3187	1416
248	SEG219	3137	1416
249	SEG218	3087	1416
250	SEG217	3037	1416
251	SEG216	2987	1416
252	SEG215	2936	1416
253	SEG214	2886	1416
254	SEG213	2836	1416
255	SEG212	2786	1416
256	SEG211	2736	1416
257	SEG210	2685	1416
258	SEG209	2635	1416
259	SEG208	2585	1416
260	SEG207	2535	1416
261	SEG206	2485	1416
262	SEG205	2434	1416
263	SEG204	2384	1416
264	SEG203	2334	1416
265	SEG202	2284	1416
266	SEG201	2234	1416
267	SEG200	2183	1416
268	SEG199	2133	1416
269	SEG198	2083	1416
270	SEG197	2033	1416
271	SEG196	1983	1416
272	SEG195	1932	1416
273	SEG194	1882	1416
274	SEG193	1832	1416
275	SEG192	1782	1416
276	SEG191	1732	1416
277	SEG190	1682	1416
278	SEG189	1631	1416
279	SEG188	1581	1416
280	SEG187	1531	1416
281	SEG186	1481	1416
282	SEG185	1431	1416
283	SEG184	1380	1416
284	SEG183	1330	1416
285	SEG182	1280	1416
286	SEG181	1230	1416
287	SEG180	1180	1416
288	SEG179	1129	1416
289	SEG178	1079	1416
290	SEG177	1029	1416
291	SEG176	979	1416
292	SEG175	929	1416
293	SEG174	878	1416
294	SEG173	828	1416
295	SEG172	778	1416
296	SEG171	728	1416
297	SEG170	678	1416
298	SEG169	627	1416
299	SEG168	577	1416
300	SEG167	527	1416
301	SEG166	477	1416
302	SEG165	427	1416
303	SEG164	376	1416
304	SEG163	326	1416
305	SEG162	276	1416
306	SEG161	226	1416
307	SEG160	176	1416
308	SEG159	125	1416
309	SEG158	75	1416
310	SEG157	25	1416
311	SEG156	-25	1416
312	SEG155	-75	1416
313	SEG154	-125	1416
314	SEG153	-176	1416
315	SEG152	-226	1416
316	SEG151	-276	1416
317	SEG150	-326	1416
318	SEG149	-376	1416
319	SEG148	-427	1416
320	SEG147	-477	1416
321	SEG146	-527	1416
322	SEG145	-577	1416
323	SEG144	-627	1416
324	SEG143	-678	1416
325	SEG142	-728	1416
326	SEG141	-778	1416
327	SEG140	-828	1416
328	SEG139	-878	1416
329	SEG138	-929	1416
330	SEG137	-979	1416
331	SEG136	-1029	1416
332	SEG135	-1079	1416
333	SEG134	-1129	1416
334	SEG133	-1180	1416
335	SEG132	-1230	1416
336	SEG131	-1280	1416
337	SEG130	-1330	1416
338	SEG129	-1380	1416
339	SEG128	-1431	1416
340	SEG127	-1481	1416
341	SEG126	-1531	1416
342	SEG125	-1581	1416
343	SEG124	-1631	1416
344	SEG123	-1682	1416
345	SEG122	-1732	1416
346	SEG121	-1782	1416
347	SEG120	-1832	1416
348	SEG119	-1882	1416
349	SEG118	-1932	1416
350	SEG117	-1983	1416
351	SEG116	-2033	1416
352	SEG115	-2083	1416
353	SEG114	-2133	1416
354	SEG113	-2183	1416
355	SEG112	-2234	1416
356	SEG111	-2284	1416
357	SEG110	-2334	1416
358	SEG109	-2384	1416
359	SEG108	-2434	1416
360	SEG107	-2485	1416
361	SEG106	-2535	1416
362	SEG105	-2585	1416
363	SEG104	-2635	1416
364	SEG103	-2685	1416
365	SEG102	-2736	1416
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367	SEG100	-2836	1416
368	SEG99	-2886	1416
369	SEG98	-2936	1416
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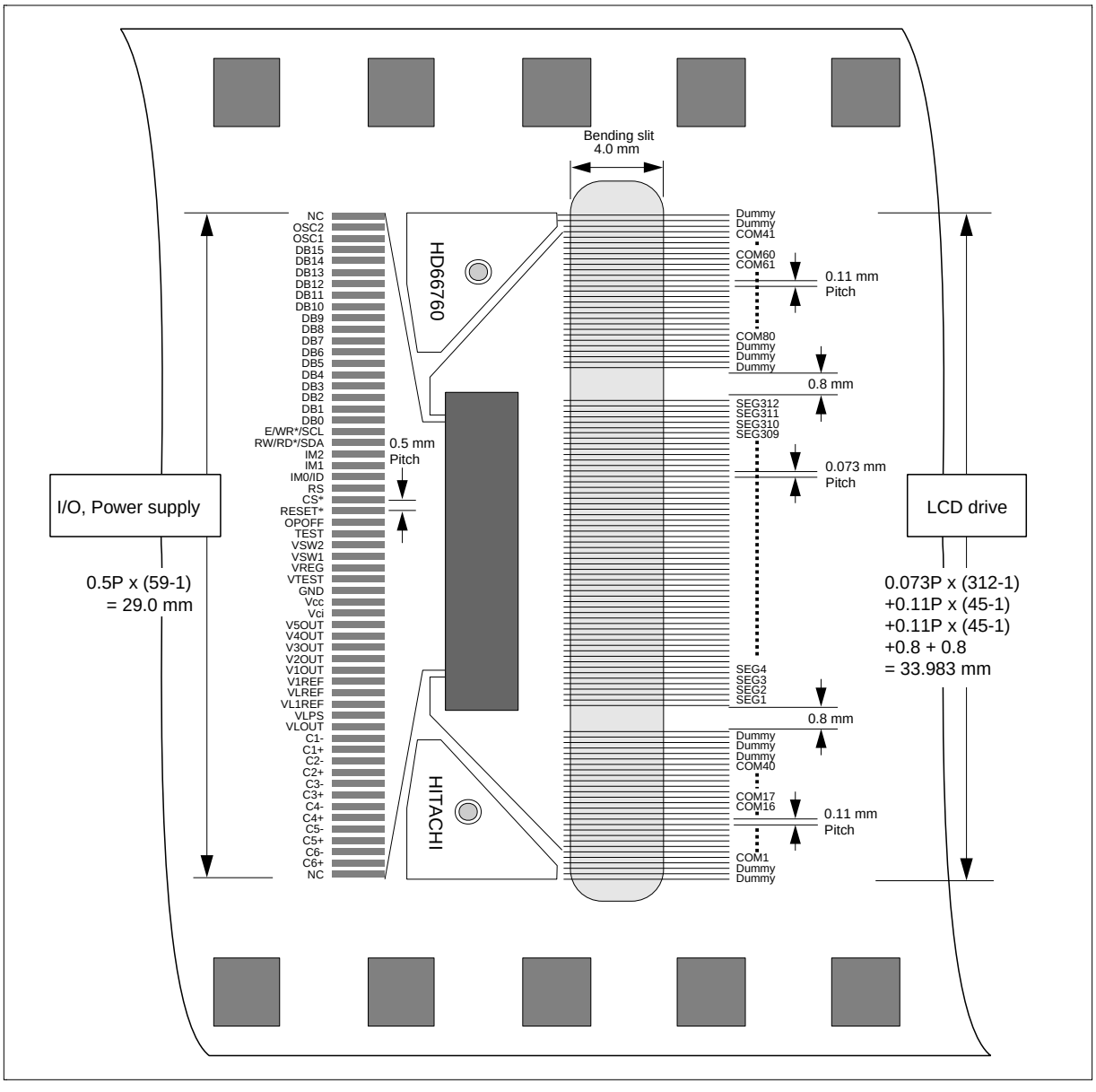
372	SEG95	-3087	1416
373	SEG94	-3137	1416
374	SEG93	-3187	1416
375	SEG92	-3238	1416
376	SEG91	-3288	1416
377	SEG90	-3338	1416
378	SEG89	-3388	1416
379	SEG88	-3438	1416
380	SEG87	-3488	1416
381	SEG86	-3539	1416
382	SEG85	-3589	1416
383	SEG84	-3639	1416
384	SEG83	-3689	1416
385	SEG82	-3739	1416
386	SEG81	-3790	1416
387	SEG80	-3840	1416
388	SEG79	-3890	1416
389	SEG78	-3940	1416
390	SEG77	-3990	1416
391	SEG76	-4041	1416
392	SEG75	-4091	1416
393	SEG74	-4141	1416
394	SEG73	-4191	1416
395	SEG72	-4241	1416
396	SEG71	-4292	1416
397	SEG70	-4342	1416
398	SEG69	-4392	1416
399	SEG68	-4442	1416
400	SEG67	-4492	1416
401	SEG66	-4543	1416
402	SEG65	-4593	1416
403	SEG64	-4643	1416
404	SEG63	-4693	1416
405	SEG62	-4743	1416
406	SEG61	-4794	1416
407	SEG60	-4844	1416
408	SEG59	-4894	1416
409	SEG58	-4944	1416
410	SEG57	-4994	1416
411	SEG56	-5045	1416
412	SEG55	-5095	1416
413	SEG54	-5145	1416
414	SEG53	-5195	1416
415	SEG52	-5245	1416
416	SEG51	-5295	1416
417	SEG50	-5346	1416
418	SEG49	-5396	1416
419	SEG48	-5446	1416
420	SEG47	-5496	1416
421	SEG46	-5546	1416
422	SEG45	-5597	1416
423	SEG44	-5647	1416
424	SEG43	-5697	1416
425	SEG42	-5747	1416
426	SEG41	-5797	1416
427	SEG40	-5848	1416
428	SEG39	-5898	1416
429	SEG38	-5948	1416
430	SEG37	-5998	1416
431	SEG36	-6048	1416
432	SEG35	-6099	1416
433	SEG34	-6149	1416
434	SEG33	-6199	1416
435	SEG32	-6249	1416
436	SEG31	-6299	1416
437	SEG30	-6350	1416
438	SEG29	-6400	1416
439	SEG28	-6450	1416
440	SEG27	-6500	1416
441	SEG26	-6550	1416
442	SEG25	-6601	1416
443	SEG24	-6651	1416
444	SEG23	-6701	1416
445	SEG22	-6751	1416
446	SEG21	-6801	1416
447	SEG20	-6852	1416
448	SEG19	-6902	1416
449	dummy33	-7066	1416
450	SEG18	-7066	1245
451	SEG17	-7066	1194
452	SEG16	-7066	1144
453	SEG15	-7066	1094
454	SEG14	-7066	1044
455	SEG13	-7066	994
456	SEG12	-7066	943
457	SEG11	-7066	893
458	SEG10	-7066	843
459	SEG9	-7066	793
460	SEG8	-7066	743
461	SEG7	-7066	692
462	SEG6	-7066	642
463	SEG5	-7066	592
464	SEG4	-7066	542
465	SEG3	-7066	492
466	SEG2	-7066	442
467	SEG1	-7066	391
468	COM40	-7066	341
469	COM39	-7066	291
470	COM38	-7066	241
471	COM37	-7066	191
472	COM36	-7066	140
473	COM35	-7066	90
474	COM34	-7066	40
475	COM33	-7066	-10
476	COM32	-7066	-60
477	COM31	-7066	-111
478	COM30	-7066	-161
479	COM29	-7066	-211
480	COM28	-7066	-261
481	COM27	-7066	-311
482	COM26	-7066	-362
483	COM25	-7066	-412
484	COM24	-7066	-462
485	COM23	-7066	-512
486	COM22	-7066	-562
487	COM21	-7066	-613
488	COM20	-7066	-663
489	COM19	-7066	-713
490	COM18	-7066	-763
491	COM17	-7066	-813
492	COM16	-7066	-864
493	COM15	-7066	-914
494	COM14	-7066	-964
495	COM13	-7066	-1014
496	COM12	-7066	-1064
497	COM11	-7066	-1115
498	COM10	-7066	-1165
499	COM9	-7066	-1215
500	dummy1	-7066	-1387
501	COM8	-6897	-1387
502	COM7	-6837	-1387
503	COM6	-6776	-1387
504	COM5	-6716	-1387
505	COM4	-6656	-1387
506	COM3	-6596	-1387
507	COM2	-6536	-1387
508	COM1	-6475	-1387

TCP Dimensions (HD66760TB0)



Pin Functions

Table 1 Pin Functional Description

<table>
<tr><th>Signals</th><th>Number of Pins</th><th>I/O</th><th>Connected to</th><th>Functions</th></tr>
<tr><td>IM2, IM1, IM0/ID</td><td>3</td><td>I</td><td>GND or V_{CC}</td><td>Selects the MPU interface mode:
<table>
<tr><th>IM2</th><th>IM1</th><th>IM0/ID</th><th>MPU interface mode</th></tr>
<tr><td>GND</td><td>GND</td><td>GND</td><td>68-system 16-bit bus interface</td></tr>
<tr><td>GND</td><td>GND</td><td>Vcc</td><td>68-system 8-bit bus interface</td></tr>
<tr><td>GND</td><td>Vcc</td><td>GND</td><td>80-system 16-bit bus interface</td></tr>
<tr><td>GND</td><td>Vcc</td><td>Vcc</td><td>80-system 8-bit bus interface</td></tr>
<tr><td>Vcc</td><td>GND</td><td>ID</td><td>Clock synchronized serial interface</td></tr>
<tr><td>Vcc</td><td>Vcc</td><td>ID</td><td>I2C bus interface</td></tr>
</table>
Inputs the ID of the device ID code for an I2C bus and clock synchronized serial interface.</td></tr>
<tr><td>CS*</td><td>1</td><td>I</td><td>MPU</td><td>Low: HD66760 is selected and can be accessed
High: HD66760 is not selected and cannot be accessed
Must be fixed at GND level when not in use.</td></tr>
<tr><td>RS</td><td>1</td><td>I</td><td>MPU</td><td>Selects the register. (Low: Index/status, High: Control)
Must be fixed at GND level when not in use.</td></tr>
<tr><td>E/WR*/SCL</td><td>1</td><td>I</td><td>MPU</td><td>For a 68-system bus interface, serves as an enable signal to activate data read/write operation.
For an 80-system bus interface, serves as a write strobe signal and writes data at the low level.
For an I2C bus or clock synchronized serial interface, inputs the serial transfer clock.</td></tr>
<tr><td>RW/RD*/ SDA</td><td>1</td><td>I</td><td>MPU</td><td>For a 68-system bus interface, serves as a signal to select data read/write operation. (Low: Write, High: Read)
For an 80-system bus interface, serves as a read strobe signal and reads data at the low level.
For an I2C bus or clock synchronized serial interface, serves as the bi-directional serial transfer data. Sends/Receives data.</td></tr>
<tr><td>DB0-DB15</td><td>16</td><td>I/O</td><td>MPU</td><td>Serves as a 16-bit bidirectional data bus.
For an 8-bit bus interface, data transfer uses DB15-DB8; fix unused DB7-DB0 to the Vcc or GND level.
When I2C or clock synchronized serial interface is used, fix DB0-DB15 to the Vcc or GND level.</td></tr>
</table>

Table 1 Pin Functional Description (cont)

Signals	Number of Pins	I/O	Connected to	Functions
COM1–COM80	80	O	LCD	Output signals for common drive: All the unused pins output unselected waveforms. In the display-off period (D1-0 = 00, 01), sleep mode (SLP = 1), or standby mode (STB = 1), all pins output GND level. The CMS bit can change the shift direction of the common signal. For example, if CMS = 0, COM1 shifts to COM80. If CMS = 1, COM80 shifts to COM1. Note that the start position of the common output is shifted by screen-division driving.
SEG1–SEG312	312	O	LCD	Output signals for segment drive. In the display-off period (D1-0 = 00, 01), sleep mode (SLP = 1), or standby mode (STB = 1), all pins output GND level. The SGS bit can change the shift direction of the segment signal. For example, if SGS = 0, RAM address 0000 is output from SEG1. If SGS = 1, it is output from SEG312. SEG1, SEG4, ... display red (R), SEG2, SEG5, ... display green (G), and SEG3, SEG6, ... display blue (B) (SGS = 0).
V1OUT–V5OUT	5	I/O	Capacitor	Used for output from the internal operational amplifiers when they are used (OPOFF = GND); attach a capacitor to stabilize the output. When the amplifiers are not used (OPOFF = V_{CC}), V1 to V5 voltages can be supplied to these pins from outside. Adjust the contrast for V1OUT ≥ V_{CC}, V_{Ci}.
V_{LPS}	1	—	Power supply	Power supply for LCD drive. V_{LCD} (= V_{LPS} – GND) = 15.5 V max.
V_{CC}, GND	1	—	Power supply	Power supply for logic circuit
OSC1, OSC2	2	I	Oscillation-resistor	Connect an external resistor for R-C oscillation.
Vci	1	I	Power supply	Inputs a reference voltage and supplies power to the step-up circuit; generates the liquid crystal display drive voltage from the operating voltage. The step-up output voltage must not be larger than the absolute maximum ratings. Must be left disconnected when the step-up circuit is not used.
VLOUT	1	O	V_{LPS} pin/step-up capacitance	Potential difference between Vci and GND is three- to six-times-stepped up and then output. Magnitude of step-up is selected by instruction.
C1+, C1–	2	—	Step-up capacitance	External capacitance should be connected here for step-up.
C2+, C2–	2	—	Step-up capacitance	External capacitance should be connected here for step-up.

Table 1 Pin Functional Description (cont)

Signals	Number of Pins	I/O	Connected to	Functions
C3+, C3–	2	—	Step-up capacitance	External capacitance should be connected here for step-up.
C4+, C4–	2	—	Step-up capacitance	External capacitance should be connected here for step-up.
C5+, C5–	2	—	Step-up capacitance	External capacitance should be connected here for step-up.
C6+, C6–	2	—	Step-up capacitance	External capacitance should be connected here for step-up.
RESET*	1	I	MPU or external R-C circuit	Reset pin. Initializes the LSI when low. Must be reset after power-on.
OPOFF	1	I	V_{CC} or GND	Turns the internal operational amplifier off when OPOFF = V_{CC}, and turns it on when OPOFF = GND. When internal amplifier is not used, supply V1 to V5 voltage level to the V1OUT to V5OUT pins.
VSW1, VSW2	2	I	GND	Test pins. Must be VSW1, VSW2 = GND.
VREG	1	I	Input pin	This pin is used when the reference voltage of the internal power-supply regulator is externally supplied. When the internal reference voltage (1/2 Vci) is used, VREG must be opened since the 1/2-Vci level is output.
VLREF	1	I	Input pin	Use this pin when the LCD drive voltage is externally supplied. When the internal power-supply regulator is used, short VLREF with the V1REF pin.
V1REF	1	O	Output pin	Outputs the LCD drive voltage generated in the internal power-supply regulator. Insert this pin when the external temperature-compensation circuit is used between V1REF and VLREF. If the circuit is not used, short V1REF and VLREF.
V_{CC}DUM	2	O	Input pins	Outputs the internal V_{CC} level; shorting this pin sets the adjacent input pin to the V_{CC} level.
GNDDUM	4	O	Input pins	Outputs the internal GND level; shorting this pin sets the adjacent input pin to the GND level.
Dummy	4	—	—	Dummy pad. Must be left disconnected.
TEST	1	I	GND	Test pin. Must be fixed at GND level.
VTEST	1	—	—	Test pin. Must be left disconnected.
VL1REF	1	O	—	Test pin. Must be left disconnected.

Block Function Description

System Interface

The HD66760 has four high-speed system interfaces: an 80-system 16-bit/8-bit bus, a 68-system 16-bit/8-bit bus, an I2C bus interface and a clock synchronized serial interface. The interface mode is selected by the IM2-0 pins.

The HD66760 has three 16-bit registers: an index register (IR), a write data register (WDR), and a read data register (RDR). The IR stores index information from the control registers and the GRAM. The WDR temporarily stores data to be written into control registers and the GRAM, and the RDR temporarily stores data read from the GRAM. Data written into the GRAM from the MPU is first written into the WDR and then is automatically written into the GRAM by internal operation. Data is read through the RDR when reading from the GRAM, and the first read data is invalid and the second and the following data are normal. When a logic operation is performed inside of the HD66760 by using the display data set in the GRAM and the data written from the MPU, the data read through the RDR is used. Accordingly, the MPU does not need to read data twice nor to fetch the read data into the MPU. This enables high-speed processing.

Execution time for instruction excluding oscillation start is 0 clock cycle and instructions can be written in succession.

Table 2 Register Selection

80-series Bus		68- series Bus		
WR Bits	RD Bits	R/W Bits	RS Bits	Operations
0	1	0	0	Writes indexes into IR
1	0	1	0	Reads internal status
0	1	0	1	Writes into control registers and GRAM through WDR
1	0	1	1	Reads from GRAM through RDR

Bit Operation

The HD66760 supports the following functions: a swap function that writes the data written from the MPU into the GRAM by reversing the display position vertically in byte units, a write data mask function that selects and writes data into the GRAM in bit units, and a logic operation function that performs logic operations or conditional determination on the display data set in the GRAM and writes into the GRAM. With the 16-bit bus interface, these functions can greatly reduce the processing loads of the MPU graphics software and can rewrite the display data in the GRAM at high speed. For details, see the Graphics Operation Function section.

Address Counter (AC)

The address counter (AC) assigns addresses to the GRAM. When an address set instruction is written into the IR, the address information is sent from the IR to the AC.

After writing into the GRAM, the AC is automatically incremented by 1 (or decremented by 1). After reading from the data, the AC is not updated.

Graphics RAM (GRAM)

The graphics RAM (GRAM) has eight bits/pixel and stores the bit-pattern data of 104×80 bytes.

Grayscale Palette (GSP)

The grayscale palette (GSP) is a palette table that converts the information (three bits for each color: two bits for B) read from the GRAM to 4-bit grayscale data. Any 256 of the 4,096 possible colors can be displayed at the same time. For details, see the Grayscale Palette section.

Grayscale Control Circuit

The grayscale control circuit performs 16-grayscale control with the frame rate control (FRC) method for grayscale display for each color. For details, see the Grayscale Palette section.

Timing Generator

The timing generator generates timing signals for the operation of internal circuits such as the GRAM. The RAM read timing for display and internal operation timing by MPU access are generated separately to avoid interference with one another.

Oscillation Circuit (OSC)

The HD66760 can provide R-C oscillation simply through the addition of an external oscillation-resistor between the OSC1 and OSC2 pins. The appropriate oscillation frequency for operating voltage, display size, and frame frequency can be obtained by adjusting the external-resistor value. Clock pulses can also be supplied externally. Since R-C oscillation stops during the standby mode, current consumption can be reduced. For details, see the Oscillation Circuit section.

Liquid Crystal Display Driver Circuit

The liquid crystal display driver circuit consists of 80 common signal drivers (COM1 to COM80) and 312 segment signal drivers (SEG1 to SEG312). When the number of lines are selected by a program, the required common signal drivers automatically output drive waveforms, while the other common signal drivers continue to output unselected waveforms.

Display pattern data is latched when 312-bit data has arrived. The latched data then enables the segment signal drivers to generate drive waveform outputs. The shift direction of 312-bit data can be changed by the

SGS bit. The shift direction for the common driver can also be changed by the CMS bit by selecting an appropriate direction for the device mounting configuration.

When multiplexing drive is not used, or during the standby or sleep mode, all the above common and segment signal drivers output the GND level, halting the display.

Step-up Circuit (DC-DC Converter)

The step-up generates three-, four-, five-, or six-times voltage input to the Vci pin. With this, both the internal logic units and LCD drivers can be controlled with a single power supply. Step-up output level from three-times to six-times step-up can be selected by software. For details, see the Power Supply for Liquid Crystal Display Drive section.

V-Pin Voltage Follower

A voltage follower for each voltage level (V1 to V5) reduces current consumption by the LCD drive power supply circuit. No external resistors are required because of the internal bleeder-resistor, which generates different levels of LCD drive voltage. This internal bleeder-resistor can be software-specified from 1/4 bias to 1/10 bias, according to the liquid crystal display drive duty value. For details, see the Power Supply for Liquid Crystal Display Drive section.

Contrast Adjuster

The contrast adjuster can be used to adjust LCD contrast in 128 steps by varying the LCD drive voltage by software. This can be used to select an appropriate LCD brightness or to compensate for temperature.

Power-supply Regulator

The power-supply regulator generates the LCD drive voltage from the reference voltage, which does not depend on the LCD load current. The fluctuating LCD drive voltage can be controlled for the fluctuating LCD load current. For details, see the Liquid Crystal Display Voltage Generator section.

GRAM Address Map (HD66760)

Table 3 Relationship between Display Position and GRAM Address (GS = 0, SGS = 0)

SEG/COM Pin		SEG1	SEG2	SEG3	SEG4	SEG5	SEG6	SEG7	SEG8	SEG9	SEG10	SEG11	SEG12	.....	SEG301	SEG302	SEG303	SEG304	SEG305	SEG306	SEG307	SEG308	SEG309	SEG310	SEG311	SEG312
CMS=0	CMS=1	DB 15 - DB 8			DB 7 - DB 0			DB 15 - DB 8			DB 7 - DB 0				DB 15 - DB 8			DB 7 - DB 0			DB 15 - DB 8			DB 7 - DB 0		
COM1	COM80	"0000"H						"0001"H						.....	"0032"H						"0033"H					
COM2	COM79	"0100"H						"0101"H						.....	"0132"H						"0133"H					
COM3	COM78	"0200"H						"0201"H						.....	"0232"H						"0233"H					
COM4	COM77	"0300"H						"0301"H						.....	"0332"H						"0333"H					
COM5	COM76	"0400"H						"0401"H						.....	"0432"H						"0433"H					
COM6	COM75	"0500"H						"0501"H						.....	"0532"H						"0533"H					
COM7	COM74	"0600"H						"0601"H						.....	"0632"H						"0633"H					
COM8	COM73	"0700"H						"0701"H						.....	"0732"H						"0733"H					
COM9	COM72	"0800"H						"0801"H						.....	"0832"H						"0833"H					
COM10	COM71	"0900"H						"0901"H						.....	"0932"H						"0933"H					
COM11	COM70	"0A00"H						"0A01"H						.....	"0A32"H						"0A33"H					
COM12	COM69	"0B00"H						"0B01"H						.....	"0B32"H						"0B33"H					
COM13	COM68	"0C00"H						"0C01"H						.....	"0C32"H						"0C33"H					
COM14	COM67	"0D00"H						"0D01"H						.....	"0D32"H						"0D33"H					
COM15	COM66	"0E00"H						"0E01"H						.....	"0E32"H						"0E33"H					
COM16	COM65	"0F00"H						"0F01"H						.....	"0F32"H						"0F33"H					
COM17	COM64	"1000"H						"1001"H						.....	"1032"H						"1033"H					
COM18	COM63	"1100"H						"1101"H						.....	"1132"H						"1133"H					
COM19	COM62	"1200"H						"1201"H						.....	"1232"H						"1233"H					
COM20	COM61	"1300"H						"1301"H						.....	"1332"H						"1333"H					
⋮	⋮	⋮						⋮							⋮						⋮					
COM73	COM8	"4800"H						"4801"H						.....	"4832"H						"4833"H					
COM74	COM7	"4900"H						"4901"H						.....	"4932"H						"4933"H					
COM75	COM6	"4A00"H						"4A01"H						.....	"4A32"H						"4A33"H					
COM76	COM5	"4B00"H						"4B01"H						.....	"4B32"H						"4B33"H					
COM77	COM4	"4C00"H						"4C01"H						.....	"4C32"H						"4C33"H					
COM78	COM3	"4D00"H						"4D01"H						.....	"4D32"H						"4D33"H					
COM79	COM2	"4E00"H						"4E01"H						.....	"4E32"H						"4E33"H					
COM80	COM1	"4F00"H						"4F01"H						.....	"4F32"H						"4F33"H					

Table 4 Relationship between GRAM Data and Display Contents

GRAM Data	DB 15	DB 14	DB 13	DB 12	DB 11	DB 10	DB 9	DB 8	DB 7	DB 6	DB 5	DB 4	DB 3	DB 2	DB 1	DB 0
Selection Palette	RK palette			GK palette			BK palette		RK palette			GK palette			BK palette	
Output Pin	SEG (6n+1)			SEG (6n+2)			SEG (6n+3)		SEG (6n+4)			SEG (6n+5)			SEG (6n+6)	

Note: n = Lower 7-bit address (0 to 51)

Table 5 Relationship between Display Position and GRAM Address (GS = 0, SGS = 1)

SEG/COM Pin		SEG1	SEG2	SEG3	SEG4	SEG5	SEG6	SEG7	SEG8	SEG9	SEG10	SEG11	SEG12	.....	SEG301	SEG302	SEG303	SEG304	SEG305	SEG306	SEG307	SEG308	SEG309	SEG310	SEG311	SEG312
CMS=0	CMS=1	DB 0 - DB 7			DB 8 - DB 15			DB 0 - DB 7			DB 8 - DB 15				DB 0 - DB 7			DB 8 - DB 15			DB 0 - DB 7			DB 8 - DB 15		
COM1	COM80	"0033"H						"0032"H						.....	"0001"H						"0000"H					
COM2	COM79	"0133"H						"0132"H						.....	"0101"H						"0100"H					
COM3	COM78	"0233"H						"0232"H						.....	"0201"H						"0200"H					
COM4	COM77	"0333"H						"0332"H						.....	"0301"H						"0300"H					
COM5	COM76	"0433"H						"0432"H						.....	"0401"H						"0400"H					
COM6	COM75	"0533"H						"0532"H						.....	"0501"H						"0500"H					
COM7	COM74	"0633"H						"0632"H						.....	"0601"H						"0600"H					
COM8	COM73	"0733"H						"0732"H						.....	"0701"H						"0700"H					
COM9	COM72	"0833"H						"0832"H						.....	"0801"H						"0800"H					
COM10	COM71	"0933"H						"0932"H						.....	"0901"H						"0900"H					
COM11	COM70	"0A33"H						"0A32"H						.....	"0A01"H						"0A00"H					
COM12	COM69	"0B33"H						"0B32"H						.....	"0B01"H						"0B00"H					
COM13	COM68	"0C33"H						"0C32"H						.....	"0C01"H						"0C00"H					
COM14	COM67	"0D33"H						"0D32"H						.....	"0D01"H						"0D00"H					
COM15	COM66	"0E33"H						"0E32"H						.....	"0E01"H						"0E00"H					
COM16	COM65	"0F33"H						"0F32"H						.....	"0F01"H						"0F00"H					
COM17	COM64	"1033"H						"1032"H						.....	"1001"H						"1000"H					
COM18	COM63	"1133"H						"1132"H						.....	"1101"H						"1100"H					
COM19	COM62	"1233"H						"1232"H						.....	"1201"H						"1200"H					
COM20	COM61	"1333"H						"1332"H						.....	"1301"H						"1300"H					
⋮	⋮	⋮						⋮							⋮						⋮					
COM73	COM8	"4833"H						"4832"H						.....	"4801"H						"4800"H					
COM74	COM7	"4933"H						"4932"H						.....	"4901"H						"4900"H					
COM75	COM6	"4A33"H						"4A32"H						.....	"4A01"H						"4A00"H					
COM76	COM5	"4B33"H						"4B32"H						.....	"4B01"H						"4B00"H					
COM77	COM4	"4C33"H						"4C32"H						.....	"4C01"H						"4C00"H					
COM78	COM3	"4D33"H						"4D32"H						.....	"4D01"H						"4D00"H					
COM79	COM2	"4E33"H						"4E32"H						.....	"4E01"H						"4E00"H					
COM80	COM1	"4F33"H						"4F32"H						.....	"4F01"H						"4F00"H					

Table 6 Relationship between GRAM Data and Display Contents

GRAM Data	DB 15	DB 14	DB 13	DB 12	DB 11	DB 10	DB 9	DB 8	DB 7	DB 6	DB 5	DB 4	DB 3	DB 2	DB 1	DB 0
Selection Palette	RK palette			GK palette			BK palette		RK palette			GK palette			BK palette	
Output Pin	SEG (312-6n)			SEG (311-6n)			SEG (310-6n)		SEG (309-6n)			SEG (308-6n)			SEG (307-6n)	

Note: n = Lower 7-bit address (0 to 51)

Table 7 Relationship between Display Position and GRAM Address (GS = 1, SGS = 0)

SEG/COM Pin		SEG1 .... SEG12	SEG13 .... SEG24	SEG25 ---- SEG36	SEG37 .... SEG48	.....	SEG265 .... SEG276	SEG277 .... SEG288	SEG289 .... SEG300	SEG301 .... SEG312
CMS=0	CMS=1	DB15 ---- DB8	DB7 .... DB0	DB15 ---- DB8	DB7 .... DB0		DB15 ---- DB8	DB7 .... DB0	DB15 ---- DB8	DB7 .... DB0
COM1	COM80	"0000"H		"0001"H		.....	"000B"H		"000C"H	
COM2	COM79	"0100"H		"0101"H		.....	"010B"H		"010C"H	
COM3	COM78	"0200"H		"0201"H		.....	"020B"H		"020C"H	
COM4	COM77	"0300"H		"0301"H		.....	"030B"H		"030C"H	
COM5	COM76	"0400"H		"0401"H		.....	"040B"H		"040C"H	
COM6	COM75	"0500"H		"0501"H		.....	"050B"H		"050C"H	
COM7	COM74	"0600"H		"0601"H		.....	"060B"H		"060C"H	
COM8	COM73	"0700"H		"0701"H		.....	"070B"H		"070C"H	
COM9	COM72	"0800"H		"0801"H		.....	"080B"H		"080C"H	
COM10	COM71	"0900"H		"0901"H		.....	"090B"H		"090C"H	
COM11	COM70	"0A00"H		"0A01"H		.....	"0A0B"H		"0A0C"H	
COM12	COM69	"0B00"H		"0B01"H		.....	"0B0B"H		"0B0C"H	
COM13	COM68	"0C00"H		"0C01"H		.....	"0C0B"H		"0C0C"H	
COM14	COM67	"0D00"H		"0D01"H		.....	"0D0B"H		"0D0C"H	
COM15	COM66	"0E00"H		"0E01"H		.....	"0E0B"H		"0E0C"H	
COM16	COM65	"0F00"H		"0F01"H		.....	"0F0B"H		"0F0C"H	
COM17	COM64	"1000"H		"1001"H		.....	"100B"H		"100C"H	
COM18	COM63	"1100"H		"1101"H		.....	"110B"H		"110C"H	
COM19	COM62	"1200"H		"1201"H		.....	"120B"H		"120C"H	
COM20	COM61	"1300"H		"1301"H		.....	"130B"H		"130C"H	
⋮	⋮	⋮		⋮			⋮		⋮	
COM73	COM8	"4800"H		"4801"H		.....	"480B"H		"480C"H	
COM74	COM7	"4900"H		"4901"H		.....	"490B"H		"490C"H	
COM75	COM6	"4A00"H		"4A01"H		.....	"4A0B"H		"4A0C"H	
COM76	COM5	"4B00"H		"4B01"H		.....	"4B0B"H		"4B0C"H	
COM77	COM4	"4C00"H		"4C01"H		.....	"4C0B"H		"4C0C"H	
COM78	COM3	"4D00"H		"4D01"H		.....	"4D0B"H		"4D0C"H	
COM79	COM2	"4E00"H		"4E01"H		.....	"4E0B"H		"4E0C"H	
COM80	COM1	"4F00"H		"4F01"H		.....	"4F0B"H		"4F0C"H	

Note: When the GS bit is updated, the RAM data must be rewritten.

Table 8 Relationship between GRAM Data and Display Contents

GRAM Data	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Selection Palette	RK, GK, BK		RK, GK, BK		RK, GK, BK		RK, GK, BK		RK, GK, BK		RK, GK, BK		RK, GK, BK		RK, GK, BK	
Output Pin	SEG (24n+1) ⋮ SEG (24n+3)		SEG (24n+4) ⋮ SEG (24n+6)		SEG (24n+7) ⋮ SEG (24n+9)		SEG (24n+10) ⋮ SEG (24n+12)		SEG (24n+13) ⋮ SEG (24n+15)		SEG (24n+16) ⋮ SEG (24n+18)		SEG (24n+19) ⋮ SEG (24n+21)		SEG (24n+22) ⋮ SEG (24n+24)	

Note: n = Lower 4-bit address (0 to 12)

Table 9 Relationship between Display Position and GRAM Address (GS = 1, SGS = 1)

SEG/COM Pin		SEG1 .... SEG12	SEG13 .... SEG24	SEG25 ---- SEG36	SEG37 .... SEG48	.....	SEG265 .... SEG276	SEG277 .... SEG288	SEG289 .... SEG300	SEG301 .... SEG312
CMS=0	CMS=1	DB 0 ---- DB 7	DB 8 ---- DB 15	DB 0 ---- DB 7	DB 8 ---- DB 15		DB 0 ---- DB 7	DB 8 ---- DB 15	DB 0 ---- DB 7	DB 8 ---- DB 15
COM1	COM80	"000C"H		"000B"H		.....	"0001"H		"0000"H	
COM2	COM79	"010C"H		"010B"H		.....	"0101"H		"0100"H	
COM3	COM78	"020C"H		"020B"H		.....	"0201"H		"0200"H	
COM4	COM77	"030C"H		"030B"H		.....	"0301"H		"0300"H	
COM5	COM76	"040C"H		"040B"H		.....	"0401"H		"0400"H	
COM6	COM75	"050C"H		"050B"H		.....	"0501"H		"0500"H	
COM7	COM74	"060C"H		"060B"H		.....	"0601"H		"0600"H	
COM8	COM73	"070C"H		"070B"H		.....	"0701"H		"0700"H	
COM9	COM72	"080C"H		"080B"H		.....	"0801"H		"0800"H	
COM10	COM71	"090C"H		"090B"H		.....	"0901"H		"0900"H	
COM11	COM70	"0A0C"H		"0A0B"H		.....	"0A01"H		"0A00"H	
COM12	COM69	"0B0C"H		"0B0B"H		.....	"0B01"H		"0B00"H	
COM13	COM68	"0C0C"H		"0C0B"H		.....	"0C01"H		"0C00"H	
COM14	COM67	"0D0C"H		"0D0B"H		.....	"0D01"H		"0D00"H	
COM15	COM66	"0E0C"H		"0E0B"H		.....	"0E01"H		"0E00"H	
COM16	COM65	"0F0C"H		"0F0B"H		.....	"0F01"H		"0F00"H	
COM17	COM64	"100C"H		"100B"H		.....	"1001"H		"1000"H	
COM18	COM63	"110C"H		"110B"H		.....	"1101"H		"1100"H	
COM19	COM62	"120C"H		"120B"H		.....	"1201"H		"1200"H	
COM20	COM61	"130C"H		"130B"H		.....	"1301"H		"1300"H	
⋮	⋮	⋮		⋮			⋮		⋮	
COM73	COM8	"480C"H		"480B"H		.....	"4801"H		"4800"H	
COM74	COM7	"490C"H		"490B"H		.....	"4901"H		"4900"H	
COM75	COM6	"4A0C"H		"4A0B"H		.....	"4A01"H		"4A00"H	
COM76	COM5	"4B0C"H		"4B0B"H		.....	"4B01"H		"4B00"H	
COM77	COM4	"4C0C"H		"4C0B"H		.....	"4C01"H		"4C00"H	
COM78	COM3	"4D0C"H		"4D0B"H		.....	"4D01"H		"4D00"H	
COM79	COM2	"4E0C"H		"4E0B"H		.....	"4E01"H		"4E00"H	
COM80	COM1	"4F0C"H		"4F0B"H		.....	"4F01"H		"4F00"H	

Note: When the GS bit is updated, the RAM data must be rewritten.

Table 10 Relationship between GRAM Data and Display Contents

GRAM Data	DB 15	DB 14	DB 13	DB 12	DB 11	DB 10	DB 9	DB 8	DB 7	DB 6	DB 5	DB 4	DB 3	DB 2	DB 1	DB 0
Selection Palette	RK, GK, BK		RK, GK, BK		RK, GK, BK		RK, GK, BK		RK, GK, BK		RK, GK, BK		RK, GK, BK		RK, GK, BK	
Output Pin	SEG (312-24n) ⋮ SEG (310-24n)		SEG (309-24n) ⋮ SEG (307-24n)		SEG (306-24n) ⋮ SEG (304-24n)		SEG (303-24n) ⋮ SEG (301-24n)		SEG (300-24n) ⋮ SEG (298-24n)		SEG (297-24n) ⋮ SEG (295-24n)		SEG (294-24n) ⋮ SEG (292-24n)		SEG (291-24n) ⋮ SEG (289-24n)	

Note: n = Lower 4-bit address (0 to 12)

Instructions

Outline

The HD66760 uses the 16-bit bus architecture. Before the internal operation of the HD66760 starts, control information is temporarily stored in the registers described below to allow high-speed interfacing with a high-performance microcomputer. The internal operation of the HD66760 is determined by signals sent from the microcomputer. These signals, which include the register selection signal (RS), the read/write signal (R/W), and the data bus signals (DB15 to DB0), make up the HD66760 instructions. There are eight categories of instructions that:

- Specify the index
- Read the status
- Control the display
- Control power management
- Process the graphics data
- Set internal GRAM addresses
- Transfer data to and from the internal GRAM
- Set grayscale level for the internal grayscale palette table

Normally, instructions that write data are used the most. However, an auto-update of internal GRAM addresses after each data write can lighten the microcomputer program load.

Because instructions are executed in 0 cycles, they can be written in succession.

Instruction Descriptions

Index

The index instruction specifies the RAM control indexes (R00h to R39h). It sets the register number in the range of 000000 to 111001 in binary form. However, R40h to R44h are disabled since they are test registers.

R/W	RS	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
W	0	*	*	*	*	*	*	*	*	*	ID6	ID5	ID4	ID3	ID2	ID1	ID0

Figure 1 Index Instruction

Status Read

The status read instruction reads the internal status of the HD66760.

L7–0: Indicate the driving raster-row position where the liquid crystal display is being driven.

C6–0: Read the contrast setting values (CT6-0).

R/W	RS	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
R	0	0	L6	L5	L4	L3	L2	L1	L0	0	C6	C5	C4	C3	C2	C1	C0

Figure 2 Status Read Instruction

Start Oscillation (R00h)

The start oscillation instruction restarts the oscillator from the halt state in the standby mode. After issuing this instruction, wait at least 10 ms for oscillation to stabilize before issuing the next instruction. (See the Standby Mode section.)

If this register is read forcibly, 8760H is read.

R/W	RS	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
W	1	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	1
R	1	1	0	0	0	0	1	1	1	0	1	1	0	0	0	0	0

Figure 3 Start Oscillation Instruction

Driver Output Control (R01h)

CMS: Selects the output shift direction of a common driver. When CMS = 0, COM1 shifts to COM80. When CMS = 1, COM80 shifts to COM1.

SGS: Selects the output shift direction of a segment driver. When SGS = 0, SEG1 shifts to SEG312. When SGS = 1, SEG312 shifts to SEG1. When SGS = 0, the SEG1 pin assigns the color display to R, G, or B. When SGS = 1, the SEG312 pin assigns R, G, or B to the color display.

NL3–0: Specify the LCD drive duty ratio. The duty ratio can be adjusted for every eight raster-rows. GRAM address mapping does not depend on the setting value of the drive duty ratio.

R/W	RS	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
W	1	0	0	0	0	0	0	CMS	SGS	0	0	0	0	NL3	NL2	NL1	NL0

Figure 4 Driver Output Control Instruction

Table 11 NL Bits and Drive Duty

NL3	NL2	NL1	NL0	Display Size	LCD Drive Duty	Common Driver Used
0	0	0	0	Setting disabled	Setting disabled	Setting disabled
0	0	0	1	312 x 16 dots	1/16 Duty	COM1–COM16
0	0	1	0	312 x 24 dots	1/24 Duty	COM1–COM24
0	0	1	1	312 x 32 dots	1/32 Duty	COM1–COM32
0	1	0	0	312 x 40 dots	1/40 Duty	COM1–COM40
0	1	0	1	312 x 48 dots	1/48 Duty	COM1–COM48
0	1	1	0	312 x 56 dots	1/56 Duty	COM1–COM56
0	1	1	1	312 x 64 dots	1/64 Duty	COM1–COM64
1	0	0	0	312 x 72 dots	1/72 Duty	COM1–COM72
1	0	0	1	312 x 80 dots	1/80 Duty	COM1–COM80

LCD-Driving-Waveform Control (R02h)

RST: When RST = 1, software function is started. This function is same as hardware RESET* pin. It takes 10 clock cycle period. The RST will be automatically cleared. Therefore, after 10 clock cycle other instruction can be issued. Do not set the RST during stand-by mode.

B/C: When B/C = 0, a B-pattern waveform is generated and alternates in every frame for LCD drive. When B/C = 1, a C-pattern waveform is generated and alternates in each raster-row specified by bits EOR and NW4-NW0 in the LCD-driving-waveform control register. For details, see the n-raster-row Reversed AC Drive section.

EOR: When the C-pattern waveform is set (B/C = 1) and EOR = 1, the odd/even frame-select signals and the n-raster-row reversed signals are EORed for alternating drive. EOR is used when the LCD is not alternated by combining the set values of the LCD drive duty ratio and the n raster-row. For details, see the n-raster-row Reversed AC Drive section.

NW4–0: Specify the number of raster-rows n that will alternate at the C-pattern waveform setting (B/C = 1). NW4-NW0 alternate for every set value + 1 raster-row, and the first to the 32nd raster-rows can be selected.

R/W	RS	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
W	1	0	0	0	0	0	0	0	RST	0	B/C	EOR	NW4	NW3	NW2	NW1	NW0

Figure 5 LCD-Driving-Waveform Control Instruction

Power Control (R03h)

BS2–0: The LCD drive bias value is set within the range of a 1/4 to 1/10 bias. The LCD drive bias value can be selected according to its drive duty ratio and voltage. For details, see the Liquid-crystal-display Drive-bias Selector section.

BT1–0: The output factor of VLOUT between three-times, four-times, five-times, and six-times step-up is switched. The LCD drive voltage level can be selected according to its drive duty ratio and bias. Lower amplification of the step-up circuit consumes less current.

PS1–0: The internal or external power supply is selected as the reference power supply for the LCD drive-voltage generator.

DC1–0: The operating frequency in the step-up circuit is selected. When the step-up operating frequency is high, the driving ability of the step-up circuit and the display quality become high, but the current consumption is increased. Adjust the frequency considering the display quality and the current consumption.

AP1–0: The amount of fixed current from the fixed current source in the operational amplifier for V pins (V1 to V5) is adjusted. When the amount of fixed current is large, the LCD driving ability and the display quality become high, but the current consumption is increased. Adjust the fixed current considering the display quality and the current consumption.

During no display, when AP1-0 = 00, the current consumption can be reduced by ending the operational amplifier and step-up circuit operation.

SLP: When SLP = 1, the HD66760 enters the sleep mode, where the internal display operations are halted except for the R-C oscillator, thus reducing current consumption. For details, see the Sleep Mode section. Only the following instructions can be executed during the sleep mode.

a. Power control (BS2-0, BT1-0, DC1-0, AP1-0, SLP, and STB bits)
b. Software reset (RST = 1)

During the sleep mode, the other GRAM data and instructions cannot be updated although they are retained.

STB: When STB = 1, the HD66760 enters the standby mode, where display operation completely stops, halting all the internal operations including the internal R-C oscillator. Further, no external clock pulses are supplied. For details, see the Standby Mode section.

Only the following instructions can be executed during the standby mode.

a. Standby mode cancel (STB = 0)
b. Start oscillation
c. Power control (BS2-0, BT1-0, DC1-0, AP1-0, SLP, and STB bits)

During the standby mode, the GRAM data and instructions may be lost. To prevent this, they must be set again after the standby mode is canceled.

Table 12 BS Bits and LCD Drive Bias Value

BS2	BS1	BS0	LCD Drive Bias Value
0	0	0	Setting disabled
0	0	1	1/10 bias drive
0	1	0	1/9 bias drive
0	1	1	1/8 bias drive
1	0	0	1/7 bias drive
1	0	1	1/6 bias drive
1	1	0	1/5 bias drive
1	1	1	1/4 bias drive

Table 13 BS Bits and Output Level

BT1	BT0	VLOUT Output Level
0	0	Three-times step-up
0	1	Four-times step-up
1	0	Five-times step-up
1	1	Six-times step-up

Table 14 DC Bits and Operating Clock Frequency

DC1	DC0	Operating Clock Frequency in the Step-up Circuit
0	0	32-divided clock
0	1	16-divided clock
1	0	128-divided clock
1	1	64-divided clock

Table 15 AP Bits and Amount of Fixed Current

AP1	AP0	Amount of Fixed Current in the Operational Amplifier
0	0	Operational amplifier and booster do not operate.
0	1	Small
1	0	Middle
1	1	Large

Table 16 Switching Reference Power Supply

PS1	PS0	VREG Pin	V1REF Pin	VLREF Pin	VLREF Regulator
0	0	Output (1/2Vci)	Output (1/2Vci ¥ N-times)	Input (from V1REF pin)	Unused
0	1	Output (1/2Vci)	Output (1/2Vci ¥ N-times)	Input (from V1REF pin)	Used
1	0	Input (Vreg)	Output (Vreg ¥ N-times)	Input (from V1REF pin)	Unused
1	1	Open (High-Z)	Open (High-Z)	Input (Vlcd: LCD voltage)	Unused

R/W	RS	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
W	1	0	0	0	BS2	BS1	BS0	BT1	BT0	PS1	PS0	DC1	DC0	AP1	AP0	SLP	STB

Figure 6 Power Control Instruction

Contrast Control (R04h)

CT6–0: These bits control the LCD drive voltage (potential difference between V1 and GND) to adjust 128-step contrast. For details, see the Contrast Adjuster section.

R/W	RS	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
W	1	0	0	0	0	0	VR2	VR1	VR0	0	CT6	CT5	CT4	CT3	CT2	CT1	CT0

Figure 7 Contrast Control Instruction

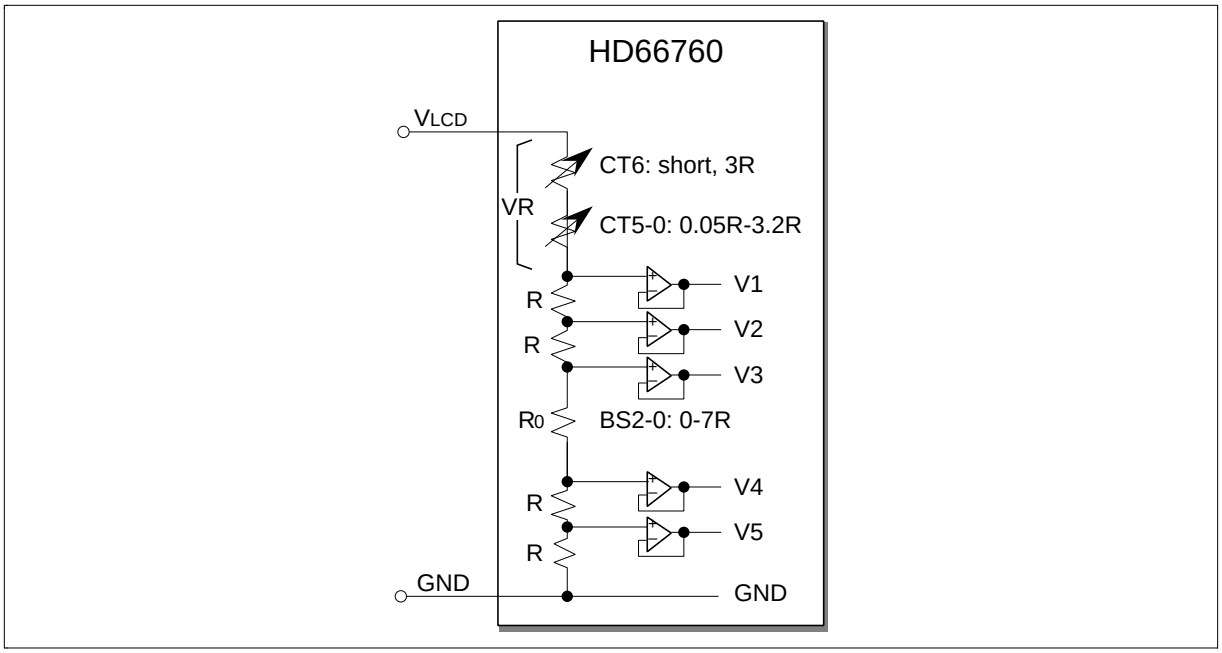


Figure 8 Contrast Adjuster

Table 17 G Bits and Variable Registor Value of Contrast Adjuster

CT Set Value						Variable Resistor (VR)	
CT5	CT4	CT3	CT2	CT1	CT0	CT6 = 0	CT6 = 1
0	0	0	0	0	0	6.20 × R	3.20 × R
0	0	0	0	0	1	6.15 × R	3.15 × R
0	0	0	0	1	0	6.10 × R	3.10 × R
0	0	0	0	1	1	6.05 × R	3.05 × R
0	0	0	1	0	0	6.00 × R	3.00 × R
			•			•	•
			•			•	•
1	1	1	1	0	1	3.15 × R	0.15 × R
1	1	1	1	1	0	3.10 × R	0.10 × R
1	1	1	1	1	1	3.05 × R	0.05 × R

VR2–0: These bits adjust the output voltage (V1REF) in the LCD drive reference generator in the range of four- to 11-times of Vreg (1/2Vci or VREG pin input voltage).

Table 18 VR Bits and V1REF Voltage

VR2	VR1	VR0	V1REF Voltage Setting
0	0	0	Vreg × 4-times
0	0	1	Vreg × 5-times
0	1	0	Vreg × 6-times
0	1	1	Vreg × 7-times
1	0	0	Vreg × 8-times
1	0	1	Vreg × 9-times
1	1	0	Vreg × 10-times
1	1	1	Vreg × 11-times

Entry Mode (R05h)

Compare Register (R06h)

The write data sent from the microcomputer is modified in the HD66760 and written to the GRAM. The display data in the GRAM can be quickly rewritten to reduce the load of the microcomputer software processing. For details, see the Graphics Operation Function section.

SWP: When SWP = 1, the upper and lower bytes in the two-byte data sent from the microcomputer are swapped and written to the GRAM. When SWP = 0, this bit directly writes the two-byte data sent from the microcomputer to the GRAM. This swap processing is performed only for the data sent from the microcomputer before logical operation. When SWP = 1, the upper and lower bytes in the write data mask (WM15-0) are swapped to be executed with the write data.

I/D: When I/D = 1, the address counter (AC) is automatically incremented by 1 after the data is written to the GRAM. When I/D = 0, the AC is automatically decremented by 1 after the data is written to the GRAM.

AM: Set the automatic update method of the AC after the data is written to the GRAM. When AM = 0, the data is continuously written in parallel. When AM = 1, the data is continuously written vertically.

LG2-0: Compare the data read from the GRAM by the microcomputer with the compare registers (CP7-0) by a compare/logical operation and write the results to GRAM. For details, see the Logical/Compare Operation Function.

CP7-0: Set the compare register for the compare operation with the data read from the GRAM or written by the microcomputer.

R/W	RS	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
W	1	0	0	0	0	0	0	0	SWP	0	0	0	I/D	AM	LG2	LG1	LG0
W	1	0	0	0	0	0	0	0	0	CP7	CP6	CP5	CP4	CP3	CP2	CP1	CP0

Figure 9 Entry Mode and Compare Register

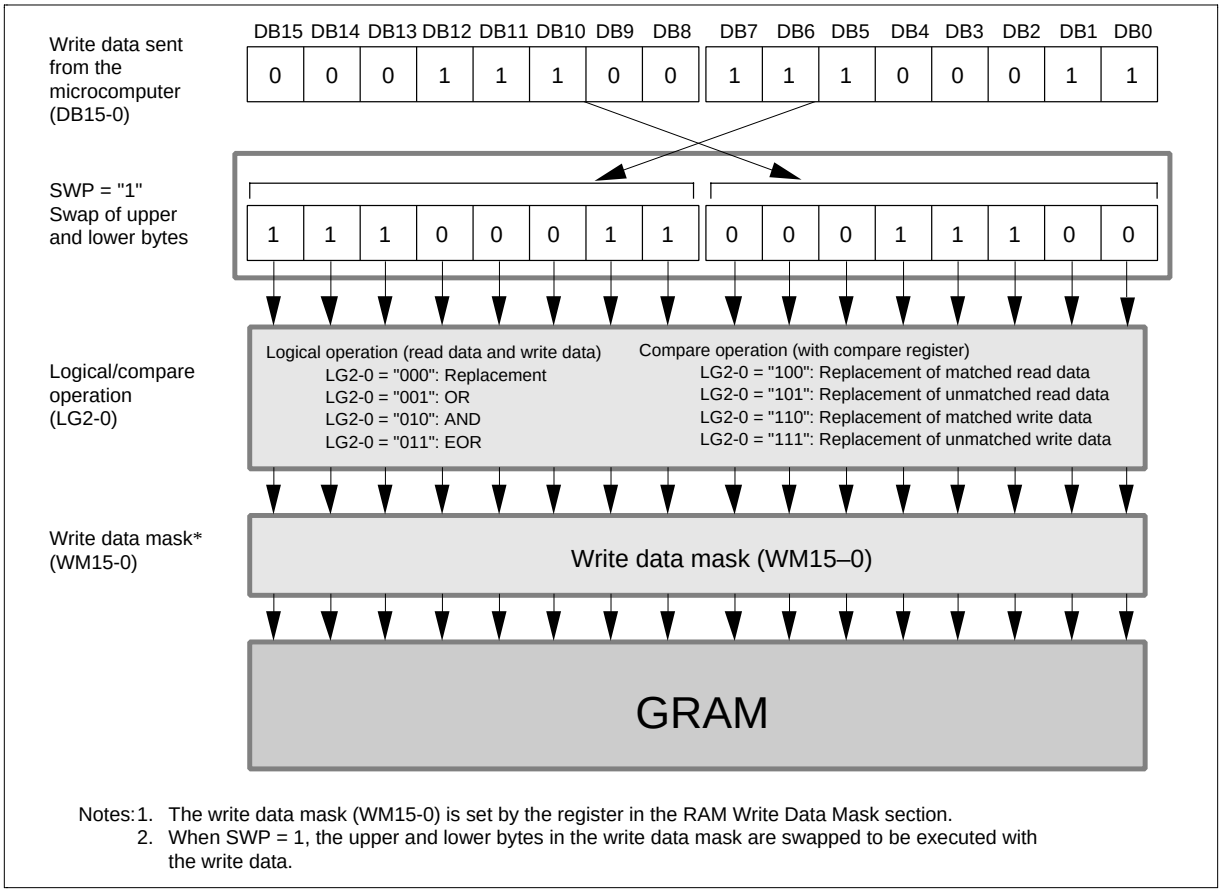


Figure 10 Logical/Compare Operation and Swapping for the GRAM

Display Control (R07h)

VLE2–1: When VLE1 = 1, a vertical scroll is performed in the 1st screen. When VLE2 = 1, a vertical scroll is performed in the 2nd screen. Vertical scrolling on the two screens can be independently controlled.

SPT: When SPT = 1, the 2-division LCD drive is performed. For details, see the Screen-division Driving Function section.

E: When E = 1, "pixel on/off" mode is enabled. Displayed pixel can be "all on" or "all off" regardless GRAM contents. The "all on" or "all off" can be seleced B/W bit setting. When the "pixel on/off" mode is enabled (E=1), the D0 and D1 should be 1 and REV should be 0 (display on and no reverse mode).

B/W: When E = 1 and B/W = 0, displayed pixel is "all off" regardless GRAM contents. When E = 1 and B/W = 1, displayed pixel is "all on" regardless GRAM contents.

GS: When GS = 0, the display is in eight grayscale mode and displays 256 colors by selecting eight grayscales from 16 grayscale levels. When GS = 1, the display is in four grayscales and displays 256 colors by selecting four grayscales from 16 grayscale levels. In four-grayscale mode, four colors can be displayed with two bits per pixel (RGB). GRAM data must be rewritten when the GS bit is swapped.

When GS = 1, the GRAM address increments or decrements addresses from 0000H to 4F0CH. For details, see the Grayscale Palette and Four-color Display Mode sections.

REV: Displays all character and graphics display sections with reversal when REV = 1. For details, see the Reversed Display Function section. Since the grayscale level can be reversed, display of the same data is enabled on normally-white and normally-black panels.

D1–0: Display is on when D1 = 1 and off when D1 = 0. When off, the display data remains in the GRAM, and can be displayed instantly by setting D1 = 1. When D1 is 0, the display is off with the SEG1 to SEG312 outputs and COM1 to COM80 outputs set to the GND level. Because of this, the HD66760 can control the charging current for the LCD with AC driving.

When D1-0 = 01, the internal display of the HD66760 is performed although the display is off. When D1-0 = 00, the internal display operation halts and the display is off.

Table 19 D Bits and Operation

D1	D0	SEG/COM Output	HD66760 Internal Display Operation
0	0	GND	Halt
0	1	GND	Operate
1	0	Unlit display	Operate
1	1	Display	Operate

Notes: 1. The internal power supply can operate independently from D1-0.
2. Writing from the microcomputer to the GRAM is independent from D1-0.
3. In the sleep and standby modes, D1-0 = 00. However, the register contents of D1-0 are not modified.

R/W	RS	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
W	1	0	0	0	0	0	VLE2	VLE1	SPT	0	0	E	B/W	GS	REV	D1	D0

Figure 11 Display Control Instruction

Cursor Control (R08h)

C: When C = 1, the window cursor display is started. The display mode is selected by the CM1-0 bits, and the display area is specified in a pixel unit by the horizontal cursor position register (HS6-0 and HE6-0 bits) and vertical cursor position register (VS6-0 and VE6-0 bits). The cursor color (CR, CG, or CB) can be set to any of eight colors in the window cursor. However, the cursor color cannot be controlled by the grayscale. For details, see the Color Window Cursor Control section.

CM1-0: The display mode of the window cursor is selected. These bits can display a eight-color cursor, reversed cursor, eight-color blink cursor, and reversed blink cursor.

CR/CB/CG: The window cursor color can be specified. Red, blue, green, white, black, or any combination color can be displayed. However, the cursor color cannot be controlled by the grayscale. For details, see the Color Window Cursor Control section.

R/W	RS	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
W	1	0	0	0	0	0	CR	CG	CB	0	0	0	C	0	0	CM1	CM0

Figure 12 Cursor Control Instruction

Table 20 CM Bits and Window Cursor Display Mode

D1	D0	Window Cursor Display Mode
0	0	Eight-color cursor (displaying the window cursor with the color specified by CR, CG, or CB)
0	1	Reversed cursor (displaying reversed grayscale data in the window cursor)
1	0	Eight-color blink cursor (alternately blinking normal and eight-color display of CR, CG, or CB in the window cursor)
1	1	Reversed blink cursor (alternately blinking normal and reversed display of the grayscale data in the window cursor)

Grayscale and Blink Synchronization (R09h)

Initializes the blink and frame counters, which control the blink cycle and grayscale generation, respectively.

R/W	RS	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
W	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 13 Grayscale and Blink Synchronization Instructions

Vertical Scroll Control (R11h)

VL16–11: Specify the display-start raster-row at the 1st screen display for vertical smooth scrolling. Any raster-row from the first to 80th can be selected. After the 80th raster-row is displayed, the display restarts from the first raster-row. The display-start raster-row (VL16-10) is valid only when VLE1 = 1. The raster-row display is fixed when VLE1 = 0. (VLE1 is the 1st-screen vertical-scroll enable bit.)

VL26–20: Specify the display-start raster-row at the 2nd screen display. The display-start raster-row (VL26-20) is valid only when VLE2 = 1. The raster-row display is fixed when VLE2 = 0. (VLE2 is the 2nd-screen vertical-scroll enable bit.) The vertical scroll for the 1st and 2nd screens can be independently set.

R/W	RS	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
W	1	0	VL26	VL25	VL24	VL23	VL22	VL21	VL20	0	VL16	VL15	VL14	VL13	VL12	VL11	VL10

Figure 14 Vertical Scroll Control Instruction

Table 21 VL Bits and Display-start Raster-row

VL26 VL16	VL25 VL15	VL24 VL14	VL23 VL13	VL22 VL12	VL21 VL11	VL20 VL10	Display-start Raster-row
0	0	0	0	0	0	0	1st raster-row
0	0	0	0	0	0	1	2nd raster-row
0	0	0	0	0	1	0	3rd raster-row
0	0	0	0	0	1	1	4th raster-row
0	0	0	0	1	0	0	5th raster-row
:	:	:	:	:	:	:	:
1	0	0	1	1	1	0	79th raster-row
1	0	0	1	1	1	1	80th raster-row

Note: Do not set over the 80th (4FH) raster-row.

Horizontal Cursor Position (R12h)

Vertical Cursor Position (R13h)

HS6–0: Specify the start position for horizontally displaying the window cursor in a pixel unit. The cursor is displayed from the 'set value + 1' pixel. Ensure that HS6-0 ≤ HE6-0.

HE6–0: Specify the end position for horizontally displaying the window cursor in a pixel unit. The cursor is displayed to the 'set value + 1' pixel. Ensure that HS6-0 ≤ HE6-0.

VS6–0: Specify the start position for vertically displaying the window cursor in a raster-row unit. The cursor is displayed from the 'set value + 1' raster-row. Ensure that VS6-0 ≤ VE6-0.

VE6–0: Specify the end position for vertically displaying the window cursor in a raster-row unit. The cursor is displayed to the 'set value + 1' raster-row. Ensure that VS6-0 ≤ VE6-0.

R/W	RS	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
W	1	0	HE6	HE5	HE4	HE3	HE2	HE1	HE0	0	HS6	HS5	HS4	HS3	HS2	HS1	HS0
W	1	0	VE6	VE5	VE4	VE3	VE2	VE1	VE0	0	VS6	VS5	VS4	VS3	VS2	VS1	VS0

Figure 15 Horizontal Cursor Position and Vertical Cursor Position Instructions

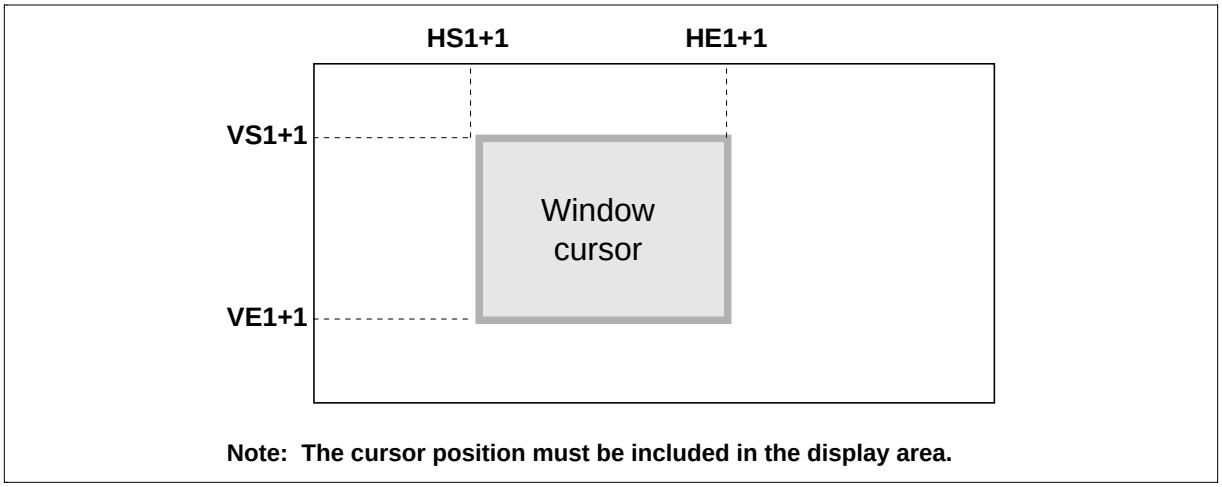


Figure 16 Window Cursor Position

1st Screen Driving Position (R14h)

2nd Screen Driving Position (R15h)

SS16–0: Specify the driving start position for the first screen in a line unit. The LCD driving starts from the 'set value + 1' common driver.

SE16–0: Specify the driving end position for the first screen in a line unit. The LCD driving is performed to the 'set value + 1' common driver. For instance, when SS16-10 = 07H and SE16-10 = 10H are set, the LCD driving is performed from COM8 to COM17, and non-selection driving is performed for COM1 to COM7, COM18, and others. Ensure that SS16-10 ≤ SE16-10 ≤ 4FH. For details, see the Screen-division Driving Function section.

SS26–0: Specify the driving start position for the second screen in a line unit. The LCD driving starts from the 'set value + 1' common driver. The second screen is driven when SPT = 1.

SE26–0: Specify the driving end position for the second screen in a line unit. The LCD driving is performed to the 'set value + 1' common driver. For instance, when SPT = 1, SS26-20 = 20H, and SE26-20 = 4FH are set, the LCD driving is performed from COM33 to COM80. Ensure that SS16-10 ≤ SE16-10 < SS26-20 ≤ SE26-20 ≤ 4FH. For details, see the Screen-division Driving Function section.

R/W	RS	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
W	1	0	SE16	SE15	SE14	SE13	SE12	SE11	SE10	0	SS16	SS15	SS14	SS13	SS12	SS11	SS10
W	1	0	SE26	SE25	SE24	SE23	SE22	SE21	SE20	0	SS26	SS25	SS24	SS23	SS22	SS21	SS20

Figure 17 1st Screen Driving Position and 2nd Screen Driving Position

RAM Write Data Mask (R20h)

WM15–0: In writing to the GRAM, these bits mask writing in a bit unit. When WM15 = 1, this bit masks the write data of DB15 and does not write to the GRAM. Similarly, the WM14-0 bits mask the write data of DB14-0 in a bit unit. When SWP = 1, the upper and lower bytes in the write data mask are swapped. For details, see the Graphics Operation Function section.

R/W	RS	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
W	1	WM15	WM14	WM13	WM12	WM11	WM10	WM9	WM8	WM7	WM6	WM5	WM4	WM3	WM2	WM1	WM0

Figure 18 RAM Write Data Mask Instruction

RAM Address Set (R21h)

AD14–0: Initially set GRAM addresses to the address counter (AC). Once the GRAM data is written, the AC is automatically updated according to the AM and I/D bit settings. This allows consecutive accesses without resetting addresses. Address update range is 0000H-4F33H (GS=0) and 0000H-4F0CH (GS=1). Once the GRAM data is read, the AC is not automatically updated. GRAM address setting is not allowed in the sleep mode or standby mode.

R/W	RS	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
W	1	0	AD14	AD13	AD12	AD11	AD10	AD9	AD8	0	0	AD5	AD4	AD3	AD2	AD1	AD0

Figure 19 RAM Address Set Instruction

Table 22 GRAM Address Range in Eight-grayscale Mode (GS = 0)

AD14–AD0	GRAM Setting
"0000"H–"0033"H	Bitmap data for COM1
"0100"H–"0133"H	Bitmap data for COM2
"0200"H–"0233"H	Bitmap data for COM3
"0300"H–"0333"H	Bitmap data for COM4
:	:
"AC00"H–"4C33"H	Bitmap data for COM77
"AD00"H–"4D33"H	Bitmap data for COM78
"AE00"H–"4E33"H	Bitmap data for COM79
"AF00"H–"4F33"H	Bitmap data for COM80

Table 23 GRAM Address Range in Four-grayscale Mode (GS = 1)

AD14–AD0	GRAM Setting
"0000"H–"000C"H	Bitmap data for COM1
"0100"H–"010C"H	Bitmap data for COM2
"0200"H–"020C"H	Bitmap data for COM3
"0300"H–"030C"H	Bitmap data for COM4
:	:
"AC00"H–"4C0C"H	Bitmap data for COM77
"AD00"H–"4D0C"H	Bitmap data for COM78
"AE00"H–"4E0C"H	Bitmap data for COM79
"AF00"H–"4F0C"H	Bitmap data for COM80

Write Data to GRAM (R22h)

WD15–0 : Write 16-bit data to the GRAM. This data calls each grayscale palette. After a write, the address is automatically updated according to the AM and I/D bit settings. During the sleep and standby modes, the GRAM cannot be accessed.

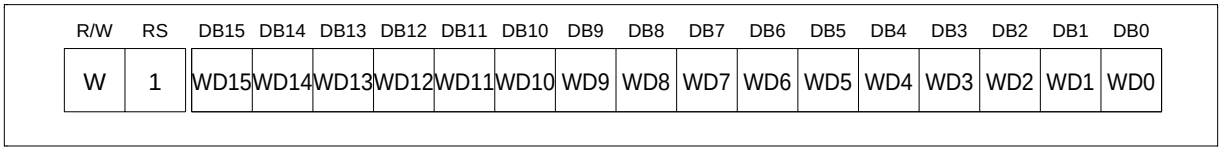


Figure 20 Write Data to GRAM Instruction

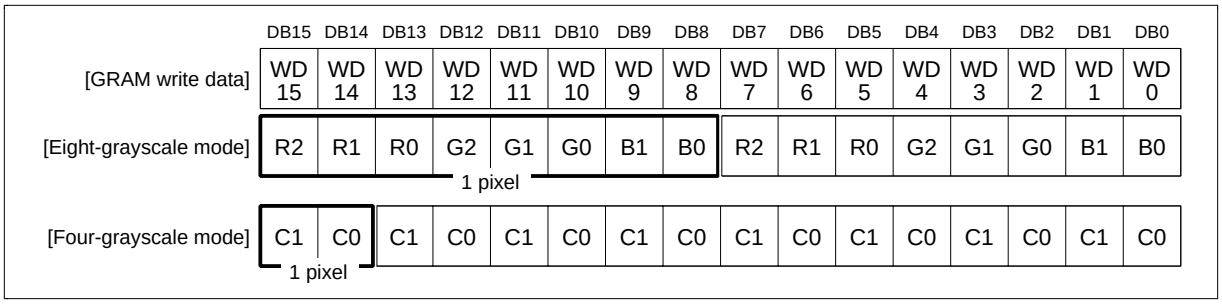


Figure 21 GRAM Write Data

Table 24 GRAM Data and R Grayscale Palette in the Eight-grayscale Mode (GS = 0)

GRAM Data Setting						
R2	R1	R0	<R> Grayscale Palette			
0	0	0	RK03	RK02	RK01	RK00
0	0	1	RK13	RK12	RK11	RK10
0	1	0	RK23	RK22	RK21	RK20
0	1	1	RK33	RK32	RK31	RK30
1	0	0	RK43	RK42	RK41	RK40
1	0	1	RK53	RK52	RK51	RK50
1	1	0	RK63	RK62	RK61	RK60
1	1	1	RK73	RK72	RK71	RK70

Table 25 GRAM Data and G Grayscale Palette in the Eight-grayscale Mode (GS = 0)

GRAM Data Setting						
G2	G1	G0	<G> Grayscale Palette			
0	0	0	GK03	GK02	GK01	GK00
0	0	1	GK13	GK12	GK11	GK10
0	1	0	GK23	GK22	GK21	GK20
0	1	1	GK33	GK32	GK31	GK30
1	0	0	GK43	GK42	GK41	GK40
1	0	1	GK53	GK52	GK51	GK50
1	1	0	GK63	GK62	GK61	GK60
1	1	1	GK73	GK72	GK71	GK70

Table 26 GRAM Data and B Grayscale Palette in the Eight-grayscale Mode (GS = 0)

GRAM Data Setting					
B1	B0	<B> Grayscale Palette			
0	0	BK03	BK02	BK01	BK00
0	1	BK13	BK12	BK11	BK10
1	0	BK23	BK22	BK21	BK20
1	1	BK33	BK32	BK31	BK30

Table 27 GRAM Data and Grayscale Palette in the Four-grayscale Mode (GS = 1)

GRAM Data Setting													
C1	**C0**	**<R> Grayscale Palette**				**<G> Grayscale Palette**				**<B> Grayscale Palette**			
0	0	RK03	RK02	RK01	RK00	GK03	GK02	GK01	GK00	BK03	BK02	BK01	BK00
0	1	RK13	RK12	RK11	RK10	GK13	GK12	GK11	GK10	BK13	BK12	BK11	BK10
1	0	RK23	RK22	RK21	RK20	GK23	GK22	GK21	GK20	BK23	BK22	BK21	BK20
1	1	RK33	RK32	RK31	RK30	GK33	GK32	GK31	GK30	BK33	BK32	BK31	BK30

Read Data from GRAM (R22h)

RD15–0: Read 16-bit data from the GRAM. When the data is read to the microcomputer, the first-word read immediately after the GRAM address setting is latched from the GRAM to the internal read-data latch. The data on the data bus (DB15-0) becomes invalid and the second-word read is normal.

When bit processing, such as a logical operation, is performed within the HD66760, only one read can be processed since the latched data in the first word is used.

R/W	RS	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
R	1	RD 15	RD 14	RD 13	RD 12	RD 11	RD 10	RD 9	RD 8	RD 7	RD 6	RD 5	RD 4	RD 3	RD 2	RD 1	RD 0

Figure 22 Read Data from GRAM Instruction

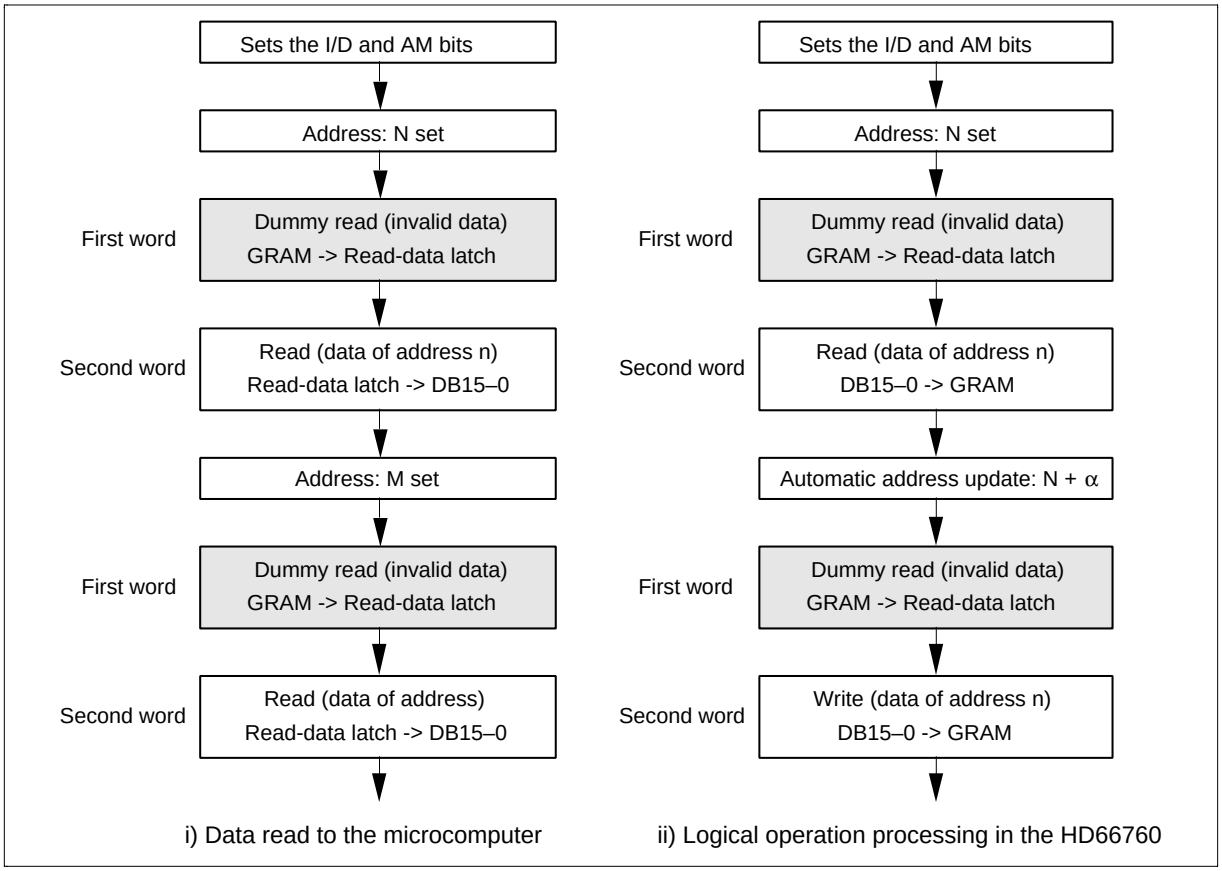


Figure 23 GRAM Read Sequence

Grayscale Palette Control (R30h to R39h)

RK73–00: Specify the R-grayscale level for eight palettes from the 16-grayscale level. For details, see the Grayscale Palette and Grayscale Palette Table sections.

In four-grayscale display mode, the number of palettes to be used is four. For details, see the Four-grayscale Display Mode section.

GK73–00: Specify the G-grayscale level for eight palettes from the 16-grayscale level. For details, see the Grayscale Palette and Grayscale Palette Table sections.

In four-grayscale display mode, the number of palettes to be used is four. For details, see the Four-grayscale Display Mode section.

BK33–00: Specify the B-grayscale level for four palettes from the 16-grayscale level. For details, see the Grayscale Palette and Grayscale Palette Table sections.

In four-grayscale display mode, the number of palettes to be used is four. For details, see the Four-grayscale Display Mode section.

	R/W	RS	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
R30	W	1	0	0	0	0	RK 13	RK 12	RK 11	RK 10	0	0	0	0	RK 03	RK 02	RK 01	RK 00
R31	W	1	0	0	0	0	RK 33	RK 32	RK 31	RK 30	0	0	0	0	RK 23	RK 22	RK 21	RK 20
R32	W	1	0	0	0	0	RK 53	RK 52	RK 51	RK 50	0	0	0	0	RK 43	RK 42	RK 41	RK 40
R33	W	1	0	0	0	0	RK 73	RK 72	RK 71	RK 70	0	0	0	0	RK 63	RK 62	RK 61	RK 60
R34	W	1	0	0	0	0	GK 13	GK 12	GK 11	GK 10	0	0	0	0	GK 03	GK 02	GK 01	GK 00
R35	W	1	0	0	0	0	GK 33	GK 32	GK 31	GK 30	0	0	0	0	GK 23	GK 22	GK 21	GK 20
R36	W	1	0	0	0	0	GK 53	GK 52	GK 51	GK 50	0	0	0	0	GK 43	GK 42	GK 41	GK 40
R37	W	1	0	0	0	0	GK 73	GK 72	GK 71	GK 70	0	0	0	0	GK 63	GK 62	GK 61	GK 60
R38	W	1	0	0	0	0	BK 13	BK 12	BK 11	BK 10	0	0	0	0	BK 03	BK 02	BK 01	BK 00
R39	W	1	0	0	0	0	BK 33	BK 32	BK 31	BK 30	0	0	0	0	BK 23	BK 22	BK 21	BK 20

Figure 24 Grayscale Palette Control Instruction

Test Register (R40h to R44h)

Index registers R40h-R44h cannot be used or set since they are test registers. Do not change the contents of the instruction bits in these registers.

R/W	RS	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
W	1	Test register															

Figure 25 Test Register Instruction

Table 28 Instruction List

Reg. No.	Register Name	R/W	RS	Upper Code DB 15	DB 14	DB 13	DB 12	DB 11	DB 10	DB 9	DB 8	Lower Code DB 7	DB 6	DB 5	DB 4	DB 3	DB 2	DB 1	DB 0	Description	Execution Cycle
IR	Index	0	0	*	*	*	*	*	*	*	*	*	ID6	ID5	ID4	ID3	ID2	ID1	ID0	Sets the index register value.	0
SR	Status read	1	0	0	L6	L5	L4	L3	L2	L1	L0	0	C6	C5	C4	C3	C2	C1	C0	Reads the driving raster-row position (L7–0) and contrast setting (C6–0).	0
R00h	Start oscillation	0	1	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	1	Starts the oscillation mode.	10 ms
	Device code read	1	1	1	0	0	0	0	1	1	1	0	1	1	0	0	0	0	0	Reads 8760h	0
R01h	Driver output control	0	1	0	0	0	0	0	0	CMS	SGS	0	0	0	0	NL3	NL2	NL1	NL0	Sets the common driver shift direction (CMS), segment driver shift direction (SGS), and driving duty ratio (NL3–0).	0
R02h	LCD-driving-waveform control	0	1	0	0	0	0	0	0	0	RST	0	B/C	EOR	NW4	NW3	NW2	NW1	NW0	Software reset (RST), LCD drive AC waveform (B/C), EOR output (EOR), and the number of n-raster-rows (NW4–0) at C-pattern AC drive.	10 tcyc
R03h	Power control	0	1	0	0	0	BS2	BS1	BS0	BT1	BT0	PS1	PS0	DC1	DC0	AP1	AP0	SLP	STB	Sets the sleep mode (SLP), standby mode (STB), LCD power on (AP1–0), boosting cycle (DC1–0), boosting output multiplying factor (BT1–0), and LCD drive bias value (BS2–0).	0
R04h	Contrast control	0	1	0	0	0	0	0	VR2	VR1	VR0	0	CT6	CT5	CT4	CT3	CT2	CT1	CT0	Sets the contrast adjustment (CT6–0) and regulator adjustment (VR2–0).	0
R05h	Entry mode	0	1	0	0	0	0	0	0	0	SWP	0	0	0	I/D	AM	LG2	LG1	LG0	Specifies the logical operation (LG2–0), AC counter mode (AM), increment/decrement mode (I/D), and swap (SWP).	0
R06h	Compare register	0	1	0	0	0	0	0	0	0	0	CP7	CP6	CP5	CP4	CP3	CP2	CP1	CP0	Sets the compare register (CP7–0).	0
R07h	Display control	0	1	0	0	0	0	0	VLE2	VLE1	SPT	0	0	E	B/W	GS	REV	D1	D0	Specifies display on (D1–0), reversed display (REV), 4-/16-grayscale mode (GS), pixel mode enable (E), pixel on/off (B/W), screen division driiving (SPT), and vertical scroll (VLE2–1).	0
R08h	Cursor control	0	1	0	0	0	0	0	CR	CG	CB	0	0	0	C	0	0	CM1	CM0	Specifies cursor display on (C), cursor display mode (CM1–0), and cursor color (CR, CG, or CB).	
R09h	Grayscale and blink synchroni-zation	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	Synchronizes the grayscale with the blink cycle.	0
R11h	Vertical scroll control	0	1	0	VL26	VL25	VL24	VL23	VL22	VL21	VL20	0	VL16	VL15	VL14	VL13	VL12	VL11	VL10	Specifies the 1st-screen display-start raster-row (VL16–10) and 2nd-screen display-start raster-row (VL26–20).	0
R12h	Horizontal cursor position	0	1	0	HE6	HE5	HE4	HE3	HE2	HE1	HE0	0	HS6	HS5	HS4	HS3	HS2	HS1	HS0	Sets horizontal cursor start (HS6–0) and end (HE6–0).	0
R13h	Vertical cursor position	0	1	0	VE6	VE5	VE4	VE3	VE2	VE1	VE0	0	VS6	VS5	VS4	VS3	VS2	VS1	VS0	Sets vertical cursor start (VS6–0) and end (VE6–0).	0
R14h	1st screen driving position	0	1	0	SE16	SE15	SE14	SE13	SE12	SE11	SE10	0	SS16	SS15	SS14	SS13	SS12	SS11	SS10	Sets 1st-screen driving start (SS16–10) and end (SE16–10).	0
R15h	2nd screen driving position	0	1	0	SE26	SE25	SE24	SE23	SE22	SE21	SE20	0	SS26	SS25	SS24	SS23	SS22	SS21	SS20	Sets 2nd-screen driving start (SS26–20) and end (SE26–20).	0
R20h	RAM write data mask	0	1	WM15	WM14	WM13	WM12	WM11	WM10	WM9	WM8	WM7	WM6	WM5	WM4	WM3	WM2	WM1	WM0	Specifies write data mask (WM15–0) at RAM write.	0

Table 28 Instruction List (cont)

Reg. No.	Register Name	R/W	RS	Upper Code DB 15	DB 14	DB 13	DB 12	DB 11	DB 10	DB 9	DB 8	Lower Code DB 7	DB 6	DB 5	DB 4	DB 3	DB 2	DB 1	DB 0	Description	Execution Cycle
R21h	RAM address set	0	1	0	AD14–8 (upper)							0	0	AD5–0 (lower)						Initially set the RAM address to the address counter (AC).	0
R22h	Write data to GRAM	0	1	Write Data (upper)								Write Data (lower)								Writes data to the RAM.	0
	Read data from GRAM	1	1	Read Data (upper)								Read Data (lower)								Reads data from the RAM.	0
R30h	R-grayscale palette control (1)	0	1	0	0	0	0	RK 13	RK 12	RK 11	RK 10	0	0	0	0	RK 03	RK 02	RK 01	RK 00	Specifies the R-grayscale palette.	0
R31h	R-grayscale palette control (2)	0	1	0	0	0	0	RK 33	RK 32	RK 31	RK 30	0	0	0	0	RK 23	RK 22	RK 21	RK 20	Specifies the R-grayscale palette.	0
R32h	R-grayscale palette control (3)	0	1	0	0	0	0	RK 53	RK 52	RK 51	RK 50	0	0	0	0	RK 43	RK 42	RK 41	RK 40	Specifies the R-grayscale palette.	0
R33h	R-grayscale palette control (4)	0	1	0	0	0	0	RK 73	RK 72	RK 71	RK 70	0	0	0	0	RK 63	RK 62	RK 61	RK 60	Specifies the R-grayscale palette.	0
R34h	G-grayscale palette control (1)	0	1	0	0	0	0	GK 13	GK 12	GK 11	GK 10	0	0	0	0	GK 03	GK 02	GK 01	GK 00	Specifies the G-grayscale palette.	0
R35h	G-grayscale palette control (2)	0	1	0	0	0	0	GK 33	GK 32	GK 31	GK 30	0	0	0	0	GK 23	GK 22	GK 21	GK 20	Specifies the G-grayscale palette.	0
R36h	G-grayscale palette control (3)	0	1	0	0	0	0	GK 53	GK 52	GK 51	GK 50	0	0	0	0	GK 43	GK 42	GK 41	GK 40	Specifies the G-grayscale palette.	0
R37h	G-grayscale palette control (4)	0	1	0	0	0	0	GK 73	GK 72	GK 71	GK 70	0	0	0	0	GK 63	GK 62	GK 61	GK 60	Specifies the G-grayscale palette.	0
R38h	B-grayscale palette control (1)	0	1	0	0	0	0	BK 13	BK 12	BK 11	BK 10	0	0	0	0	BK 03	BK 02	BK 01	BK 00	Specifies the B-grayscale palette.	0
R39h	B-grayscale palette control (2)	0	1	0	0	0	0	BK 33	BK 32	BK 31	BK 30	0	0	0	0	BK 23	BK 22	BK 21	BK 20	Specifies the B-grayscale palette.	0
R40h	Test register (1)	0	1	Test register (disabled)																Disables the use or setting of this register since this is the test register.	0
R41h	Test register (2)	0	1	Test register (disabled)																Disables the use or setting of this register since this is the test register.	0
R42h	Test register (3)	0	1	Test register (disabled)																Disables the use or setting of this register since this is the test register.	0
R43h	Test register (4)	0	1	Test register (disabled)																Disables the use or setting of this register since this is the test register.	0
R44h	Test register (5)	0	1	Test register (disabled)																Disables the use or setting of this register since this is the test register.	0

Note: '*' means 'doesn't matter'.

Reset Function

The HD66760 is internally initialized by RESET input. Because the busy flag (BF) indicates a busy state (BF = 1) during the reset period, no instruction or GRAM data access from the MPU is accepted. The reset input must be held for at least 1 ms. Do not access the GRAM or initially set the instructions until the R-C oscillation frequency is stable after power has been supplied (10 ms).

Instruction Set Initialization:

1. Start oscillation executed
2. Driver output control (NL3–0 = 1001, SGS = 0, CMS = 0)
3. B-pattern waveform AC drive (RST = 0, B/C = 0, ECR = 0, NW4–0 = 00000)
4. Power control (PS1–0 = 00, DC1–0 = 00, AP1–0 = 00: LCD power off, SLP = 0: Sleep mode off, STB = 0: Standby mode off)
5. 1/10 bias drive (BS2–0 = 001), Three-times step-up (BT1–0 = 00), Weak contrast (CT6–0 = 0000000)
6. Entry mode set (SWP = 0, I/D = 1: Increment by 1, AM = 0: Horizontal move, LG2–0 = 000: Replace mode)
7. Compare register (CP7–0: 00000000)
8. Display control (VLE2–1 = 00: No vertical scroll, SPT = 0, E = 0, B/W = 0, GS = 0: Eight-grayscale mode, REV = 0, D1–0 = 00: Display off)
9. Cursor control (CR/CG/CB = 000, C = 0: Cursor display off, CM1–0 = 00)
10. Vertical scroll (VL26–20 = 000000, VL16–10 = 000000)
11. Window cursor display position (HS6–0 = HE6–0 = VS6–0 = VE6–0 = 00000000)
12. 1st screen division (SS16–10 = 00000000, SE16–10 = 11111111)
13. 2nd screen division (SS26–20 = 00000000, SE26–20 = 11111111)
14. RAM write data mask (WM15–0 = 0000H: No mask)
15. RAM address set (AD14–0 = 0000H)
16. Grayscale palette
    (RK03–00 = 0000, RK13–10 = 0011, RK23–20 = 0101, RK33–30 = 0111,
    RK43–40 = 1001, RK53–50 = 1011, RK63–60 = 1101, RK73–70 = 1111,
    GK03–00 = 0000, GK13–10 = 0011, GK23–20 = 0101, GK33–30 = 0111,
    GK43–40 = 1001, GK53–50 = 1011, GK63–60 = 1101, GK73–70 = 1111,
    BK03–00 = 0000, BK13–10 = 0101, BK23–20 = 1001, BK33–30 = 1111)

GRAM Data Initialization:

This is not automatically initialized by reset input but must be initialized by software while display is off (D1-0 = 00).

Output Pin Initialization:

1. LCD driver output pins (SEG/COM): Output GND level
2. Step-up circuit output pin (VLOUT): Outputs Vcc level
3. Oscillator output pin (OSC2): Outputs oscillation signal

Parallel Data Transfer

16-bit Bus Interface

Setting the IM2-0 (interface mode) to the GND/GND/GND level allows 68-system E-clock-synchronized 16-bit parallel data transfer. Setting the IM2-0 to the GND/Vcc/GND level allows 80-system 16-bit parallel data transfer. When the number of buses or the mounting area is limited, use an 8-bit bus interface.

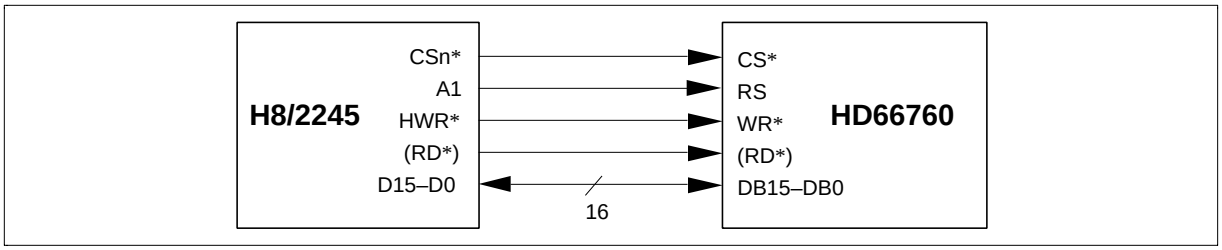


Figure 26 Interface to 16-bit Microcomputer

8-bit Bus Interface

Setting the IM2-0 (interface mode) to the GND/GND/Vcc level allows 68-system E-clock-synchronized 8-bit parallel data transfer using pins DB15-DB8. Setting the IM2-0 to the GND/Vcc/Vcc level allows 80-system 8-bit parallel data transfer. The 16-bit instructions and RAM data are divided into eight upper/lower bits and the transfer starts from the upper eight bits. Fix unused pins DB7-DB0 to the Vcc or GND level. Note that the upper bytes must also be written when the index register is written to.

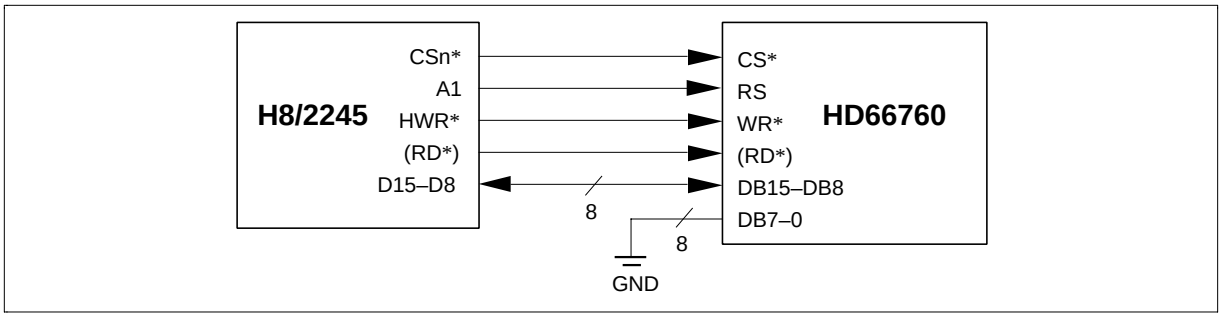


Figure 27 Interface to 8-bit Microcomputer

Note: Transfer synchronization function for an 8-bit bus interface
The HD66760 supports the transfer synchronization function which resets the upper/lower counter to count upper/lower 8-bit data transfer in the 8-bit bus interface. Noise causing transfer mismatch between the eight upper and lower bits can be corrected by a reset triggered by consecutively writing a 00H instruction four times. The next transfer starts from the upper eight bits. Executing synchronization function periodically can recover any runaway in the display system.

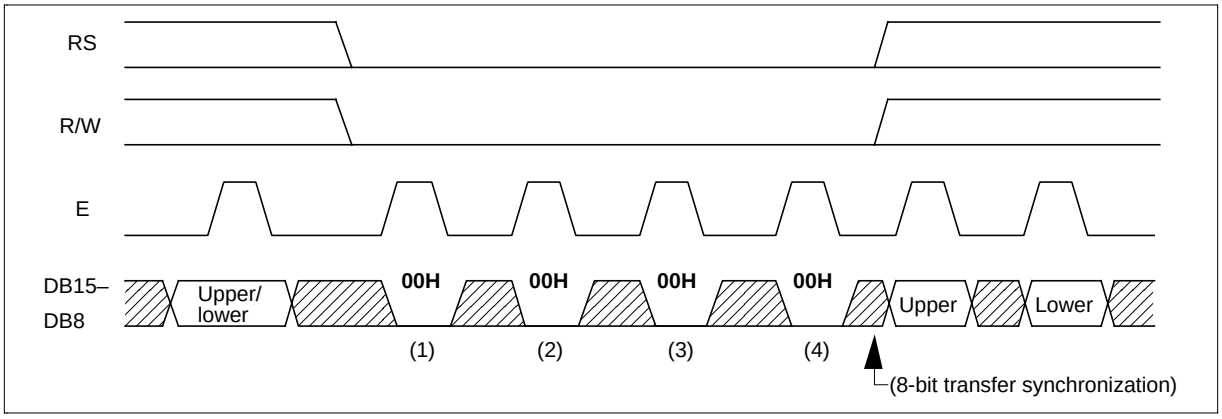


Figure 28 8-bit Transfer Synchronization

Serial Data Transfer (I2C bus interface)

Setting the IM2=Vcc and IM1=Vcc level allows I2C bus interface, using the serial data line (SDA) and serial transfer clock line (SCL). For the I2C bus interface, the IM0/ID pin function uses an ID pin.

The HD66760W is initiated serial data transfer by transferring the first byte when a high SCL level at the falling edge of the SDA input is sampled; it ends serial data transfer when a high SCL level at the rising edge of the SDA input is sampled.

Table 29 illustrates the start byte of I2C bus interface data and Figure 29 and 30 show the I2C bus interface timing sequence.

The HD66760W is selected when the higher 6-bit slave address in the first byte transferred from the master device match the 6-bits device identification code assigned to the HD66760W. The HD66760W, when selected, receive the subsequent data string. The lower 1-bit of the device identification code can be determined by the ID pin; select an appropriate code that is not assigned to any other slave device. The upper five bits are fixed to 01110. One slave address is assigned to a single HD66760W.

The ninth bit of the first byte is a receive-data acknowledge bit (ACK). When the received slave address matches the device ID code, HD66760W pulls down the ACK bit to a low level. Therefore, the ACK output buffer is an open-drain structure, only allowing low-level output. However, the ACK bit is undermined immediately after power-on; make sure to initialize the LSI using the RESET* input.

After identifying the address in the first byte, the HD66760W receives the subsequent data as an HD66760W index or as RAM data. Having received 8-bit data normally, HD66760W pulls down the ninth bit (ACK) to a low level. The index register or RAM data is 16-bits data format. Therefore data transfer has to be two 8-bit access cycles after first byte transfer.

Five bytes of GRAM read data after the start byte are invalid. The HD66760W start to read correct GRAM data from sixth byte.

Table 29 Start Byte Format

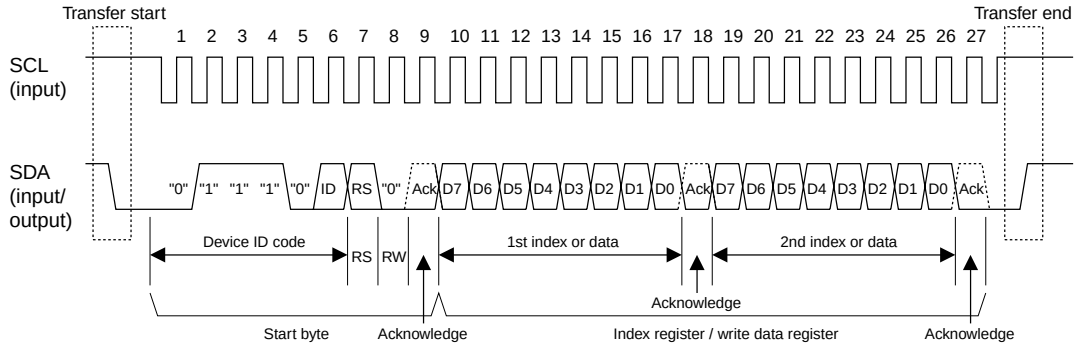
Transfer Bit	S	1	2	3	4	5	6	7	8	9
Start byte format	Transfer start	Device ID code						RS	R/W	ACK
		0	1	1	1	0	ID			

Note: ID bit is selected by the IM0/ID pin.

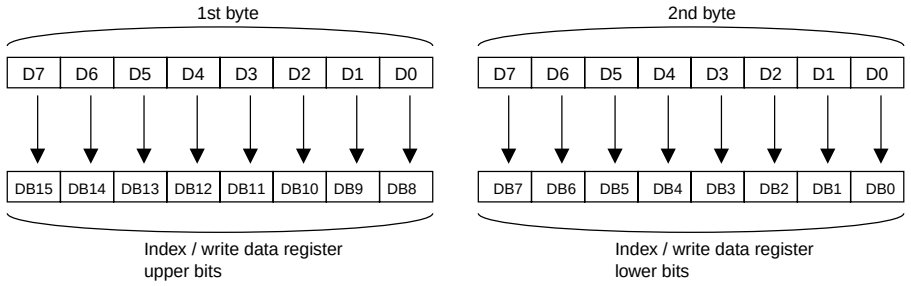
Table 30 RS and R/W bit function

RS	R/W	Function
0	0	Write index register to index
0	1	Reads status
1	0	Write control register or GRAM via write data register
1	1	Read GRAM via read data register

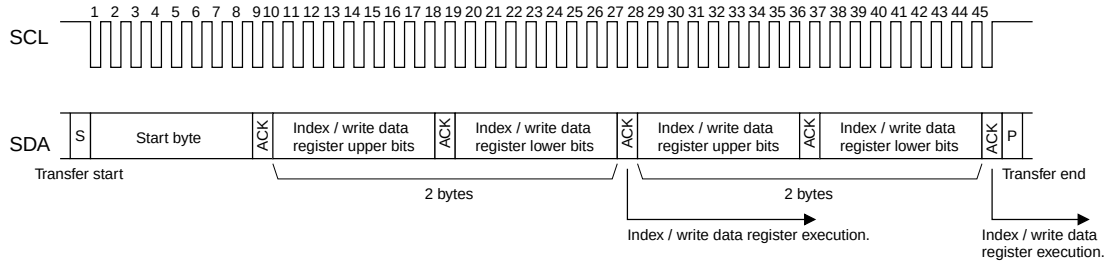
a) Basic data-receive timing through the I²C bus interface



b) 1st and 2nd byte assignment



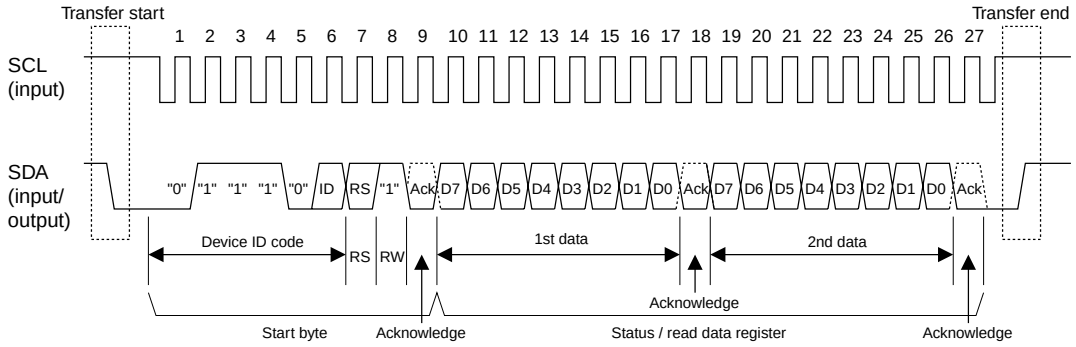
c) Consecutive data-receive timing through the I²C bus interface



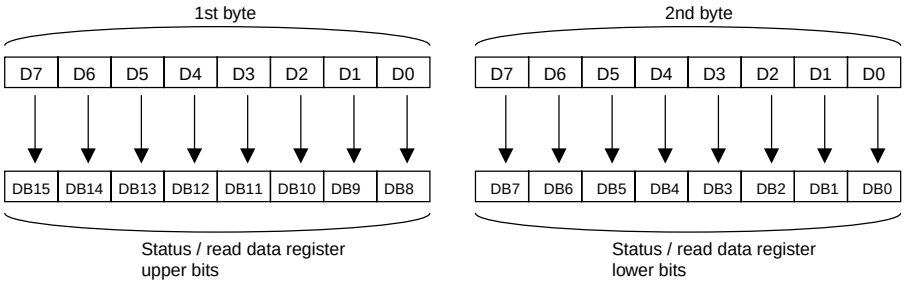
note:
- After start byte transfer, upper bits of the index or write data register should be written first.
- Start byte should be transfered just after start (S).
- Index or write data register is executed when upper and lower bits are written.
  Therefore, data transfer unit has to be twice byte access cycle.

Figure 29 I²C bus interface data-receive sequence

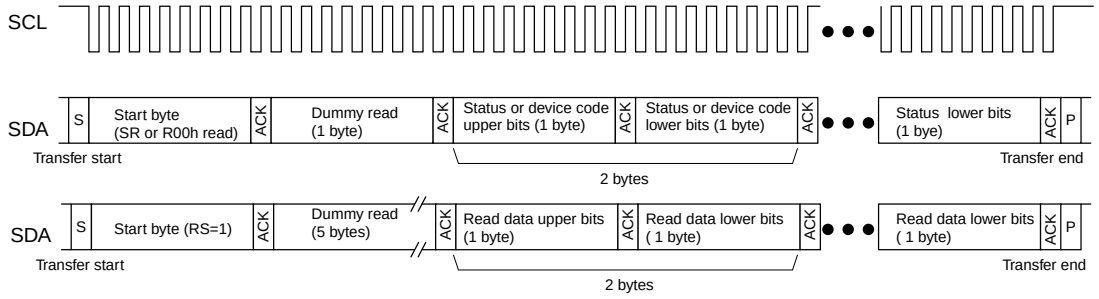
a) Basic data-send timing through the I²C bus interface



b) 1st and 2nd byte assignment



c) Consecutive data-send timing through the I²C bus interface



note:
- After start byte transfer, upper bits of the status or read data register should be read first.
- Start byte should be transfered just after start (S).

Figure 30 I²C bus interface data-send sequence

Serial Data Transfer (Clock synchronized serial interface)

Setting the IM2=Vcc and IM1=GND level allows standard clock synchronized serial data transfer, using the chip select line (CS*), serial data line (SDA) and serial transfer clock line (SCL). For the clock synchronized serial interface, the IM0/ID pin function uses an ID pin.

The HD66760 initiates clock synchronized serial data transfer by transferring the first byte at the falling edge of CS* input. It ends clock synchronized serial data transfer the rising edge of CS* input.

The HD66760 is selected when the higher 6-bit slave address in the first byte transferred from the transmitting device match the 6-bits device identification code assigned to the HD66760. The HD66760, when selected, receive the subsequent data string. The lower 1-bit of the device identification code can be determined by the ID pin. The upper five bits are fixed to 01110. Two different chip address must be assigned to a single HD66760 because the seventh bit of the start byte is used as a register select bit (RS); that is, when RS=0, an index can be written, and when RS=1, control register and GRAM data can be written or read from GRAM. Read or write is selected according to the eighth bit of the start byte (R/W bit). The data is received when the R/W bit is 0, and is transmitted when the R/W bit is 1.

After receiving the start byte, the HD66760 receives the subsequent data as an HD66760 index or as GRAM data.

Five bytes of GRAM read data after the start byte are invalid. The HD66760 start to read correct GRAM data from sixth byte.

Table 30a Start Byte Format

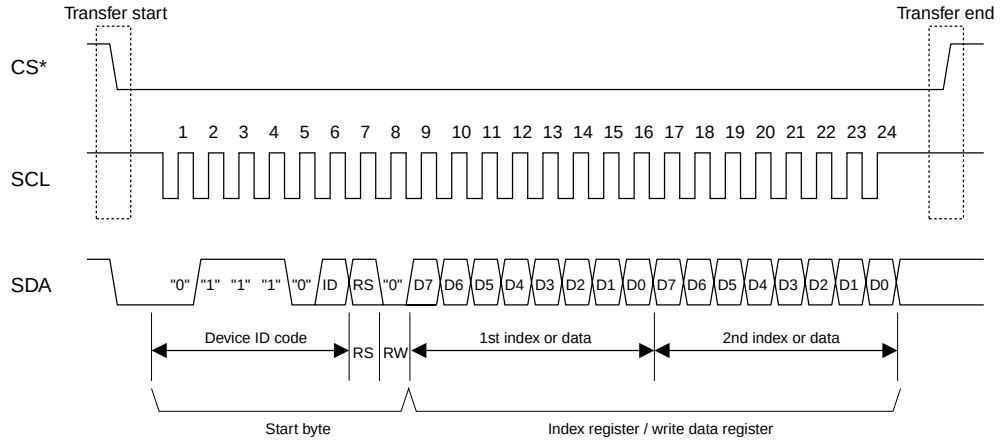
Transfer Bit	S	1	2	3	4	5	6	7	8
Start byte format	Transfer start	Device ID code						RS	R/W
		0	1	1	1	0	ID		

Note: ID bit is selected by the IM0/ID pin.

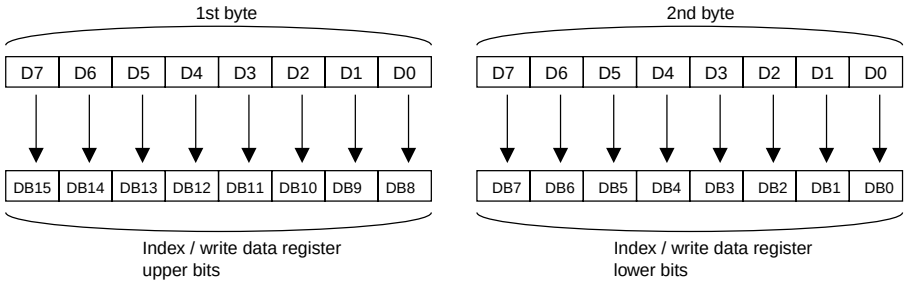
Table 30b RS and R/W bit function

RS	R/W	Function
0	0	Write index register to index
0	1	Reads status
1	0	Write control register or GRAM via write data register
1	1	Read GRAM via read data register

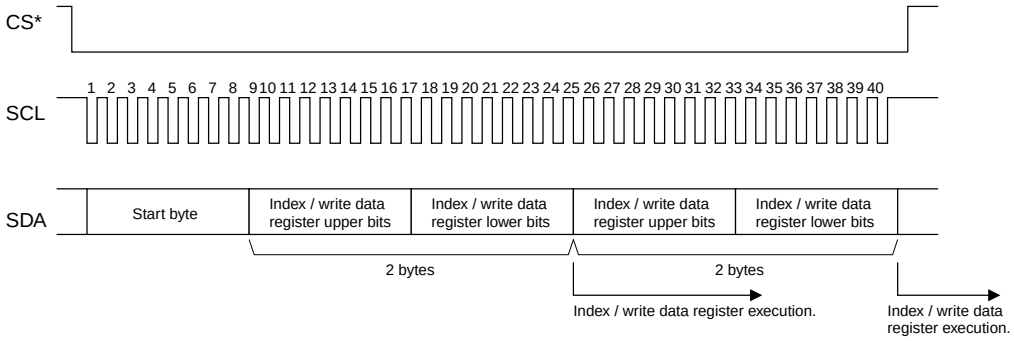
a) Basic data-receive timing through the clock synchronized serial interface



b) 1st and 2nd byte assignment



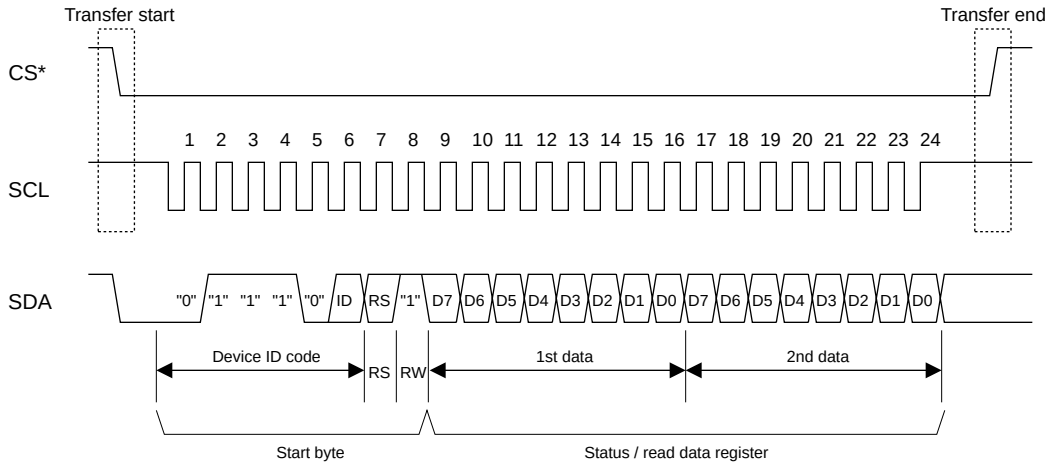
c) Consecutive data-receive timing through the clock synchnorized serial interface



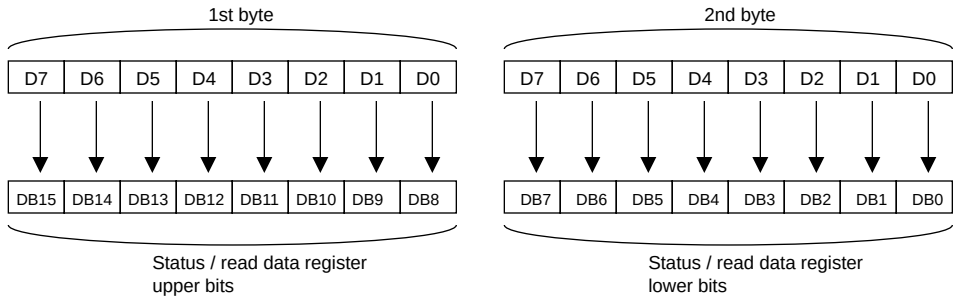
note:
- After start byte transfer, upper bits of the index or write data register should be written first.
- Start byte should be transfered first.
- Index or write data register is executed when upper and lower bits are written.
  Therefore, data transfer unit has to be twice byte access cycle.

Figure 30a Clock synchronized serial interface data-receive sequence

a) Basic data-send timing through the clock synchronized serial interface



b) 1st and 2nd byte assignment



c) Consecutive data-send timing through the clock synchnorized serial interface

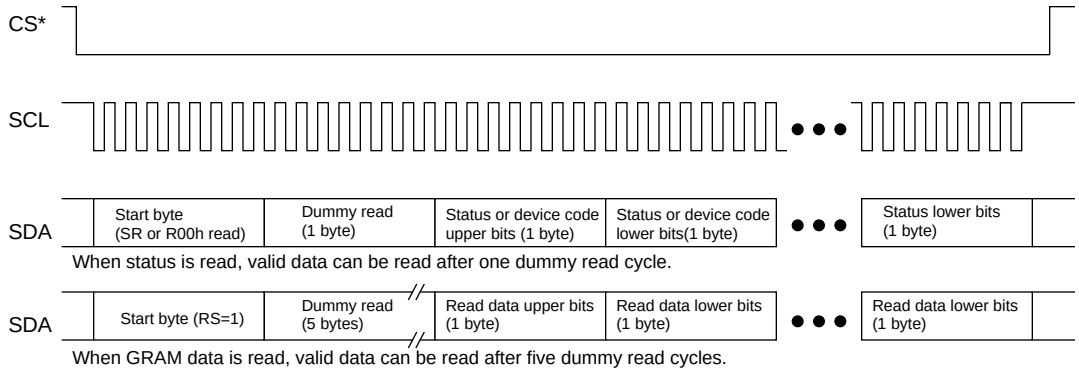


Figure 30b Clock synchronized serial interface data-send sequence

Graphics Operation Function

The HD66760 can greatly reduce the load of the microcomputer graphics software processing through the 16-bit bus architecture and internal graphics-bit operation function. This function supports the following:

1. A swap function that exchanges the upper and lower bytes in the 16-bit data sent from the microcomputer.
2. A write data mask function that selectively rewrites some of the bits in the 16-bit write data.
3. A logical operation write function that writes the data sent from the microcomputer and the original RAM data by a logical operation.
4. A conditional write function that compares the original RAM data or write data and the compare-bit data and writes the data sent from the microcomputer only when the conditions match.

Even if the display size is large, the display data in the graphics RAM (GRAM) can be quickly rewritten.

The graphics bit operation can be controlled by combining the entry mode register, the bit set value of the RAM-write-data mask register, and the read/write from the microcomputer.

Table 31 Graphics Operation

	Bit Setting			
Operation Mode	**I/D**	**AM**	**LG2–0**	**Operation and Usage**
Write mode 1	0/1	0	000	Horizontal data replacement, horizontal-border drawing
Write mode 2	0/1	1	000	Vertical data replacement, vertical-border drawing
Write mode 3	0/1	0	110 111	Conditional horizontal data replacement, horizontal-border drawing
Write mode 4	0/1	1	110 111	Conditional vertical data replacement, vertical-border drawing
Read/write mode 1	0/1	0	001 010 011	Horizontal data write with logical operation, horizontal-border drawing
Read/write mode 2	0/1	1	001 010 011	Vertical data write with logical operation, vertical-border drawing
Read/write mode 3	0/1	0	100 101	Conditional horizontal data replacement, horizontal-border drawing
Read/write mode 4	0/1	1	100 101	Conditional vertical data replacement, vertical-border drawing

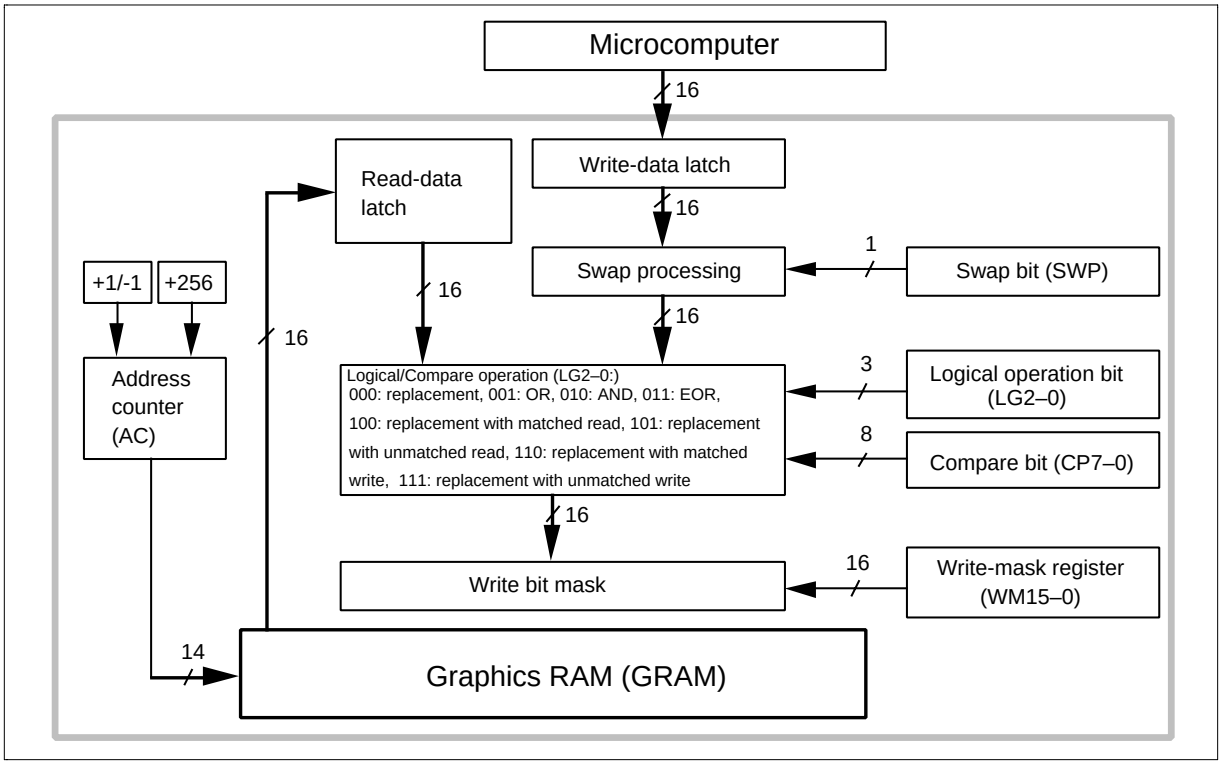


Figure 31 Data Processing Flow of the Graphics Bit Operation

Swap Function

The HD66760 has a byte-wise swap function that exchanges the upper and lower bytes in the two-byte data sent from the microcomputer. When SWP = 0, the data written by the microcomputer is directly transferred to the inside. When SWP = 1, the data written by the microcomputer is internally transferred by exchanging the upper and lower bytes.

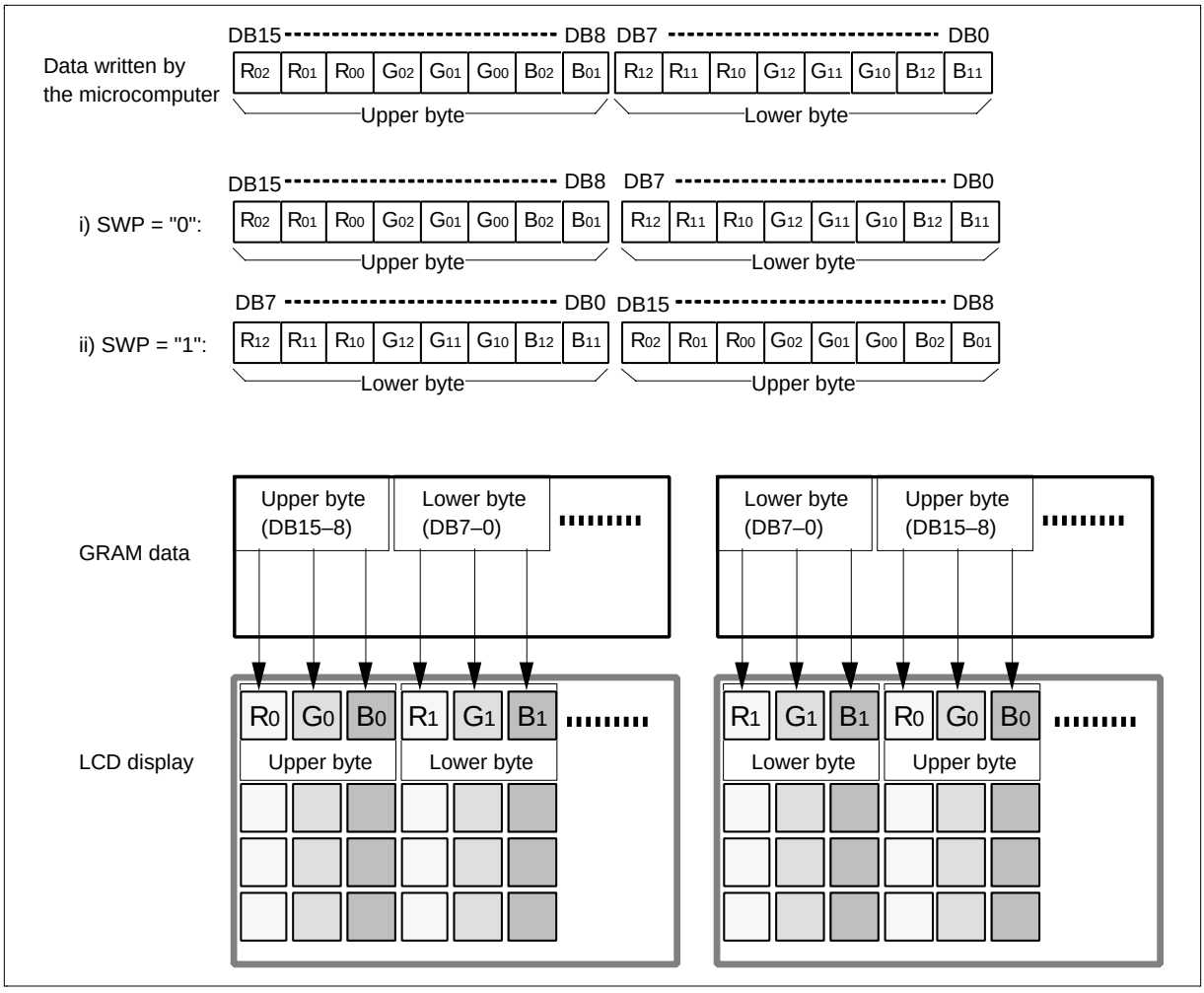


Figure 32 Example of Swap Function Operation

Write-data Mask Function

The HD66760 has a bit-wise write-data mask function that controls writing the two-byte data from the microcomputer to the GRAM. Bits that are 0 in the write-data mask register (WM15-0) cause the corresponding DB bit to be written to the GRAM. Bits that are 1 prevent writing to the corresponding GRAM bit to the GRAM; the data in the GRAM is retained. This function can be used when only one-pixel data is rewritten or the particular display color is selectively rewritten.

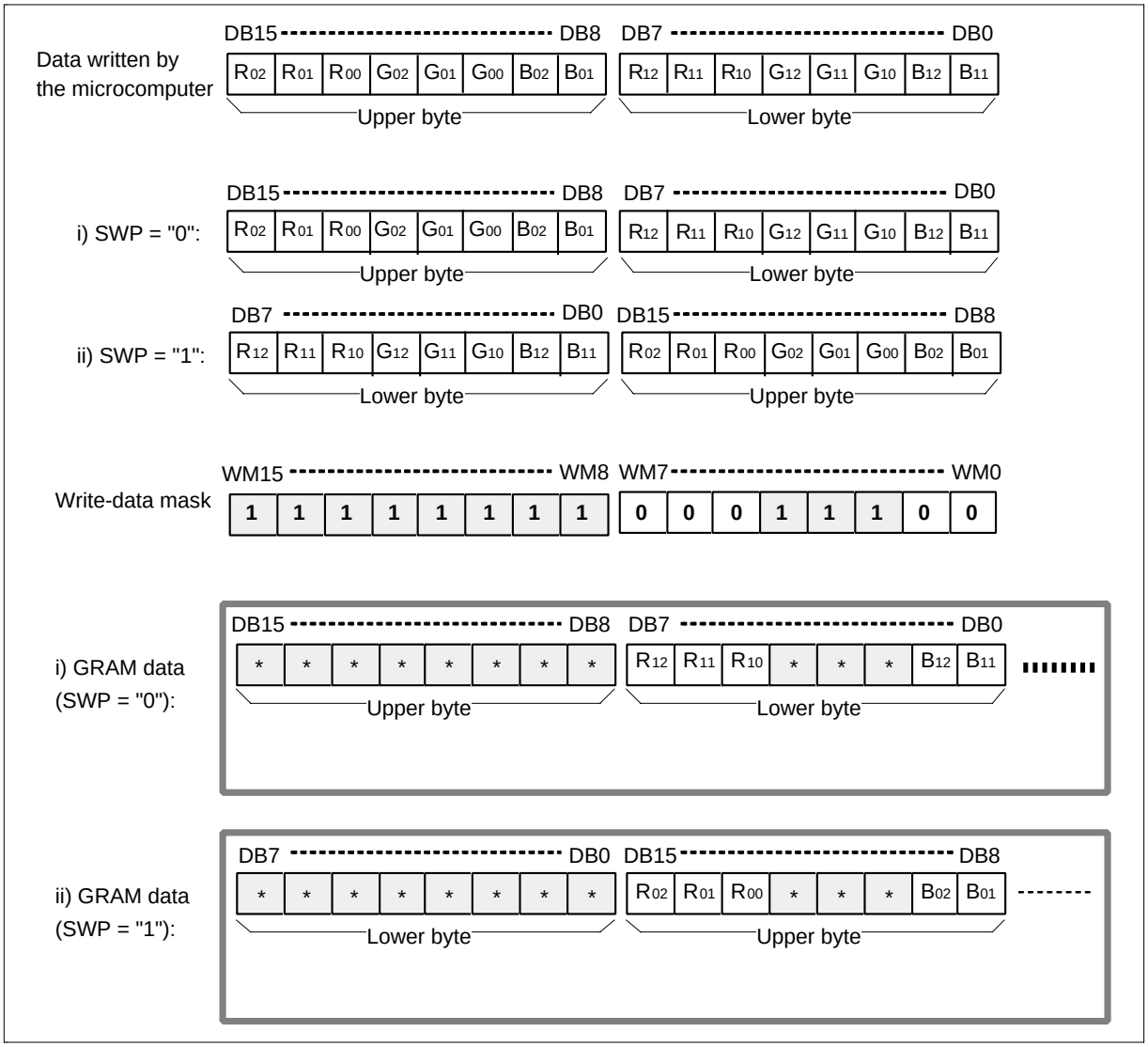


Figure 33 Example of Write-data Mask Function Operation

Logical/Compare Operation Function

The HD66760 performs a logical operation or conditional replacement between the two-byte write data sent from the microcomputer and the read data from the GRAM. The logical operation function has four types: replacement, OR, AND, and EOR. The conditional replacement performs a compare operation for the set value of the compare register (CP7-0) and the read data value from the GRAM, and rewrites only the pixel data in the GRAM that satisfies the conditions (in a byte unit). This function can be used when a particular color is selectively rewritten. The swap function or write-data mask function can be effectively used.

Table 32 Logical/Compare Operation

Bit Setting			
LG2	**LG1**	**LG0**	**Description of Logical/Compare Operation Function**
0	0	0	Writes the data written from the microcomputer directly to the GRAM. Only write processing is performed since the data in the read-data latch is not used.
0	0	1	ORs the data in the read-data latch and the data written by the microcomputer. Writes the result to GRAM. Read, modify, or write processing is performed.
0	1	0	ANDs the data in the read-data latch and the data written by the microcomputer. Writes the result to GRAM.
0	1	1	EORs the data in the read-data latch and the data written by the microcomputer. Writes the result to GRAM.
1	0	0	Compares the data in the read-data latch and the set value of the compare register (CP7–0). When the read data matches CP7–0, the data from the microcomputer is written to the GRAM. Only the particular color specified in the compare register can be rewritten. Read, modify, or write processing is performed.
1	0	1	Compares the data in the read-data latch and the set value of the compare register (CP7–0). When the read data does not match CP7-0, the data from the microcomputer is written to the GRAM. Colors other than the particular one specified in the compare register can be rewritten. Read, modify, or write processing is performed.
1	1	0	Compares the data written to the GRAM by the microcomputer and the set value of the compare register (CP7–0). When the write data matches CP7-0, the data from the microcomputer is written to the GRAM. Only write processing is performed.
1	1	1	Compares the data written to the GRAM by the microcomputer and the set value of the compare register (CP7–0). When the write data does not match CP7-0, the data from the microcomputer is written to the GRAM. Only write processing is performed.

Graphics Operation Processing

1. Write mode 1: AM = 0, LG2–0 = 000

   This mode is used when the data is horizontally written at high speed. It can also be used to initialize the graphics RAM (GRAM) or to draw borders. The swap function (SWP) and write-data mask function (WM15–0) are also enabled in these operations. After writing, the address counter (AC) automatically increments by 1 (I/D = 1) or decrements by 1 (I/D = 0), and automatically jumps to the counter edge one-raster-row below after it has reached the left or right edge of the GRAM.

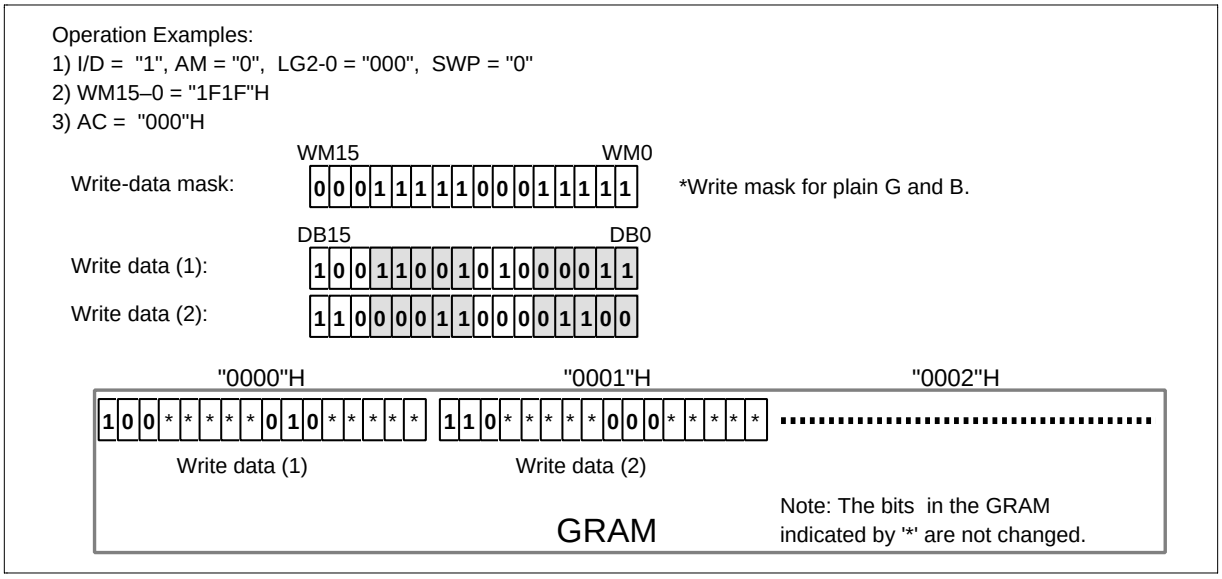


Figure 34 Writing Operation of Write Mode 1

2. Write mode 2: AM = 1, LG2–0 = 000

   This mode is used when the data is vertically written at high speed. It can also be used to initialize the GRAM, develop the font pattern in the vertical direction, or draw borders. The swap function (SWP) and write-data mask function (WM15–0) are also enabled in these operations. After writing, the address counter (AC) automatically increments by 256, and automatically jumps to the upper-right edge (I/D = 1) or upper-left edge (I/D = 0) following the I/D bit after it has reached the lower edge of the GRAM.

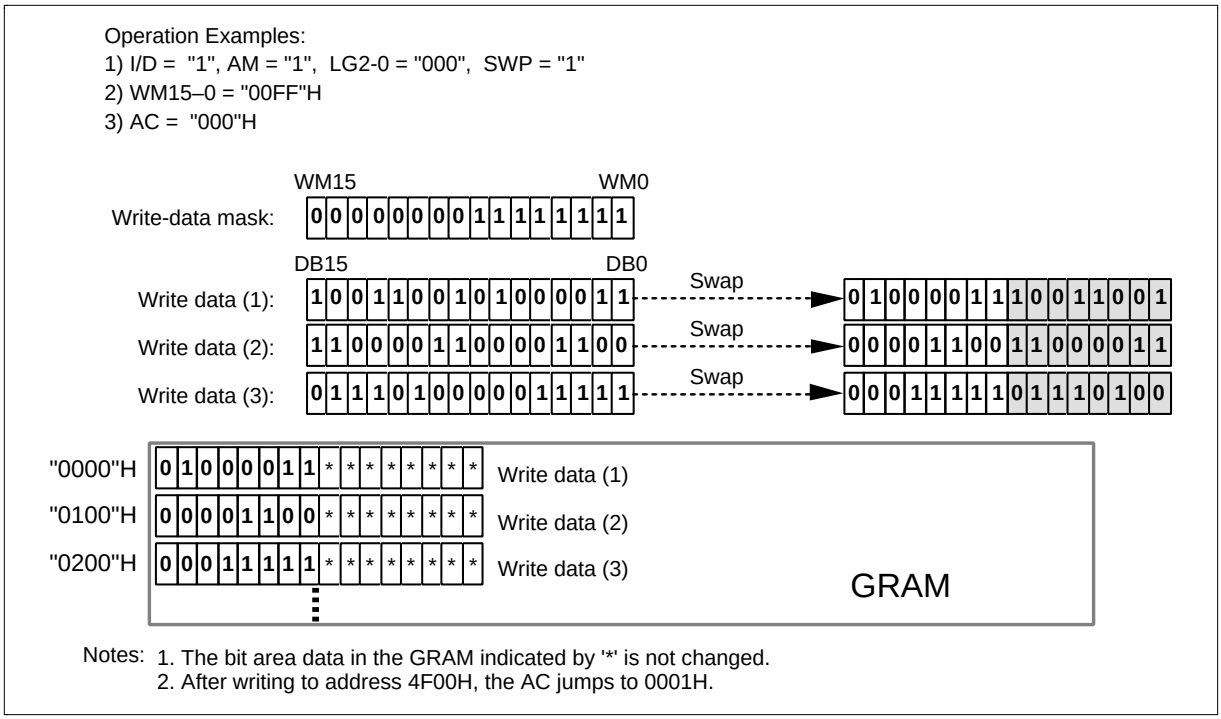


Figure 35 Writing Operation of Write Mode 2

3. Write mode 3: AM = 0, LG2–0 = 110/111

   This mode is used when the data is horizontally written by comparing the write data and the set value of the compare register (CP7–0). When the result of the comparison in a byte unit satisfies the condition, the write data sent from the microcomputer is written to the GRAM. In this operation, the swap function (SWP) and write-data mask function (WM15–0) are also enabled. After writing, the address counter (AC) automatically increments by 1 (I/D = 1) or decrements by 1 (I/D = 0), and automatically jumps to the counter edge one-raster-row below after it has reached the left or right edge of the GRAM.

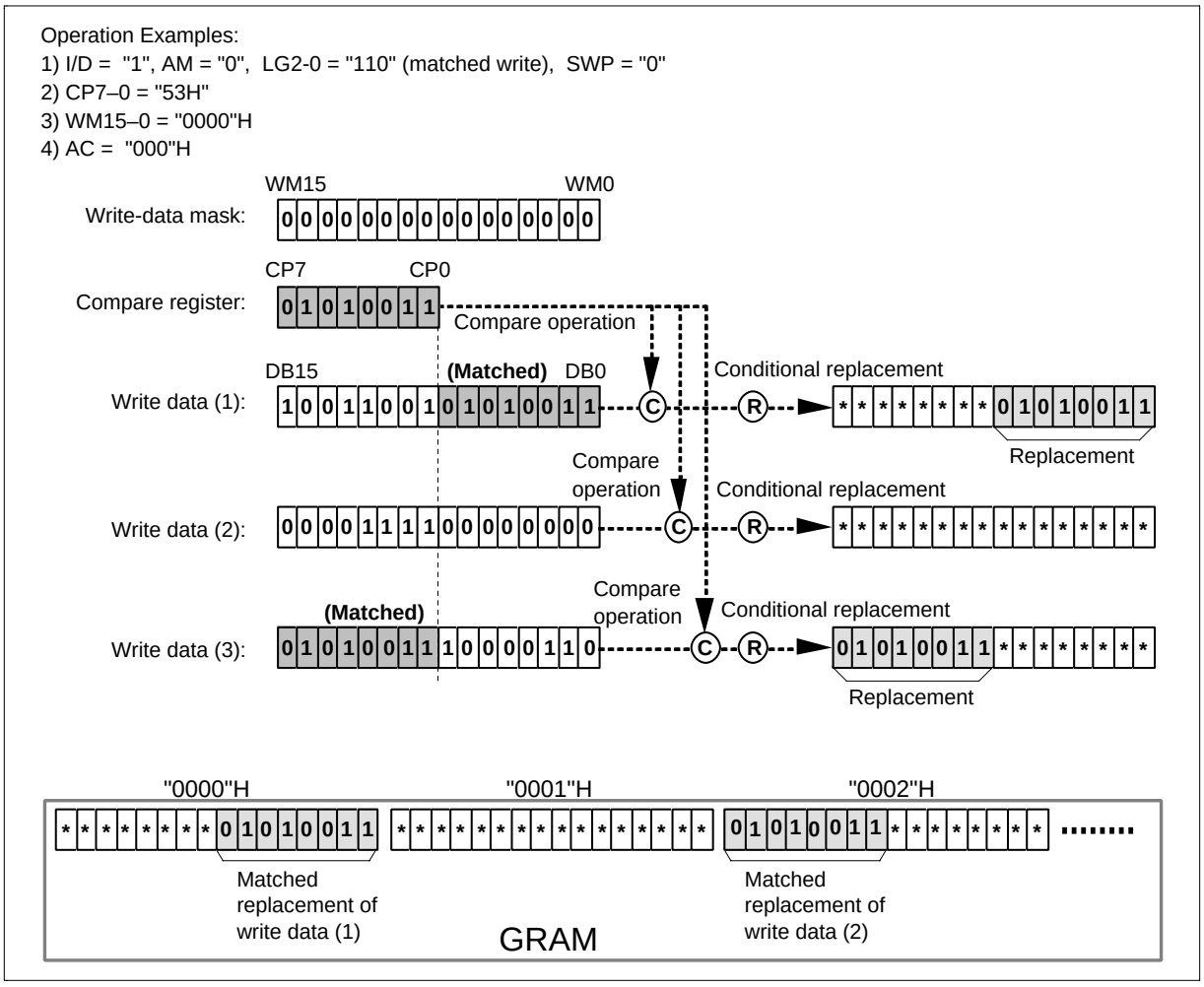


Figure 36 Writing Operation of Write Mode 3

4. Write mode 4: AM = 1, LG2–0 = 110/111

   This mode is used when a vertical comparison is performed between the write data and the set value of the compare register (CP7–0) to write the data. When the result by the comparison in a byte unit satisfies the condition, the write data sent from the microcomputer is written to the GRAM. In this operation, the swap function (SWP) and write-data mask function (WM15–0) are also enabled. After writing, the address counter (AC) automatically increments by 256, and automatically jumps to the upper-right edge (I/D = 1) or upper-left edge (I/D = 0) following the I/D bit after it has reached the lower edge of the GRAM.

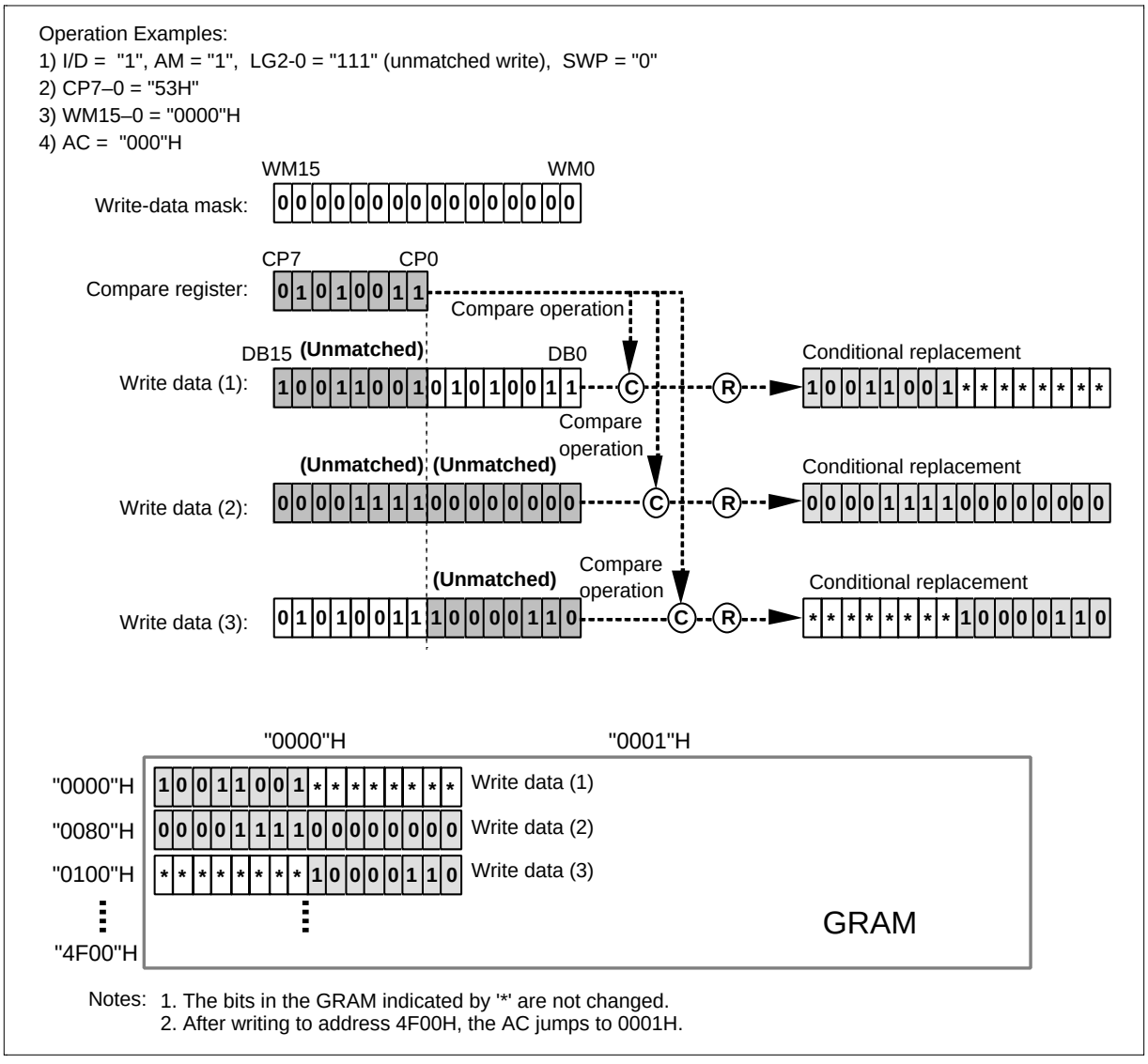


Figure 37 Writing Operation of Write Mode 4

5. Read/Write mode 1: AM = 0, LG2–0 = 001/010/011

   This mode is used when the data is horizontally written at high speed by performing a logical operation with the original data. It reads the display data (original data), which has already been written in the GRAM, performs a logical operation with the write data sent from the microcomputer, and rewrites the data to the GRAM. This mode reads the data during the same access-pulse width (68-system: enabled high level, 80-system: RD* low level) as the write operation since reading the original data does not latch the read data into the microcomputer but temporarily holds it in the read-data latch. However, the bus cycle requires the same time as the read operation. The swap function (SWP) or write-data mask function (WM15–0) are also enabled in these operations. After writing, the address counter (AC) automatically increments by 1 (I/D = 1) or decrements by 1 (I/D = 0), and automatically jumps to the counter edge one-raster-row below after it has reached the left or right edges of the GRAM.

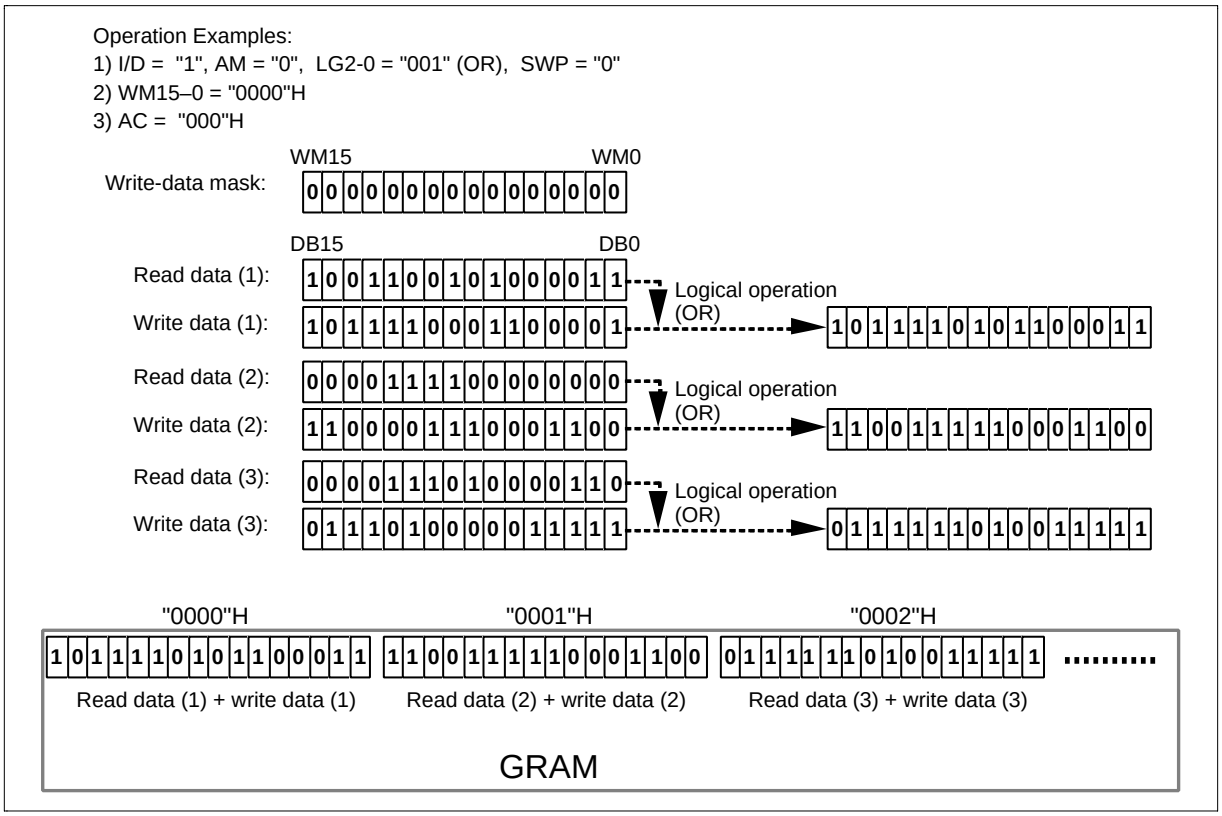


Figure 38 Writing Operation of Read/Write Mode 1

6. Read/Write mode 2: AM = 1, LG1–0 = 001/010/011

This mode is used when the data is vertically written at high speed by performing a logical operation with the original data. It reads the display data (original data), which has already been written in the GRAM, performs a logical operation with the write data sent from the microcomputer, and rewrites the data to the GRAM. This mode can read the data during the same access-pulse width (68-system: enabled high level, 80-system: RD* low level) as for the write operation since the read operation of the original data does not latch the read data into the microcomputer and temporarily holds it in the read-data latch. However, the bus cycle requires the same time as the read operation. The swap function (SWP) or write-data mask function (WM15–0) are also enabled in these operations. After writing, the address counter (AC) automatically increments by 256, and automatically jumps to the upper-right edge (I/D = 1) or upper-left edge (I/D = 0) following the I/D bit after it has reached the lower edge of the GRAM.

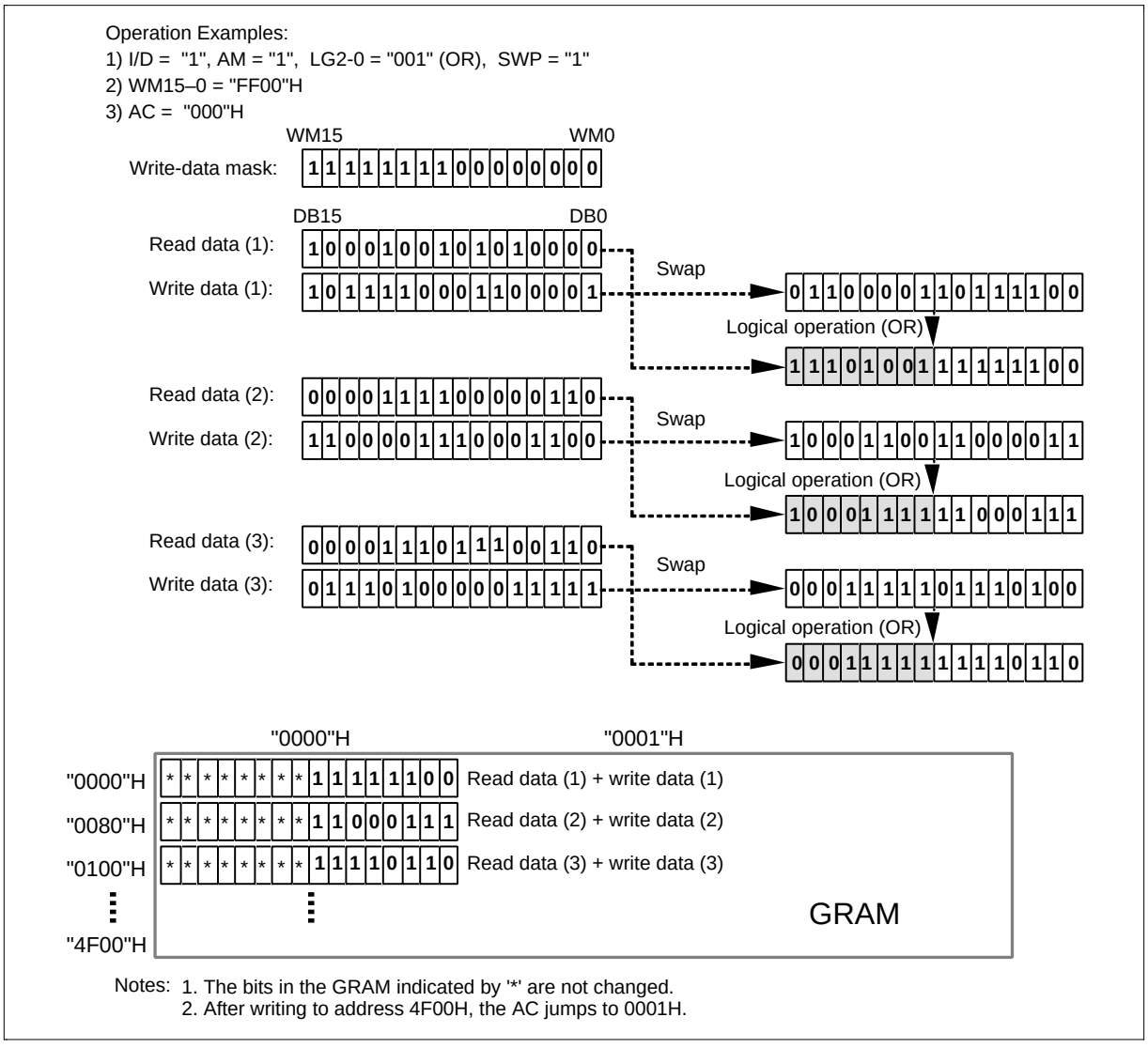


Figure 39 Writing Operation of Read/Write Mode 2

7. Read/Write mode 3: AM = 0, LG2–0 = 100/101

   This mode is used when the data is horizontally written by comparing the original data and the set value of compare register (CP7–0). It reads the display data (original data), which has already been written in the GRAM, compares the original data and the set value of the compare register in byte units, and writes the data sent from the microcomputer to the GRAM only when the result of the comparison satisfies the condition. This mode reads the data during the same access-pulse width (68-system: enabled high level, 80-system: RD* low level) as write operation since reading the original data does not latch the read data into the microcomputer but temporarily holds it in the read-data latch. However, the bus cycle requires the same time as the read operation. The swap function (SWP) and write-data mask function (WM15–0) are also enabled in these operations. After writing, the address counter (AC) automatically increments by 1 (I/D = 1) or decrements by 1 (I/D = 0), and automatically jumps to the counter edge one-raster-row below after it has reached the left or right edges of the GRAM.

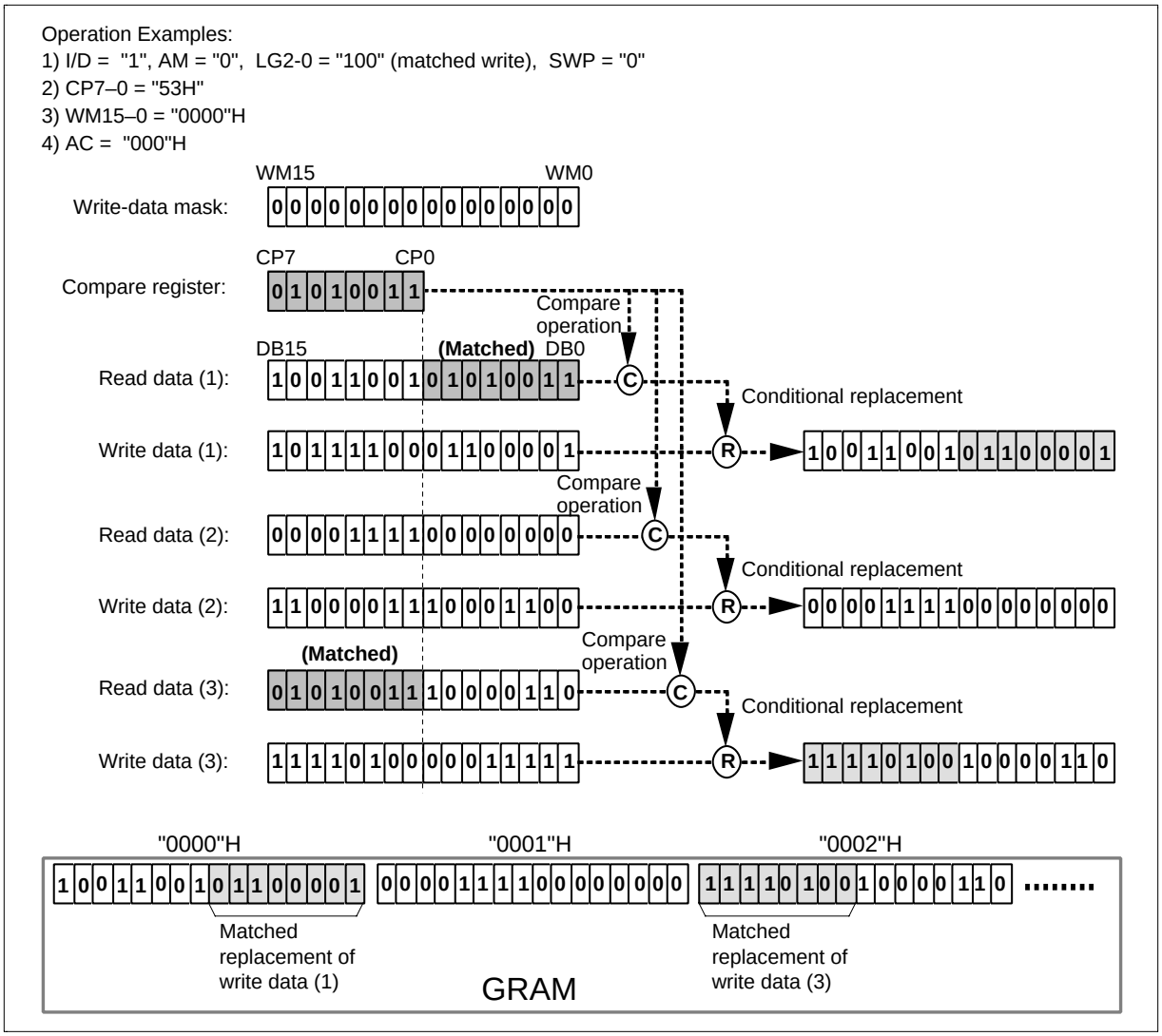


Figure 40 Writing Operation of Read/Write Mode 3

8. Read/Write mode 4: AM = 1, LG2–0 = 100/101

This mode is used when the data is vertically written by comparing the original data and the set value of the compare register (CP7–0). It reads the display data (original data), which has already been written in the GRAM, compares the original data and the set value of the compare register in byte units, and writes the data sent from the microcomputer to the GRAM only when the result of the compare operation satisfies the condition. This mode reads the data during the same access-pulse width (68-system: enabled high level, 80-system: RD* low level) as the write operation since reading the original data does not latch the read data into the microcomputer but temporarily holds it in the read-data latch. However, the bus cycle requires the same time as the read operation. The swap function (SWP) and write-data mask function (WM15–0) are also enabled in these operations. After writing, the address counter (AC) automatically increments by 256, and automatically jumps to the upper-right edge (I/D = 1) or upper-left edge (I/D = 0) following the I/D bit after it has reached the lower edge of the GRAM.

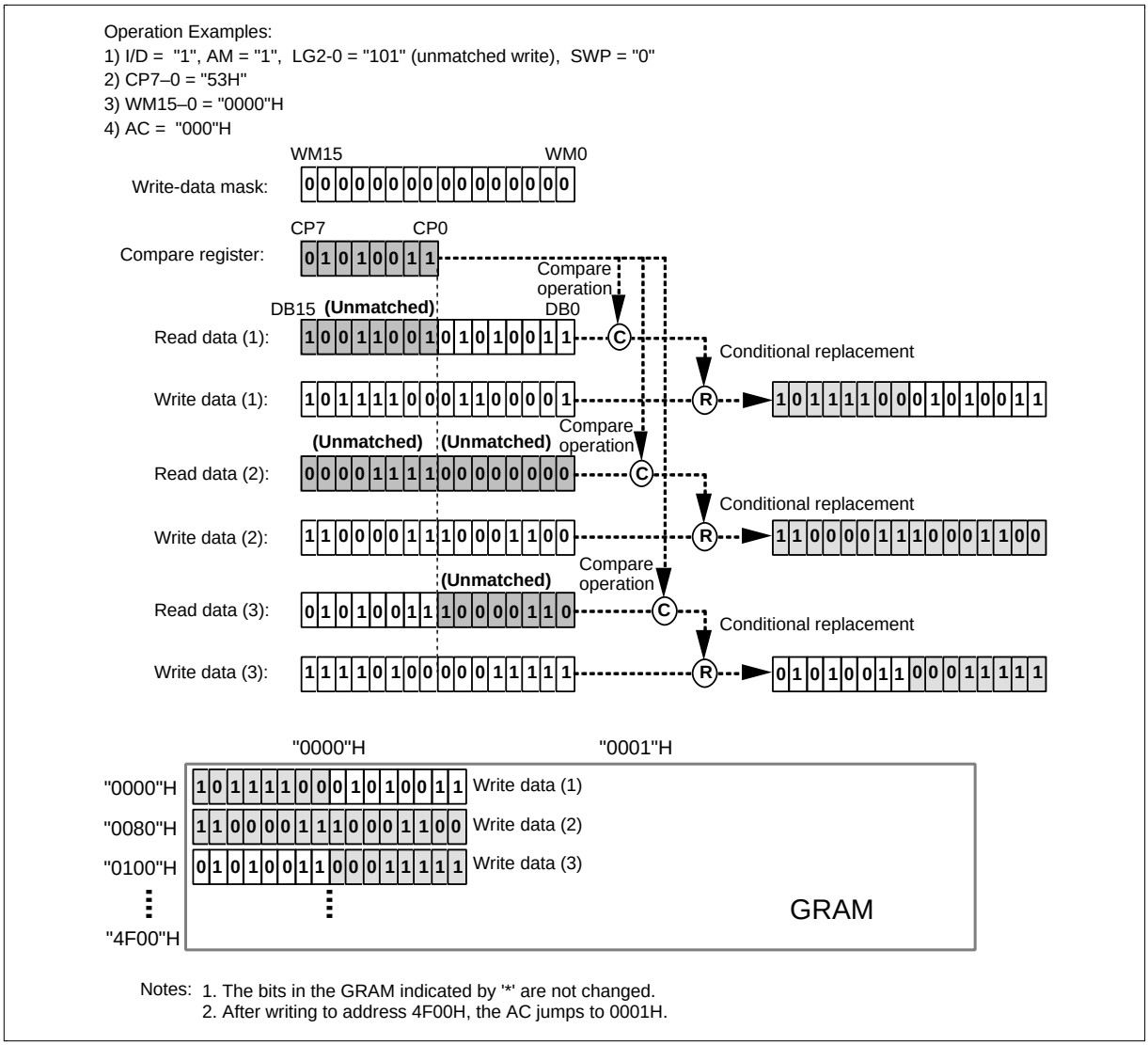


Figure 41 Writing Operation of Read/Write Mode 4

Grayscale Palette

The HD66760 incorporates a grayscale palette to simultaneously display 256 of the 4,096 possible colors. The R and G grayscales consist of eight four-bit palettes, and the B grayscale consists of four four-bit palettes. The 16-stage grayscale levels can be selected from the four-bit palette data.

For the display data of R and G, the three-bit data in the GRAM written from the microcomputer is used. For the display data of B, the two-bit data in the GRAM is used.

In this palette, a curtailed frame grayscale system, which has low charging current in the LCD panel, is used. Although the system is the same for each color, the curtailed frame timing is adjusted between adjacent dots to reduce flickering.

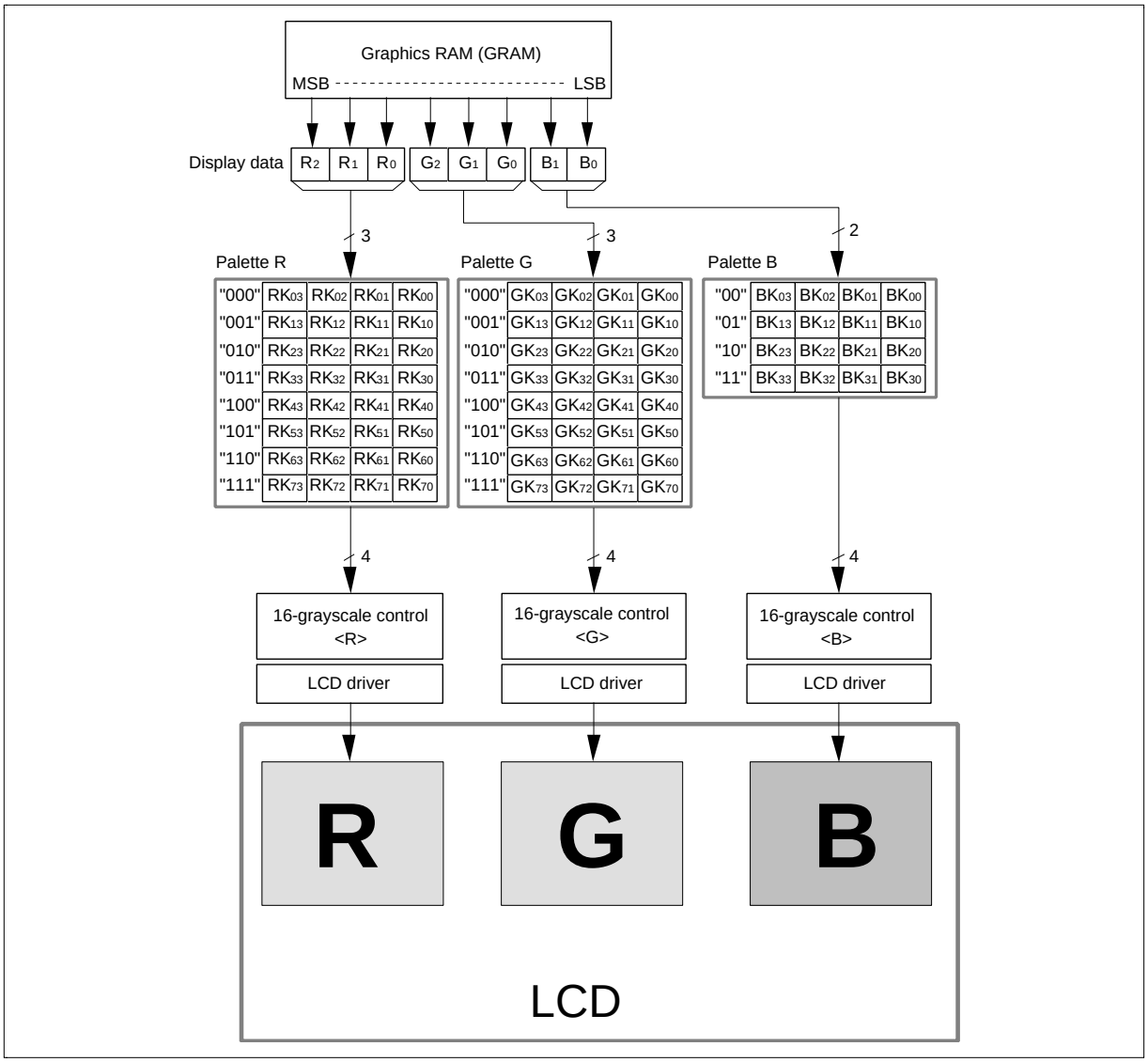


Figure 42 Grayscale Palette Control

Grayscale Palette Table

The grayscale register that is set for each palette register (RK, GK, or BK) can be set to any level. 16-grayscale lighting levels can be set according to palette values (0000 to 1111).

Table 33 Grayscale Control Level

Palette Register Value (RK, GK, or BK)				Grayscale Control Level
0	0	0	0	Unlit level*[1]
0	0	0	1	2/16 level
0	0	1	0	3/16 level
0	0	1	1	4/16 level
0	1	0	0	5/16 level
0	1	0	1	6/16 level
0	1	1	0	7/16 level
0	1	1	1	8/16 level
1	0	0	0	9/16 level
1	0	0	1	10/16 level
1	0	1	0	11/16 level
1	0	1	1	12/16 level
1	1	0	0	13/16 level
1	1	0	1	14/16 level
1	1	1	0	15/16 level
1	1	1	1	All-lit level*[2]

Notes: 1. The unlit level corresponds to a black display when a normally-black color-LCD panel is used, and a white display when a normally-white color-LCD panel is used.

2. The all-lit level corresponds to a white display when a normally-black color-LCD panel is used, and a black display when a normally-white color-LCD panel is used.

Four-color Display Mode

The HD66760 has the four-color display mode consisting of two-bit-per-pixel data. Since the byte-wise processing of four-pixel display data is enabled, the processing performance is four times that of the normal 256-color display. When the internal grayscale palette is used, four colors of the possible 4,096 colors can be displayed at the same time. The two-bit display data in the GRAM written from the microcomputer is assigned to the lower two bits of R and G; one of these bits, always 0, synthesizes the three-bit data. Therefore, this display mode uses 000, 001, 010, 011 in grayscale palettes R and G.

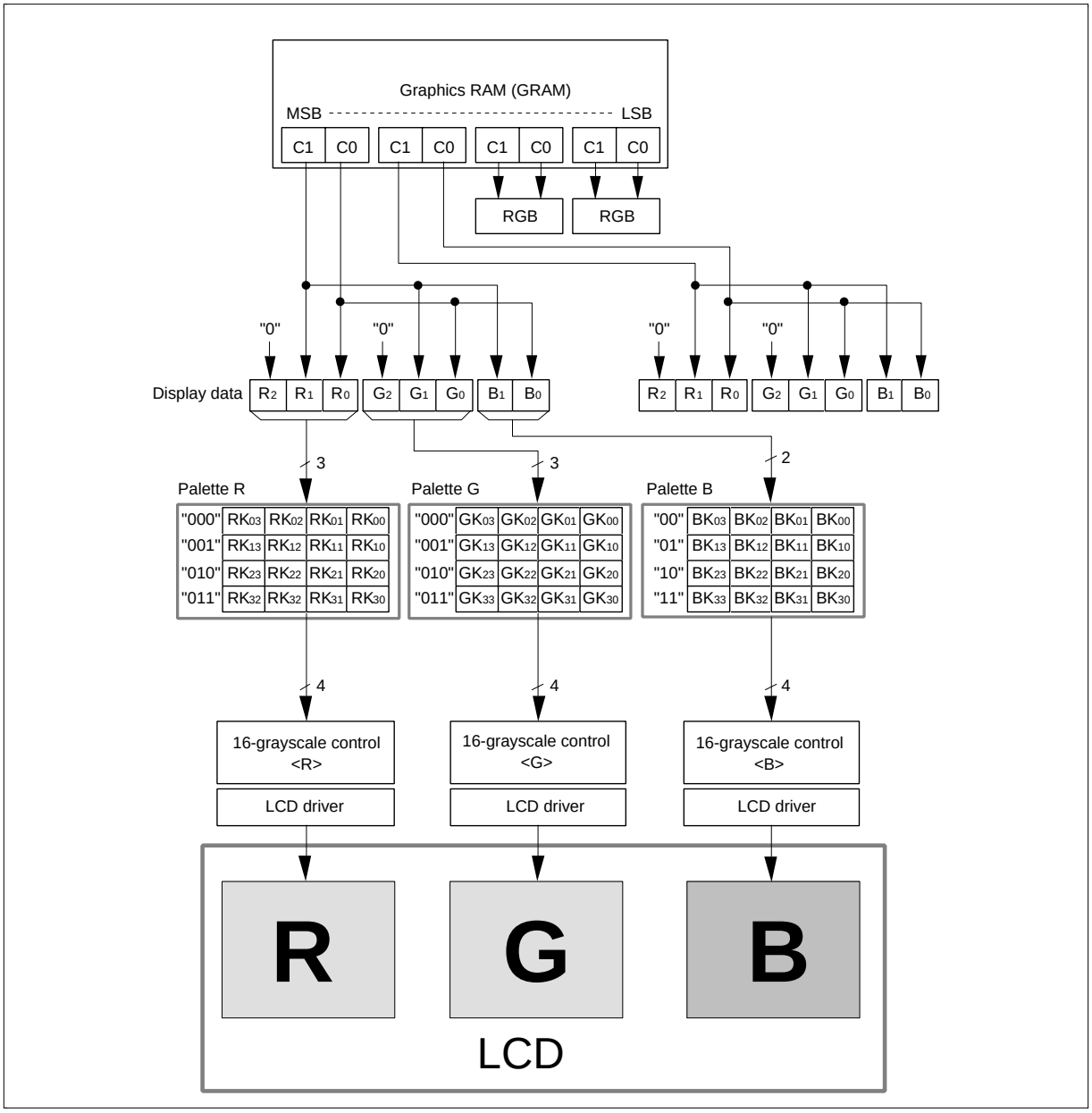


Figure 43 Four-color Display Control

Color Window Cursor Control

A cursor is displayed in the window area specified by the cursor-start position register (CSX or CSY) and cursor-end position register (CEX or CEY). The cursor display mode can be selected from four types in table 34 by changing cursor-mode bit (CM1–0).

The eight-color cursor display can be selected by the cursor-color bit (CR, CG, or CB) and displays red, blue, green, white, black or a combined color. However, the grayscale of the cursor color cannot be controlled.

Table 34 Cursor Display Control

Register Setting			
C	**CM1**	**CM0**	**Cursor Display Control**
0	*	*	Displays no cursor.
1	0	0	Displays eight colors specified by the cursor-color bit (CR, CG, or CB) in the window area.
1	0	1	Reverses and displays the four-bit grayscale data of each color in the window area.
1	1	0	Alternately repeats the normal display in the window area and the eight-color display specified by the cursor-color bit (CR, CG, or CB) every 32 frame for blinking display.
1	1	1	Alternately repeats the normal display in the window area and the reversal display of the four-bit grayscale data every 32 frame for blinking display.

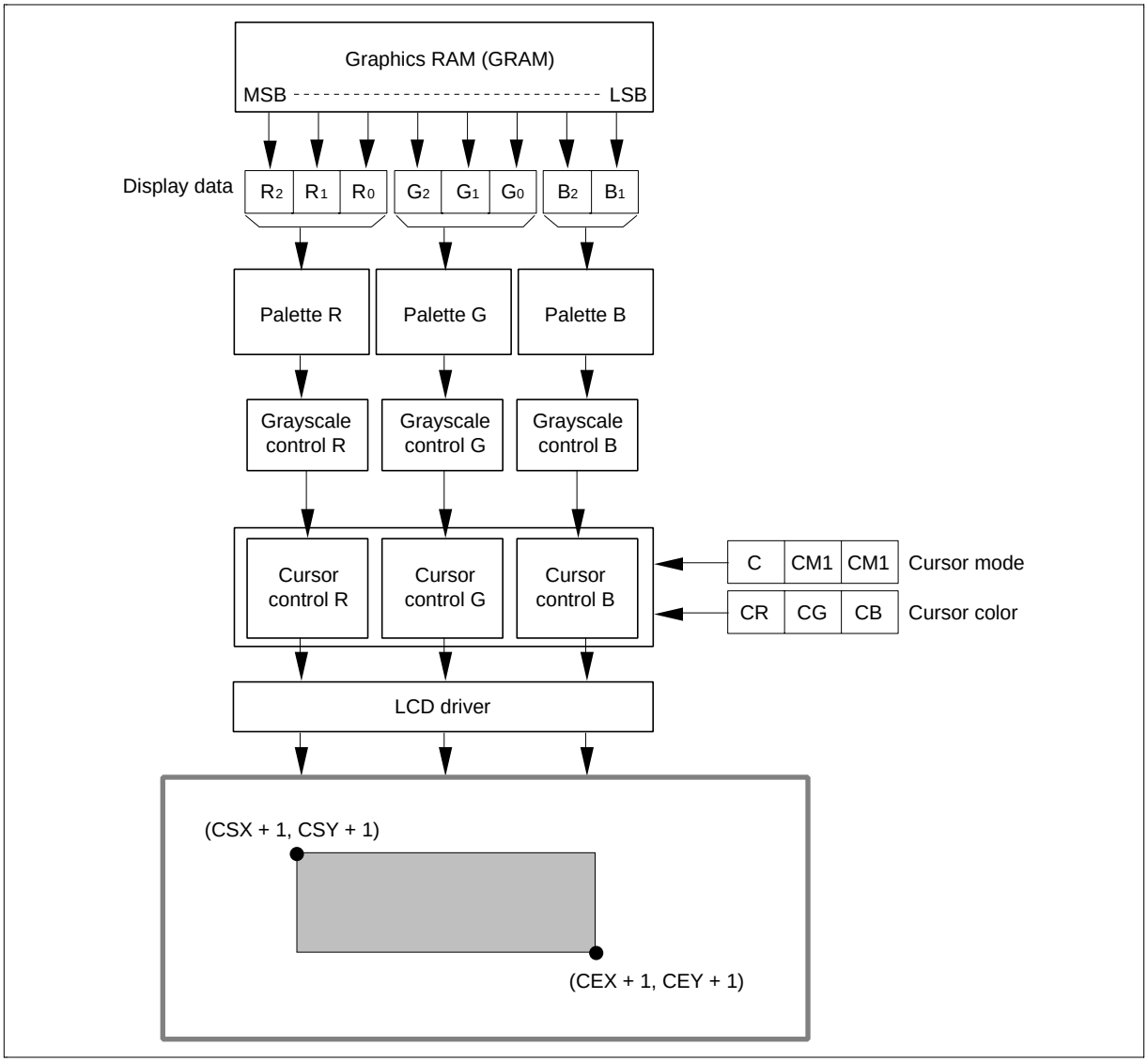


Figure 44 Color-cursor Display

Oscillation Circuit

The HD66760 can oscillate between the OSC1 and OSC2 pins using an internal R-C oscillator with an external oscillation resistor. Note that in R-C oscillation, the oscillation frequency is changed according to the external resistance value, wiring length, or operating power-supply voltage. If Rf is increased or power supply voltage is decrease, the oscillation frequency decreases. For the relationship between Rf resistor value and oscillation frequency, see the Electric Characteristics Notes section.

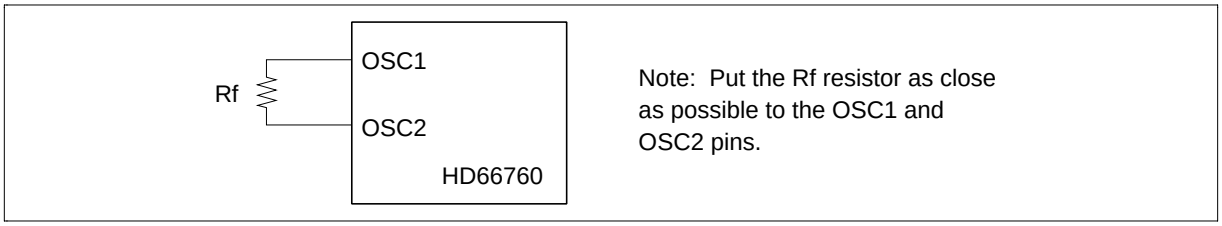


Figure 45 Oscillation Circuits

Table 35 Relationship between Liquid Crystal Drive Duty Ratio and Frame Frequency

LCD Duty	NL4–0 Set Value	Recommended Drive Bias Value	Frame Frequency	One-frame Clock
1/16	01H	1/5	70 Hz	2560
1/24	02H	1/6	70 Hz	2560
1/32	03H	1/6	70 Hz	2568
1/40	04H	1/7	70 Hz	2560
1/48	05H	1/8	71 Hz	2544
1/56	06H	1/8	70 Hz	2576
1/64	07H	1/9	70 Hz	2560
1/72	08H	1/9.5	71 Hz	2520
1/80	09H	1/10	70 Hz	2560

Note: The frame frequency above is for 180-kHz operation and proportions the oscillation frequency (fosc).

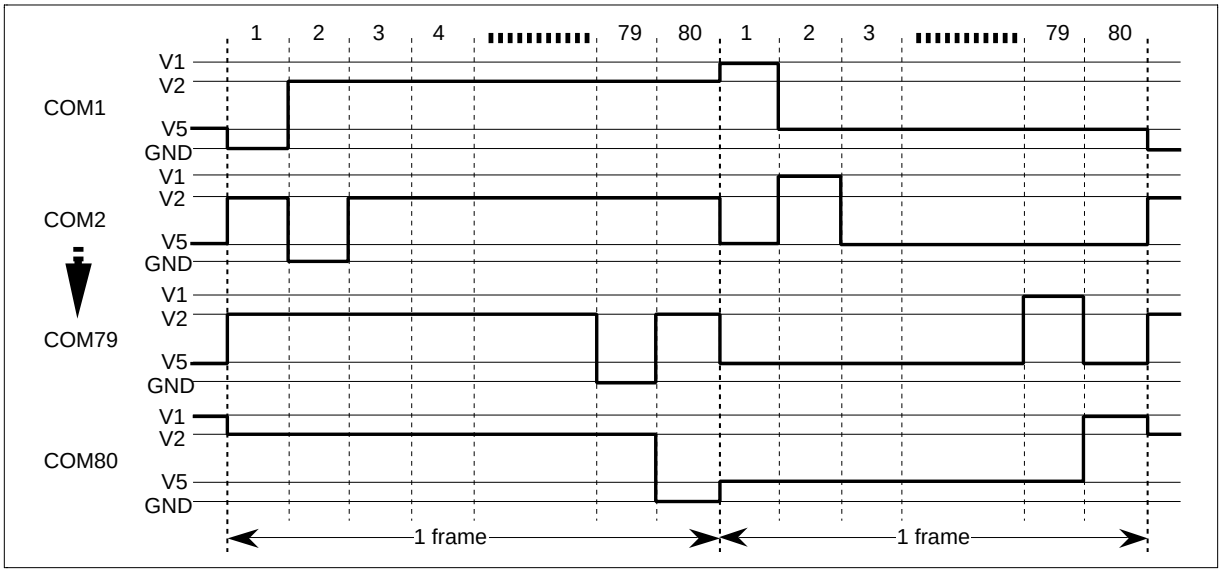


Figure 46 LCD Drive Output Waveform (B-pattern AC Drive with 1/80 Multiplexing Duty Ratio)

n-raster-row Reversed AC Drive

The HD66760 supports not only the LCD reversed AC drive in a one-frame unit (B-pattern waveform) but also the n-raster-row reversed AC drive which alternates in an n-raster-row unit from one to 32 raster-rows (C-pattern waveform). When a problem affecting display quality occurs, such as crosstalk at high-duty driving of more than 1/64 duty, the n-raster-row reversed AC drive (C-pattern waveform) can improve the quality.

Determine the number of raster-rows n (NW bit set value + 1) for alternating after confirmation of the display quality with the actual LCD panel. However, if the number of AC raster-rows is reduced, the LCD alternating frequency becomes high. Because of this, the charge or discharge current is increased in the LCD cells.

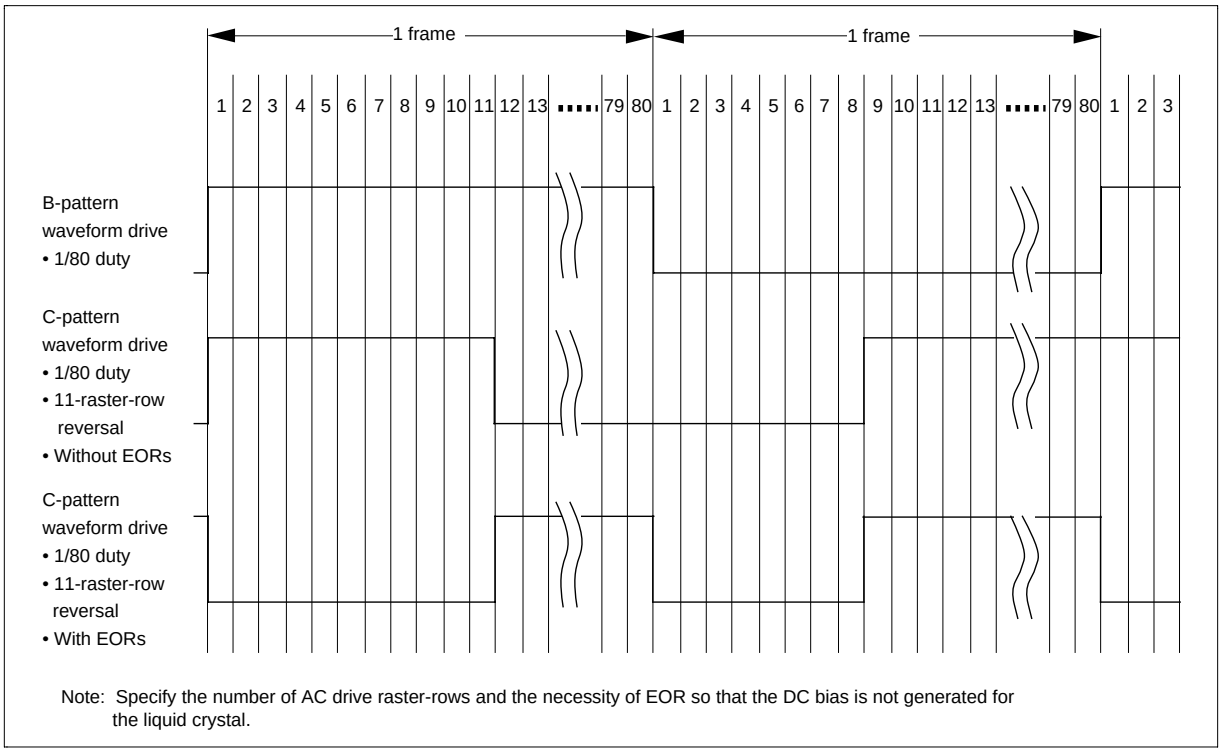


Figure 47 Example of an AC Signal under n-raster-row Reversed AC Drive

Liquid-crystal-display Drive-bias Selector

An optimum liquid-crystal-display bias value can be selected using the BS2-0 bits, according to the liquid crystal drive duty ratio setting (NL3–0 bits). The liquid-crystal-display drive duty ratio and bias value can be displayed while switching software applications to match the LCD panel display status. The optimum bias value calculated using the following expression is a logical optimum value. Driving by using a lower value than the optimum bias value provides lower logical contrast and lower liquid-crystal-display voltage (the potential difference between V1 and GND), which results in better image quality. When the liquid-crystal-display voltage is insufficient even if a six-times step-up circuit is used, when the step-up driving ability is lowered by setting a high factor for the step-up circuit, or when the output voltage is lowered because the battery life has been reached, the display can be made easier to see by lowering the liquid-crystal-display bias.

The liquid crystal display can be adjusted by using the contrast adjustment register (CT6–0 bits) and selecting the step-up output level (BT1/0 bits).

$$\text{Optimum bias value for 1/N duty ratio drive voltage} = \frac{1}{\sqrt{N} + 1}$$

Table 36 Optimum Drive Bias Values

LCD drive duty ratio	1/80	1/72	1/64	1/56	1/48	1/40	1/32	1/24	1/16
(NL3-0 set value)	1001	1000	0111	0110	0101	0100	0011	0010	0001
Optimum drive bias value	1/10	1/9	1/9	1/8	1/8	1/7	1/6	1/6	1/5
(BS2-0 set value)	001	010	010	011	011	100	101	101	110

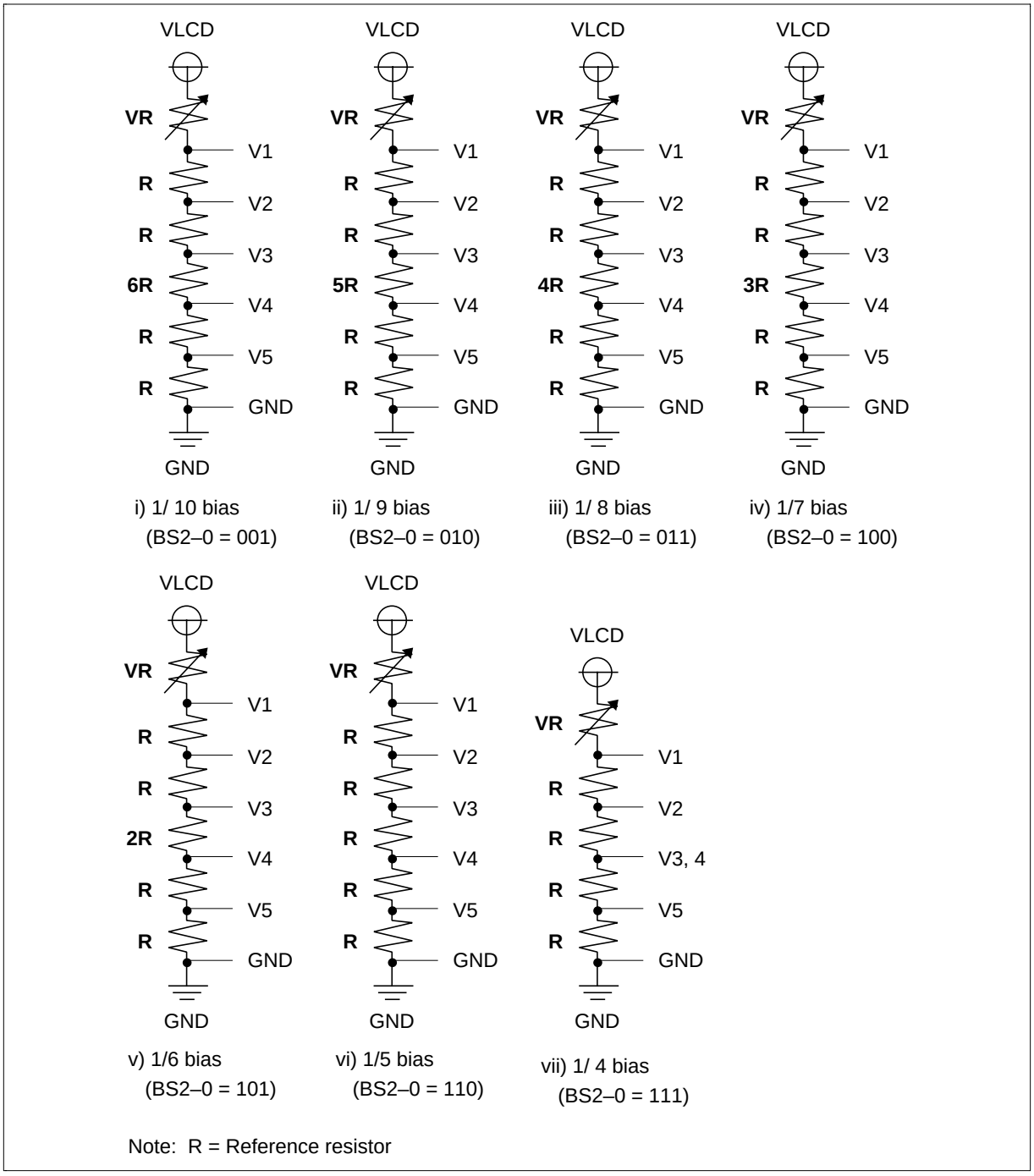


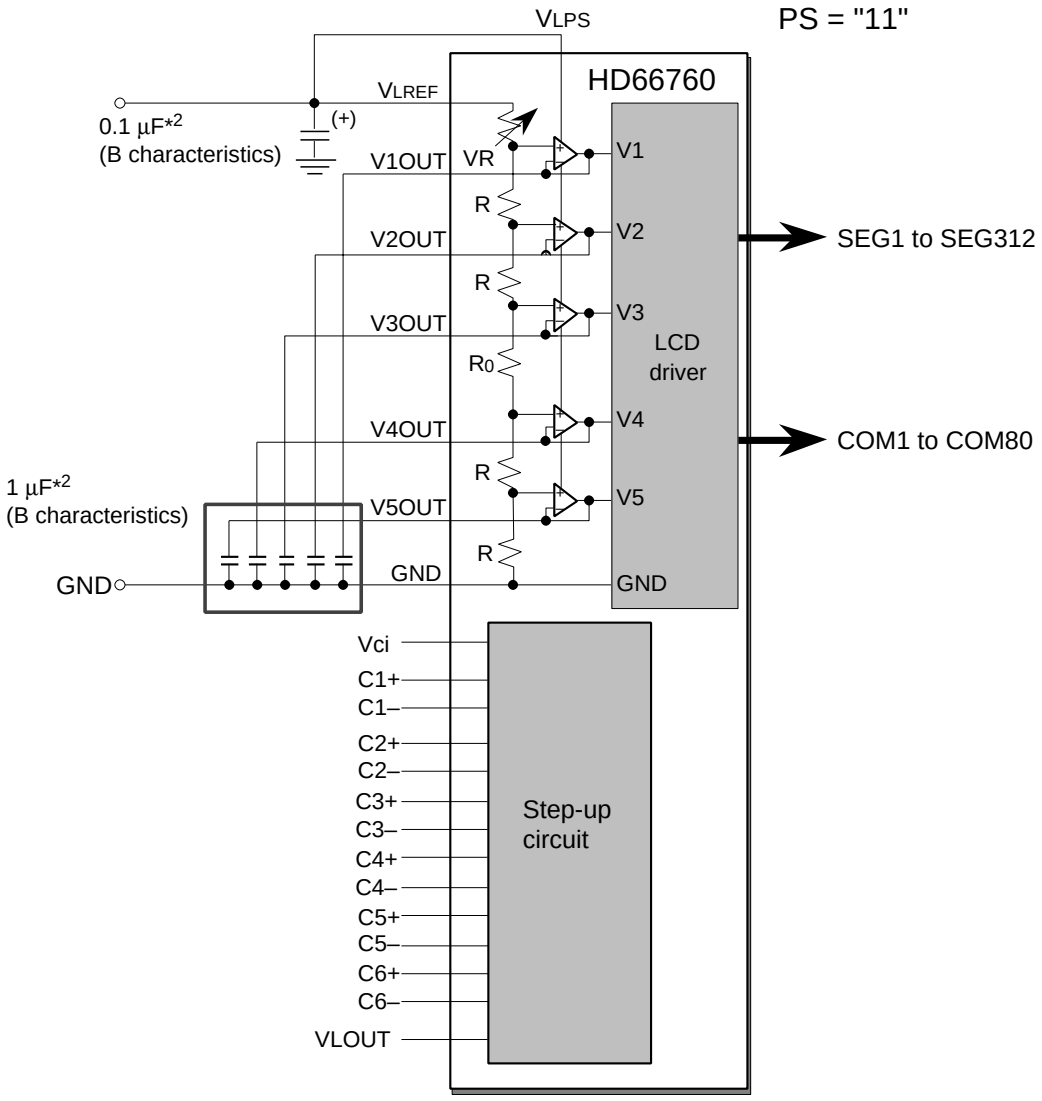
Figure 48 Liquid Crystal Display Drive Bias Circuit

Liquid Crystal Display Voltage Generator

When External Power Supply and Internal Operational Amplifiers are Used

To supply LCD drive voltage directly from the external power supply without using the internal step-up circuit, circuits should be connected as shown in figure 49. Here, contrast can be adjusted by software through the CT bits of the contrast adjustment register. Minimize the voltage variation since the VLREF input is a reference voltage that determines the LCD drive voltage.

The HD66760 incorporates a voltage-follower operational amplifier for each V1 to V5 to reduce current flowing through the internal bleeder-resistors, which generate different levels of liquid-crystal drive voltages. Thus, potential difference between V_{LPS} and V1 must be 0.1 V or higher, and that between V4 and GND must be 1.4 V or higher. Note that the OPOFF pin must be grounded when using the operational amplifiers. Place a capacitor of about 1 µF (B characteristics) between each internal operational amplifier (V1OUT to V5OUT outputs) and GND and stabilize the output level of the operational amplifier. Adjust the capacitance value of the stabilized capacitor after the LCD panel has been mounted and the screen quality has been confirmed.



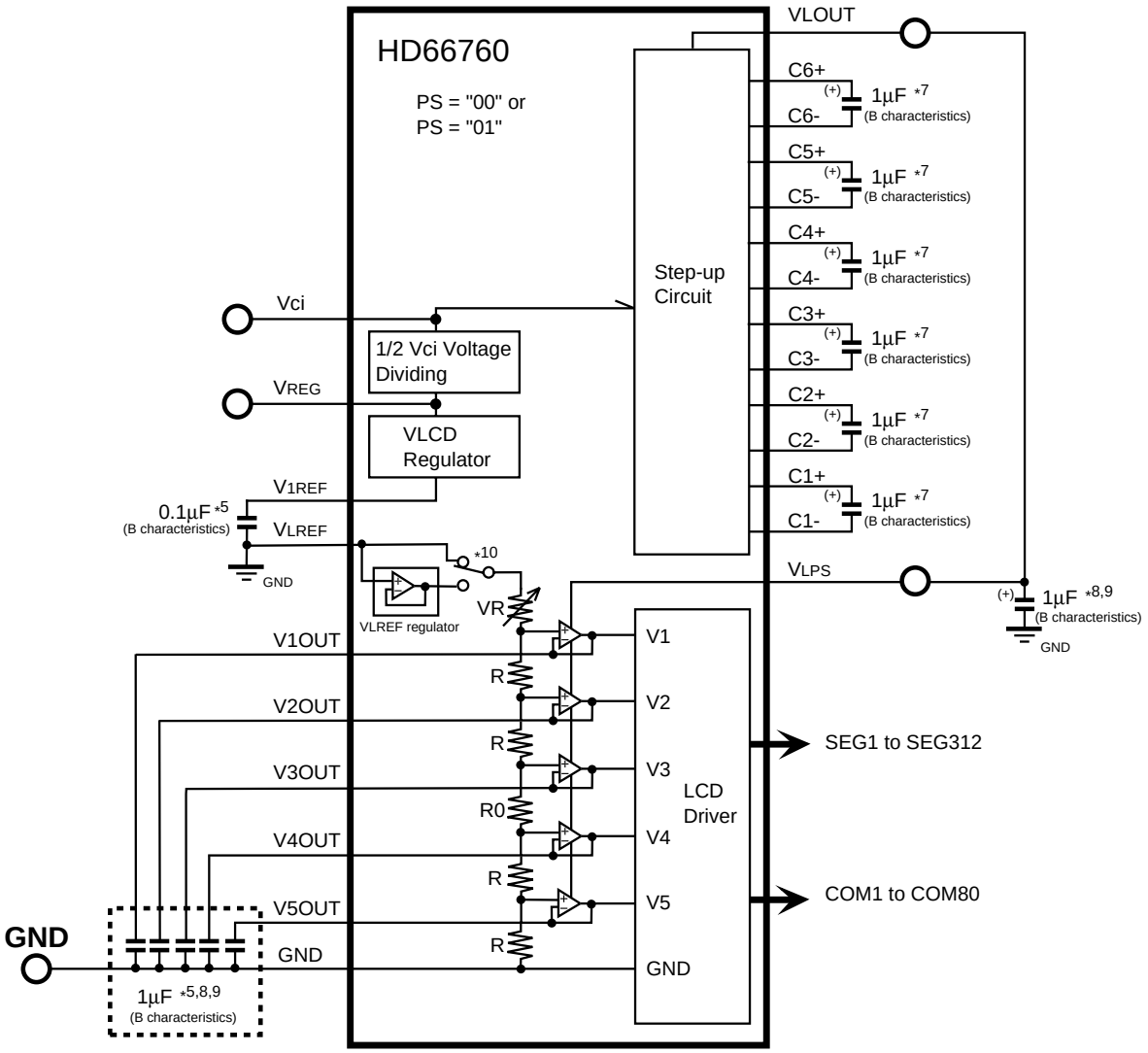
Notes: 1. Adjust the capacitance value of the capacitor after the LCD panel has been mounted.
2. Use the capacitors with breakdown voltages equal to or higher than the VLCD (= VLPS–GND) voltage for connecting to VLPS and V1OUT through V5OUT. Determine the capacitor breakdown voltages by checking VLCD voltage fluctuation.

Figure 49 External Power Supply Circuit for LCD Drive Voltage Generation

When an Internal Booster and Internal Operational Amplifiers are Used

To supply LCD drive voltage using the internal VLCD regulator and step-up circuit, an internal booster and internal operational amplifiers should be connected as shown in figure 50. Keep the power-supply voltage (VLPS) of the operational amplifier higher than the output voltage (V1REF) of the VLCD regulator. Contrast can be adjusted through the CT bits of the contrast control instruction.

The HD66760 incorporates a voltage-follower operational amplifier for each of V1 to V5 to reduce current flowing through the internal bleeder-resistors, which generate different liquid-crystal drive voltages. Thus, potential difference between V_{LPS} and V1 must be 0.1 V or higher, and that between V4 and GND must be 1.4 V or higher. Note that the OPOFF pin must be grounded when using the operational amplifiers. Place a capacitor of about 1 µF (B characteristics) between each internal operational amplifier (V1OUT to V5OUT outputs) and GND and stabilize the output level of the operational amplifier. Adjust the capacitance value of the stabilized capacitor after the LCD panel has been mounted and the screen quality has been confirmed.



Notes:
1. The reference voltage input (Vci) must be adjusted so that the output voltage after boosting will not exceed the absolute maximum rating for the liquid-crystal power supply voltage (16.5 V).
2. Vci is both a reference voltage and power supply for the step-up circuit; the sufficient current must be obtained.
3. Polarized capacitors must be connected correctly.
4. Circuits for temperature compensation should be based on the sample circuits in figures 51 and 52.
5. Adjust the capacitance value of the stabilized capacitor after the LCD panel has been mounted.
6. The breakdown voltages of the capacitors connected to C3+/C3- and C6+/C6- should be three times or higher than the Vci voltage.
7. The breakdown voltages of the capacitors connected to C1+/C1-, C2+/C2-, C4+/C4-, and C5+/C5- should be equal to or higher than the Vci voltage.
8. The breakdown voltages of the capacitors connected to VLOUT and V1OUT through V5OUT should be n times or higher than the Vci voltage (n: step-up magnification).
9. Determine the breakdown voltages of the capacitors used in 6 to 8 above by checking Vci voltage fluctuation.
10. VLREF regulator is not used when PS = "00". VLREF regulator is used when PS = "01".

Figure 50 Internal Step-up Circuit for LCD Drive Voltage Generation

Temperature can be compensated either through the CT bits, by controlling the reference input voltage for the VLCD regulator (VREG pin) using a thermistor, or by controlling the reference output voltage of the VLCD regulator (V1REF pin).

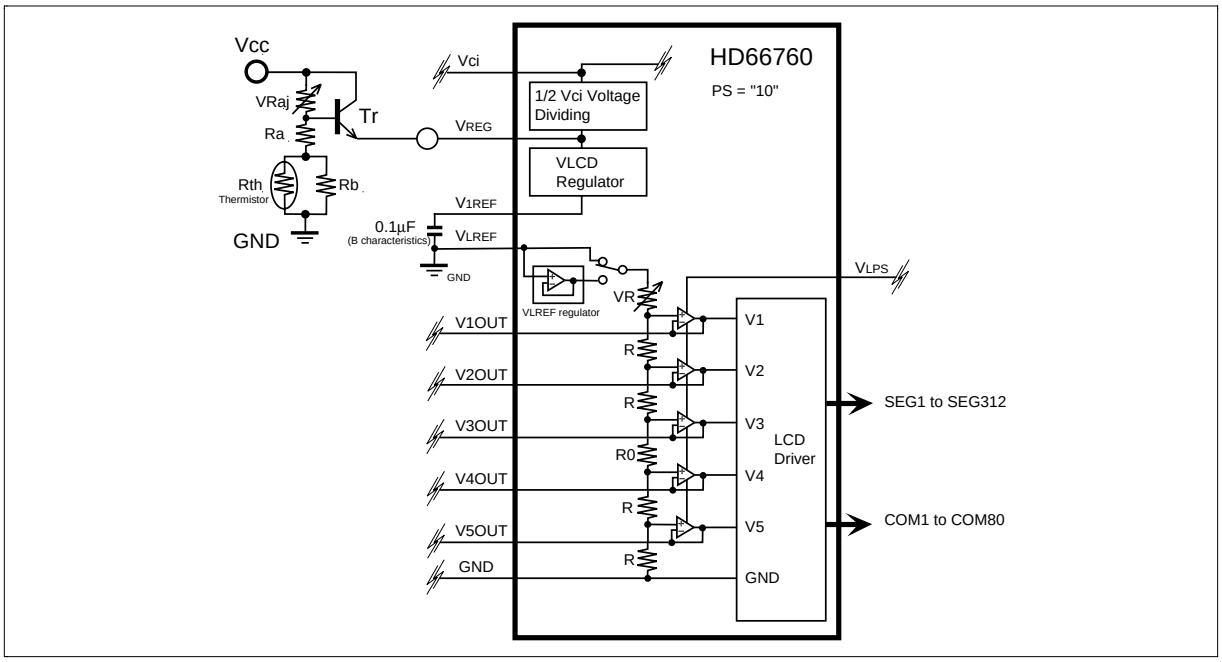


Figure 51 Temperature Compensation Circuits (1)

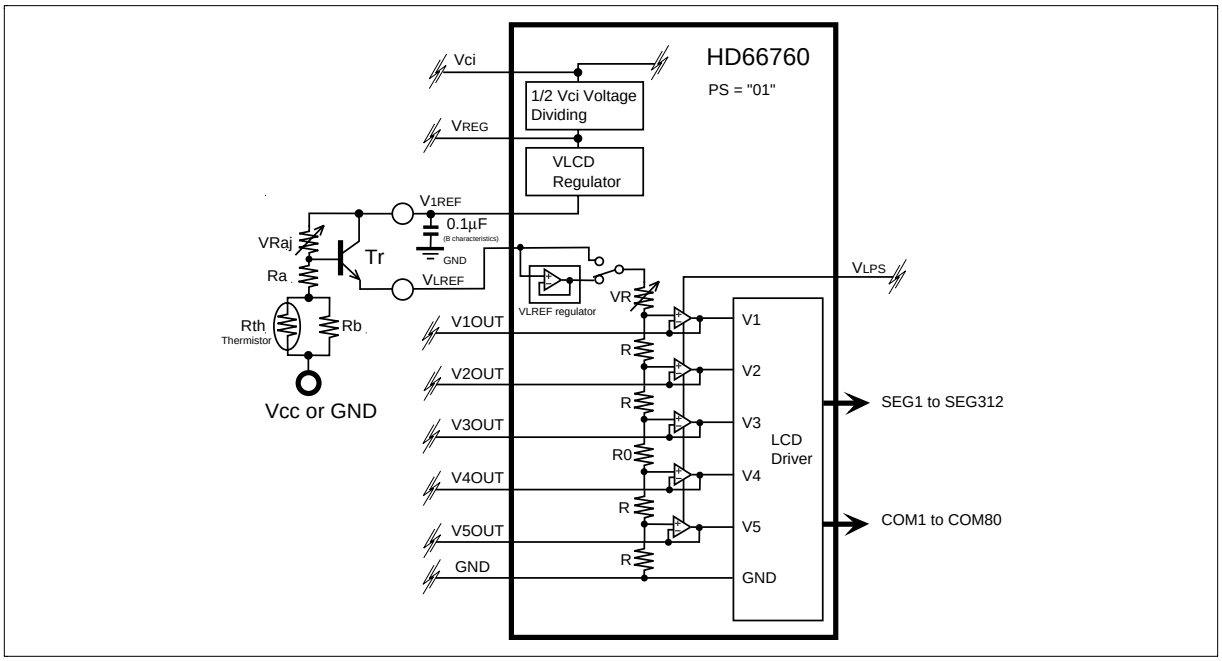


Figure 52 Temperature Compensation Circuits (2)

Switching the Step-up Factor

Instruction bits (BT1/0 bits) can optionally select the step-up factor of the internal step-up circuit. According to the display status, power consumption can be reduced by changing the LCD drive duty and the LCD drive bias, and by controlling the step-up factor for the minimum requirements. For details, see the Partial-display-on Function section.

According to the maximum step-up factor, external capacitors need to be connected. For example, when the maximum step-up is five times, capacitors between C6+ and C6– or between C5+ and C5– are needed as in the case of the six-times step-up.

Place a capacitor with a breakdown voltage of three times or more the Vci-GND voltage between C6+ and C6– and between C3+ and C3–, a capacitor with a breakdown voltage larger than the Vci-GND voltage between C1+ and C1–, C2+ and C2–, C4+ and C4–, and C5+ and C5–, and a capacitor with a breakdown voltage of n times or more the Vci-GND voltage to VLOUT (n: step-up factor) (see figure 53).

Note: Determine the capacitor breakdown voltages by checking Vci voltage fluctuation.

Table 37 VLOUT Output Status

BT1	BT0	VLOUT Output Status
0	0	Three-times step-up output
0	1	Four-times step-up output
1	0	Five-times step-up output
1	1	Six-times step-up output

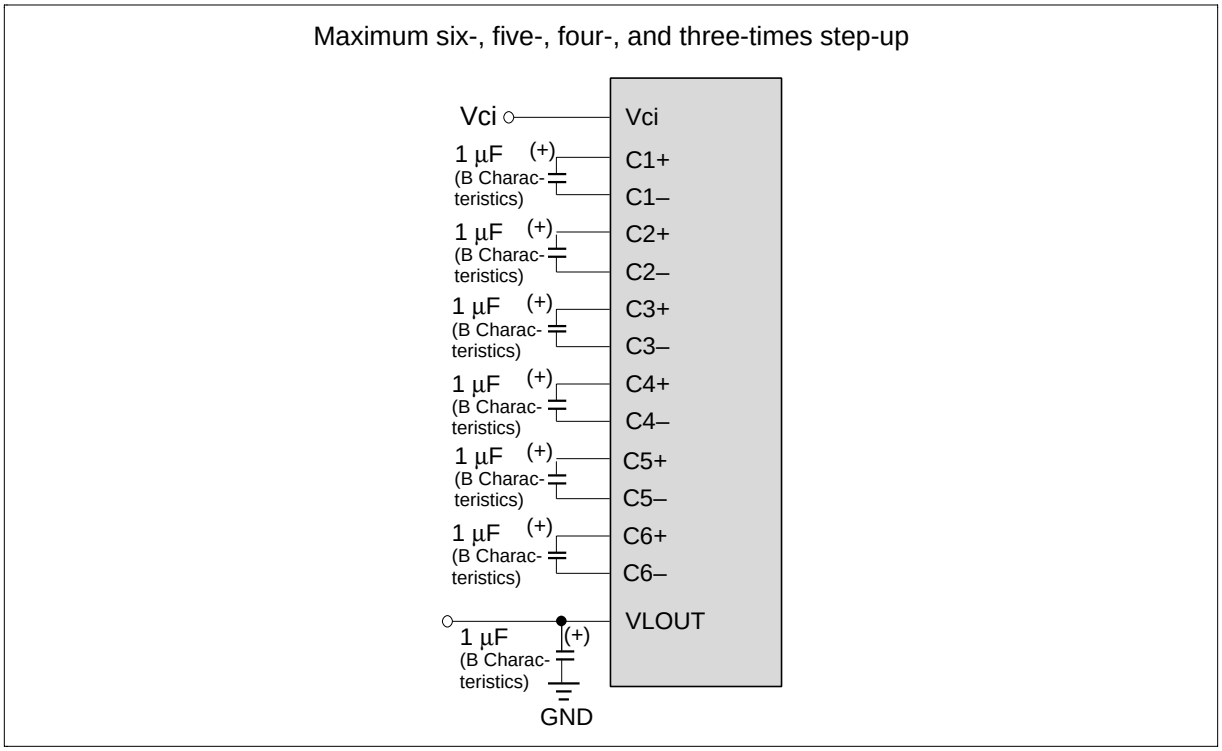


Figure 53 Step-up Circuit Output Factor Switching

Example of Power-supply Voltage Generator for More Than Seven-times Step-up Output

The HD66760 incorporates a step-up circuit for up to six-times step-up. However, the LCD drive voltage (VLCD) will not be enough for six-times step-up from Vcc when the power-supply voltage of Vcc is low or when the LCD drive voltage is high for the high-contrast LCD display. In this case, the reference voltage (Vci) for step-up can be set higher than the power-supply voltage of Vcc.

Set the Vci input voltage for the step-up circuit to 3.6 V or less within the range of Vcc + 1.0 V. Control the Vci voltage so that the step-up output voltage (VLOUT) should be less than the absolute maximum ratings (16.5 V).

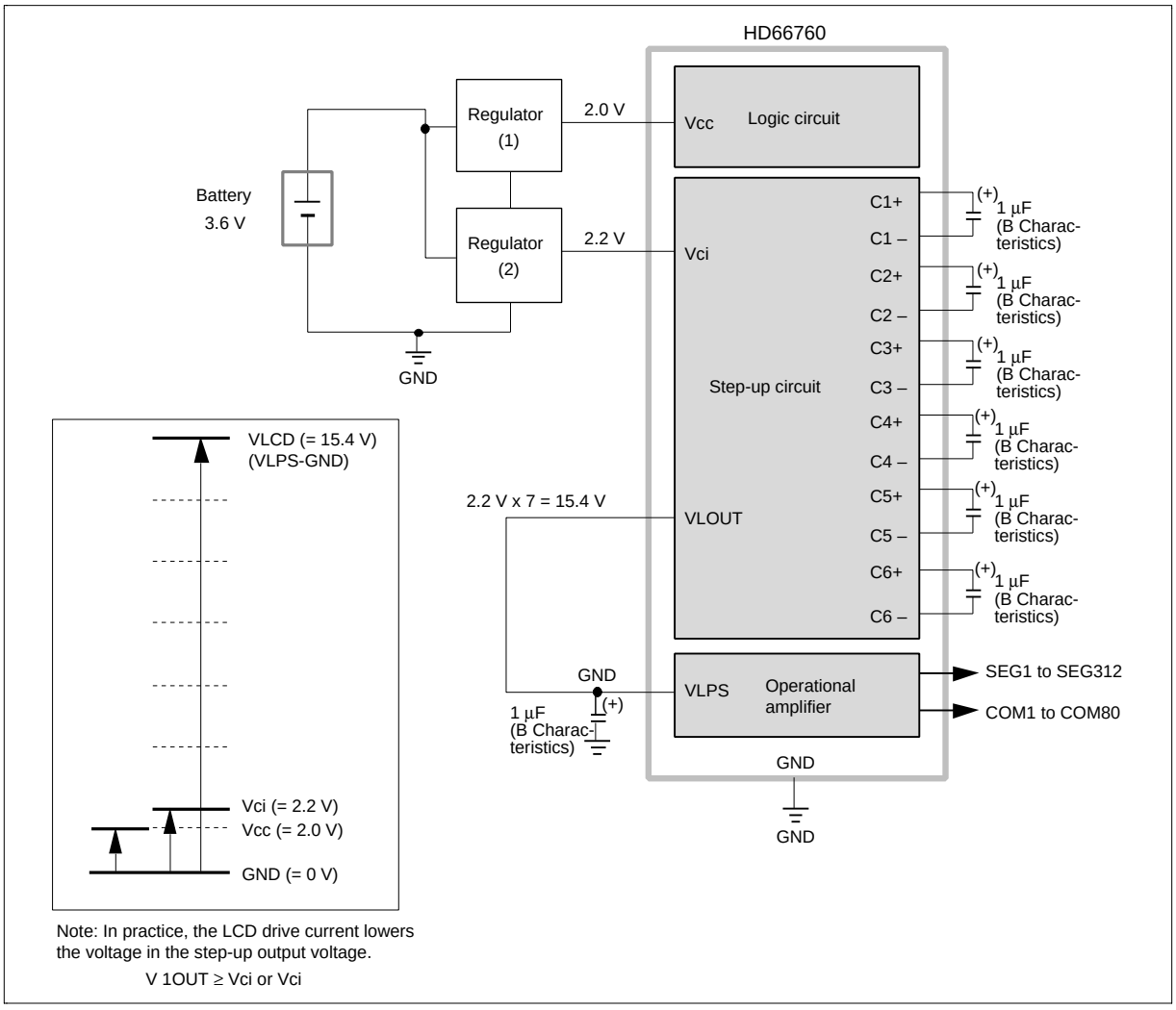


Figure 54 Usage Example of Step-up Circuit at Vci > Vcc

Restrictions on the 1st/2nd Screen Driving Position Register Settings

The following restrictions must be satisfied when setting the start line (SS16–10) and end line (SE16–10) of the 1st screen driving position register (R14h) and the start line (SS26–20) and end line (SE26–20) of the 2nd screen driving position register (R15h) for the HD66760. Note that incorrect display may occur if the restrictions are not satisfied.

Table 38 Restrictions on the 1st/2nd Screen Driving Position Register Settings

	1st Screen Driving (STP = 0)	2nd Screen Driving (STP = 1)
Register setting	SS16-10 ≤ SE16-0 ≤ 4FH	SS16-10 ≤ SE16-10 < SS26-20 ≤ SE26-20 ≤ 4FH
Display operation	• Time-sharing driving for COM pins (SS1+1) to (SE1+1) • Non-selection level driving for others	• Time-sharing driving for COM pins (SS1+1) to (SE1+1) and (SS2+1) to (SE2+1) • Non-selection level driving for others

Notes: 1. When the total line count in screen division driving settings is less than the duty setting, non-selection level driving is performed without the screen division driving setting range.
2. When the total line count in screen division driving settings is larger than the duty setting, the start line, the duty-setting line, and the lines between them are displayed and non-selection level driving is performed for other lines.
3. For the 1st screen driving, the SS26-20 and SE26-20 settings are ignored.

Sleep Mode

Setting the sleep mode bit (SLP) to 1 puts the HD66760 in the sleep mode, where the device stops all internal display operations, thus reducing current consumption. Specifically, LCD operation is completely halted. Here, all the SEG (SEG1 to SEG312) and COM (COM1 to COM80) pins output the GND level, resulting in no display. If the AP1–0 bits in the power control register are set to 00 in the sleep mode, the LCD drive power supply can be turned off, reducing the total current consumption of the LCD module.

Table 39 Comparison of Sleep Mode and Standby Mode

Function	Sleep Mode (SLP = 1)	Standby Mode (STB = 1)
LCD control	Turned off	Turned off
R-C oscillation circuit	Operates normally	Operation stopped

Standby Mode

Setting the standby mode bit (STB) to 1 puts the HD66760 in the standby mode, where the device stops completely, halting all internal operations including the R-C oscillation circuit, thus further reducing current consumption compared to that in the sleep mode. Specifically, all the SEG (SEG1 to SEG312) and COM (COM1 to COM80) pins for the time-sharing drive output the GND level, resulting in no display. If the AP1–0 bits are set to 00 in the standby mode, the LCD drive power supply can be turned off.

During the standby mode, no instructions can be accepted other than the start-oscillation instruction. To cancel the standby mode, issue the start-oscillation instruction to stabilize R-C oscillation before setting the STB bit to 0.

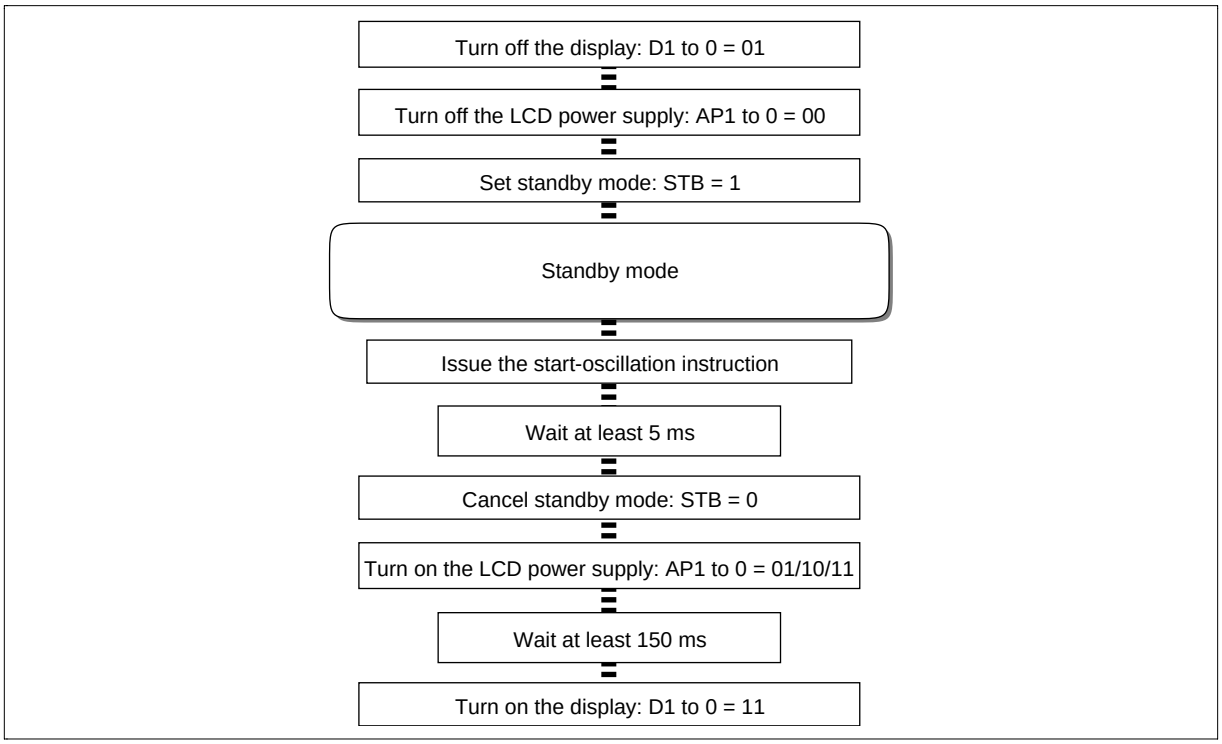


Figure 55 Procedure for Setting and Canceling Standby Mode

Power-on/off Sequence

To prevent pulse lighting of LCD screens at power-on/off, the power-on/off sequence is activated as shown below. However, since the sequence depends on LCD materials to be used, confirm the conditions by using your own system.

Power-on Sequence

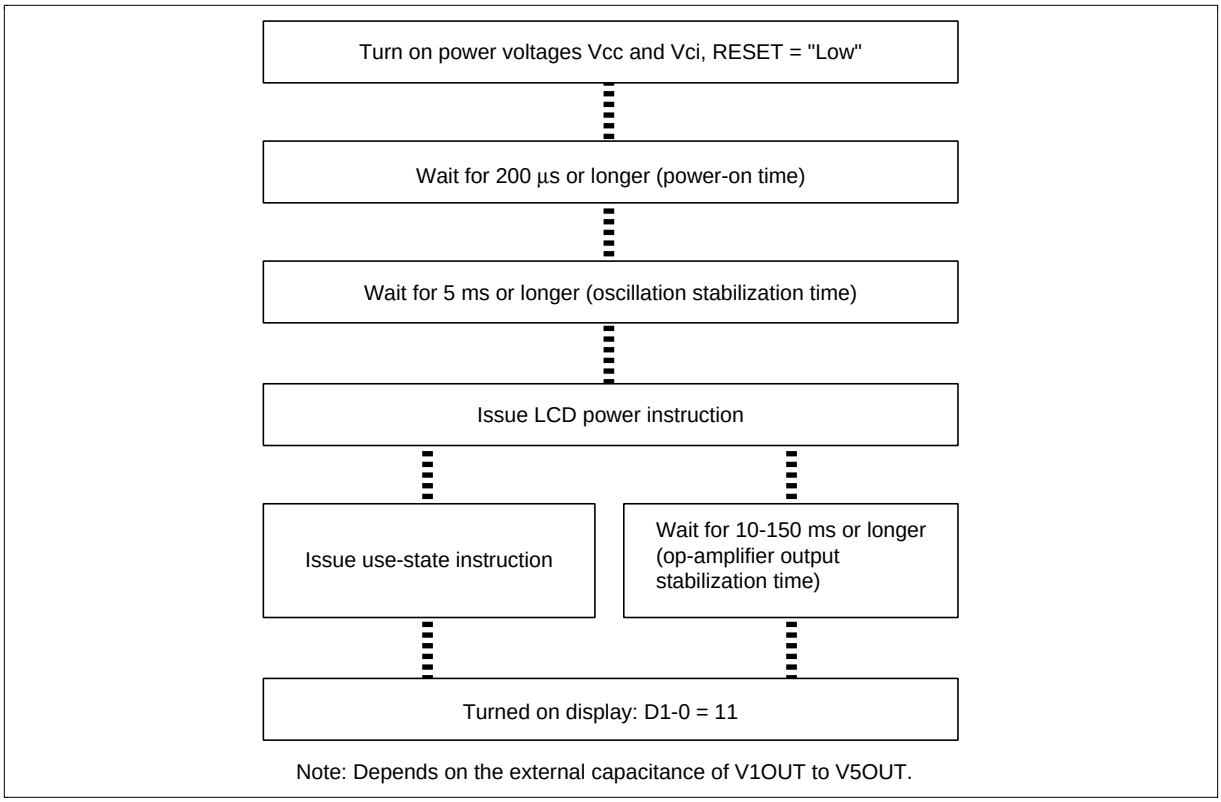


Figure 56 Power-on Sequence

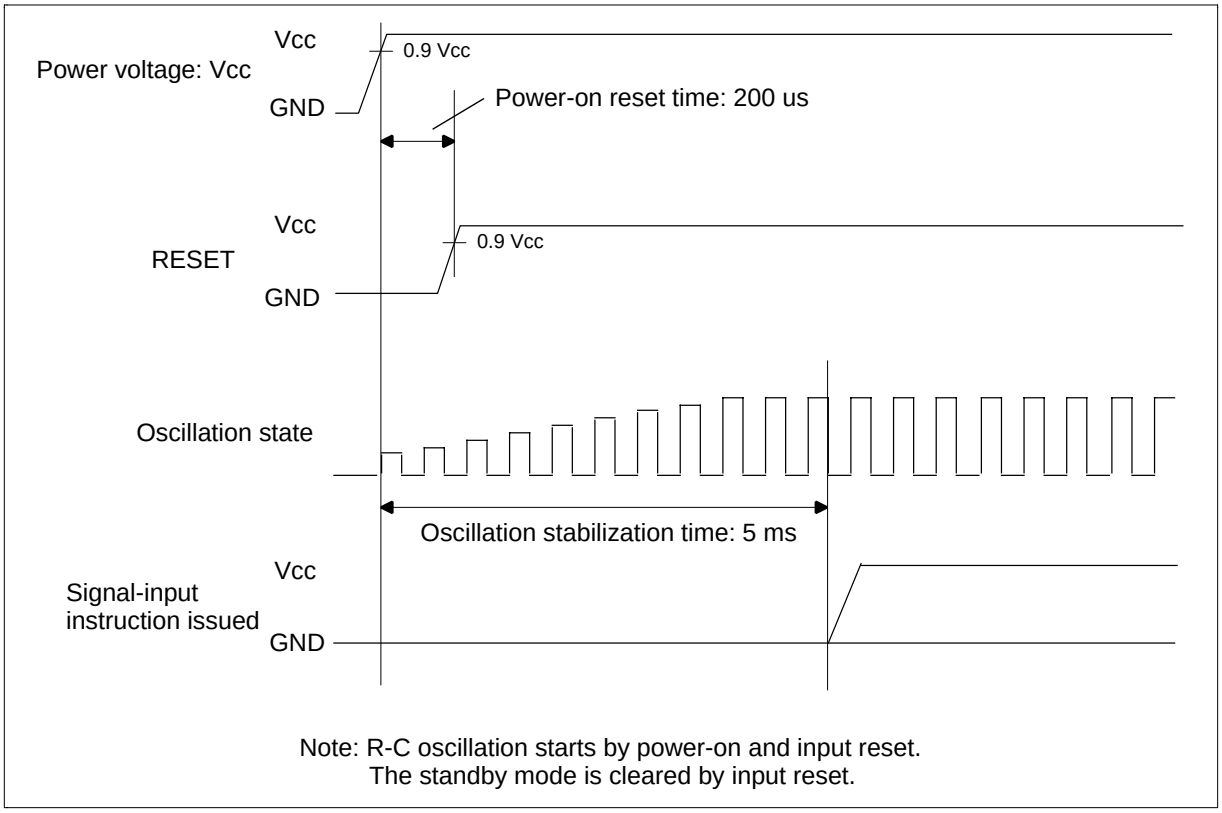


Figure 57 Power-on Timing

Power-off Sequence

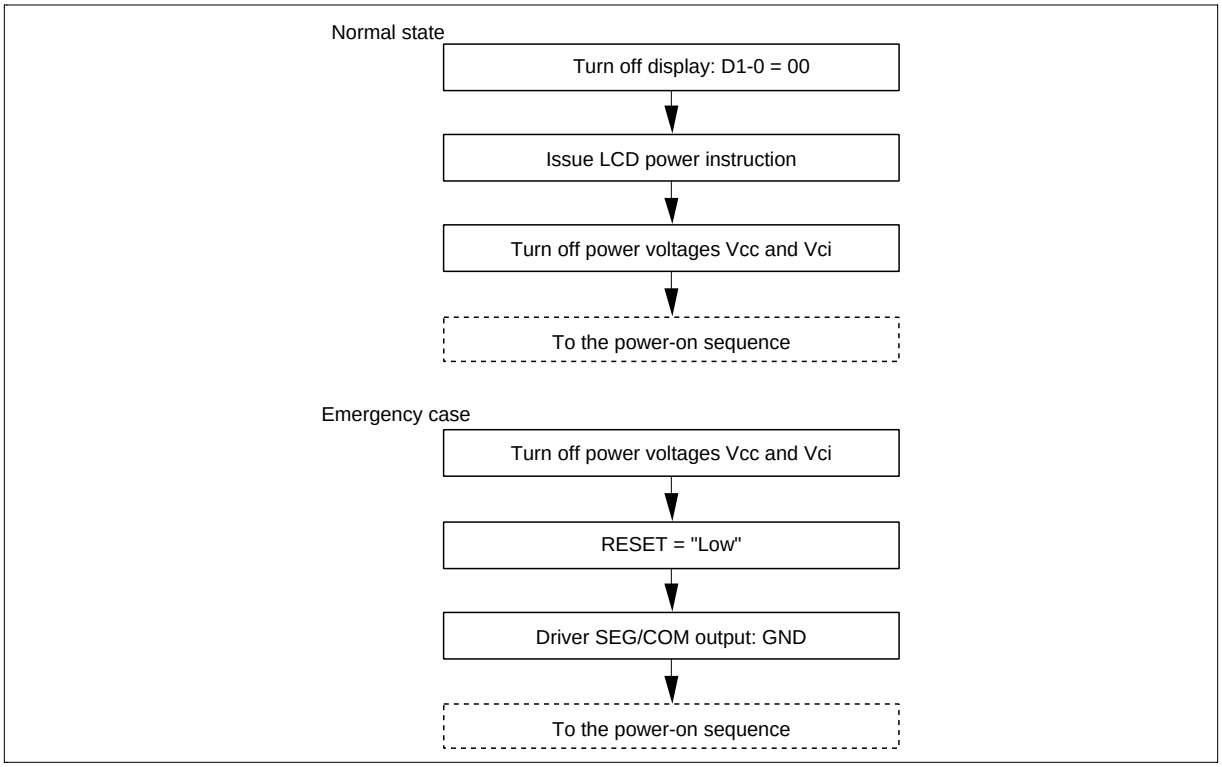


Figure 58 Power-off Sequence

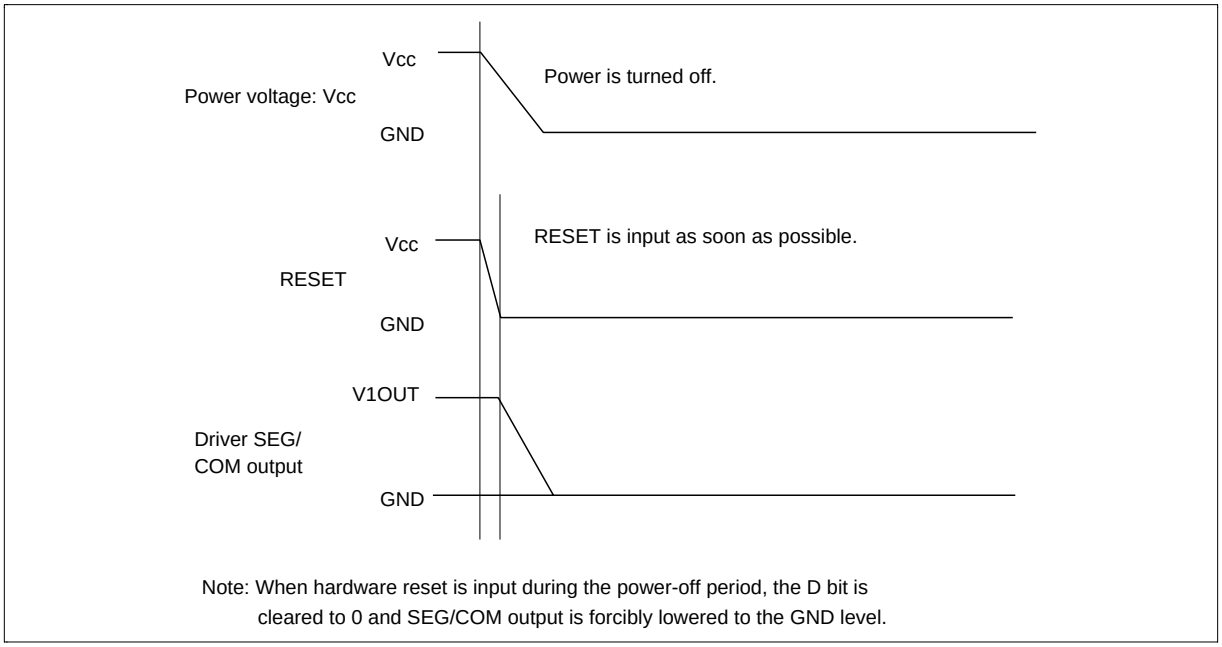


Figure 59 Power-off Timing

Absolute Maximum Ratings

Item	Symbol	Unit	Value	Notes*
Power supply voltage (1)	V_{CC}	V	–0.3 to +4.6	1, 2
Power supply voltage (2)	V_{LCD} – GND	V	–0.3 to +16.5	1, 3
Input voltage	Vt	V	–0.3 to V_{CC} + 0.3	1
Operating temperature	Topr	℃	–40 to +85	1, 4
Storage temperature	Tstg	℃	–55 to +110	1, 5

Notes: 1. If the LSI is used above these absolute maximum ratings, it may become permanently damaged. Using the LSI within the following electrical characteristics limits is strongly recommended for normal operation. If these electrical characteristic conditions are also exceeded, the LSI will malfunction and cause poor reliability.

2. $V_{CC} \geq$ GND must be maintained.
3. $V_{LCD} \geq$ GND must be maintained.
4. For die and wafer products, specified up to 85˚C.
5. This temperature specifications apply to the TCP package.

DC Characteristics (V_{CC} = 2.2 to 3.6 V, Ta = –40 to +85°C*[1])

Item	Symbol	Min	Typ	Max	Unit	Test Condition	Notes
Input high voltage	V_{IH}	0.7 V_{CC}	—	V_{CC}	V	V_{CC} = 2.2 to 3.6 V	2, 3
Input low voltage (1) (Except I^2C bus I/F pins)	V_{IL1}	–0.3	—	0.15 V_{CC}	V	V_{CC} = 2.2 to 3.6 V	2, 3
Input low voltage (2) (SDA and SCL : I^2C bus interface pins)	V_{IL2}	–0.3	—	0.3 V_{CC}	V	V_{CC} = 2.2 to 3.6 V	2, 3
Output high voltage (1) (DB0-15 pins, SDA : Clock synchronized serial I/F)	V_{OH1}	0.75 V_{CC}	—	—	V	I_{OH} = –0.1 mA	2
Output low voltage (1) (DB0-15 pins)	V_{OL1}	—	—	0.2 V_{CC}	V	V_{CC} = 2.2 to 2.4 V, I_{OL} = 0.1 mA	2
		—	—	0.15 V_{CC}	V	V_{CC} = 2.4 to 3.6 V, I_{OL} = 0.1 mA	2
Output low voltage (2) (SDA : I^2C bus I/F)	V_{OL2}	—	—	0.2 V_{CC}	V	I_{OL} = 0.4 mA	2
Output low voltage (3) (SDA : I^2C bus I/F)	V_{OL3}	—	—	0.4	V	I_{OL} = 3 mA	2
Driver ON resistance (COM pins)	R_{COM}	—	3	10	kΩ	±Id = 0.05 mA, V_{LCD} = 10 V	4
Driver ON resistance (SEG pins)	R_{SEG}	—	3	10	kΩ	±Id = 0.05 mA, V_{LCD} = 10 V	4
I/O leakage current	I_{Li}	–1	—	1	µA	Vin = 0 to V_{CC}	5
Current consumption during normal operation (V_{CC} – GND)	I_{OP}	—	130	180	µA	CR oscillation, V_{CC} = 3.0 V, Ta = 25°C, f_{OSC} = 180 kHz (1/80 duty), display all 1	6, 7
Current consumption during standby mode (V_{CC} – GND)	I_{ST}	—	0.2	5	µA	V_{CC} = 3 V, Ta = 25°C	6, 7
LCD drive power supply current (V_{LPS} – GND)	I_{LCD}	—	27	60	µA	V_{CC} = 3.0 V, V_{LCD} = 15 V, 1/10 bias, CR oscillation, f_{OSC} = 180 kHz (1/80 duty), AP1-0 = "01", Ta = 25°C, display all 1	7

Note: For the numbered notes, refer to the Electrical Characteristics Notes section following these tables.

DC Characteristics (cont) (V_{CC} = 2.2 to 3.6 V, Ta = –40 to +85°C*[1])

Item	Symbol	Min	Typ	Max	Unit	Test Condition	Notes
LCD drive voltage (V_{LPS} – GND)	V_{LCD}	5.0	—	15.5	V		8
VREG input voltage (VREG pin)	V_{REG}	—	1.3	2.5	V	VREG external input (PS1-0 = "10"), Ta = 25°C	
V1REF output voltage (V1REF pin)	V_{1REF}	—	13.0	—	V	VREG = 1.3 V, Ta = 25°C, 10 times VREG (VR2-0 = "110") V1REF ≤ VLPS – 0.5V	
LCD output voltage range (1)	V_{1OUT} V_{2OUT} V_{2OUT}	VLPS/2 – 0.5	—	VLPS – 0.5 V	V		
LCD output voltage range (2)	V_{4OUT} V_{5OUT}	0.5	—	VLPS/2	V		

Step-up Circuit Characteristics

Item	Symbol	Min	Typ	Max	Unit	Test Condition	Notes
Three-times step-up output voltage (VLOUT pin)	V_{UP3}	7.6	7.9	8.1	V	V_{CC} = Vci = 2.7 V, I_O = 30 µA, C = 1 µF, f_{OSC} = 180 kHz, Ta = 25°C	11
Four-times step-up output voltage (VLOUT pin)	V_{UP4}	10.3	10.6	10.8	V	V_{CC} = Vci = 2.7 V, I_O = 30 µA, C = 1 µF, f_{OSC} = 180 kHz, Ta = 25°C	11
Five-times step-up output voltage (VLOUT pin)	V_{UP5}	13.0	13.3	13.5	V	V_{CC} = Vci = 2.7 V, I_O = 30 µA, C = 1 µF, f_{OSC} = 180 kHz, Ta = 25°C	11
Six-times step-up output voltage (VLOUT pin)	V_{UP6}	14.2	14.7	15.0	V	V_{CC} = Vci = 2.5 V, I_O = 30 µA, C = 1 µF, f_{OSC} = 180 kHz, Ta = 25°C	11
Use range of step-up output voltages	V_{UP3} V_{UP4} V_{UP5} V_{UP6}	V_{CC}	—	15.5	V	For three- to six-times step-up	11

Note: For the numbered notes, refer to the Electrical Characteristics Notes section following these tables.

AC Characteristics (V_{CC} = 2.2 to 3.6 V, Ta = –40 to +85°C*[1])

Clock Characteristics (V_{CC} = 2.2 to 3.6 V)

Item	Symbol	Min	Typ	Max	Unit	Test Condition	Notes
External clock frequency	fcp	120	180	240	kHz		9
External clock duty ratio	Duty	45	50	55	%		9
External clock rise time	trcp	—	—	0.2	µs		9
External clock fall time	tfcp	—	—	0.2	µs		9
R-C oscillation clock	f_{OSC}	144	180	216	kHz	Rf = 200 kΩ, V_{CC} = 3 V	10

Note: For the numbered notes, refer to the Electrical Characteristics Notes section following these tables.

68-system Bus Interface Timing Characteristics

(Vcc = 2.2 to 2.4 V)

Item		Symbol	Min	Typ	Max	Unit	Test Condition
Enable cycle time	Write	t_{CYCE}	600	—	—	ns	Figure 67
	Read	t_{CYCE}	800	—	—		
Enable high-level pulse width	Write	PW_{EH}	120	—	—	ns	Figure 67
	Read	PW_{EH}	350	—	—		
Enable low-level pulse width	Write	PW_{EL}	300	—	—	ns	Figure 67
	Read	PW_{EL}	400	—	—		
Enable rise/fall time		t_{Er}, t_{Ef}	—	—	25	ns	Figure 67
Setup time (RS, R/W to E, CS*)		t_{ASE}	10	—	—	ns	Figure 67
Address hold time		t_{AHE}	20	—	—	ns	Figure 67
Write data setup time		t_{DSWE}	60	—	—	ns	Figure 67
Write data hold time		t_{HE}	20	—	—	ns	Figure 67
Read data delay time		t_{DDRE}	—	—	300	ns	Figure 67
Read data hold time		t_{DHRE}	5	—	—	ns	Figure 67

(Vcc = 2.4 to 3.6 V)

Item		Symbol	Min	Typ	Max	Unit	Test Condition
Enable cycle time	Write	t_{CYCE}	300	—	—	ns	Figure 67
	Read	t_{CYCE}	500	—	—		
Enable high-level pulse width	Write	PW_{EH}	70	—	—	ns	Figure 67
	Read	PW_{EH}	250	—	—		
Enable low-level pulse width	Write	PW_{EL}	100	—	—	ns	Figure 67
	Read	PW_{EL}	200	—	—		
Enable rise/fall time		t_{Er}, t_{Ef}	—	—	25	ns	Figure 67
Setup time (RS, R/W to E, CS*)		t_{ASE}	10	—	—	ns	Figure 67
Address hold time		t_{AHE}	5	—	—	ns	Figure 67
Write data setup time		t_{DSWE}	60	—	—	ns	Figure 67
Write data hold time		t_{HE}	15	—	—	ns	Figure 67
Read data delay time		t_{DDRE}	—	—	200	ns	Figure 67
Read data hold time		t_{DHRE}	5	—	—	ns	Figure 67

80-system Bus Interface Timing Characteristics

(Vcc = 2.2 to 2.4 V)

Item		Symbol	Min	Typ	Max	Unit	Test Condition
Bus cycle time	Write	t_{CYCW}	600	—	—	ns	Figure 68
	Read	t_{CYCR}	800	—	—	ns	Figure 68
Write low-level pulse width		PW_{LW}	120	—	—	ns	Figure 68
Read low-level pulse width		PW_{LR}	350	—	—	ns	Figure 68
Write high-level pulse width		PW_{HW}	300	—	—	ns	Figure 68
Read high-level pulse width		PW_{HR}	400	—	—	ns	Figure 68
Write/Read rise/fall time		t_{WRr} , $_{WRf}$	—	—	25	ns	Figure 68
Setup time (RS to CS*, WR*, RD*)		t_{AS}	10	—	—	ns	Figure 68
Address hold time		t_{AH}	20	—	—	ns	Figure 68
Write data setup time		t_{DSW}	60	—	—	ns	Figure 68
Write data hold time		t_{HWR}	20	—	—	ns	Figure 68
Read data delay time		t_{DDR}	—	—	300	ns	Figure 68
Read data hold time		t_{DHR}	5	—	—	ns	Figure 68

(Vcc = 2.4 to 3.6 V)

Item		Symbol	Min	Typ	Max	Unit	Test Condition
Bus cycle time	Write	t_{CYCW}	300	—	—	ns	Figure 68
	Read	t_{CYCR}	500	—	—	ns	Figure 68
Write low-level pulse width		PW_{LW}	70	—	—	ns	Figure 68
Read low-level pulse width		PW_{LR}	250	—	—	ns	Figure 68
Write high-level pulse width		PW_{HW}	100	—	—	ns	Figure 68
Read high-level pulse width		PW_{HR}	200	—	—	ns	Figure 68
Write/Read rise/fall time		$t_{WRr, WRf}$	—	—	25	ns	Figure 68
Setup time (RS to CS*, WR*, RD*)		t_{AS}	10	—	—	ns	Figure 68
Address hold time		t_{AH}	5	—	—	ns	Figure 68
Write data setup time		t_{DSW}	60	—	—	ns	Figure 68
Write data hold time		t_{HWR}	15	—	—	ns	Figure 68
Read data delay time		t_{DDR}	—	—	200	ns	Figure 68
Read data hold time		t_{DHR}	5	—	—	ns	Figure 68

Clock Synchronized Serial Interface Timing Characteristics

(Vcc = 2.2 to 3.6 V)

Item	Symbol	Min	Typ	Max	Unit	Test Condition
Serial clock cycle time	t_{SCYC}	142	—	—	ns	Figure 70
		330	—	—	ns	Figure 71
Serial clock high-level pulse width	t_{SCH}	50	—	—	ns	Figure 70
		130	—	—	ns	Figure 71
Serial clock low-level pulse width	t_{SCL}	50	—	—	ns	Figure 70
		130	—	—	ns	Figure 71
Serial clock rise/fall time	t_{SCr} , t_{SCf}	—	—	25	ns	Figure 70, 71
CS* Setup time	t_{CSU}	20	—	—	ns	Figure 70
		60	—	—	ns	Figure 71
CS* hold time	t_{CH}	100	—	—	ns	Figure 70
		60	—	—	ns	Figure 71
Serial input data setup time	t_{SISU}	40	—	—	ns	Figure 70
Serial input data hold time	t_{SIH}	40	—	—	ns	Figure 70
Serial output data delay time	t_{SOD}	—	—	130	ns	Figure 71
Serial output data hold time	t_{SOH}	0	—	—	ns	Figure 71

I2C Bus Interface Timing Characteristics

(Vcc = 2.2 to 3.6 V)

Item	Symbol	Min	Typ	Max	Unit	Test Condition
SCL clock frequency	f_{SCL}	0	—	1300	kHz	Figure 72
SCL clock high-level pulse width	t_{SCLH}	120	—	—	ns	Figure 72
SCL clock low-level pulse width	t_{SCLL}	240	—	—	ns	Figure 72
SCL/SDA rise time	t_{Sr}	10	—	160	ns	Figure 72
SCL/SDA fall time	t_{Sf}	10	—	70	ns	Figure 72
Bus free time	t_{BUF}	240	—	—	ns	Figure 72
Start condition hold time	t_{STAH}	320	—	—	ns	Figure 72
Setup time for a repeated START condition	t_{STAS}	320	—	—	ns	Figure 72
Setup time for STOP condition	t_{STOS}	320	—	—	ns	Figure 72
SDA data setup time	t_{SDAS}	40	—	—	ns	Figure 72
SDA data hold time	t_{SDAH}	0	—	—	ns	Figure 72
SCL/SDA spike pulse width	t_{SP}	0	—	10	ns	Figure 72

Reset Timing Characteristics (V_{CC} = 2.2 to 3.6 V)

Item	Symbol	Min	Typ	Max	Unit	Test Condition
Reset low-level width	t_{RES}	200	—	—	µs	Figure 69

Electrical Characteristics Notes

1. For bare die and wafer products, specified up to 85°C.
2. The following three circuits are I/O pin configurations (figure 60).

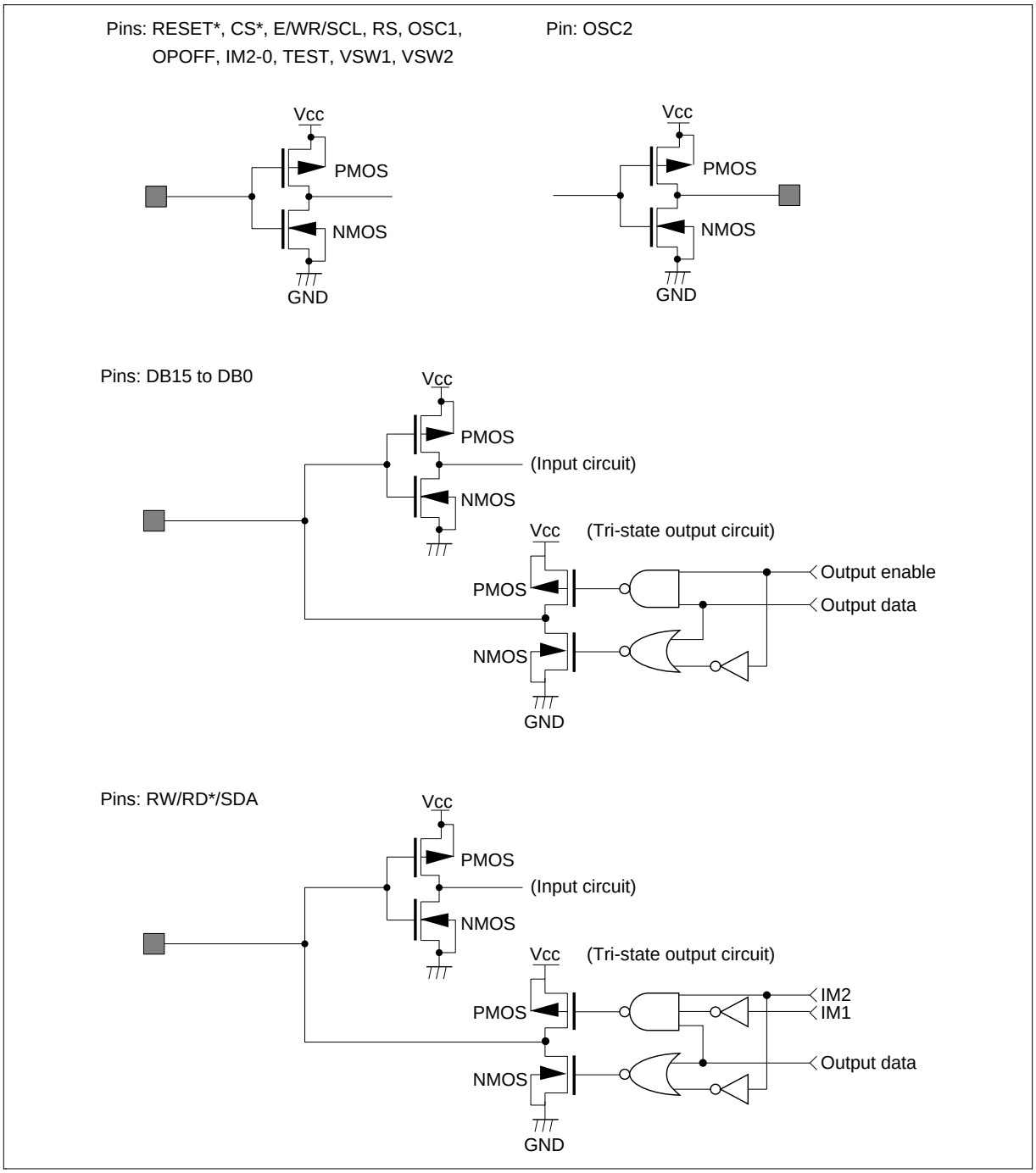


Figure 60 I/O Pin Configuration

3. The TEST, VSW1, and VSW2 pins must be grounded and the IM2-0 and OPOFF pins must be grounded or connected to Vcc.
4. Applies to the resistor value (RCOM) between power supply pins V1OUT, V2OUT, V5OUT, GND and common signal pins, and resistor value (RSEG) between power supply pins V1OUT, V3OUT, V4OUT, GND and segment signal pins.
5. This excludes the current flowing through output drive MOSs.
6. This excludes the current flowing through the input/output units. The input level must be fixed high or low because through current increases if the CMOS input is left floating. Even if the CS pin is low or high when an access with the interface pin is not performed, current consumption does not change.
7. The following shows the relationship between the operation frequency (fosc) and current consumption (Icc) (figure 61).

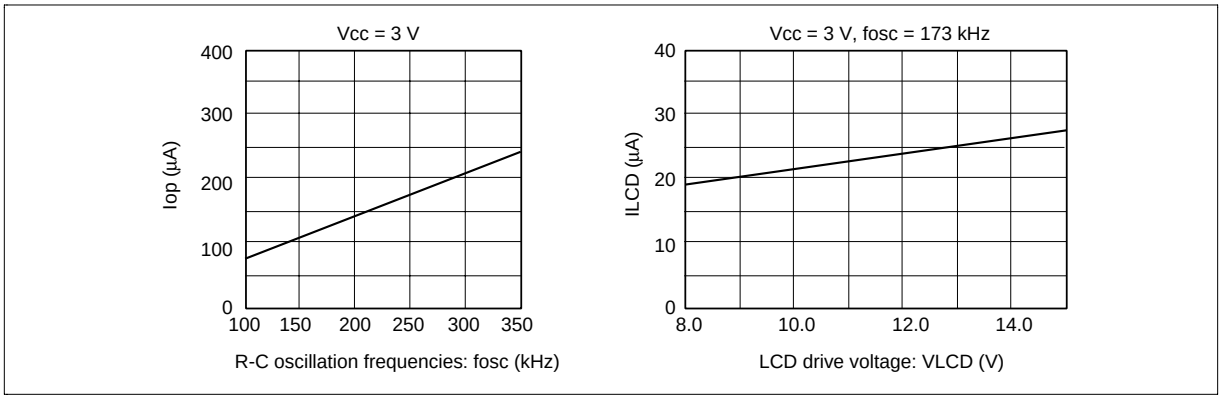


Figure 61 Relationship between the Operation Frequency and Current Consumption

8. Each COM and SEG output voltage is within Å}0.15 V of the LCD voltage (Vcc, V1, V2, V3, V4, V5) when there is no load.
9. Applies to the external clock input (figure 62).

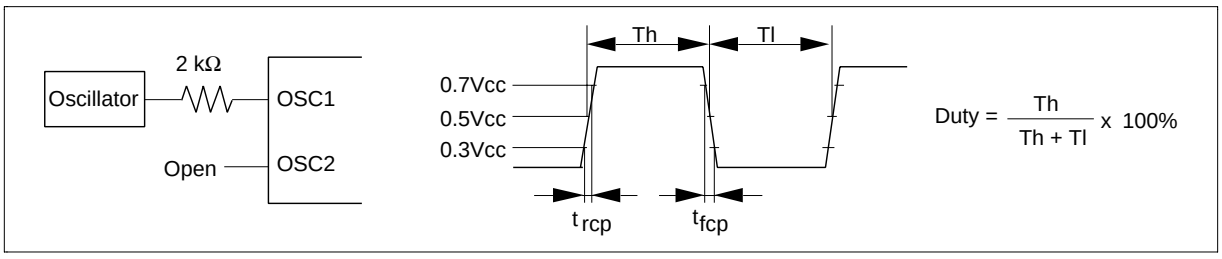
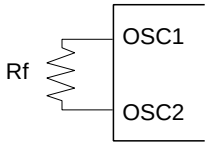


Figure 62 External Clock Supply

10. Applies to the internal oscillator operations using external oscillation resistor Rf (figure 63 and table 40).



Since the oscillation frequency varies depending on the OSC1 and OSC2 pin capacitance, the wiring length to these pins should be minimized.

Figure 63 Internal Oscillation

Table 40 External Resistance Value and R-C Oscillation Frequency (Referential Data)

External Resistance (Rf)	R-C Oscillation Frequency: fosc (kHz)		
	Vcc = 2.2 V	Vcc = 3.0 V	Vcc = 3.6 V
91 kΩ	283	337	359
110 kΩ	243	287	304
130 kΩ	212	249	263
160 kΩ	180	209	220
200 kΩ	151	173	181
240 kΩ	131	148	155
330 kΩ	101	113	117
470 kΩ	76	84	86

11. The step-up characteristics test circuit is shown in figure 64.

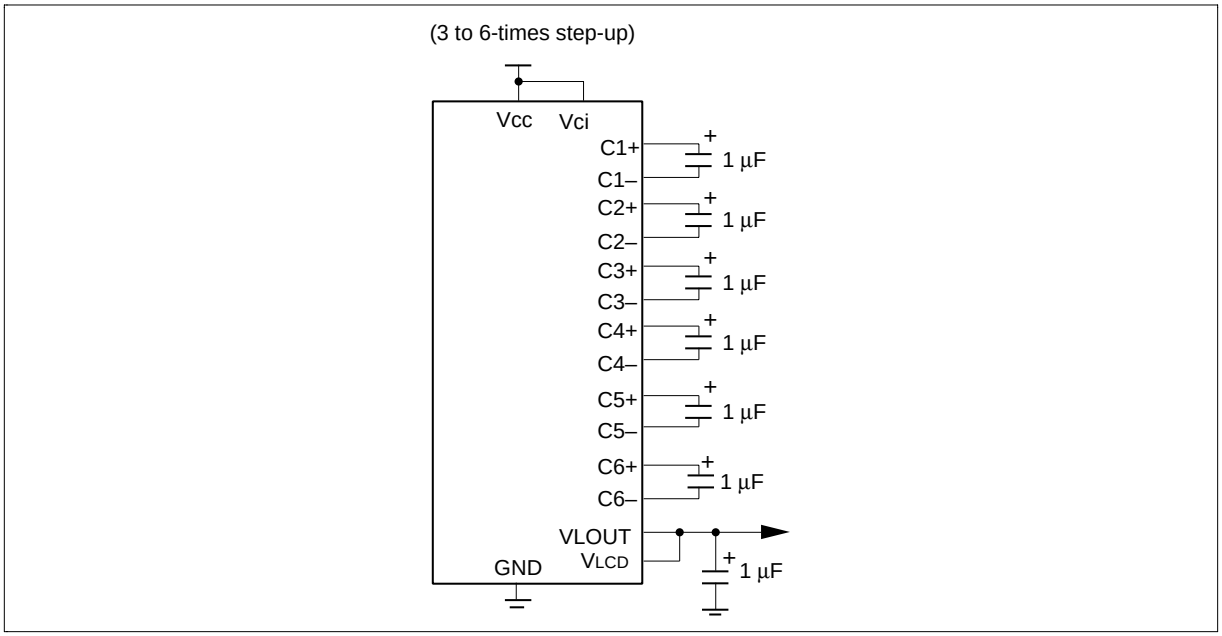


Figure 64 Step-up Characteristics Test Circuit

Referential data

VUP3 = VLCD - GND (x3 times boost), VUP4 = VLCD - GND (x4 times boost)
VUP5 = VLCD - GND (x5 times boost), VUP6 = VLCD - GND (x6 times boost)

(i) Relation between the obtained voltage and input voltage

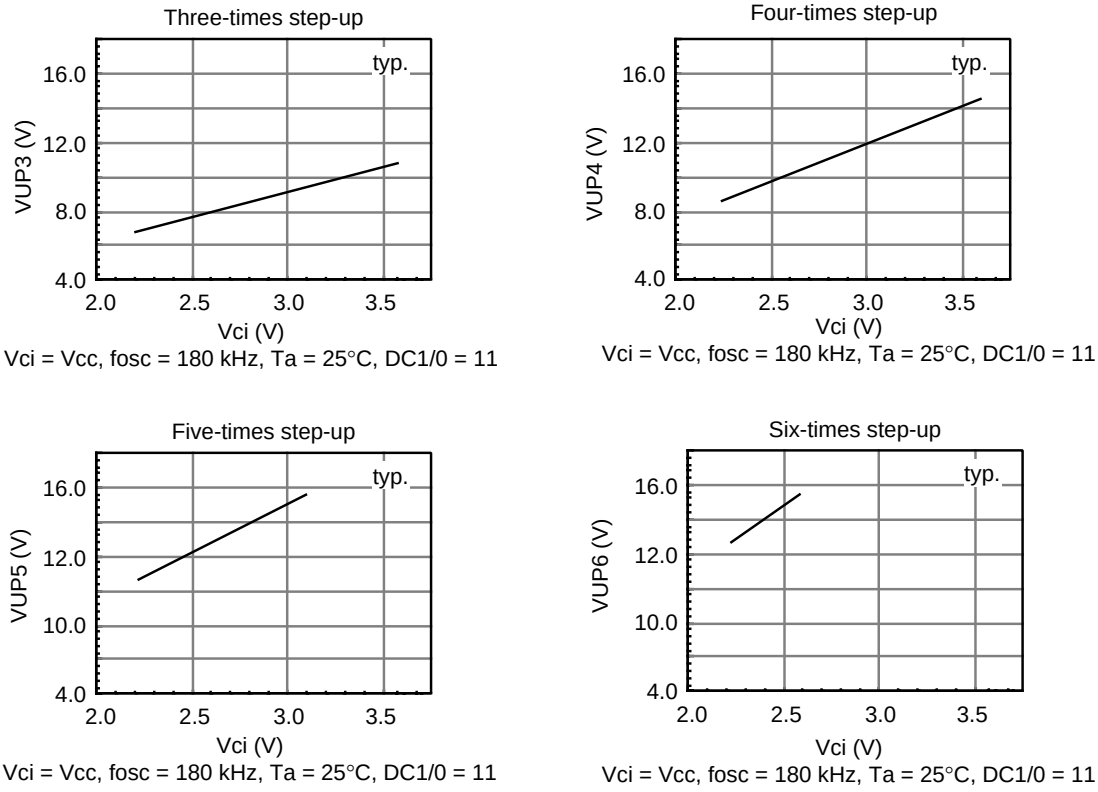
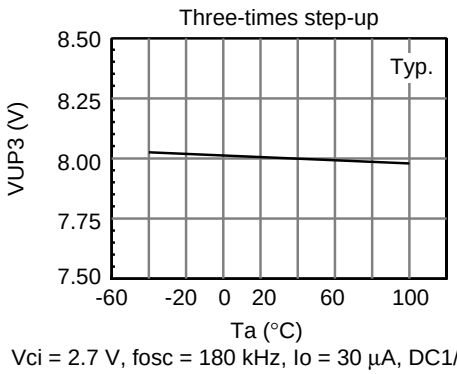
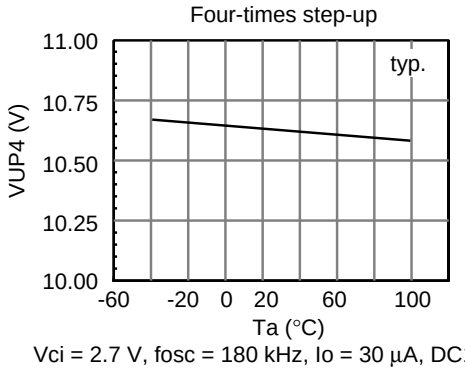


Figure 65 Step-up

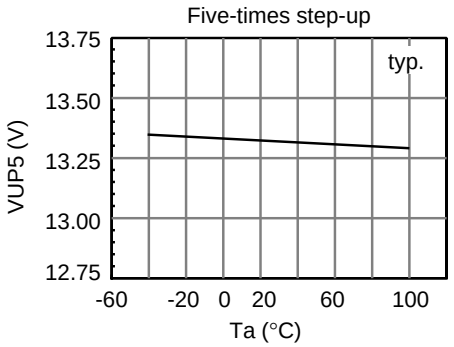
(ii) Relation between the obtained voltage and temperature



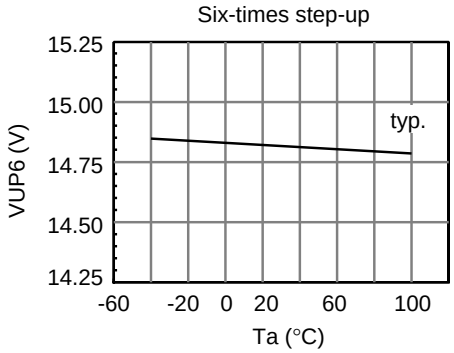
Vci = 2.7 V, fosc = 180 kHz, Io = 30 µA, DC1/0 = 11



Vci = 2.7 V, fosc = 180 kHz, Io = 30 µA, DC1/0 = 11



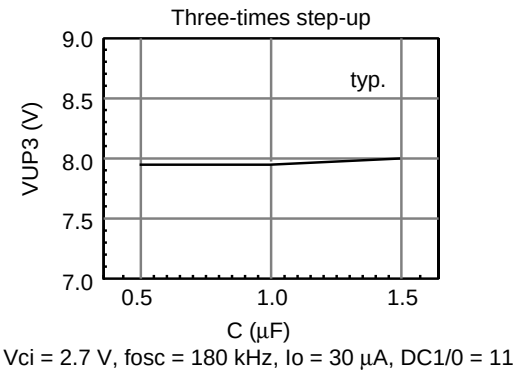
Vci = 2.7 V, fosc = 180 kHz, Io = 30 µA, DC1/0 = 11



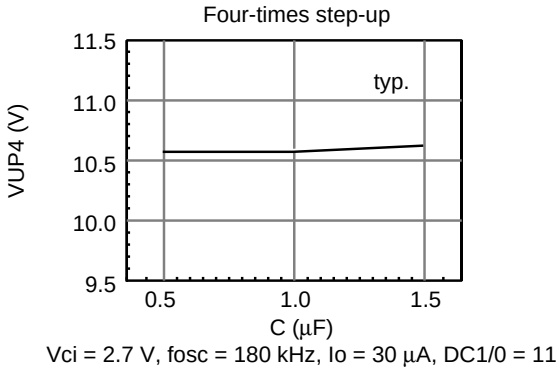
Vci = 2.5 V, fosc = 180 kHz, Io = 30 µA, DC1/0 = 11

Figure 65 Step-up (cont)

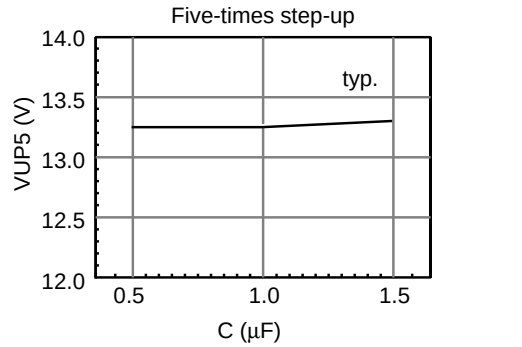
(iii) Relation between the obtained voltage and capacity



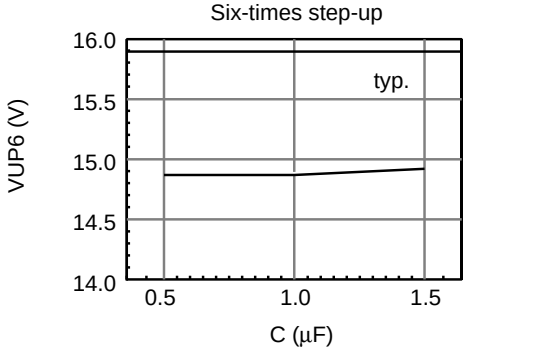
Vci = 2.7 V, fosc = 180 kHz, Io = 30 µA, DC1/0 = 11



Vci = 2.7 V, fosc = 180 kHz, Io = 30 µA, DC1/0 = 11



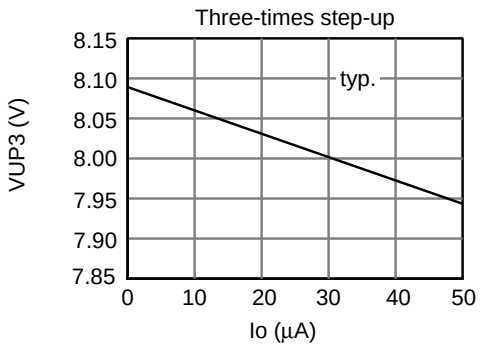
Vci = 2.7 V, fosc = 180 kHz, Io = 30 µA, DC1/0 = 11



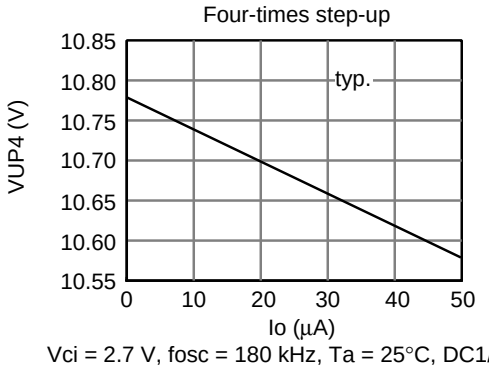
Vci = 2.5 V, fosc = 180 kHz, Io = 30 µA, DC1/0 = 11

Figure 65 Step-up (cont)

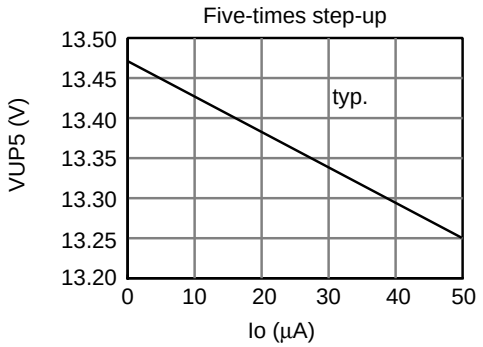
(iv) Relation between the obtained voltage and current



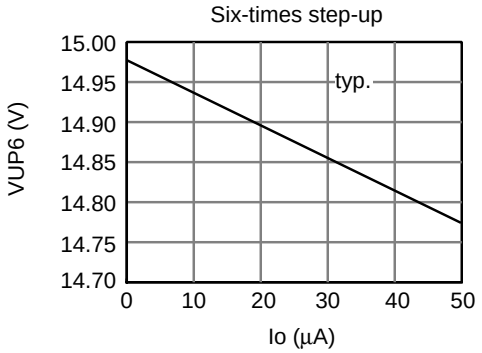
Vci = 2.7 V, fosc = 180 kHz, Ta = 25°C, DC1/0 = 11



Vci = 2.7 V, fosc = 180 kHz, Ta = 25°C, DC1/0 = 11



Vci = 2.7 V, fosc = 180 kHz, Ta = 25°C, DC1/0 = 11



Vci = 2.5 V, fosc = 180 kHz, Ta = 25°C, DC1/0 = 11

Figure 65 Step-up (cont)

Load Circuits

AC Characteristics Test Load Circuits

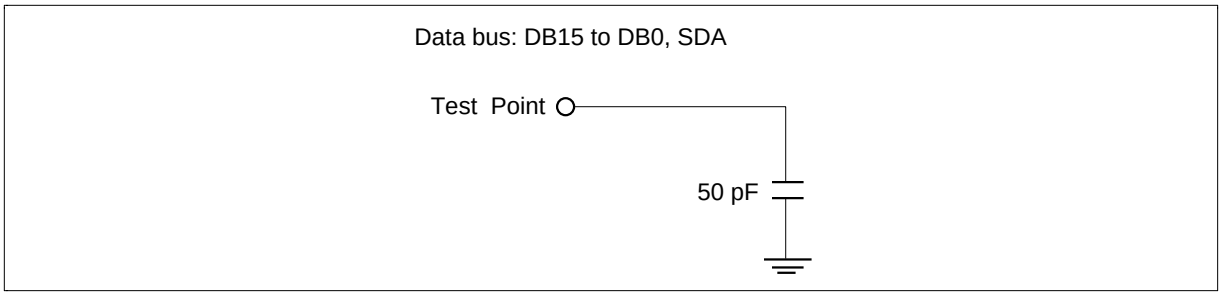
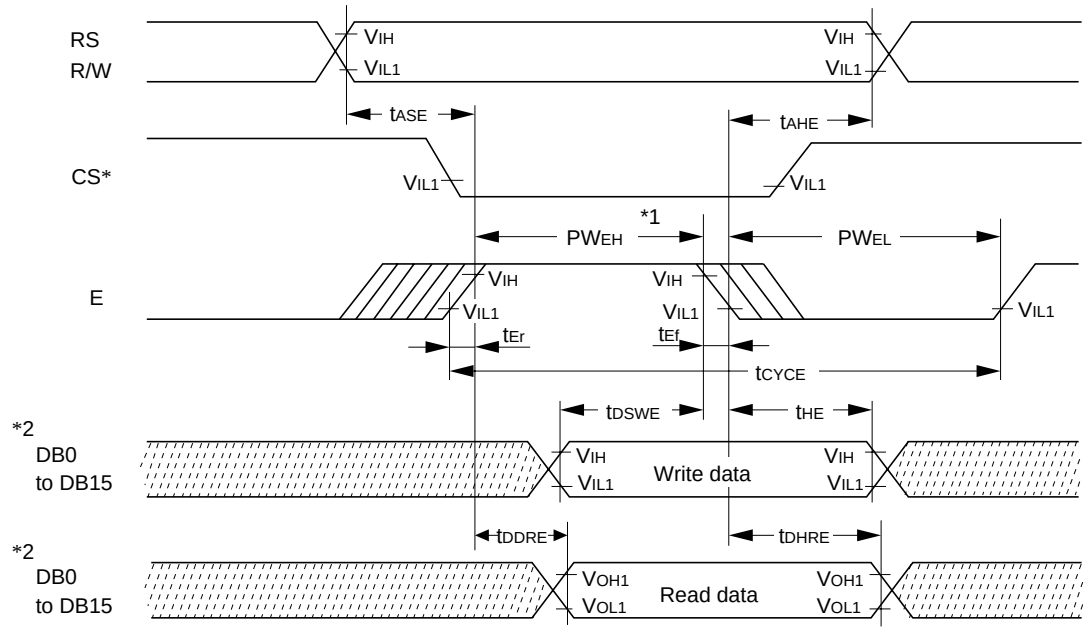


Figure 66 Load Circuit

Timing Characteristics

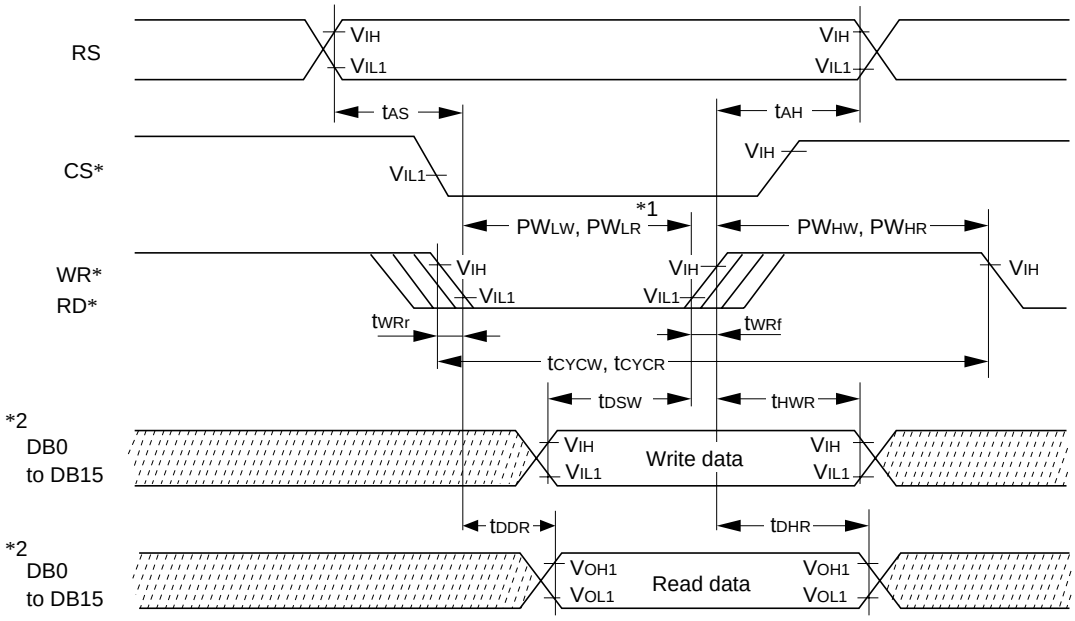
68-system Bus Operation



Note: 1. PWEH is specified in the overlapped period when CS* is low and E is high.
2. Parallel data transfer is enabled on the DB15-8 pins when the 8-bit bus interface is used. Fix tje DB7-0 pins to Vcc or GND.

Figure 67 68-system Bus Timing

80-system Bus Operation



Note: 1. PW_{LW} and PW_{LR} are specified in the overlapped period when CS* is low and WR* or RD* is low.
2. Parallel data transfer is enabled on the DB15-8 pins when the 8-bit bus interface is used.
Fix tje DB7-0 pins to Vcc or GND.

Figure 68 80-system Bus Timing

Reset Operation

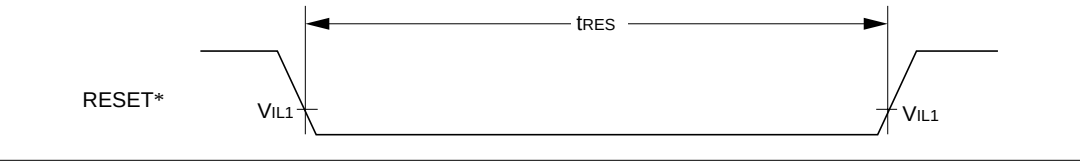


Figure 69 Reset Timing

Clock Synchronized Serial Interface Operation

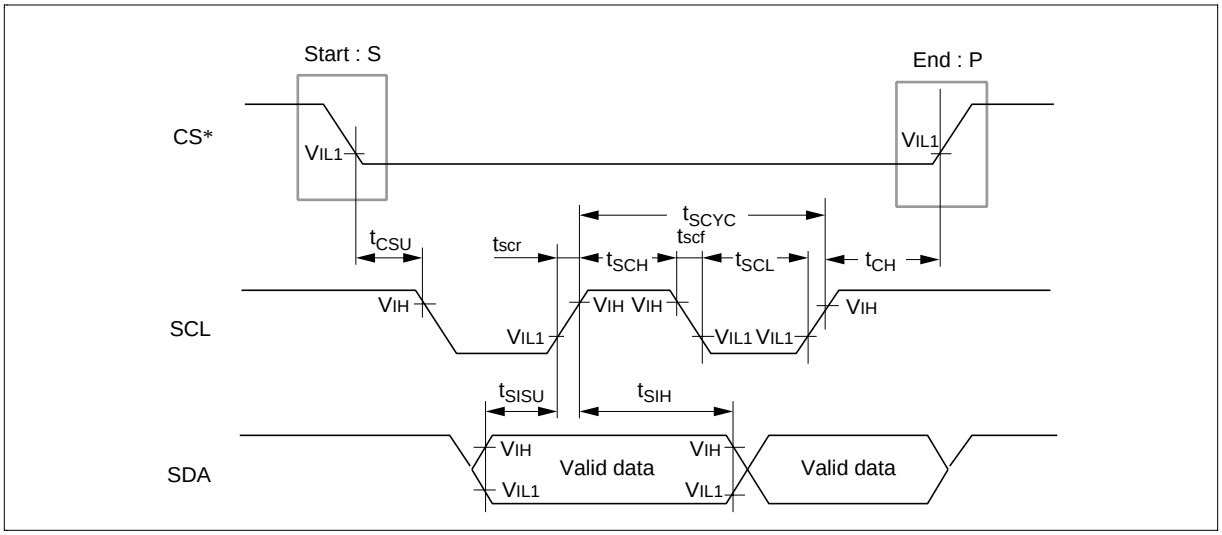


Figure 70 Clock Synchronized Serial Interface Input Timing

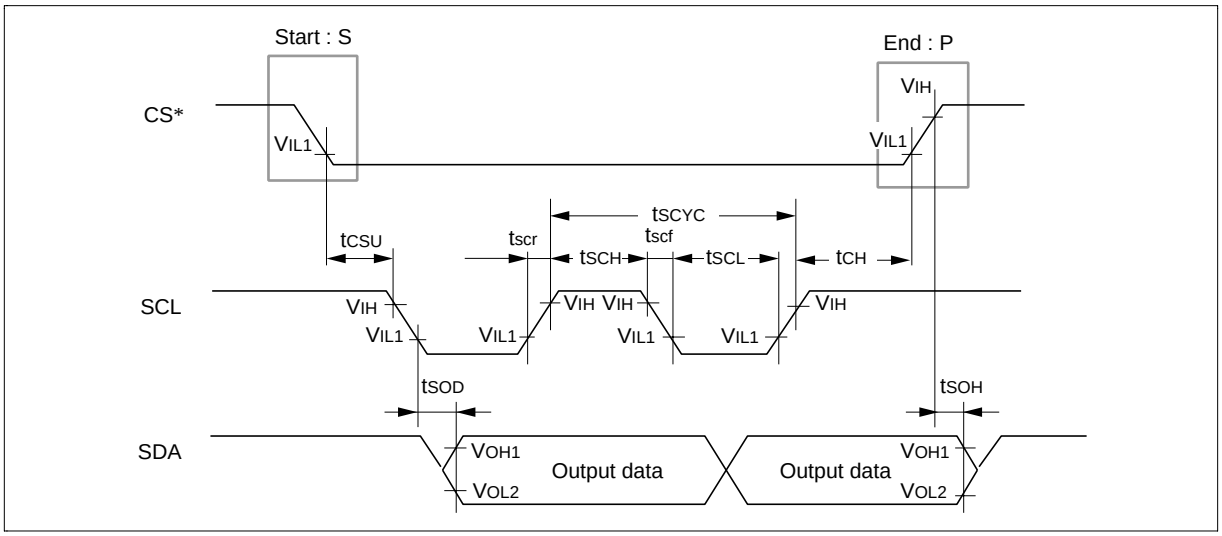


Figure 71 Clock Synchronized Serial Interface Output Timing

I2C Bus Interface Operation

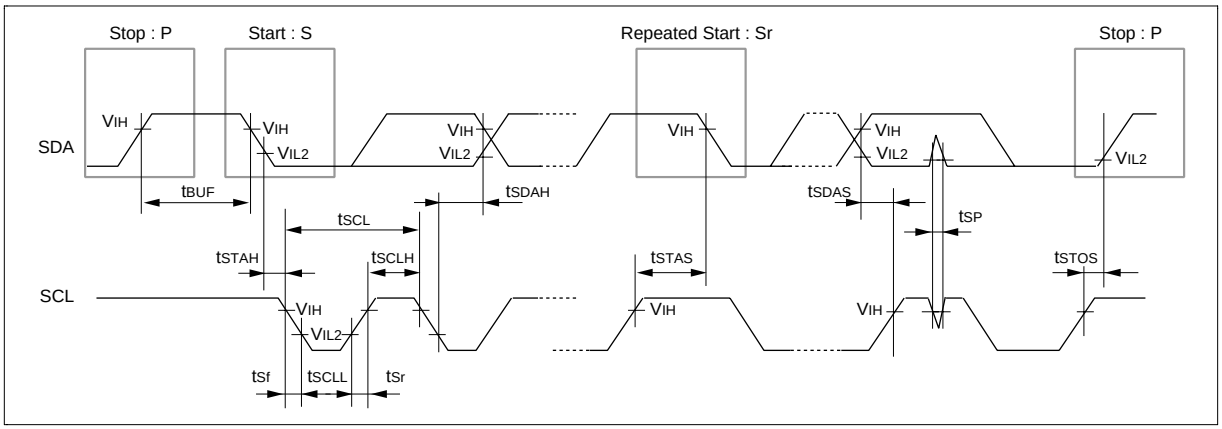


Figure 72 I2C Bus Interface Timing

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