

# LH5P832

## CMOS 256K (32K × 8) Pseudo-Static RAM

### FEATURES

- 32,768 × 8 bit organization
- Access time: 100/120 ns (MAX.)
- Cycle time: 160/190 ns (MIN.)
- Power consumption:
  - Operating: 357.5/303 mW
  - Standby: 16.5 mW
- TTL compatible I/O
- 256 refresh cycle/4 ms
- Auto refresh is executed by internal counter (controlled by OE/RFSH pin)
- Self refresh is executed by internal timer
- Single +5 V power supply
- Packages:
  - 28-pin, 600-mil DIP
  - 28-pin, 300-mil SK-DIP
  - 28-pin, 450-mil SOP

### DESCRIPTION

The LH5P832 is a 256K bit Pseudo-Static RAM organized as 32,768 × 8 bits. It is fabricated using silicon-gate CMOS process technology.

The LH5P832 uses convenient on-chip refresh circuitry with a DRAM memory cell for pseudo static operation. This simplifies external clock inputs, while providing the same simple, non-multiplexed pinout as industry standard SRAMs. Moreover, due to the functional similarities between PSRAMs and SRAMs, many 32K × 8 SRAM sockets can be filled with the LH5P832 with little or no changes. The advantage is the cost savings realized with the lower cost PSRAM.

The LH5P832 PSRAM has the ability to fill the gap between DRAM and SRAM by offering low cost, low standby power, and a simple interface.

Three methods of refresh control are provided for maximum versatility. A 'CE-Only' refresh cycle refreshes the addressed row of memory cells transparently. All 256 rows must be refreshed or accessed every four milliseconds. 'Auto Refresh' automatically cycles through a different row on every OE/RFSH clock pulse, accomplishing the row refreshes without the need to supply row addresses externally. 'Self Refresh' further simplifies the refresh requirements by eliminating the need for address inputs and clock pulses entirely. An automatic timer senses time periods when memory accesses have ceased, and provides full refresh of all rows of memory without any external assistance.

### PIN CONNECTIONS

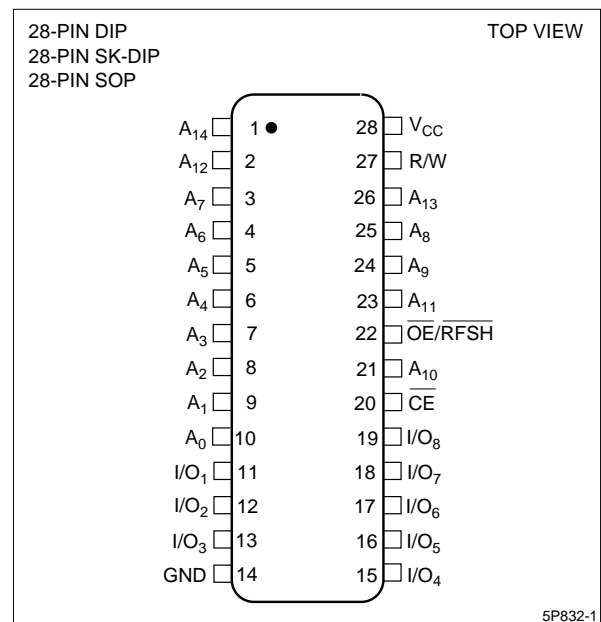


Figure 1. Pin Connections for DIP, SK-DIP, and SOP Packages

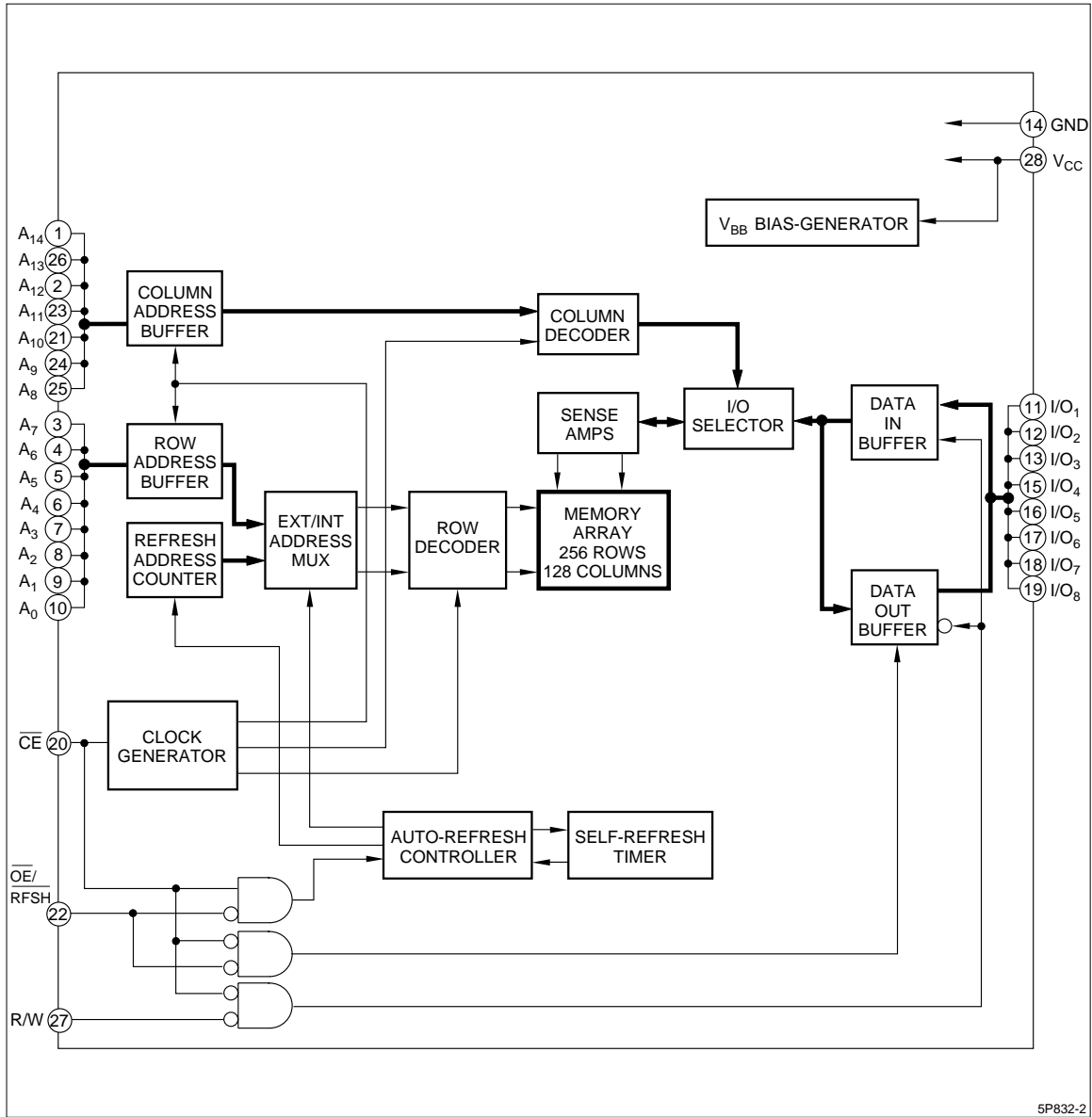


Figure 2. LH5P832 Block Diagram

**PIN DESCRIPTION**

SIGNAL	PIN NAME
R/W	Read/Write input
OE/RFSH	Output Enable/Refresh input
I/O <sub>1</sub> - I/O <sub>8</sub>	Data inputs and outputs
A <sub>0</sub> - A <sub>7</sub>	Row address inputs

SIGNAL	PIN NAME
A <sub>8</sub> - A <sub>14</sub>	Column Address inputs
CE	Chip Enable input
V <sub>CC</sub>	Power supply
GND	Ground

**TRUTH TABLE**

CE	R/W	OE/RFSH	MODE	I/O <sub>1</sub> - I/O <sub>8</sub>	I <sub>CC</sub>	NOTE
L	L	X	Write	Data in	Operating (I <sub>CC1</sub> )	1
L	H	L	Read	Data out	Operating (I <sub>CC1</sub> )	
L	H	H	CE-Only Refresh	High-Z	Operating (I <sub>CC1</sub> )	
H	X	L	Auto Refresh	High-Z	Operating (I <sub>CC1</sub> )	1, 2
H	X	L	Self Refresh	High-Z	Self Refresh (I <sub>CC3</sub> )	1, 3
H	X	H	Standby	High-Z	Standby (I <sub>CC2</sub> )	1

**NOTES:**

- X = H or L
- OE Pulsewidth < 8 μs
- OE Pulsewidth ≥ 8 μs

**ABSOLUTE MAXIMUM RATINGS**

PARAMETER	SYMBOL	RATING	UNIT	NOTE
Applied voltage on any pin	$V_T$	-1.0 to +7.0	V	1
Output short circuit current	$I_O$	50	mA	
Power dissipation	$P_D$	600	mW	
Operating temperature	$T_{opr}$	0 to +70	°C	
Storage temperature	$T_{stg}$	-55 to +150	°C	

**NOTE:**

1. Referenced to GND

**RECOMMENDED OPERATING CONDITIONS ( $T_A = 0$  to +70°C)**

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage	$V_{CC}$	4.5	5.0	5.5	V
Input voltage	$V_{IH}$	2.4		$V_{CC} + 0.3$	V
	$V_{IL}$	-1.0		+0.8	V

**CAPACITANCE ( $V_{CC} = 5.0$  V ±10%,  $T_A = 0$  to +70°C,  $f = 1$  MHz)**

PARAMETER	CONDITIONS	SYMBOL	MIN.	MAX.	UNIT
Input capacitance	$A_0 - A_{14}$ , R/W	$C_{IN1}$		8	pF
	CE, OE/RFSH	$C_{IN2}$		5	pF
Input/output capacitance	$I/O_1 - I/O_8$	$C_{OUT1}$		12	pF

**DC CHARACTERISTICS ( $V_{CC} = 5$  V ±10%,  $T_A = 0$  to +70°C)**

PARAMETER	SYMBOL	CONDITIONS	MIN.	MAX.	UNIT	NOTE
Operating current	$I_{CC1}$	$t_{RC} = 160$ ns		65	mA	1, 2
Operating current	$I_{CC1}$	$t_{RC} = 190$ ns		55	mA	1, 2
Standby current	$I_{CC2}$	CE = $V_{IH}$ , OE/RFSH = $V_{IH}$		3	mA	1
Self refresh average current	$I_{CC3}$	CE = $V_{IH}$ , OE/RFSH = $V_{IL}$		3	mA	1
CPU internal cycle average current	$I_{CC4}$	$t_{RC} = 160$ ns		65	mA	1, 2
CPU internal cycle average current	$I_{CC4}$	$t_{RC} = 190$ ns		55	mA	1, 2
Input leakage current	$I_{LI}$	$0$ V ≤ $V_{IN}$ ≤ 6.5 V	-10	10	μA	
Output leakage current	$I_{LO}$	$0$ V ≤ $V_{OUT}$ ≤ $V_{CC} + 0.3$ V	-10	10	μA	3
Output High voltage	$V_{OH}$	$I_{OUT} = -1$ mA	2.4		V	
Output Low voltage	$V_{OL}$	$I_{OUT} = 4$ mA		0.4	V	

**NOTES:**

1. Specified values are with outputs open.
2.  $I_{CC1}$  and  $I_{CC4}$  depend on the cycle time.
3. The output pins are in high-impedance state.

**AC TEST CONDITIONS**

PARAMETER	MODE	NOTE
Input voltage amplitude	0.6 to 2.4 V	
Input rise/fall time	5 ns	
Timing reference level	1.5 V	
Output load conditions	1TTL gate, $C_L = 100$ pF	1

**NOTE:**

1. Includes scope and jig capacitance.

## AC CHARACTERISTICS

READ AND WRITE CYCLES <sup>1,2</sup> ( $V_{CC} = 5.0 \text{ V} \pm 10\%$ ,  $T_A = 0 \text{ to } 70^\circ\text{C}$ )

PARAMETER	SYMBOL	160 ns		190 ns		UNIT	NOTE
		MIN.	MAX.	MIN.	MAX.		
Random read, write cycle time	$t_{RC}$	160		190		ns	
Read modify write cycle time	$t_{RMW}$	225		280		ns	
CE pulse width	$t_{CE}$	100	10,000	120	10,000	ns	
CE precharge time	$t_P$	50		60		ns	
Address setup time	$t_{AS}$	0		0		ns	
Address hold time	$t_{AH}$	20		30		ns	
Read command hold time	$t_{RCH}$	0		0		ns	
Read command setup time	$t_{RCS}$	0		0		ns	
CE access time	$t_{CEA}$		100		120	ns	3
OE access time	$t_{OEA}$		40		50	ns	3
CE to output in Low-Z	$t_{CLZ}$	10		10		ns	
OE to output in Low-Z	$t_{OLZ}$	0		0		ns	
Output enable from end of write	$t_{WLZ}$	0		0		ns	
Chip disable to output in High-Z	$t_{CHZ}$	0	30	0	35	ns	2
Output disable to output in High-Z	$t_{OHZ}$	0	30	0	35	ns	2
Write enable to output in High-Z	$t_{WHZ}$	0	30	0	35	ns	2
$\overline{OE}$ setup time	$t_{OES}$	10		10		ns	
OE hold time	$t_{OEH}$	0		0		ns	
OE lead time	$t_{OEL}$	10		10		ns	
Write command pulse width	$t_{WCP}$	60		85		ns	
Write command setup time	$t_{WCS}$	60		85		ns	
Write command hold time	$t_{WCH}$	60		85		ns	
Data setup time from write	$t_{DSW}$	40		50		ns	
Data setup time from $\overline{CE}$	$t_{DSC}$	40		50		ns	
Data hold time from write	$t_{DHW}$	0		0		ns	
Data hold time from $\overline{CE}$	$t_{DHC}$	0		0		ns	
Transition time (rise and fall)	$t_T$	3	35	3	35	ns	
Refresh time interval	$t_{REF}$		4		4	ms	

## REFRESH CYCLE

Auto refresh cycle time	$t_{FC}$	160		190		ns	
Refresh delay time from $\overline{CE}$	$t_{RFD}$	50		60		ns	
Refresh pulse width (Auto refresh)	$t_{FAP}$	60	8,000	80	8,000	ns	
Refresh precharge time (Auto refresh)	$t_{FP}$	30		30		ns	
CE delay time from refresh active (Auto refresh)	$t_{FCE}$	190		225		ns	
Refresh pulse width (Self refresh)	$t_{FAS}$	8,000		8,000		ns	
CE delay time from refresh precharge (Self refresh)	$t_{FRS}$	190		225		ns	

## NOTES:

- At least 200  $\mu\text{s}$  of pause time after power on should be given for proper device operation.  
CE and OE/RFSH must be fixed at  $V_{IH}$  for 200  $\mu\text{s}$  from the  $V_{DD}$  reached to the specified voltage level and followed by at least 8 dummy cycles.
- AC characteristics are measured at  $t_T = 5 \text{ ns}$ .
- Measured with a load circuit equivalent to 1TTL loads and 100 pF.

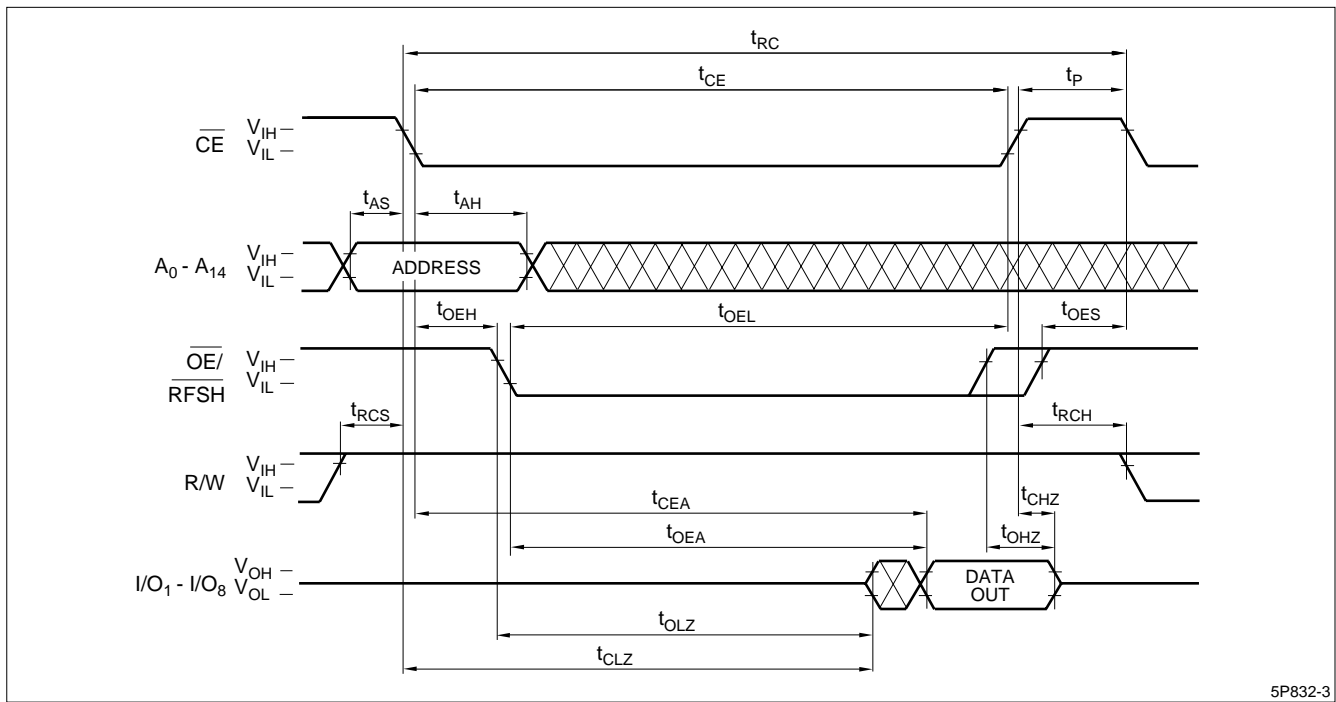


Figure 3. Read Cycle

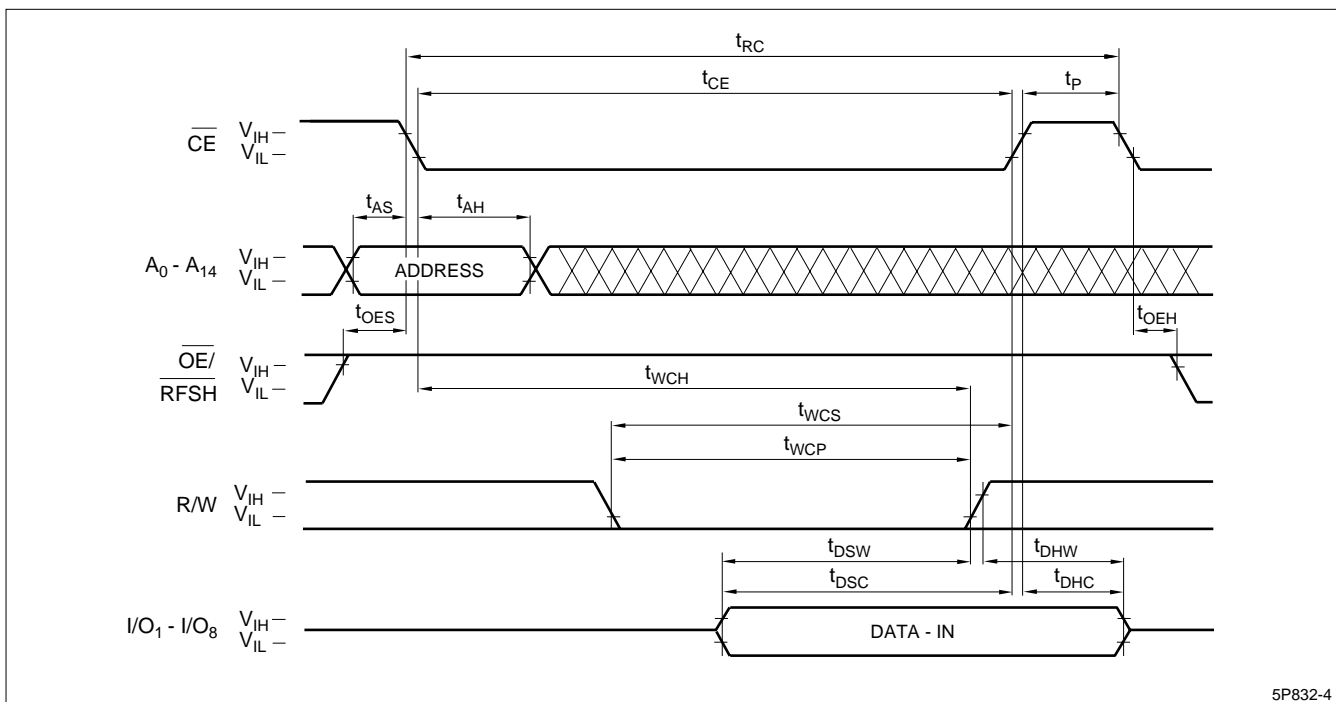
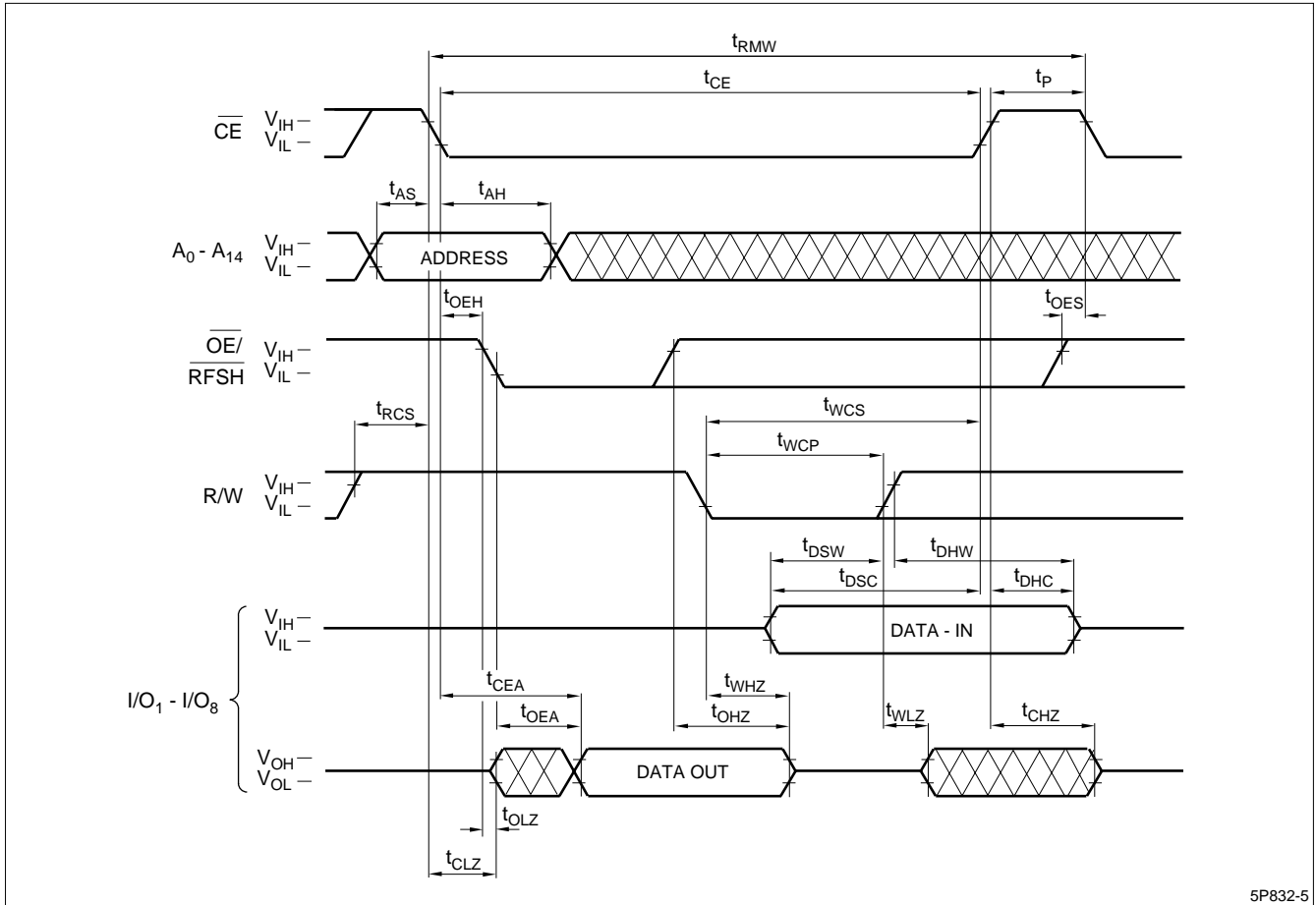
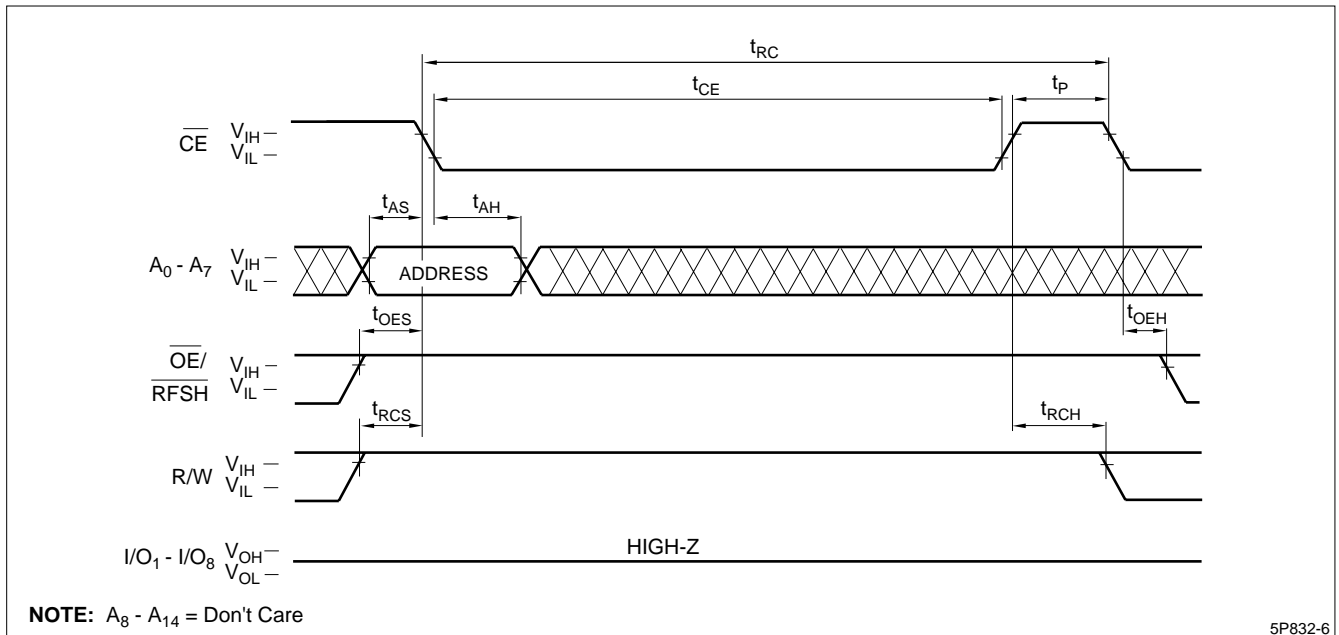


Figure 4. Write Cycle



5P832-5

Figure 5. Read/Write Cycle



NOTE:  $A_8 - A_{14} = \text{Don't Care}$

5P832-6

Figure 6.  $\overline{CE}$  Only Refresh Cycle

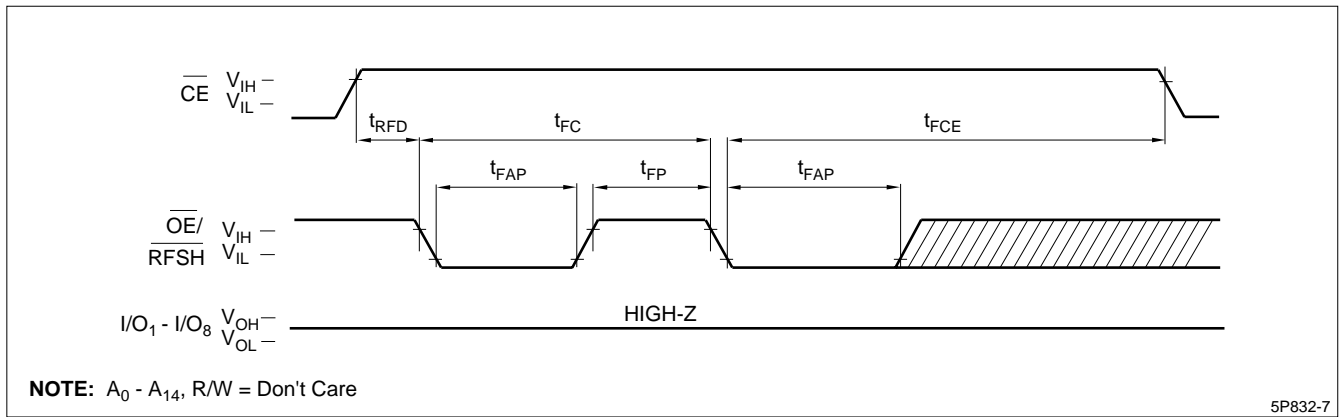


Figure 7. Auto Refresh Cycle

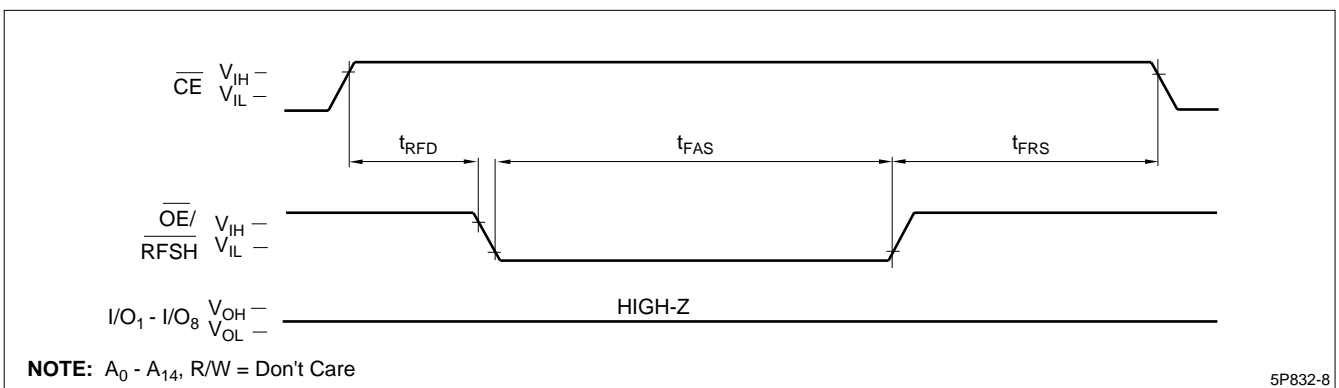
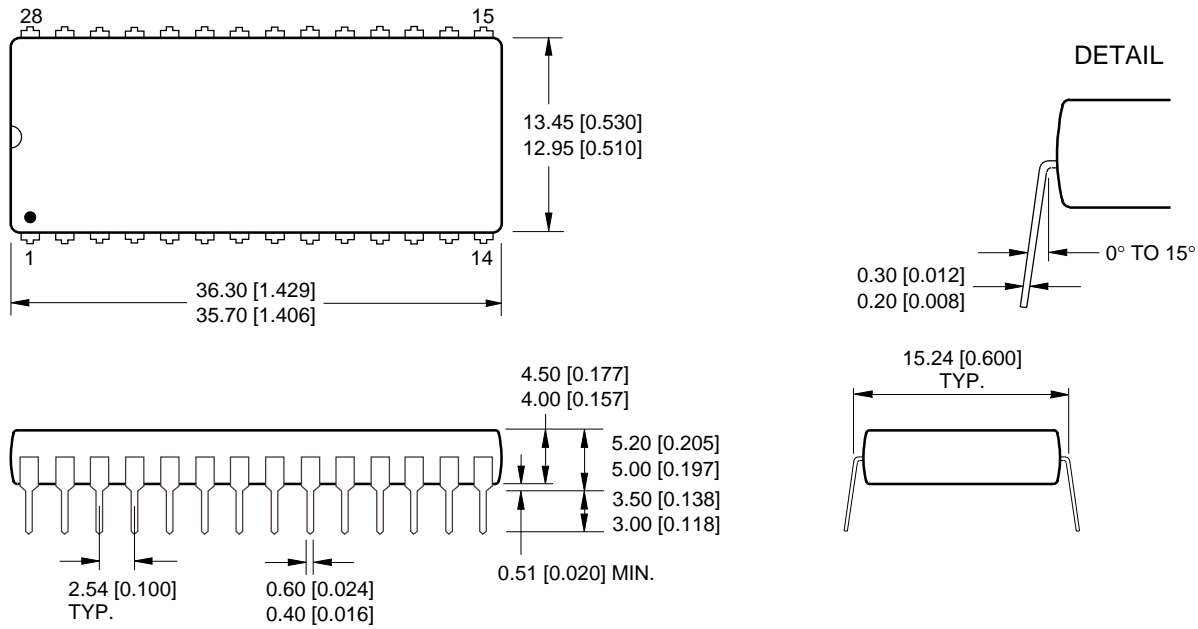


Figure 8. Self Refresh Cycle

PACKAGE DIAGRAMS

28DIP (DIP028-P-0600)

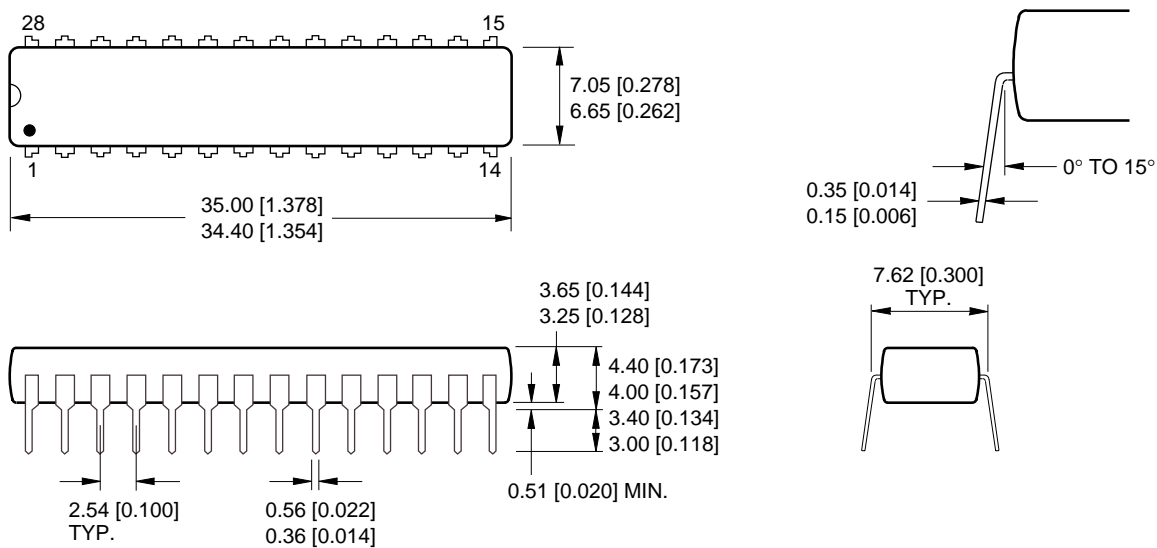


DIMENSIONS IN MM [INCHES]    MAXIMUM LIMIT  
MINIMUM LIMIT

28DIP-2

28-Pin, 600-mil DIP

28SK-DIP (DIP028-P-0300)

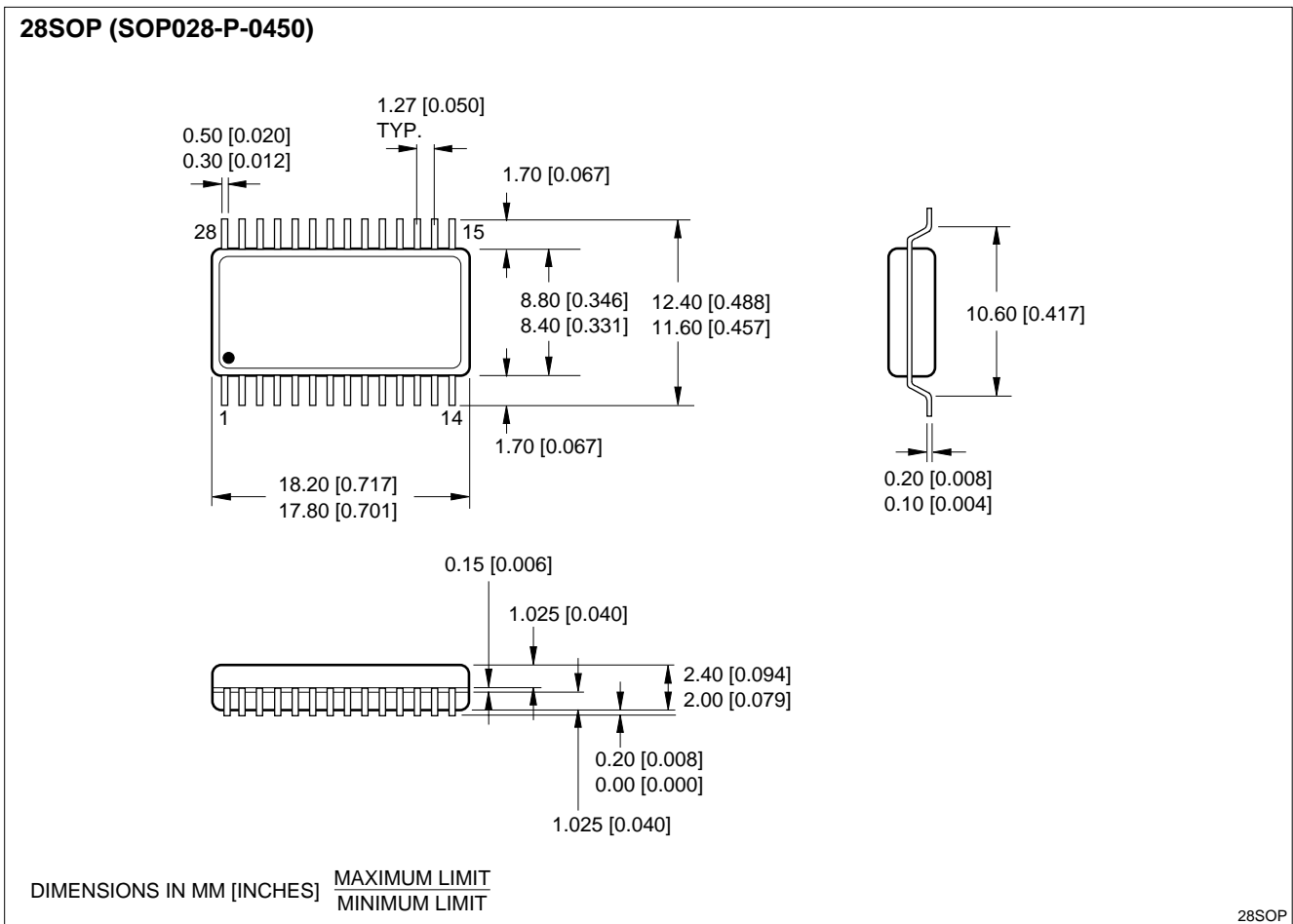


DIMENSIONS IN MM [INCHES]    MAXIMUM LIMIT  
MINIMUM LIMIT

28DIP-1

28-Pin, 300-mil SK-DIP





**28-Pin, 450-mil SOP**

**ORDERING INFORMATION**

