

# I<sup>2</sup>C Bus Compatible Video Switch Monolithic IC MM1250

May 18, 1994

## Outline

This IC is an I<sup>2</sup>C bus compatible audio/video switch IC for TVs.

## Features

1. Utilizes serial control by I<sup>2</sup>C bus
2. Provides 3 video input channels and obtains 3 channel outputs of V<sub>OUT</sub>, Y<sub>OUT</sub> and C<sub>OUT</sub>
3. Includes a 6dB amp in the V<sub>OUT</sub> channel
4. Includes an output clamp circuit in the V<sub>OUT</sub> channel
5. Includes a mute function in the Audio channel
6. Includes one channel of an output port
7. Operating supply voltage range                      8~13V
8. Video frequency response                                10MHz
9. Slave address    92H (fixed)

## Package

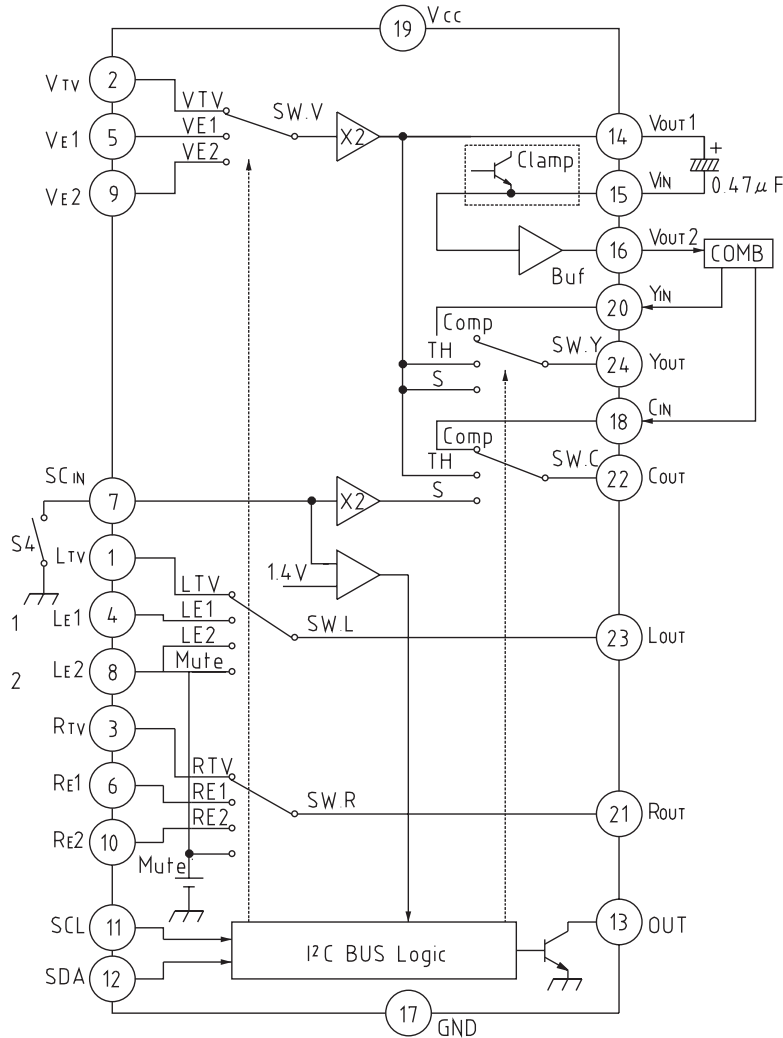
SDIP-24A (MM1250XD)

## Applications

I<sup>2</sup>C bus compatible televisions, etc.

Block Diagram

Fig. 1 Block Diagram



Absolute Maximum Ratings (Ta=25°C)

Item	Symbol	Ratings	Units
Storage temperature	T <sub>STG</sub>	-40~+125	°C
Operating temperature	T <sub>OPR</sub>	-20~+75	°C
Power supply voltage	V <sub>CC</sub>	15	V
Allowable loss	P <sub>d</sub>	1000	mW

**Electrical Characteristics** (Except where noted otherwise, Ta=25°C, Vcc=8V~13V)

Item	Symbol	Measurement circuit	Measurement conditions	Min.	Typ.	Max.	Units
Operating power supply voltage	V <sub>CC</sub>	V <sub>CC</sub>		8.0		13.0	V
Consumption current	I <sub>CC</sub>		V <sub>CC</sub> =9V	17	25	33	mA
<b>V<sub>OUT</sub> output</b>							
Voltage gain	G <sub>V1</sub>	TP9	SG1 : sine wave 1V <sub>P-P</sub> , 0.1MHz	5.5	6.0	6.5	dB
	G <sub>V2</sub>	TP7					
Frequency characteristic	F <sub>V1</sub>	TP9	SG1 : sweep signal, 1V <sub>P-P</sub> 10MHz/0.1MHz	-1.0	0	1.0	dB
	F <sub>V2</sub>	TP7					
Differential gain	DG <sub>V1</sub>	TP9	SG1 : staircase wave, 1V <sub>P-P</sub> APL=10, 50, 90%	-3	0	3	%
	DG <sub>V2</sub>	TP8					
Differential phase	DP <sub>V1</sub>	TP9	SG1 : staircase wave, 1V <sub>P-P</sub> APL=10, 50, 90%	-3	0	3	deg
	DP <sub>V2</sub>	TP8					
Input dynamic	D <sub>V1</sub>	TP9	SG1 : range sine wave, 1kHz	2.1			V <sub>P-P</sub>
	D <sub>V2</sub>	TP8					
Output offset voltage	V <sub>OFFV</sub>	TP9	V <sub>OUT1</sub> pin DC level difference during switching		0	±30	mV
Input impedance	Z <sub>IV</sub>		V <sub>TV</sub> , V <sub>E1</sub> , V <sub>E2</sub>	10	15	20	kΩ
Output impedance	Z <sub>OV2</sub>			10	20	30	Ω
<b>Y<sub>OUT</sub> output</b>							
Voltage gain	G <sub>Y1</sub>	TP1	SG1 : sine wave, 1V <sub>P-P</sub> , 0.1MHz	5.5	6.0	6.5	dB
	G <sub>Y2</sub>	TP1	SG6 : sine wave, 2V <sub>P-P</sub> , 0.1MHz	-0.5	0	0.5	dB
Frequency characteristic	F <sub>Y1</sub>	TP1	SG1 : sweep signal, 1V <sub>P-P</sub> 10MHz/0.1MHz	-1.0	0	1.0	dB
	F <sub>Y2</sub>	TP1	SG6 : sweep signal, 2V <sub>P-P</sub> 10MHz/0.1MHz	-1.0	0	1.0	dB
Differential gain	DG <sub>Y</sub>	TP2	SG1 : staircase wave, 1V <sub>P-P</sub> APL=10, 50, 90%	-3	0	3	%
Differential phase	DP <sub>Y</sub>	TP2	SG1 : staircase wave, 1V <sub>P-P</sub> APL=10, 50, 90%	-3	0	3	deg
Input dynamic range	D <sub>Y1</sub>	TP1	SG6 : sine wave, 1kHz, Comp mode	4.2			V <sub>P-P</sub>
	D <sub>Y2</sub>	TP1	SG1 : sine wave, 1kHz, TH·S mode	2.1			
Output offset voltage	V <sub>OFFY</sub>	TP1	Y <sub>OUT1</sub> pin DC level difference during switching		0	±30	mV
Input impedance	Z <sub>IY</sub>		Y <sub>IN</sub>	10	15	20	kΩ
Output impedance	Z <sub>OY</sub>			8	15	22	Ω
<b>C<sub>OUT</sub> output</b>							
Voltage gain	G <sub>C1</sub>	TP4	SG1 : sine wave, 1V <sub>P-P</sub> , 0.1MHz	5.5	6.0	6.5	dB
	G <sub>C2</sub>	TP4	SG2 : sine wave, 1V <sub>P-P</sub> , 0.1MHz	5.5	6.0	6.5	dB
	G <sub>C3</sub>	TP4	SG5 : sine wave, 2V <sub>P-P</sub> , 0.1MHz	-0.5	0	0.5	dB
Frequency characteristic	F <sub>C1</sub>	TP4	SG1 : sweep signal, 1V <sub>P-P</sub> , 10MHz/0.1MHz	-1.0	0	1.0	dB
	F <sub>C2</sub>	TP4	SG2 : sweep signal, 1V <sub>P-P</sub> , 10MHz/0.1MHz	-1.0	0	1.0	dB
	F <sub>C3</sub>	TP4	SG5 : sweep signal, 2V <sub>P-P</sub> , 10MHz/0.1MHz	-1.0	0	1.0	dB
Differential gain	DG <sub>C</sub>	TP5	SG1 : staircase wave, 1V <sub>P-P</sub> APL=10, 50, 90%	-3	0	3	%
Differential phase	DP <sub>C</sub>	TP5	SG1 : staircase wave, 1V <sub>P-P</sub> APL=10, 50, 90%	-3	0	3	deg
Input dynamic range	D <sub>C1</sub>	TP4	SG5 : sine wave, 1kHz, COMP mode	4.2			V <sub>P-P</sub>
	D <sub>C2</sub>	TP4	SG1 : sine wave, 1kHz, TH mode	2.1			
	D <sub>C3</sub>	TP4	SG2 : sine wave, 1kHz, S mode	2.1			
Output offset voltage	V <sub>OFFC</sub>	TP4	C <sub>OUT1</sub> pin DC level difference during switching		0	±30	mV
Input impedance	Z <sub>IC</sub>		C <sub>IN</sub>	10	15	20	kΩ
Output impedance	Z <sub>OC</sub>			8	15	22	Ω

Item	Symbol	Measurement circuit	Measurement conditions	Min.	Typ.	Max.	Units
<b>R<sub>OUT</sub> output</b>							
Voltage gain	G <sub>R</sub>	TP6	sine wave, 2.5V <sub>P-P</sub> , 1kHz	-0.5	0	0.5	dB
Total harmonic distortion	THD <sub>R</sub>	TP6	sine wave, 2.5V <sub>P-P</sub> , 1kHz		0.01	0.1	%
Output noise voltage	V <sub>NR</sub>	TP6	band 15kHz (except during mute)		3	30	μVrms
Mute noise	V <sub>M1</sub>	TP6	during mute		200	600	μVrms
Input dynamic range	D <sub>R</sub>	TP6	SG3 : sine wave, 1kHz, total higher harmonic distortion rate=0.5%	2.0			Vrms
Output offset voltage	V <sub>OFFR</sub>	TP6	R <sub>OUT</sub> pin DC level difference during switching		0	±15	mV
Input impedance	Z <sub>IR1</sub>		R <sub>TV</sub>	22	30	38	kΩ
	Z <sub>IR2</sub>		R <sub>E1</sub> , R <sub>E2</sub>	50	68	86	kΩ
Output impedance	Z <sub>OR</sub>			60	80	100	Ω
<b>L<sub>OUT</sub> output</b>							
Voltage gain	G <sub>L</sub>	TP3	sine wave, 2.5V <sub>P-P</sub> , 1kHz	-0.5	0	0.5	dB
Total harmonic distortion	THD <sub>L</sub>	TP3	sine wave, 2.5V <sub>P-P</sub> , 1kHz		0.01	0.1	%
Output noise voltage	V <sub>NL</sub>	TP3	band 15kHz (except during mute)		3	50	μVrms
Mute noise	V <sub>M2</sub>	TP3	during mute		200	600	μVrms
Input dynamic range	D <sub>L</sub>	TP3	SG3 : sine wave, 1kHz, total higher harmonic distortion rate=0.5%	2.0			Vrms
Output offset voltage	V <sub>OFFL</sub>	TP3	L <sub>OUT</sub> pin DC level difference during switching		0	±15	mV
Input impedance	Z <sub>IL1</sub>		L <sub>TV</sub>	22	30	38	kΩ
	Z <sub>IL2</sub>		L <sub>E1</sub> , L <sub>E2</sub>	50	68	86	kΩ
Output impedance	Z <sub>OL</sub>			60	80	100	Ω
<b>OUT output</b>							
Output voltage L	V <sub>OL</sub>	TP10	Bit4=0			0.4	V
<b>Crosstalk</b>							
V <sub>OUT2</sub>	CT <sub>V</sub>	TP7	4.43MHz *1		-70	-60	dB
Y <sub>OUT</sub>	CT <sub>Y</sub>	TP1	4.43MHz *2		-70	-60	dB
C <sub>OUT</sub>	CT <sub>C</sub>	TP4	4.43MHz *3		-70	-60	dB
R <sub>OUT</sub>	CT <sub>R</sub>	TP6	2.5V <sub>P-P</sub> , 1kHz		-80	-70	dB
L <sub>OUT</sub>	CT <sub>L</sub>	TP3	2.5V <sub>P-P</sub> , 1kHz		-80	-70	dB
<b>Pin DC voltage</b>							
1 pin voltage	Vt1		V <sub>CC</sub> =9.0V, SG1~6=no signal	4.8	5.3	5.8	V
2 pin voltage	Vt2		V <sub>CC</sub> =9.0V, SG1~6=no signal	4.1	4.6	5.1	V
3 pin voltage	Vt3		V <sub>CC</sub> =9.0V, SG1~6=no signal	4.8	5.3	5.8	V
4 pin voltage	Vt4		V <sub>CC</sub> =9.0V, SG1~6=no signal	4.8	5.3	5.8	V
5 pin voltage	Vt5		V <sub>CC</sub> =9.0V, SG1~6=no signal	4.1	4.6	5.1	V
6 pin voltage	Vt6		V <sub>CC</sub> =9.0V, SG1~6=no signal	4.8	5.3	5.8	V
7 pin voltage	Vt7		V <sub>CC</sub> =9.0V, SG1~6=no signal, S4=B	4.1	4.6	5.1	V
8 pin voltage	Vt8		V <sub>CC</sub> =9.0V, SG1~6=no signal	4.8	5.3	5.8	V
9 pin voltage	Vt9		V <sub>CC</sub> =9.0V, SG1~6=no signal	4.1	4.6	5.1	V
10 pin voltage	Vt10		V <sub>CC</sub> =9.0V, SG1~6=no signal	4.8	5.3	5.8	V
11 pin voltage	Vt13		V <sub>CC</sub> =9.0V, SG1~6=no signal, BIT4=0		0.2	0.4	V
12 pin voltage	Vt14		V <sub>CC</sub> =9.0V, SG1~6=no signal	4.1	4.6	5.1	V
13 pin voltage	Vt15		V <sub>CC</sub> =9.0V, SG1~6=no signal	3.5	4.0	4.5	V
14 pin voltage	Vt16		V <sub>CC</sub> =9.0V, SG1~6=no signal	2.1	2.6	3.1	V
15 pin voltage	Vt17		V <sub>CC</sub> =9.0V, SG1~6=no signal		0		V
16 pin voltage	Vt18		V <sub>CC</sub> =9.0V, SG1~6=no signal	4.1	4.6	5.1	V
17 pin voltage	Vt19		V <sub>CC</sub> =9.0V, SG1~6=no signal		9		V
18 pin voltage	Vt20		V <sub>CC</sub> =9.0V, SG1~6=no signal	4.1	4.6	5.1	V
19 pin voltage	Vt21		V <sub>CC</sub> =9.0V, SG1~6=no signal	4.1	4.6	5.1	V
20 pin voltage	Vt22		V <sub>CC</sub> =9.0V, SG1~6=no signal	3.4	3.9	4.4	V
21 pin voltage	Vt23		V <sub>CC</sub> =9.0V, SG1~6=no signal	4.1	4.6	5.1	V
22 pin voltage	Vt24		V <sub>CC</sub> =9.0V, SG1~6=no signal	3.4	3.9	4.4	V

**I<sup>2</sup>C Bus Recommended Operating Conditions** (Refer to diagram below)

Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Units
Input voltage L	V <sub>IL</sub>	I <sup>2</sup> C logic low level discrimination value			0.7	V
Input voltage H	V <sub>IH</sub>	I <sup>2</sup> C logic high level discrimination value	2.1		5.0	V
Clock frequency	f <sub>SCL</sub>				100	kHz
Data transfer wait time	t <sub>BUF</sub>		4.7			μs
SCL start hold time	t <sub>HD:STA</sub>		4.0			μs
SCL low level hold time	t <sub>LOW</sub>		4.7			μs
SCL high level hold time	t <sub>HIGH</sub>		4.0			μs
SCL start setup time	t <sub>SU:STA</sub>		4.7			μs
SDA data hold time	t <sub>HD:DAT</sub>		5.0			μs
SDA data setup time	t <sub>SU:DAT</sub>		250			μs
SCL rise time	t <sub>r</sub>				1000	ns
SCL fall time	t <sub>f</sub>				300	ns
SCL stop setup time	t <sub>SU:STO</sub>		4.0			μs

Notes :

\*1 Crosstalk V<sub>OUT2</sub>

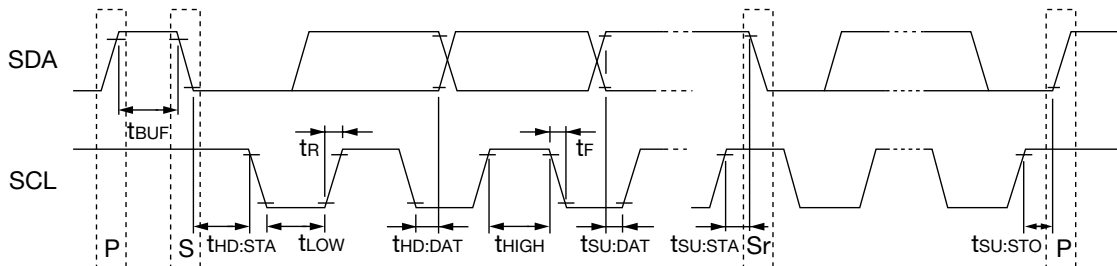
Input a 1V<sub>P-P</sub>, 4.43MHz sine wave to SG1.

Given S1=A, S5=A, S6~S10= B, Bit=011 and TP7 amplitude V01,

Combinations below : V02, then C<sub>TV</sub> is obtained as follows:

$$C_{TV} = 20 \log (V02/V01) \text{ dB}$$

**I<sup>2</sup>C Bus control signals**



Signal input	Input amplitude	Switch status								Control bit			
		S1	S4	S5	S6	S7	S8	S9	S10	Bit2	Bit1	Bit0	
SG1	1V <sub>P-P</sub>	A	A	A	B	B	B	B	B	-	0	1	
			B	A	B	B	B	B	B	-	1	0	
			-	A	B	B	B	B	B	-	1	0	
		B	-	B	A	B	B	B	B	B	-	1	1
			-	B	A	B	B	B	B	B	-	1	0
			-	B	B	B	A	B	B	B	-	1	1
			A	B	B	B	A	B	B	-	0	1	
B	B	B	B	A	B	B	-	0	1				
SG6	2V <sub>P-P</sub>	-	-	B	B	B	B	B	A	-	1	1	
SG5	2V <sub>P-P</sub>	-	-	B	B	B	B	A	B	-	1	1	
SG2	1V <sub>P-P</sub>	-	B	B	B	A	B	B	B	-	0	1	

\*2 Crosstalk  $Y_{OUT}$

Input a  $1V_{P-P}$ , 4.43MHz sine wave to SG1.

Given  $S1=A$ ,  $S5=A$ ,  $S6\sim S10=B$ , Bit=111 and TP1 amplitude  $V03$ ,

Combinations below :  $V04$ , then  $C_{TY}$  is obtained as follows:

$$C_{TY}=20\log (V04/V03) \text{ dB}$$

Signal input	Input amplitude	Switch status								Control bit		
		S1	S4	S5	S6	S7	S8	S9	S10	Bit2	Bit1	Bit0
SG1	$1V_{P-P}$	A	-	A	B	B	B	B	B	0	1	1
SG6	$2V_{P-P}$	-	B	B	B	B	B	B	A	0	0	1
		-	-	B	B	B	B	B	A	1	1	1
SG5	$2V_{P-P}$	-	-	B	B	B	B	A	B	-	1	1
SG2	$1V_{P-P}$	-	-	B	B	A	B	B	B	-	1	1

\*3 Crosstalk  $C_{OUT}$

Input a  $1V_{P-P}$ , 4.43MHz sine wave to SG1.

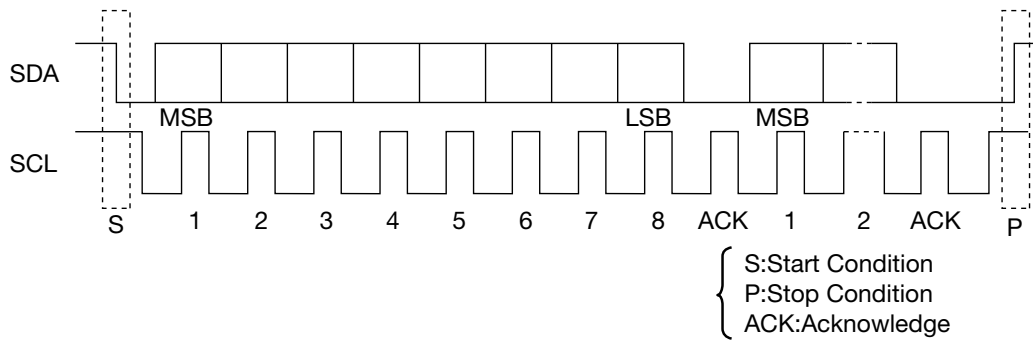
Given  $S1=A$ ,  $S5=A$ ,  $S6\sim S10=B$ , Bit=111 and TP5 amplitude  $V05$ ,

Combinations below :  $V06$ , then  $C_{TC}$  is obtained as follows:

$$C_{TC}=20\log (V06/V05) \text{ dB}$$

Signal input	Input amplitude	Switch status								Control bit		
		S1	S4	S5	S6	S7	S8	S9	S10	Bit2	Bit1	Bit0
SG1	$1V_{P-P}$	A	-	A	B	B	B	B	B	0	1	1
		B	B	B	A	B	B	B	B	-	0	1
SG6	$2V_{P-P}$	-	-	B	B	B	B	B	A	-	1	1
		-	B	B	B	B	B	B	A	-	0	1
SG5	$2V_{P-P}$	-	B	B	B	B	B	A	B	-	0	1
		-	-	B	B	B	B	A	B	1	1	1
SG2	$1V_{P-P}$	-	-	B	B	A	B	B	B	-	1	1

I<sup>2</sup>C Bus



The I<sup>2</sup>C bus (Inter IC Bus) is a bus system developed by Philips.  
 Data is transferred on two lines, SDA and SCL.  
 Data is transferred in byte units, and MSB is first from start condition.

1. Data format

S	Slave address							R/W	A	Control bits								A	P
	1	0	0	1	0	0	1	0		Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0		
Address byte									Control byte										

The first 7 bits of the address byte is the slave address, and the last bit is allocated as R/W bit. On MM1250XD, 92<sub>H</sub> is used for the slave address and 0 (write only) for the R/W bit.  
 The A at the 9th bit is an acknowledge signal added for verification from slave.

2. Control byte format

Control byte configuration on MM1250XD is allocated as shown in the table below.  
 Each bit is set at "0" when power is turned on.

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	
×	×	×	OUT	Mute	SW2	SW1	SW0	×: Don't Care

SW V, L, R control

Control		Control results			
SW1	SW0	MODE1	V <sub>OUT</sub>	L <sub>OUT</sub>	R <sub>OUT</sub>
0	0	TV	V <sub>TV</sub>	L <sub>TV</sub>	R <sub>TV</sub>
0	1	E1	V <sub>E1</sub>	L <sub>E1</sub>	R <sub>E1</sub>
1	0	E2	V <sub>E2</sub>	L <sub>E2</sub>	R <sub>E2</sub>
1	1	TV	V <sub>TV</sub>	L <sub>TV</sub>	R <sub>TV</sub>

SW Y, C control

Control			Control results		
MODE1	S4	SW2	Mode2	SW-Y	SW-C
TV	-	0	Comp	Y <sub>IN</sub>	C <sub>IN</sub>
E1	A	0	Comp	Y <sub>IN</sub>	C <sub>IN</sub>
	B	0	S	V <sub>E1</sub>	SC <sub>IN</sub>
E2	-	0	Comp	Y <sub>IN</sub>	C <sub>IN</sub>
TV	-	1	TH	V <sub>TV</sub>	V <sub>TV</sub>
E1	A	1	TH	V <sub>E1</sub>	V <sub>E1</sub>
	B	1	S	V <sub>E1</sub>	SC <sub>IN</sub>
E2	-	1	TH	V <sub>E2</sub>	V <sub>E2</sub>

Audio Mute control

Mute	L <sub>OUT</sub>	R <sub>OUT</sub>
0	SW-L	SW-R
1	Mute	Mute

Out Port control

OUT	Pin 13 status
0	Low
1	Open

Pin Description

Pin no.	Pin name	Internal equivalent circuit diagram	Pin no.	Pin name	Internal equivalent circuit diagram
1 3	L <sub>TV</sub> R <sub>TV</sub>		14	V <sub>out1</sub>	
2 5 7 9 18 20	V <sub>TV</sub> V <sub>E1</sub> S <sub>CIN</sub> V <sub>E2</sub> C <sub>IN</sub> Y <sub>IN</sub>		15	V <sub>IN</sub>	
4 6 8 10	L <sub>E1</sub> R <sub>E1</sub> L <sub>E2</sub> R <sub>E2</sub>		16	V <sub>out2</sub>	
11	SCL		17	GND	
12	SDA		19	V <sub>cc</sub>	
13	OUT		21 23	R <sub>out</sub> L <sub>out</sub>	
			22 24	C <sub>out</sub> Y <sub>out</sub>	



Measuring Circuit

