SONY

CXA3572R

Driver/Timing Generator for Color LCD Panels

Description

The CXA3572R is an IC designed to drive the color LCD panel ACX306/312.

This IC greatly reduces the number of peripheral circuits and parts by incorporating a RGB driver and timing generator for video signals and a VCO onto a single chip. This chip has a built-in serial interface circuit and electronic attenuators which allow various settings to be performed by microcomputer control, etc.

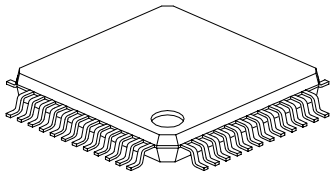
Features

- Color LCD panel ACX306/312 driver
- Supports NTSC and PAL systems
- Supports Y/color difference and RGB inputs
- Supports OSD input
- Power saving function (clock stopped)
- Various setting control using a serial interface circuit (asynchronous type)
- Electronic attenuators (D/A converter)
- VCO (no external oscillator circuit)
- LPF (fc variable)
- COMMON and PSIG output circuits
- Sharpness function
- 2-point γ correction circuit
- R, G, B signal delay time adjustment circuit
- Sync separation circuit
- D/A output pin (0 to 3V, 8 level output)
- Output polarity inversion circuit
- Supports AC drive for LCD panel during no signal

Applications

Compact LCD monitors, etc.

48 pin LQFP (Plastic)



Absolute Maximum Ratings (Ta = 25°C)

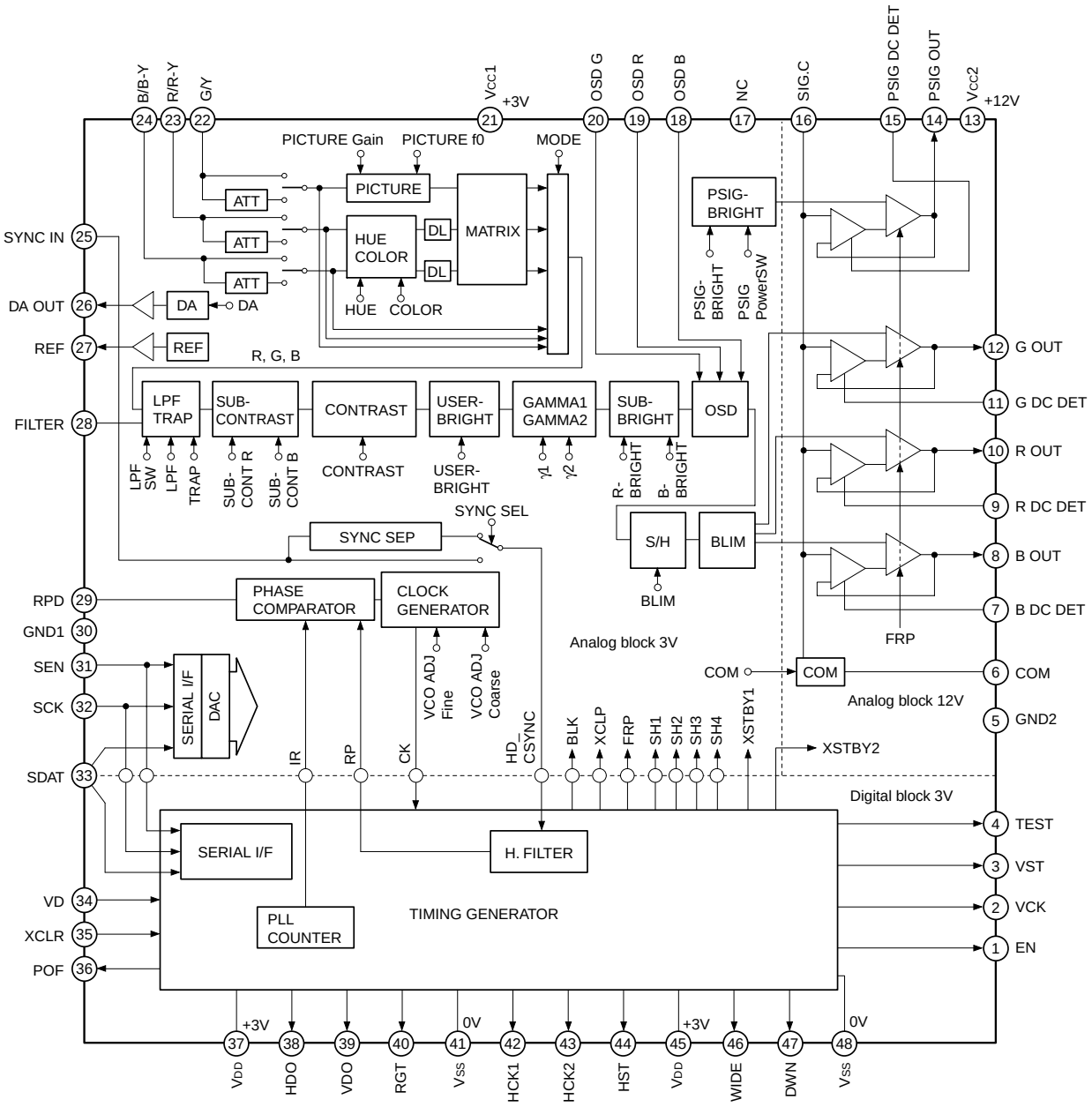
• Supply voltage	$V_{CC}1$	5.5	V
	$V_{CC}2$	15	V
	V_{DD}	4.6	V
• Analog input pin voltage			
VINA1 (Pins 18, 19, 20, 22, 23, 24 and 25)		GND – 0.3 to $V_{CC}1$ + 0.3	V
VINA2 (Pin 16)		GND – 0.3 to $V_{CC}2$ + 0.3	V
• Digital input pin voltage			
VIND (Pins 34 and 35)		V_{SS} – 0.3 to +5.5	V
• Common input pin voltage			
VINAD (Pins 31, 32 and 33)		GND, V_{SS} – 0.3 to +5.5	V
• Operating temperature	Topr	–15 to +75	°C
• Storage temperature	Tstg	–55 to +150	°C
• Allowable power dissipation (Ta ≤ 25°C)			
	P_D	600	mW

Operating Conditions

• Supply voltage	$V_{CC}1$ – GND1	2.7 to 3.6	V
	$V_{CC}2$ – GND2	11.0 to 14.0	V
	V_{DD} – V_{SS}	2.7 to 3.6	V

E00Y05A11-PS

Block Diagram

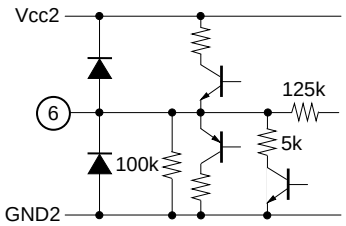
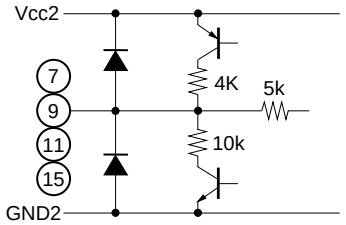
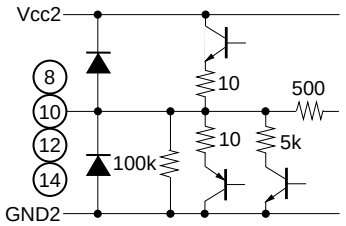
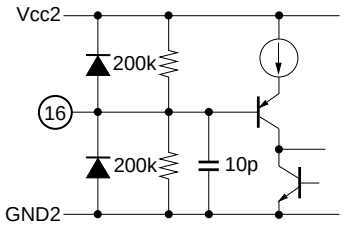


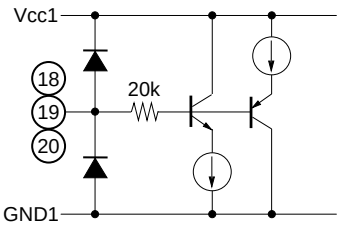
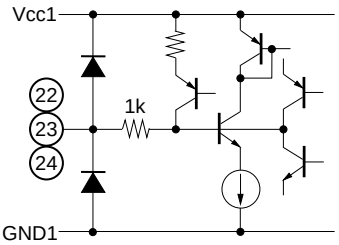
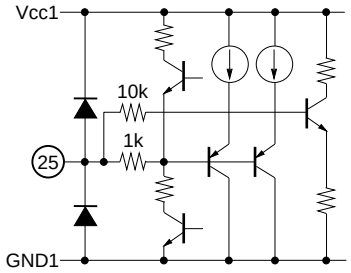
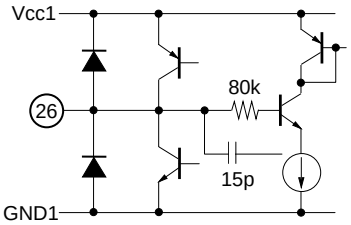
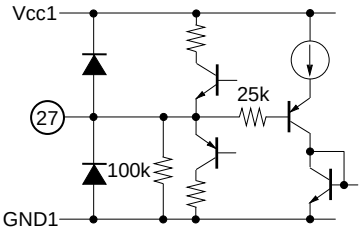
Pin Description

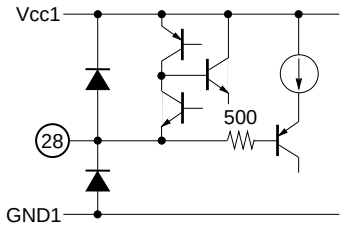
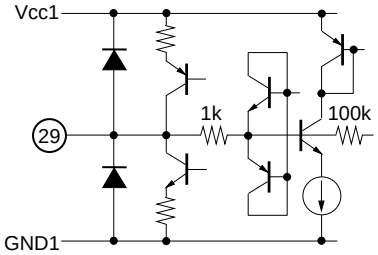
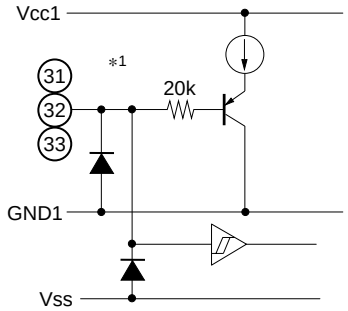
Pin No.	Symbol	I/O	Description	Input pin for open status
1	EN	O	EN pulse output	
2	VCK	O	V clock pulse output	
3	VST	O	V start pulse output	
4	TEST	—	Test (Leave this pin open.)	
5	GND2	—	Analog 12.0V GND	
6	COM	O	Common pad voltage output for LCD panel	
7	B DC DET	O	B signal DC voltage feedback circuit capacitor connection	
8	B OUT	O	B signal output	
9	R DC DET	O	R signal DC voltage feedback circuit capacitor connection	
10	R OUT	O	R signal output	
11	G DC DET	O	G signal DC voltage feedback circuit capacitor connection	
12	G OUT	O	G signal output	
13	$V_{CC}2$	—	Analog 12.0V power supply	
14	PSIG OUT	O	PSIG output	
15	PSIG DC DET	O	PSIG signal DC voltage feedback circuit capacitor connection	
16	SIG.C	I	R, G, B and PSIG output DC voltage adjustment	
17	NC	—		
18	OSD B	I	OSD B input	
19	OSD R	I	OSD R input	
20	OSD G	I	OSD G input	
21	$V_{CC}1$	—	Analog 3.0V power supply	
22	G/Y	I	G/Y signal input	
23	R/R-Y	I	R/R-Y signal input	
24	B/B-Y	I	B/B-Y signal input	
25	SYNC IN	I	Sync separation circuit input/sync signal input	
26	DA OUT	O	DAC output	
27	REF	O	Level shifter circuit REF voltage output for LCD panel	
28	FILTER	O	Internal filter circuit f0 adjusting resistor connection	
29	RPD	O	Phase comparator output	
30	GND1	—	Analog 3.0V GND	
31	SEN	I	Serial load input	
32	SCK	I	Serial clock input	
33	SDAT	I	Serial data input	
34	VD	I	Vertical sync signal input	L
35	XCLR	I	Power-on reset capacitor connection (timing output block)	
36	POF	O	LCD panel power supply on/off (Leave this pin open when not using this function.)	

Pin No.	Symbol	I/O	Description	Input pin for open status
37	V_{DD}	—	Digital 3.0V power supply	
38	HDO	O	HDO pulse output	
39	VDO	O	VDO pulse output	
40	RGT	O	Right/left inversion switching signal output	
41	V_{SS}	—	Digital 3.0V GND	
42	HCK1	O	H clock pulse 1 output	
43	HCK2	O	H clock pulse 2 output	
44	HST	O	H start pulse output	
45	V_{DD}	—	Digital 3.0V power supply	
46	WIDE	O	WIDE pulse output	
47	DWN	O	Up/down inversion switching signal output	
48	V_{SS}	—	Digital 3.0V GND	

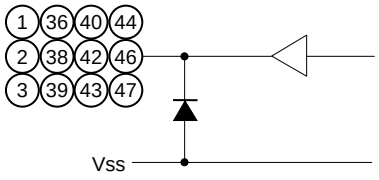
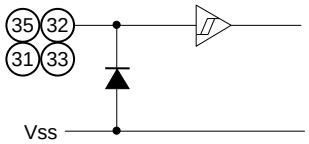
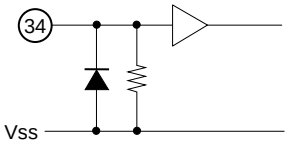
Analog Block Pin Description

Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
5	GND2	—		Analog 12.0V GND.
6	COM	—		COMMON voltage output. The output voltage is controlled by serial communication.
7 9 11 15	B DC DET R DC DET G DC DET PSIG DC DET	3.0V		Smoothing capacitor connection for the feedback circuit of R, G, B and PSIG output signal DC level control. Connect a low-leakage capacitor.
8 10 12 14	B OUT R OUT G OUT PSIG OUT	—		R, G, B and PSIG signal outputs. The DC level is controlled to match the SIG.C pin voltage. Low output in power saving mode.
13	Vcc2	12.0V		Analog 12.0V power supply.
16	SIG.C	Vcc/2		R, G, B and PSIG output DC voltage setting. Connect a 0.01µF capacitor between this pin and GND1. When using a SIG.C of other than Vcc2/2, input the SIG.C voltage from an external source.
17	NC	—		No connection.

Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
18 19 20	OSD B OSD R OSD G	Vth1 = Vcc1 × 1/3 Vth2 = Vcc1 × 2/3		OSD pulse inputs. When one of these input pins exceeds the Vth1 level, all of the outputs go to black limiter level; when an input pin exceeds the Vth2 level, only the corresponding output goes to white limiter level. Connect these pins to GND when not used.
21	Vcc1	3.0V		Analog 3.0V power supply.
22 23 24	G/Y R/R-Y B/B-Y	G/Y: 1.8V R/R-Y, B/B-Y, RGB: 1.8V Y/color difference: 2.0V		In Y/color difference input mode, input the Y signal to Pin 22, the R-Y signal to Pin 23 and the B-Y signal to Pin 24. In RGB input mode, input the G signal to Pin 22, the R signal to Pin 23 and the B signal to Pin 24. Pedestal clamp these pins with external coupling capacitors.
25	SYNC IN	0.9V		Sync separation circuit input, or composite sync/horizontal sync signal input. During input to the sync separation circuit, input via a capacitor.
26	DA OUT	—		DA output. Outputs the serial data converted to DC voltage. The current driving capacity is ±1.0mA (max.).
27	REF	Vcc1/2		REF output. The current driving capacity (sink) is 1.6mA (max.).

Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
28	FILTER	1.2V		Connect a resistor between this pin and GND1 to control the internal LPF and trap frequencies. Connect a 43kΩ resistor (tolerance ±2%, temperature characteristics ±200ppm or less). This pin is easily affected by external noise, so make the connection between the pin and external resistor, and between the GND side of the external resistor and the GND1 pin as close as possible.
29	RPD	1.8V		Phase comparator output.
30	GND1	—		Analog 3.0V GND.
31 32 33	SEN SCK SDAT	—		Serial clock, serial load and serial data inputs for serial communication.

Digital Block Pin Description

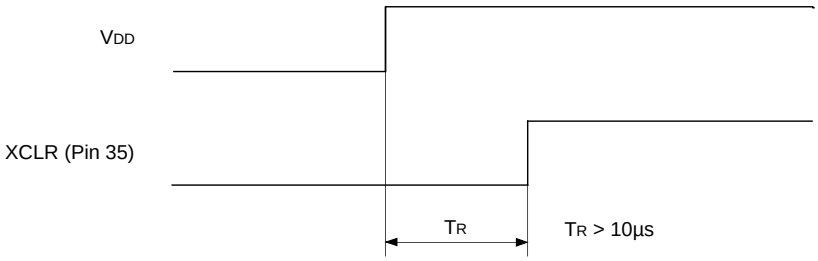
Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
1 2 3 36 38 39 40 42 43 44 46 47	EN VCK VST POF HDO VDO RGT HCK1 HCK2 HST WIDE DWN	—		Digital block outputs.
35 31 32 33	XCLR SEN SCK SDAT	—		Digital block system reset, and serial clock, serial load and serial data inputs for serial communication.
34	VD	—		Vertical sync signal input.
37 45	V_{DD}	—		Digital 3.0V power supply.
41 48	V_{SS}	—		Digital 3.0V GND.
4	TEST	—		Test. Leave this pin open.

Setting Conditions for Measuring Electrical Characteristics

Use the Electrical Characteristics Measurement Circuit on page 21 when measuring electrical characteristics. For measurement, the digital block must be initialized and power saving must be canceled by performing Settings 1, 2 and 3 below. In addition, the serial data must be set to the initial settings shown in the table below.

Setting 1. System reset

After turning on the power, activate the TG block system reset by setting XCLR (Pin 35) Low.
The serial bus is set to the default values.



System reset

Setting 2. Horizontal AFC adjustment

In the condition without sync input, adjust so that the HDO pulse output frequency is NTSC: 15.734 ± 0.1kHz and PAL: 15.625 ± 0.1kHz.

Setting 3. Canceling power saving mode

The power-on default is power saving mode, so clear (set all “1”) serial data PS0 and SYNC GEN.

Serial data initial settings

MSB ADDRESS LSB								MSB DATA LSB							
A7	A6	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	0	USER-BRIGHT (10000000/LSB)							
0	0	0	0	0	0	0	1	0	SUB-BRIGHT R (1000000/LSB)						
0	0	0	0	0	0	1	0	0	SUB-BRIGHT B (1000000/LSB)						
0	0	0	0	0	0	1	1	CONTRAST (10000000/LSB)							
0	0	0	0	0	1	0	0	0	SUB-CONTRAST R (1000000/LSB)						
0	0	0	0	0	1	0	1	0	SUB-CONTRAST B (1000000/LSB)						
0	0	0	0	0	1	1	0	0	γ-1 (0000000/LSB)						
0	0	0	0	0	1	1	1	0	γ-2 (0000000/LSB)						
0	0	0	0	1	0	0	0	PSIGSW (0)	PSIG-BRIGHT (1000000/LSB)						
0	0	0	0	1	0	0	1	0	COM-DC (1000000/LSB)						
0	0	0	0	1	0	1	0	0	COLOR (1000000/LSB)						
0	0	0	0	1	0	1	1	0	HUE (1000000/LSB)						
0	0	0	0	1	1	0	0	VCO Fine (10000000/LSB)							
0	0	0	0	1	1	0	1	0	0	BLACK-LIMITER (100000/LSB)					
0	0	0	0	1	1	1	0	PICTURE-GAIN (00000/LSB)					PICTURE-F0 (000/LSB)		
0	0	0	0	1	1	1	1	LPFSW (0)	LPF (000/LSB)			TRAP (0)	DA (000/LSB)		
0	0	0	1	0	0	0	0	0	0	VCO Coarse (000/LSB)			INPUT SEL (0)	SYNC SEL (1)	MODE (0)
0	1	0	0	0	0	0	0	0	0	TEST2 (1)	PONF (1)	TEST1 (0)	SLPOF (0)	SYNC GEN (1)	PS0 (1)
0	1	0	0	0	0	0	1	SLSYP (1)	SLEXVD (1)	SLDWN (0)	SLRGT (0)	TEST3 (0, 0)		SLWD (0)	SLNTPL (0)
0	1	0	0	0	0	1	0	SYST (0)	SLFL (0)	SLFR (0)	SL4096 (0)	SLCLP1 (0)	SLCLP0 (0)	SLVDO (0)	SLHDO (0)
0	1	0	0	0	0	1	1	0	SLMBK (0)	H POSITION (100000/LSB)					
0	1	0	0	0	1	0	0	S/H POSITION (000/LSB)		HDO POSITION (00000/LSB)					
0	1	0	0	0	1	0	1	SB POSITION (100/LSB)		V POSITION (01000/LSB)					
0	1	0	0	0	1	1	0	TEST4 (00000000/LSB)							

Note: If there is the possibility that data may be set at other than the above-noted addresses, set these data to “0”.

Electrical Characteristics — DC Characteristics

Analog Block

(Ta = 25°C, $V_{CC}1 = V_{DD} = 3.0V$, $V_{CC}2 = 12.0V$, see page 10 for the DAC)

Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Unit
Current consumption 1 (Y/color difference input)	I1	Measure the inflow current to Pin 21.	16	34	50	mA
Current consumption 2 (Y/color difference input)	I2	Measure the inflow current to Pin 13.	1.0	3.4	10	
Current consumption 1 (RGB input)	IRGB1	Measure the inflow current to Pin 21.	12	28	42	
Current consumption 2 (RGB input)	IRGB2	Measure the inflow current to Pin 13.	1.0	3.4	10	
Current consumption 1 (PS0 = 0)	IPS01	Measure the inflow current to Pin 21.	—	7	11	
Current consumption 2 (PS0 = 0)	IPS02	Measure the inflow current to Pin 13.	—	0.3	1.0	
Current consumption 1 (SYNC GEN = 0)	ISG1	Measure the inflow current to Pin 21.	—	14	27	
Current consumption 2 (SYNC GEN = 0)	ISG2	Measure the inflow current to Pin 13.	—	0.3	1.0	
B DC DET pin voltage	V7			3.0		V
R DC DET pin voltage	V9			3.0		
G DC DET pin voltage	V11			3.0		
PSIG DC DET pin voltage	V15			3.0		
SIG.C pin voltage	V16			6.0		
G/Y pin voltage	V22			1.8		
R/R-Y pin voltage 1	V23	During Y/color difference input		2.0		
R/R-Y pin voltage 2	V23	During RGB input		1.8		
B/B-Y pin voltage 1	V24	During Y/color difference input		2.0		
B/B-Y pin voltage 2	V24	During RGB input		1.8		
SYNC IN pin voltage	V25	During no input		1.1		
REF pin voltage (power saving mode)	V27			0.2		
FILTER pin voltage	V28			1.2		
OSD R, G, B input voltage			GND		$V_{CC}1$	
SIG. C input voltage	VSIG.C		5.0		6.5	

Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Unit
Y/Color difference mode Y, R-Y, B-Y signal input level 1	Y*1	INPUT SEL = 0 (–6dB Attenuate OFF)		0.35	0.4	Vp-p
	SYNC (Y on SYNC)*2			0.15	0.2	
	R-Y			0.245		
	B-Y			0.311		
Y/Color difference mode Y, R-Y, B-Y signal input level 2	Y*1	INPUT SEL = 1 (–6dB Attenuate ON)			0.7	
	SYNC (Y on SYNC)*2				0.3	
	R-Y				0.490	
	B-Y				0.622	
RGB mode R, G, B signal input level 1	R, G, B*1	INPUT SEL = 0 (–6dB Attenuate OFF)		0.35	0.5	
	SYNC (G on SYNC)*2			0.15	0.2	
RGB mode R, G, B signal input level 2	R, G, B*1	INPUT SEL = 1 (–6dB Attenuate ON)			0.7	
	SYNC (G on SYNC)*2				0.3	

*1 Y signal level (SYNC level is not included.)

*2 SYNC level of Y (G) on SYNC signal.

Control Signal Block (Sync signal, serial-serial signal, XCLR, digital output)

(Ta = –15 to +75°C, $V_{CC}1 = V_{DD}$ = 2.7 to 3.6V)

Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Unit	Applicable pins
High level input voltage	$V_{IH}1$		$V_{CC}1$ – 0.7		$V_{CC}1$	V	∗1
Low level input voltage	$V_{IL}1$		0		0.7		
High level input voltage	$V_{IH}2$		2.0		V_{DD} ($V_{CC}1$)		∗2, ∗3, ∗4
Low level input voltage	$V_{IL}2$		0		0.7		
High level input current	$\lvert I_{IH}1 \rvert$	$V_{IN} = V_{DD}$			20	μA	∗1, ∗2
Low level input current	$\lvert I_{IL}1 \rvert$	V_{IN} = 0V			20		
High level input current	$\lvert I_{IH}2 \rvert$	$V_{IN} = V_{DD}$	20		150		∗3 (pull-down)
Low level input current	$\lvert I_{IL}2 \rvert$	V_{IN} = 0V			1.0		
High level input current	$\lvert I_{IH}3 \rvert$	$V_{IN} = V_{DD}$			1.0		∗4
Low level input current	$\lvert I_{IL}3 \rvert$	V_{IN} = 0V			1.0		
High level output voltage	$V_{OH}1$	I_{OH} = –1.2mA	2.6			V	∗5
Low level output voltage	$V_{OL}1$	I_{OL} = 4.0mA			0.3		
High level output voltage	$V_{OH}2$	I_{OH} = –0.6mA	2.6				∗6
Low level output voltage	$V_{OL}2$	I_{OL} = 2.0mA			0.3		

∗1 SYNC IN (Pin 25)

∗2 SEN (Pin 31), SCK (Pin 32), SDAT (Pin 33)

∗3 VD (Pin 34)

∗4 XCLR (Pin 35)

∗5 HCK1 (Pin 42), HCK2 (Pin 43), HST (Pin 44)

∗6 EN (Pin 1), VCK (Pin 2), VST (Pin 3), POF (Pin 36), HDO (Pin 38), VDO (Pin 39), RGT (Pin 40), WIDE (Pin 46), DWN (Pin 47)

Electrical Characteristics

AC Characteristics

Unless otherwise specified, Settings 1 and 2, the serial data initial settings, and the following setting conditions are required.
Ta = 25°C, $V_{CC}1$ = 3.0V, $V_{CC}2$ = 12V, GND1 = GND2 = 0V, V_{SS} = 0V, SW8/10/12/14 = OFF, no video input, SG1 input to TP25
Note: Serial data values in the table are HEX notation.

Item	Symbol	Serial data setting (HEX)	Measurement conditions	Min.	Typ.	Max.	Unit
Maximum gain between input and output	G_{MAX}	CONT FFh MODE 00h	Input SG2 (0.2Vp-p) to TP22 and measure the output amplitude at TP12.	19	22	25	dB
Minimum gain between input and output	G_{MIN}	CONT 00h MODE 00h	Input SG2 (0.2Vp-p) to TP22 and measure the output amplitude at TP12.	–6	–3	0	dB
Inverted and non-inverted gain difference	ΔG_{INV}	CONT 2Fh	Input SG2 (0.2Vp-p) to TP22 and measure the inverted output amplitude Vinv and the non-inverted output amplitude Vninv at TP12. ΔGinv = 20 log (Vninv/Vinv)	—	—	±0.4	dB
Gain difference between R, G and B	ΔG_{RGB}	MODE 00h CONT 2Fh	Input SG2 (0.2Vp-p) to TP22 (TP23, TP24), measure the non-inverted output amplitude at TP8, TP10 and TP12, and obtain the maximum and minimum difference between these values.	—	—	0.6	dB
Sub-contrast variable amount	$\Delta G_{SC}1$	SUB-CONT 00h	Set CONT = 26h, input SG2 (0.2Vp-p) to TP22, and assume the non-inverted output amplitude at TP8 and TP10 when SUB-CONT R, B = 40h, 00h and 7Fh as V1, V2 and V3, respectively. ΔGsc1 = 20 log (V3/V1) ΔGsc2 = 20 log (V2/V1)	–4	–2.0	–1.0	dB
	$\Delta G_{SC}2$	SUB-CONT 7Fh		1.0	2.0	4.0	
Sub-bright variable amount	$\Delta V_{SB}1$	SUB-BRT R, B 00h	Set U-BRT = 1Ah and measure the non-inverted level at TP8 and TP10 relative to the non-inverted black level at TP12 when SUB-BRT R, B = 7Fh and 00h.	–2.0	–1.4	–0.9	V
	$\Delta V_{SB}2$	SUB-BRT R, B 7Fh		0.9	1.4	2.0	
R, G, B, PSIG and COM output voltage in power saving mode	V_{PSO}		Measure the R, G, B, PSIG and COM output voltages in power saving mode.	—	—	100	mV
Black limiter variable amount	$V_{BL}1$	BLK-LIM 00h	Set U-BRT = 00h, measure the non-inverted black limit level at TP12 when BLK-LIM = 00h and 3Fh, and assume the difference from the output DC voltage as $V_{BL}1$ and $V_{BL}2$, respectively.	—	2.5	3.0	V
	$V_{BL}2$	BLK-LIM 3Fh		4.5	5.0	—	

Item	Symbol	Serial data setting (HEX)	Measurement conditions	Min.	Typ.	Max.	Unit
White limiter variable amount	V_{WL}		Set CONT = FFh, input SG2 (0.2Vp-p) to TP22, measure the non-inverted white limit level, and obtain the difference from the output DC voltage.	0.3	0.6	1.0	V
Black level difference between R, G and B	ΔV_B		Measure the non-inverted black level at TP8, TP10 and TP12, and obtain the maximum and minimum difference between these values.	—	—	300	mV
RGB and PSIG output DC voltage	Vc		Measure the output DC level (average voltage) at TP8, TP10, TP12 and TP14.	5.8	6.0	6.2	V
DC voltage difference between RGB and PSIG	ΔVc		Measure the output average voltage difference at TP8, TP10 and TP14 relative to the output average voltage at TP12.	—	—	300	mV
PSIG-BRT variable amount	VPB1	PSIG-BRT 00h	Assume the PSIG output amplitude when PSIG-BRT = 00h and 7Fh as VPB1 and VPB2, respectively.	8.5	10.0	—	Vp-p
	VPB2	PSIG-BRT 7Fh		1.0	2.0	—	
USER-BRT variable amount	ΔUB1	U-BRT 00h	Measure the non-inverted black level at TP12 when U-BRT = 00h and FFh and assume the difference from the average voltage as ΔUB1 and ΔUB2, respectively.	4.5	4.8	—	V
	ΔUB2	U-BRT FFh		1.4	2.0	2.5	
Level difference between PSIG-BLK and BLK-LIM	ΔVBB	SLWD 1	Set BLK-LIM = 00h and measure the difference between the inverted and non-inverted black level at TP12 and TP14.	—	—	300	mV
HUE variable amount R	ΔHUR1	HUE 00h	Set U-BRT = 80h, CONT = 80h, COLOR = 40h, input SG4 (56mVp-p) to TP23, input SG4 (100mVp-p) to TP24, and assume the amplitude at TP8 when HUE = 80h, 00h and 3Fh as VB1, VB2 and VB3. Similarly, assume the amplitude at TP10 as VR1, VR2 and VR3. ΔHUR1 = 20 log (VR2/VR1) ΔHUR2 = 20 log (VR2/VR1) ΔHUB1 = 20 log (VB2/VB1) ΔHUB2 = 20 log (VB2/VB1)	1.5	3	—	dB
	ΔHUR2	HUE 3Fh		—	–5	–2	
HUE variable amount B	ΔHUB1	HUE 00h		—	–5	–2	
	ΔHUB2	HUE 3Fh		1.5	3	—	
Picture variable amount	GP1	PIC-G 00h	Set CONT = 80h, input SG3 to TP22, and measure the TP12 amplitude at f0 relative to the TP12 amplitude at 100kHz when PIC-G = 00h and 1Fh, respectively.	–2.5	0	2.5	dB
	GP2	PIC-G 1Fh		9	12	—	
Color variable amount	GC1	COLOR 00h	Input SG4 (160mVp-p) to TP23 and TP24, and assume the output amplitude at TP8 and TP10 when COLOR = 00h, 40h and 50h as V1, V2 and V3, respectively. GC1 = 20 log (V1/V2) GC2 = 20 log (V3/V2)	—	—	–20	dB
	GC2	COLOR 50h		0.5	—	—	

Item	Symbol	Serial data setting (HEX)	Measurement conditions	Min.	Typ.	Max.	Unit
Matrix amplitude ratio	B-Y/R-Y	CONT 80h COLOR 40h	Assume the TP10 output when SG4 (0.1Vp-p) is input to TP23 as RR, the TP8 amplitude when SG4 (0.1Vp-p) is input to TP24 as BB, the TP10 amplitude when SG5 (0.1Vp-p) is input to TP23 as RG, and the TP8 amplitude when SG5 (0.1Vp-p) is input to TP24 as BG. B-Y/R-Y = RR/BB G-Y/R-Y = RG/RR G-Y/B-Y = BG/BB	0.85	1.00	1.15	
	G-Y/R-Y			0.41	0.51	0.61	
	G-Y/B-Y			0.15	0.19	0.23	
LPF characteristics	fc1	LPF 01h MODE 00h	Input SG3 to TP22 and measure the frequency which results in –3dB relative to the TP12 amplitude at 100kHz when LPF = 01h and 07h.	—	1.5	—	MHz
	fc2	LPF 07h MODE 00h		—	5.2	—	
Trap characteristics	fo	MODE 00h TRAP 1	Set U-BRT = 30h, CONT = DFh, input SG7 (13.5MHz) to TP22, TP23 and TP24, and measure the amount by which each output is attenuated relative to SG7 (100kHz).	—	–27	–18	dB
Frequency response	fRGB	MODE 00h	Set SW8, SW10 and SW12 = ON, input SG3 to TP22, TP23 and TP24, and measure the frequency which results in –3dB relative to the TP8, TP10 and TP12 amplitude at 100kHz.	5.5	—	—	MHz
REF output voltage	VREF		Measure the REF pin output voltage at the output current 1.5mA sink.	1.3	1.5	1.7	V
DA adjustment range	VDA1	DA 00h	Measure the DA output voltage when DA = 00h and 07h. Output current 1.0mA	—	—	0.3	V
	VDA2	DA 07h	Output current –1.0mA	2.6	—	—	
γ gain	$\Delta\gamma1$	CONT 41h	Input SG2 (0.35mVp-p) to TP22 and measure the amplitude at TP8, TP10 and TP12. Assume the output amplitude when GAMMA1 = 7Fh as V1, when GAMMA1 = 3Fh as V2, and when GAMMA1 = GAMMA2 = 3Fh as V3. $\Delta\gamma1$ = 20 log (V1/V2) $\Delta\gamma2$ = 20 log (V3/V2)	12	14	16	dB
	$\Delta\gamma2$			12	14	16	
$\gamma1$ adjustment variable range	$V\gamma_{1MN}$	CONT 41h	Input SG2 (0.35mVp-p) to TP22 and read the gain transition points of the non-inverted output at TP12 when $\gamma1$ = 00h and $\gamma1$ = 7Fh from the IRE level of the input signal. $\gamma1$ = 00h: $V\gamma_{1MN}$ $\gamma1$ = 7Fh: $V\gamma_{1MX}$	—	—	0	IRE
	$V\gamma_{1MX}$			100	—	—	

Item	Symbol	Serial data setting (HEX)	Measurement conditions	Min.	Typ.	Max.	Unit
γ2 adjustment variable range	$V_{\gamma 2MN}$	CONT 41h	Input SG2 (0.35mVp-p) to TP22 and read the gain transition points of the non-inverted output at TP12 when γ2 = 00h and γ2 = 7Fh from the IRE level of the input signal. γ2 = 00h: $V_{\gamma 2MN}$ γ2 = 7Fh: $V_{\gamma 2MX}$	100	—	—	IRE
	$V_{\gamma 2MX}$			—	—	50	
COMMON control range	COMMIN	COM-DC 00h	Measure the COM output DC voltage when COM-DC = 00h and 7Fh, and measure the difference from the COM output DC voltage when COM-DC = 40h.	–1.3	–1.0	–0.8	V
	COMMX	COM-DC 7Fh		0.8	1.0	1.3	
OSD threshold value	Vth1 OSD		Input SG4 to TP18, TP19 and TP20, gradually raise the high level from 0V, and assume the high level voltage at which the output level goes to BLK-LIM level as Vth1OSD, and the high level voltage at which the output goes to WHITE-LIM level as Vth2OSD.	0.8	1.0	1.2	V
	Vth2 OSD			1.8	2.0	2.2	
Data setup time	ts0		SEN setup time, activated by the rising edge of SCK. (See Fig. 3.)	150	—	—	ns
	ts1		SDAT setup time, activated by the rising edge of SCK. (See Fig. 3.)	150	—	—	
Data hold time	th0		SEN hold time, activated by the rising edge of SCK. (See Fig. 3.)	150	—	—	ns
	th1		SDAT hold time, activated by the rising edge of SCK. (See Fig. 3.)	150	—	—	
Minimum pulse width	tw1L		SCK pulse width. (See Fig. 3.)	210	—	—	ns
	tw1H		SCK pulse width. (See Fig. 3.)	210	—	—	ns
	tw2		SEN pulse width. (See Fig. 3.)	1	—	—	µs
Output transition time	tTHL		Measure the transition time of each output. 90pF load: HST output pin 120pF load: HCK1 and HCK2 output pins (See Fig. 1.)	—	—	30	ns
	tTLH			—	—	30	
	tTHL		Measure the transition time of each output. 50pF load: DWN, WIDE, VCK, VST, TEST, EN, VDO, HDO, POF and RGT output pins (See Fig. 1.)	—	—	40	ns
	tTLH			—	—	40	
Cross-point time difference	ΔT		Measure HCK1/HCK2. 120pF load (See Fig. 2.)	—	—	—	ns
HCK duty	DTYHC		Measure the HCK1/HCK2 duty. 120pF load	48	50	52	%

Electrical Characteristic Measurement Method Diagrams

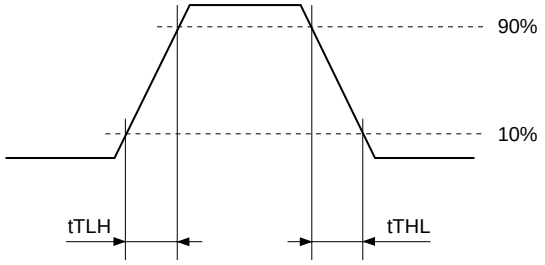


Fig. 1. Output transition time measurement conditions

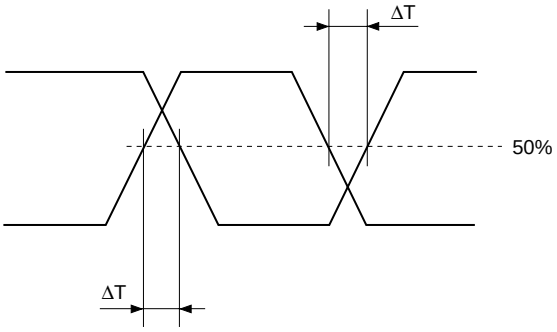


Fig. 2. Cross-point time difference measurement conditions

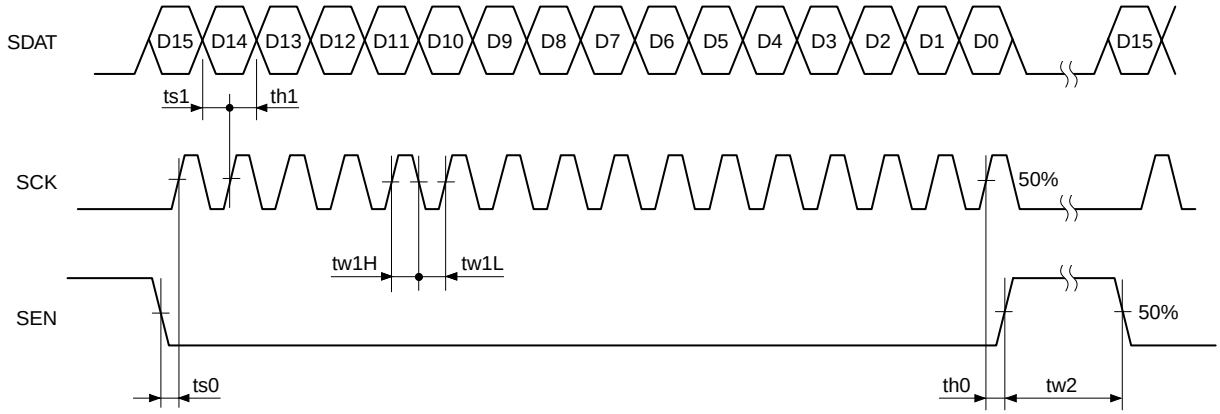
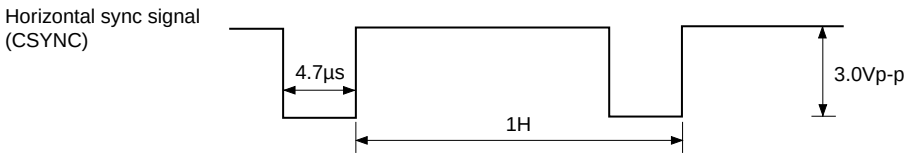
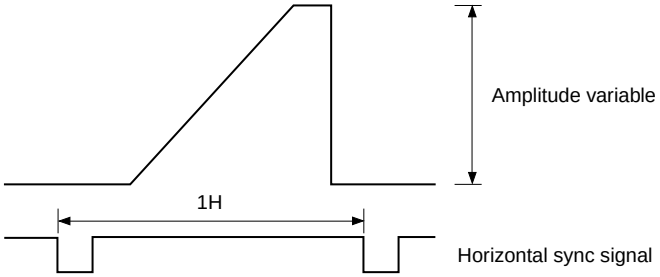
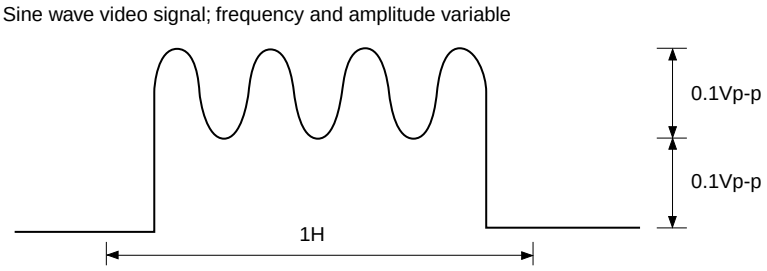
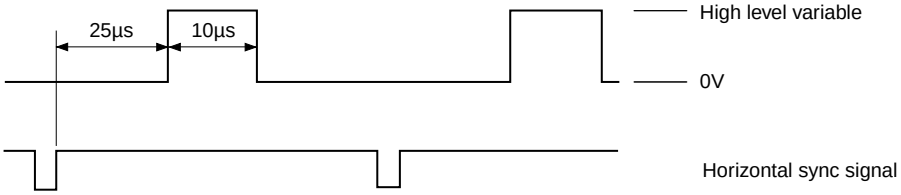
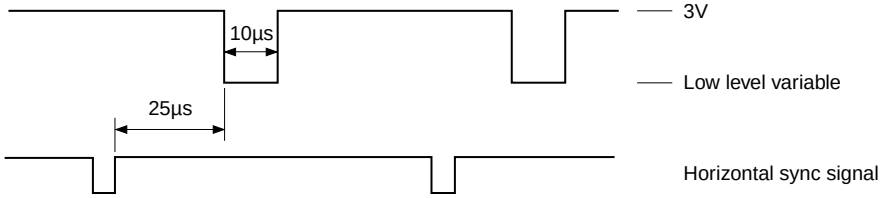
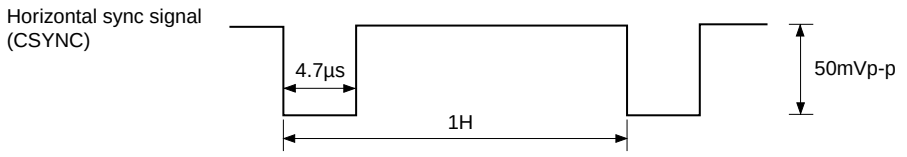
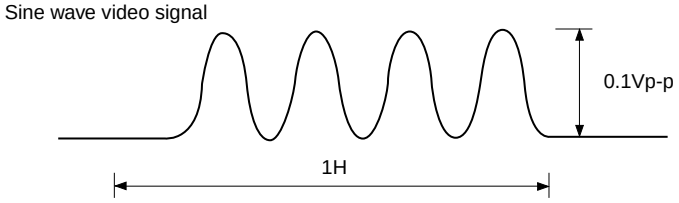
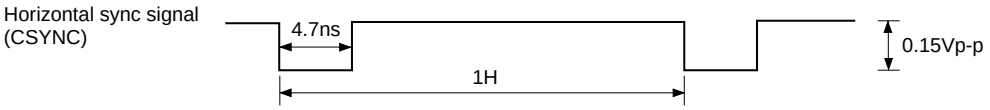
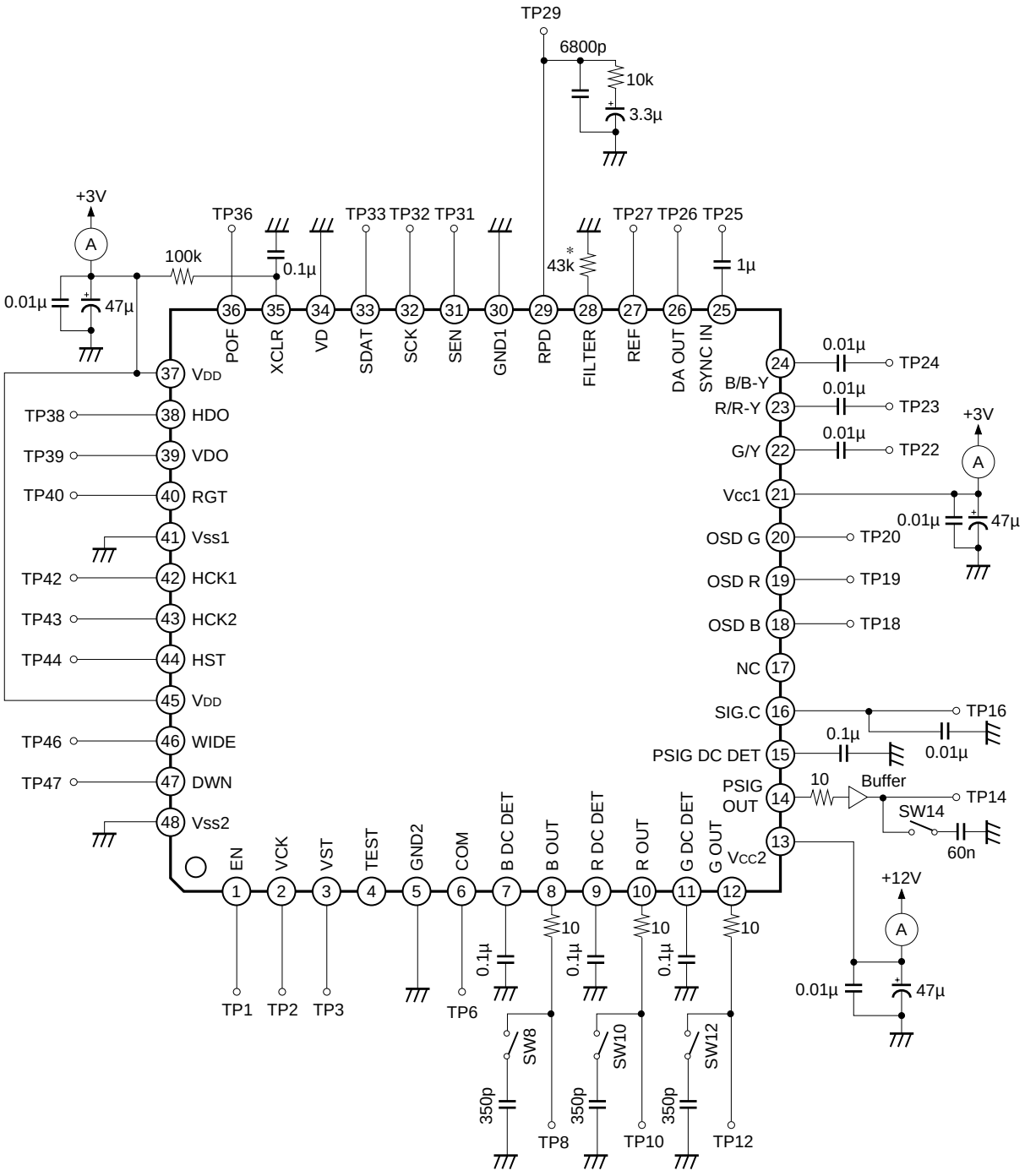


Fig. 3. Serial transfer block measurement conditions

SG No.	Waveform
SG1	
SG2	
SG3	
SG4	
SG5	

SG No.	Waveform
SG6	
SG7	
SG8	

Electrical Characteristics Measurement Circuit



* Resistance value tolerance: ±2%, temperature coefficient: ±200ppm/°C or less
Locate this resistor as close to the IC pin as possible to reduce the effects of external signals.

Description of Operation

1) RGB and Y/color difference signal processing block

Signal processing is comprised of picture, HUE, matrix, LPF/trap, contrast, OSD, sample-and-hold, γ correction, bright, sub-bright, sub-contrast and output circuits.

- Input signal mode switching
  The input mode (RGB input, Y/color difference input) can be switched by the serial communication settings.
  (During internal sync separation signal input)
  - During RGB input: The G signal is input to Pins 22 and 25, the B signal to Pin 24, and the R signal to Pin 23.
  - During Y/color difference input: The Y signal is input to Pins 22 and 25, the B-Y signal to Pin 24, and the R-Y signal to Pin 23.

  (During external sync signal input)
  - During RGB input: The G signal is input to Pin 22, the B signal to Pin 24, the R signal to Pin 23, CSYNC/HD to Pin 25, and VD to Pin 34.
  - During Y/color difference input: The Y signal is input to Pin 22, the B-Y signal to Pin 24, the R-Y signal to Pin 23, CSYNC/HD to Pin 25, and VD to Pin 34.

- NTSC/PAL switching
  The input system (NTSC/PAL) can be switched by the serial communication settings.

- Picture circuit
  This performs aperture correction for the Y signal. The center frequency to be corrected and the correction amount are controlled by serial communication.

- HUE circuit
  This is the hue adjustment circuit for the color difference signal. It is controlled by serial communication.

- Matrix circuit
  This circuit converts Y, R-Y and B-Y signals into RGB signals.

- LPF circuit
  This is the band limitation filter for the RGB signal. It is used to eliminate the noise component generated at the front end of this IC. The cut-off frequency can be controlled by serial communication. In addition, when not using the LPF, it can be turned off by serial communication.

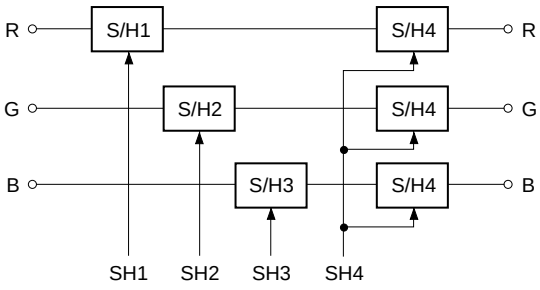
- Trap circuit
  This is used to eliminate the DSP clock and RGB decoder carrier leak generated at the front end of this IC. In addition, when not using the trap, it can be turned off by serial communication.

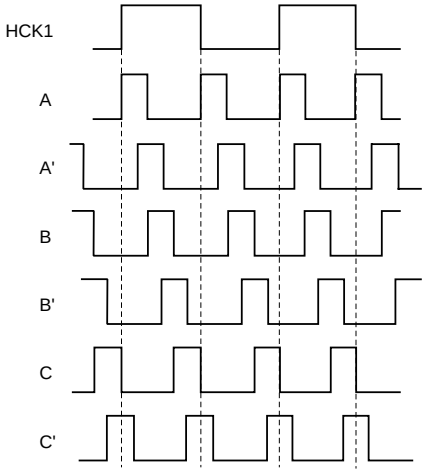
- Contrast adjustment circuit
  This adjusts the amplitude to set the input RGB signal to the appropriate output level.

- OSD
  This inputs the OSD pulses. There are two input threshold values: Vth1 (Vcc1 × 1/3) and Vth2 (Vcc1 × 2/3). When an input exceeds Vth1, the corresponding output falls to the level specified by BLACK-LIMITER. When an input exceeds Vth2, the corresponding output rises to the level specified by WHITE-LIMITER. Also, when one of the RGB inputs exceeds Vth1, any signal outputs not exceeding Vth1 also fall to the level specified by BLACK-LIMITER.

• Sample-and-hold circuit

This circuit performs time axis correction for the RGB output signals in order to support the RGB simultaneous sampling systems of LCD panels.





RGT = H (Normal)

	SHS1	SHS2	SHS3	SHS4	SHS5	SHS6
SH1	B	A'	A	C'	C	B'
SH2	Through	Through	Through	Through	Through	Through
SH3	A	C'	C	B'	B	A'
SH4	C	B'	B	A'	A	C'

RGT = L (right/left inversion)

	SHS1	SHS2	SHS3	SHS4	SHS5	SHS6
SH1	B	A'	A	C'	C	B'
SH2	A	C'	C	B'	B	A'
SH3	Through	Through	Through	Through	Through	Through
SH4	C	B'	B	A'	A	C'

SH1: R signal SH pulse
SH2: G signal SH pulse
SH3: B signal SH pulse
SH4: RGB signal SH pulse

SHS1, 2, 3, 4, 5, 6:
Serial data settings

The sample-and-hold circuit performs sample and hold by receiving the SH1 to SH4 pulses from the TG block. Since LCD panels perform color coding using an RGB delta arrangement, each horizontal line must be compensated by 1.5 dots. This relationship is reversed during right/left inversion. This compensation and other timing is also generated by the digital block. The sample-and-hold timing changes according to the phase relationship with the HCK pulse, so the timing should be set to the SHS1 to SHS6 position in accordance with the actual board.

• γ correction

In order to support the characteristics of LCD panels, the I/O characteristics are as shown in Fig. 1. The γ1 gain transition point A voltage changes as shown in Fig. 2 by adjusting the serial bus register γ1, and the γ2 gain transition point B voltage changes as shown in Fig. 3 by adjusting γ2.

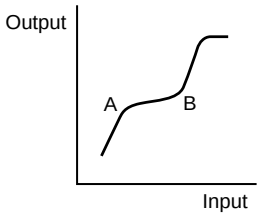


Fig. 1

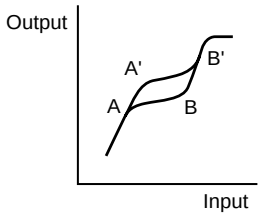


Fig. 2

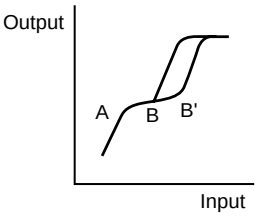


Fig. 3

• Bright circuit

This is used to adjust the black-black amplitude of polarity-inverted RGB output signals. It is not interlinked with the γ transition points.

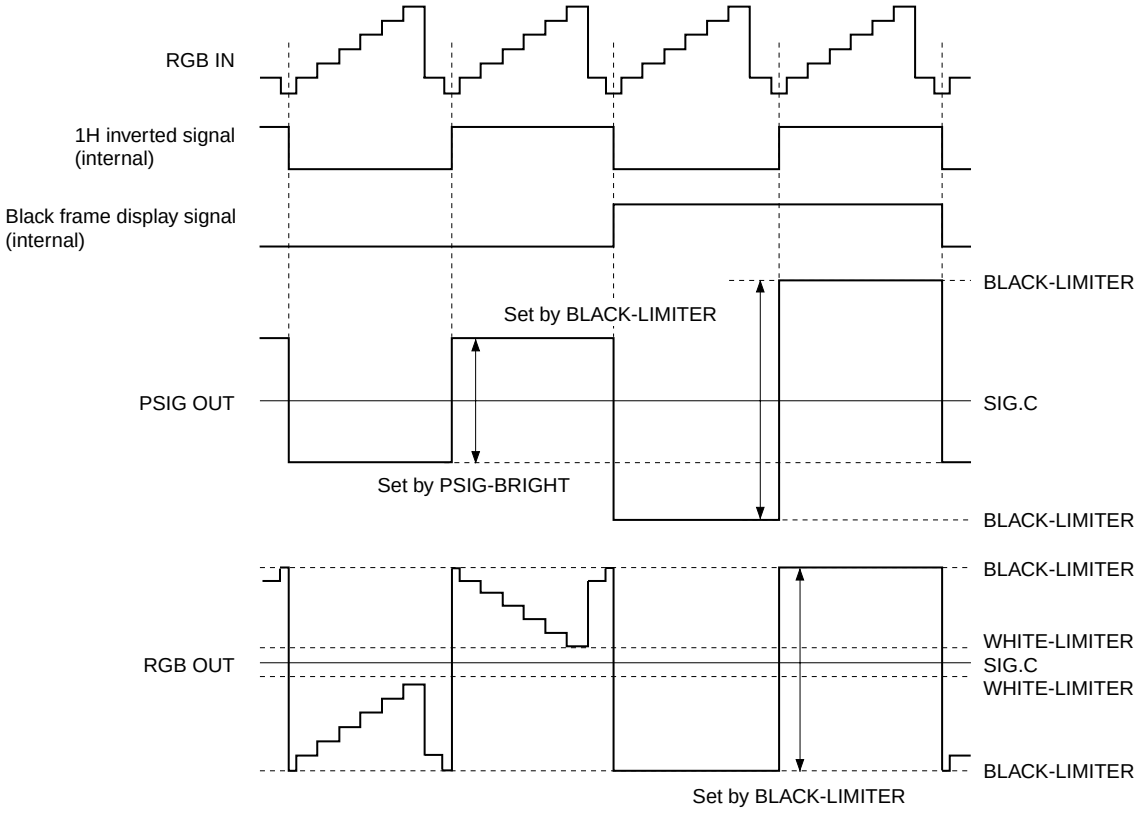
• White balance adjustment circuit

This is used to adjust the white balance. The black level is adjusted by SUB-BRIGHT, and the black-white amplitude is adjusted by SUB-CONTRAST.

• Output circuit

RGB output (Pins 8, 10, and 12) signals are inverted each horizontal line by the FRP pulse (internal pulse) supplied from the TG block as shown in the figure below. Feedback is applied so that the center voltage (SIG.C) of the output signal matches the reference voltage (Vcc2 + GND2)/2 (or the voltage input to SIG.C (Pin 16)). In addition, the white level output is clipped at the limiter operation point that is set by the serial communication WHITE-LIMITER, and the black level output is clipped at the limiter operation point that is set by the serial communication BLACK-LIMITER.

The output PSIG signal level is normally adjusted by PSIG-BRIGHT, but during black frame display the level is specified by the BLACK-LIMITER level at some timings. In addition, the RGB output also simultaneously goes to BLACK-LIMITER level output.



2) Common voltage generation circuit block

The common voltage circuit generates and supplies the common pad voltage to the LCD panel. The voltage is offset by serial communication using the SIG.C voltage as the reference and then output.

3) DA OUT output circuit

The DA OUT output circuit outputs DC 3.0V at equal divisions.

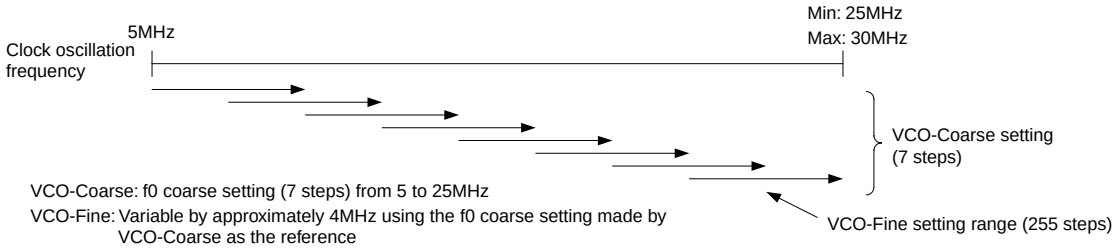
4) REF output circuit

The REF output circuit generates and supplies the panel level shifter circuit reference voltage to the LCD panel.

5) Sync system

- Internal sync separation circuit
  Sync separation is performed from the signal input from SYNC IN (Pin 25). An external sync signal can also be input from the same pin (SYNC IN) according to the serial communication setting.
  Serial communication setting
  SYNC SEL = 0: Internal sync separation.
  SYNC SEL = 1: External sync signal input. (The internal sync separation circuit is set to power saving mode.)
  Input pin (Pin 25) processing
  During internal sync separation: Input through an external capacitor (0.1µF)
  During external sync signal input: Directly coupled, input level 3Vp-p positive or negative polarity

- PLL and AFC circuits (VCO setting method)
  A PLL circuit can be comprised by connecting a PLL circuit phase comparator and frequency division counter and a VCO circuit and external LPF circuit. The PLL error detection signal is generated using the phase comparison output of the entire bottom of the horizontal sync signal and the internal frequency division counter as the RPD output. RPD output is converted to DC error voltage with the lag-lead filter, and then it controls the internal VCO circuit to stabilize the oscillation frequency.
  The internal clock oscillation frequency is set as follows by adjusting VCO-Coarse/Fine.
  Adjust the VCO-Coarse/Fine settings so that the HDO pulse output frequency in the condition without sync input is NTSC: 15.734 ± 0.1kHz and PAL: 15.625 ± 0.1kHz.



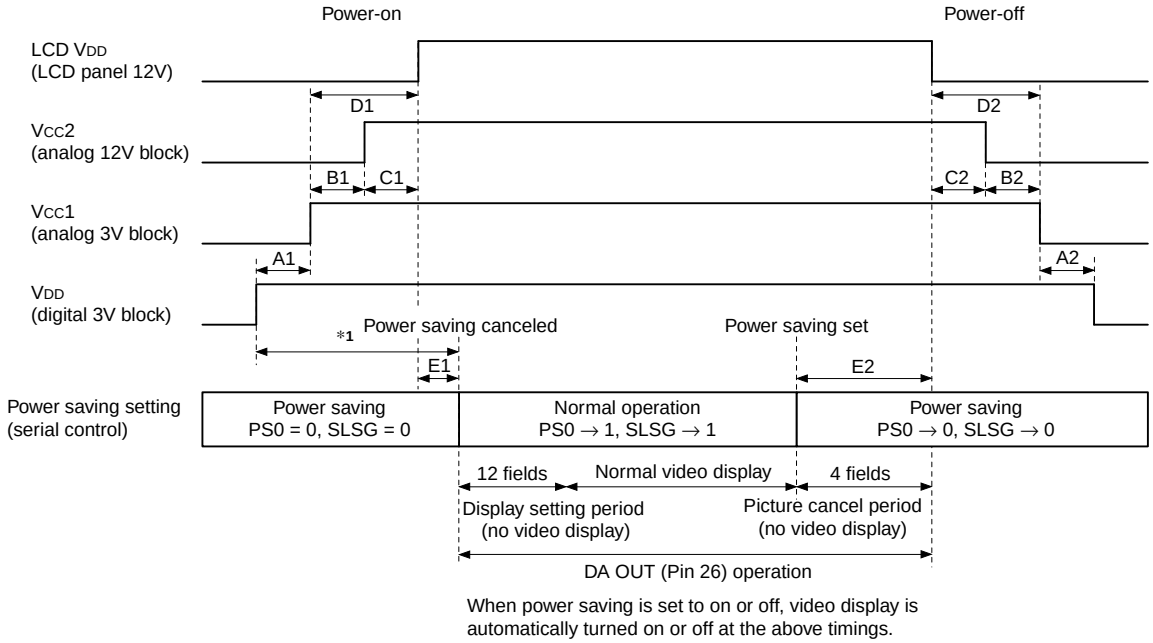
6) Power saving circuit (PS circuit)

A power saving system can be realized together with the LCD panel by independently controlling (serial communication) the operation of each output block. This system is also effective for improving picture quality during power-on/off.

The serial data PS0 and SYNC GEN must be set in order to use this IC.
For details of the setting methods, see the “Description of Serial Control Operation” and “Power supply and power saving sequence” items.

7) Power supply and power saving sequence

Power-on for the CXA3572R and the LCD panel should be performed in the following order.



When power saving is set to on or off, video display is automatically turned on or off at the above timings.

Power-on

	min.	max.	
A1	0	—	ms
B1	0	—	
C1	0	—	
D1	100*2	—	
E1	0	100	

Power-off

	min.	max.	
A2	0	—	ms
B2	0	—	
C2	0	—	
D2	*3	—	
E2	150	300	

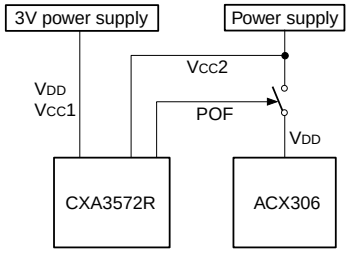
*1 After the digital 3V V_{DD} has completely risen and XCLR (Pin 35) is completely high level.

*2 After the 3V V_{DD}/$V_{CC}1$ has completely risen.

*3 After the panel 12V V_{DD} has completely fallen.

- POF (Pin 36) is output as the panel V_{DD} control signal. The POF output can be switched by the serial communication setting, and the POF setting can be made regardless of the power saving setting.

SLPOF	POF (Pin 36) output
0	Low level
1	High Level (V_{DD})



Panel power supply configuration using POF output

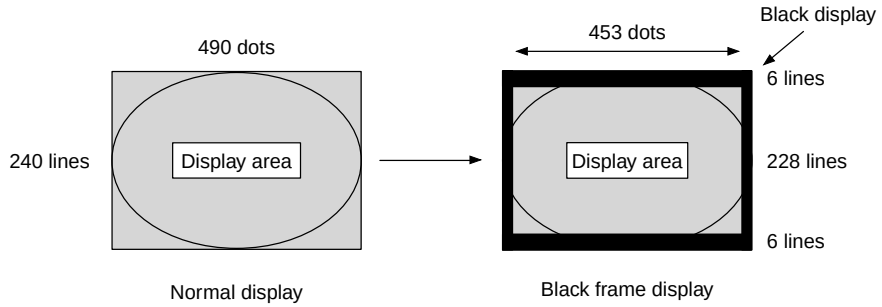
8) TG block

- H-Position
  This adjusts the horizontal display position. Set this function so that the picture center matches the center of the LCD panel.

- V-Position
  This adjusts the vertical display position. Set this function so that the picture center matches the center of the LCD panel.

- Right/left (RGT) and/or up/down (DWN) inversion
  The video display direction can be switched. The horizontal direction can be switched between right scan and left scan, and the vertical direction between down scan and up scan. Set the display direction in accordance with the LCD panel mounting position.

- Overscan display mode (SLWD)
  Displaying black in the up/down 6 lines and right/left 18 (19) dots of the display area generates an overscan area (black frame) in the display area. Fine adjustment of the black frame display position is performed by SB-Position.

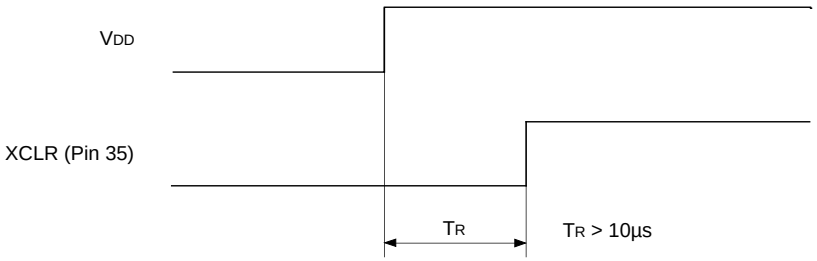


- AC driving of LCD panels during no signal
  The output signal runs freely so that the LCD panel is AC driven even when there is no sync signal from the SYNC IN (Pin 25) and VD (Pin 34) pins.

Description of Serial Control Operation

1) System reset

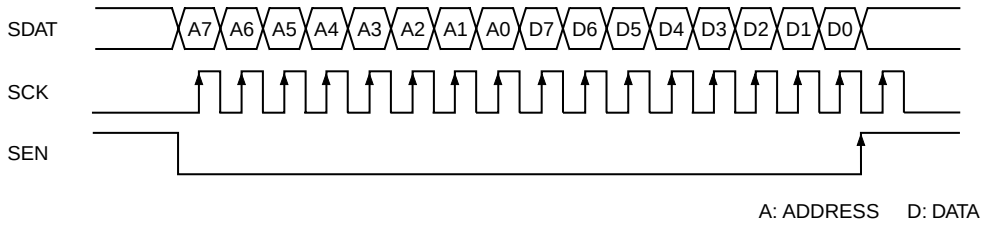
After turning on the power, activate the TG block system reset by setting XCLR (Pin 35) Low. (See Fig.)
The serial bus is set to the default values.



System reset

2) Control method

Control data consists of 16 bits of data which is loaded one bit at a time at the rising edge of SCK. This loading operation starts from the falling edge of SEN and is completed at the next rising edge.
Digital block control data is established by the vertical sync signal, so if data is transferred multiple times for the same item, the data immediately before the vertical sync signal is valid. Analog (electronic attenuator) block control data becomes valid each time the SEN signal is input.
In addition, if 16 bits or more of SCK are not input while SEN is low, the transferred data is not loaded to the inside of the IC and is ignored. If 16 bits or more of SCK are input, the 16 bits of data before the rising edge of the SEN pulse are valid data.



Serial transfer timing

2) Serial data map

The serial data map is as follows. Values inside parentheses are the default values.

MSB ADDRESS LSB								MSB DATA LSB							
A7	A6	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	0	USER-BRIGHT (10000000/LSB)							
0	0	0	0	0	0	0	1	(0)	SUB-BRIGHT R (1000000/LSB)						
0	0	0	0	0	0	1	0	(0)	SUB-BRIGHT B (1000000/LSB)						
0	0	0	0	0	0	1	1	CONTRAST (10000000/LSB)							
0	0	0	0	0	1	0	0	(0)	SUB-CONTRAST R (1000000/LSB)						
0	0	0	0	0	1	0	1	(0)	SUB-CONTRAST B (1000000/LSB)						
0	0	0	0	0	1	1	0	(0)	γ-1 (0000000/LSB)						
0	0	0	0	0	1	1	1	(0)	γ-2 (0000000/LSB)						
0	0	0	0	1	0	0	0	PSIGSW (0)	PSIG-BRIGHT (1000000/LSB)						
0	0	0	0	1	0	0	1	(0)	COM-DC (1000000/LSB)						
0	0	0	0	1	0	1	0	(0)	COLOR (1000000/LSB)						
0	0	0	0	1	0	1	1	(0)	HUE (1000000/LSB)						
0	0	0	0	1	1	0	0	VCO Fine (10000000/LSB)							
0	0	0	0	1	1	0	1	(0)	(0)	BLACK-LIMITER (100000/LSB)					
0	0	0	0	1	1	1	0	PICTURE-GAIN (00000/LSB)					PICTURE-F0 (000/LSB)		
0	0	0	0	1	1	1	1	LPFSW (0)	LPF (000/LSB)			TRAP (0)	DA (000/LSB)		
0	0	0	1	0	0	0	0	(0)	(0)	VCO Coarse (000/LSB)			INPUT SEL (0)	SYNC SEL (0)	MODE (0)
0	1	0	0	0	0	0	0	(0)	(0)	TEST2 (1)	PONF (0)	TEST1 (0)	SLPOF (0)	SYNC GEN (0)	PS0 (0)
0	1	0	0	0	0	0	1	SLSYP (0)	SLEXVD (0)	SLDWN (0)	SLRGT (0)	TEST3 (00)		SLWD (0)	SLNTPL (0)
0	1	0	0	0	0	1	0	SYST (0)	SLFL (0)	SLFR (0)	SL4096 (0)	SLCLP1 (0)	SLCLP0 (0)	SLVDO (0)	SLHDO (0)
0	1	0	0	0	0	1	1	(0)	SLMBK (0)	H POSITION (100000/LSB)					
0	1	0	0	0	1	0	0	S/H POSITION (000/LSB)		HDO POSITION (00000/LSB)					
0	1	0	0	0	1	0	1	SB POSITION (100/LSB)		V POSITION (01000/LSB)					
0	1	0	0	0	1	1	0	TEST4 (00000000/LSB)							

Note: If there is the possibility that data may be set at other than the above-noted addresses, set these data to “0”.

3) Description of control data

• USER-BRIGHT
This adjusts the brightness of the RGB output signals. Adjustment from LSB → MSB decreases the amplitude (black – black).

• SUB-BRIGHT R/B
This adjusts the brightness of the R and B output signals using the G output signal as the reference. Adjustment from LSB → MSB decreases the amplitude (black – black).

• CONTRAST
This adjusts the contrast of the RGB output signals. Adjustment from LSB → MSB increases the amplitude (black – white).

• SUB-CONTRAST R/B
This adjusts the contrast of the R and B output signals using the G output signal as the reference. Adjustment from LSB → MSB increases the amplitude (black – white).

• γ-1
This sets the black side γ point level of the RGB output signals. Adjustment from MSB → LSB lowers the γ point. When not adjusting γ-1, set γ-1: 0000000 (LSB). Set the γ-1 point to the black side (lower side) of the γ-2 point.

• γ-2
This sets the white side γ point level of the RGB output signals. Adjustment from LSB → MSB lowers the γ point. When not adjusting γ-2, set γ-2: 0000000 (LSB). Set the γ-2 point to the white side (upper side) of the γ-1 point.

• PSIG-BRIGHT
This adjusts the brightness of the PSIG output signal. Adjustment from LSB → MSB decreases the amplitude (peak to peak).

• PSIG-SW
This switches the PSIG circuit on and off.

D7	Mode
0	PSIG OFF
1	PSIG ON

• COM-DC
This adjusts the COMMON output voltage. Adjustment from LSB → MSB increases the output voltage.

• COLOR
This adjusts the color gain during Y/color difference input. Adjustment from LSB → MSB increases the gain.

• HUE
This adjusts the phase during Y/color difference input. Adjustment from LSB → MSB advances the phase.

• VCO-Fine
This finely adjusts the VCO oscillation center frequency. Adjustment from LSB → MSB increases the frequency.
Perform this adjustment after adjusting VCO-Coarse.

• VCO-Coarse
This roughly adjusts the VCO oscillation center frequency. Adjustment from LSB → MSB increases the frequency.
Adjust with VCO-Fine set to 10000000 (LSB).

• BLACK-LIMITER
This adjusts the black side limiter level of the RGB output signals. Adjustment from LSB → MSB lowers the limiter level.

• PICTURE-GAIN
This adjusts the picture gain during Y/color difference input. Adjustment from LSB → MSB raises the gain. When not using the picture function, set PICTURE-GAIN: 00000 (LSB).

• PICTURE-F0
This sets the picture center frequency (f0) during Y/color difference input. See the AC Characteristics for the output level.

D2	D1	D0	Center frequency (f0) typ.
0	0	0	1.0MHz
0	0	1	1.3MHz
0	1	0	1.6MHz
0	1	1	1.9MHz
1	0	0	2.2MHz
1	0	1	2.5MHz
1	1	0	2.8MHz
1	1	1	3.1MHz

• LPF
This switches the frequency response of the low-pass filter. Set the fc/–3dB frequency relative to the amplitude 100kHz reference. See the AC Characteristics for the output level.

D6	D5	D4	fc (RGB input/no load/typ.)
0	0	0	—
0	0	1	1.5MHz
0	1	0	2.1MHz
0	1	1	2.7MHz
1	0	0	3.5MHz
1	0	1	4.1MHz
1	1	0	4.6MHz
1	1	1	5.2MHz

• LPF-SW

This switches the LPF circuit on and off.

D7	Mode
0	LPF off
1	LPF on

• TRAP

This switches the trap circuit on and off.

D3	Mode
0	TRAP off
1	TRAP on

• DA

This adjusts the DA output voltage. Adjustment from LSB → MSB raises the output voltage level.

• INPUT-SEL

Set this according to the input signal level.

D2	Mode	Input signal level
0	Normal input	0.35Vp-p or less, 0.5Vp-p or less with sync
1	Internally attenuated by –6dB	0.35Vp-p or more, 0.5Vp-p or more with sync

• SYNC SEL

This switches between internal sync separation and external sync signal input.

D1	Mode	Input connection method
0	Internal sync separation	Input via a coupling capacitor
1	External sync signal input (internal sync separation circuit power saving)	Input level 3Vp-p positive or negative polarity

• MODE

This switches the input signal.

D0	Input signal
0	RGB input
1	Y/color difference input

• PS0 (Default: 0)

This performs the power saving setting. Be sure to use this setting as described in “Power supply and power saving sequence”. The power-on default for this IC is power saving mode, so the settings should be canceled by serial communication after power-on. The LCD panel power supply must be turned off in power saving mode.

PS0	Mode
0	Power saving
1	Normal operation

• SYNC GEN (Default: 0)

This sets the sync generator mode. In sync generator mode, only the HDO and VDO pulses are output normally, and all other pulses are low. The LCD panel power supply must be turned off in sync generator mode. Normally set to “1”.

SYNC GEN	Mode
0	Sync generator mode
1	Normal operation

• SLPOF (Default: 0)

This sets the POF (Pin 36) output. The POF output setting can be made regardless of the power saving mode.

SLPOF	Mode
0	POF = Low output
1	POF = High output

• TEST1 (Default: 0)

This is the test mode. Set to “0”.

TEST0	Mode
0	Normal operation
1	Test mode

• PONF (Default: 0)

This switches the time until the picture is displayed after power saving is canceled.

PONF	Mode
0	12 fields
1	4 fields

• TEST2 (Default: 0)

This is the test mode. Set to “1”.

TEST2	Mode
0	Test mode
1	Normal operation

• SLNTPL (Default: 0)

This switches between NTSC and PAL mode.

SLNTPL	Mode
0	NTSC
1	PAL

• SLWD (Default: 0)

This sets the up/down and/or right/left black frame display.

SLWD	Display
0	100% viewing field display
1	Black frame display (95% display)

• TEST3 (Default: 0, 0)

This is the test mode. Set to “0, 0”.

TEST3	Mode
0, 0	Normal operation
0, 1 1, 0 1, 1	Test mode

• SLRGT (Default: 0)

This switches between normal and right/left inverted display.

SLRGT	Setting
0	Normal display (right scan)
1	Right/left inverted display (left scan)

• SLDWN (Default: 0)

This switches between normal and up/down inverted display.

SLDWN	Setting
0	Normal display (down scan)
1	Up/down inverted display (up scan)

• SLEXVD (Default: 0)

This sets the external VD input. The external VD signal is input via VD (Pin 34). When using internal vertical sync separation, vertical sync separation is performed using the CSYNC input from SYNC IN (Pin 25).

SLEXVD	Setting
0	Internal vertical sync separation
1	External VSYNC input

• SLSYP (Default: 0)

This switches the input sync signal polarity. When performing sync separation with the internal sync separation circuit from YonSYNC or GonSYNC, set this to “0”.

SLSYP	HD/CSYNC, VSYNC polarity
0	Positive polarity
1	Negative polarity

• SLHDO (Default: 0)

This switches the HDO pulse output polarity.

SLHDO	HDO polarity
0	Positive polarity
1	Negative polarity

• SLVDO (Default: 0)

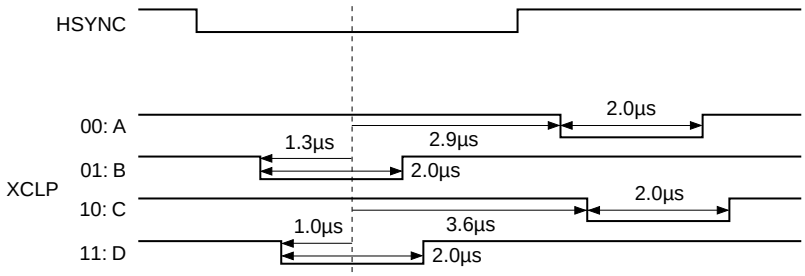
This switches the VDO pulse output polarity.

SLVDO	VDO polarity
0	Positive polarity
1	Negative polarity

• SLCLP0, SLCLP1 (Default: 0, 0)

These switch the clamp position.

SLCLP1	SLCLP0	Position
0	0	A: Back porch position (during internal sync separation)
0	1	B: Sync position (during internal sync separation)
1	0	C: Back porch position (during external sync signal input)
1	1	D: Sync position (during external sync signal input)



• SL4096 (Default: 0)

This function inverts the R, G, B and PSIG output signal polarities every 4096 fields. This further inverts the output polarities that are inverted every 1H for 4096 fields.

SL4096	Polarity inversion cycle
0	1H inversion
1	1H inversion + 4096-field inversion

• SLFR (Default: 0)

This function inverts the R, G, B and PSIG output signal polarities every field. Normally set to 1H inversion.

SLFR	Polarity inversion cycle
0	1H inversion
1	1-field inversion

• SLFL (Default: 0)

This function is used to stop R, G, B and PSIG output signal polarity inversion.

SLFL	Polarity inversion cycle
0	Polarity inversion
1	Polarity inversion stopped

• SYST (Default: 0)

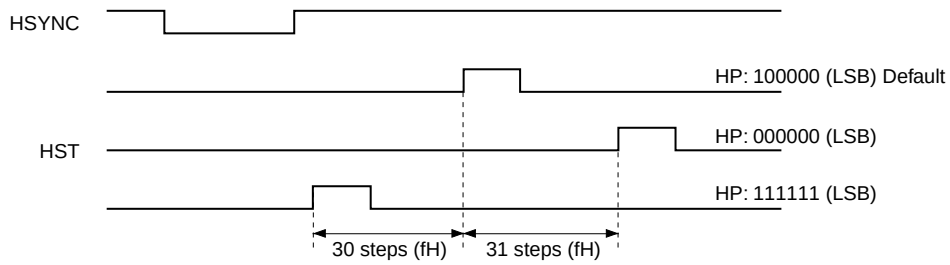
This invalidates the input horizontal sync (CSYNC, HD) and forcibly sets the free-running status.

SYST	Mode
0	Normal operation
1	Forced free-running

• H POSITION (Default: 100000/LSB)

These set the horizontal display position. The HST pulse position is adjusted using the horizontal sync signal as the reference.

Adjustment is possible in 1 bit = 1fH increments.



• SLMBK (Default: 0)

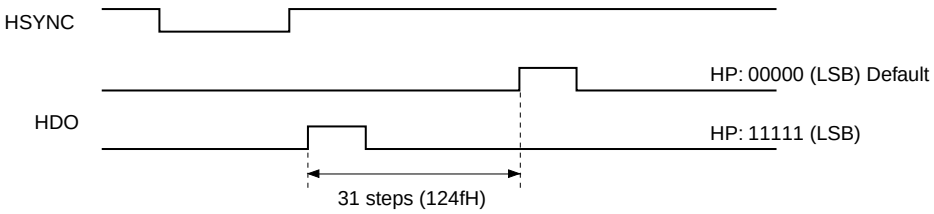
This sets the decimation cycle in PAL mode.

SLMBK	Decimation cycle
0	1/6, 1/6 decimation
1	1/6, 1/8 decimation

• HDO POSITION (Default: 00000/LSB)

These set the HDO pulse output position. The HDO pulse output position is adjusted using the horizontal sync signal as the reference.

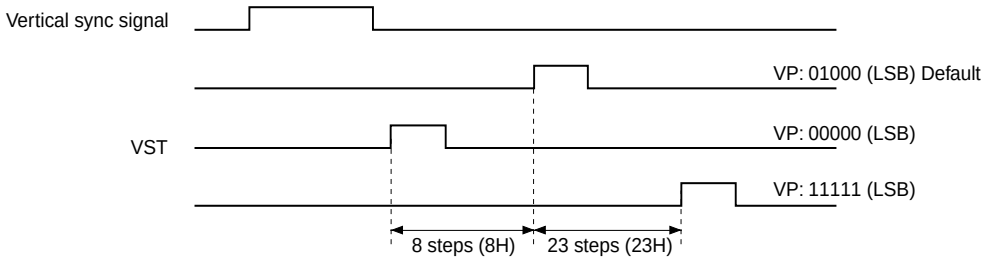
Adjustment is possible in 1 bit = 4fH increments.



• V POSITION (Default: 01000/LSB)

These set the vertical display position. The VST pulse position is adjusted using the input vertical sync signal as the reference.

Adjustment is possible in 1 bit = 1H (1 line) increments.



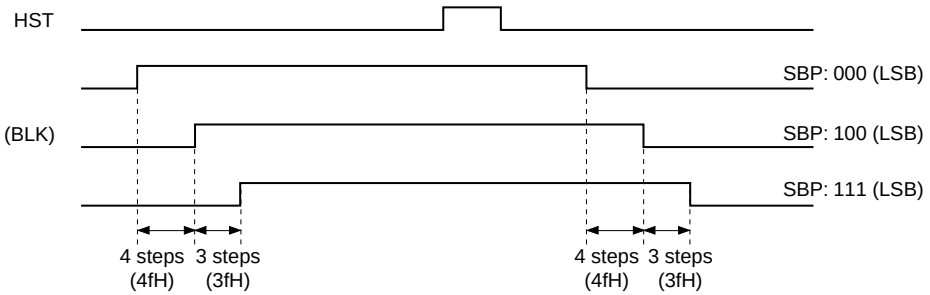
• S/H POSITION (Default: 000/LSB)

These set the sample-and-hold pulse output phase.

D7	D6	D5	Sample-and-hold position
0	0	0	SHS1
0	0	1	SHS2
0	1	0	SHS3
0	1	1	SHS4
1	0	0	SHS5
1	0	1	SHS6
1	1	0	Through (sample-and-hold off)
1	1	1	Through (sample-and-hold off)

• SB POSITION (Default: 100/LSB)

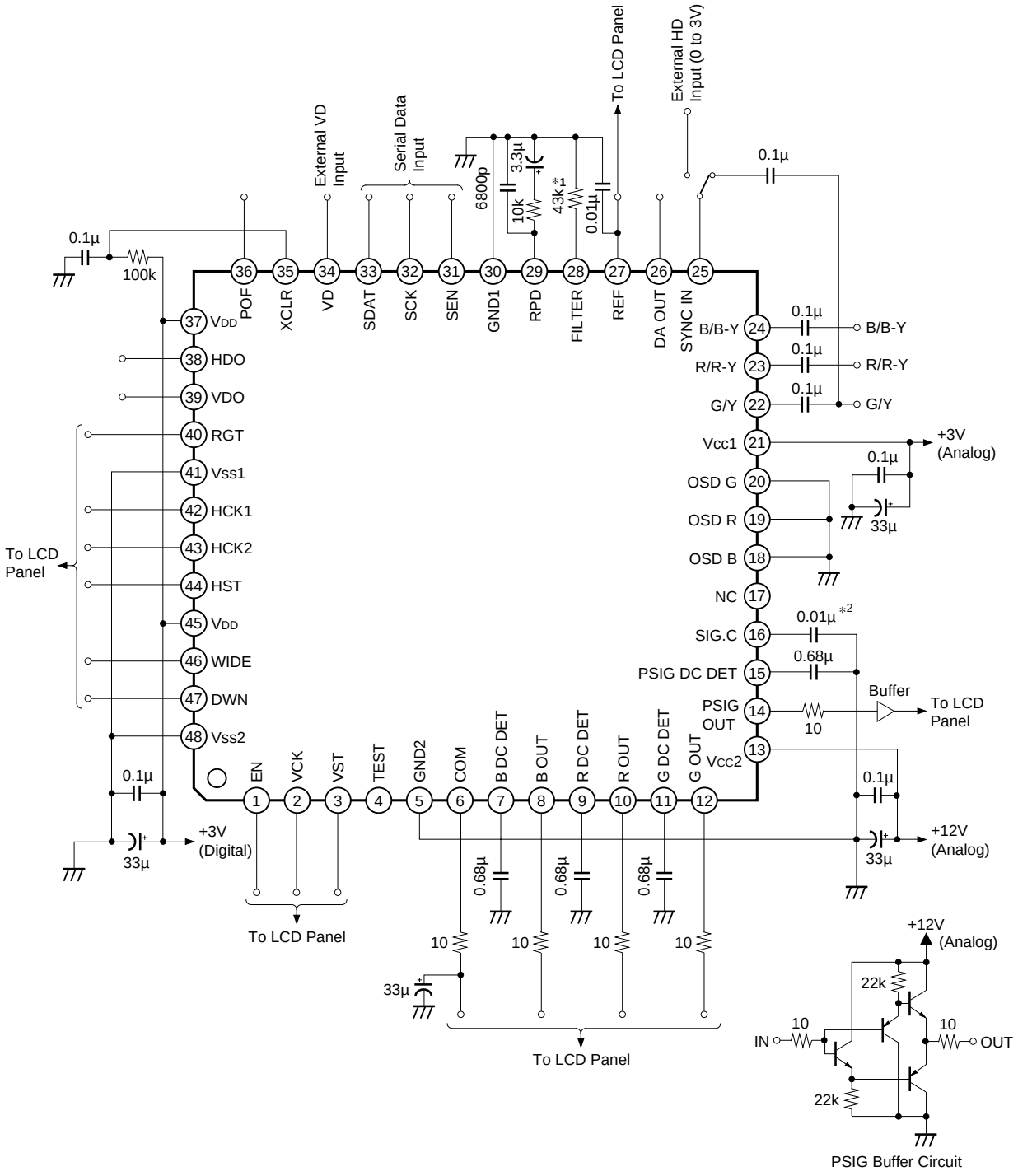
In overscan display mode, fine adjustment of the right/left overscan area (black frame) position is possible in 1 bit = 1fH increments.



• TEST4 (Default: 00000000/LSB)

This is the test mode. Set to 00000000/LSB (8 bits).

Application Circuit



*1 Resistance value tolerance: ±2%, temperature coefficient: ±200ppm/°C or less

*2 When using a signal center voltage other than Vcc2/2, input an external signal center voltage.

Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Notes on Operation

(1) This IC contains digital circuits, so the set board pattern must be designed in consideration of undesired radiation, interference to analog circuits, etc. Care should also be taken for the following items when designing the pattern.

- The digital and analog IC power supplies should be separated, but the GND and V_{SS} should not be separated and should use a plain GND (V_{SS}) pattern in order to reduce impedance as much as possible. The power supplies should also use a plain pattern.
- Use ceramic capacitors for the by-pass capacitors between the power supplies and GND, and connect these capacitors as close to the pins as possible.
- The resistor connected to Pin 28 should be connected as close to the pin as possible, and the wiring from the pin to GND should be as short as possible. Also, do not pass other signal lines close to this pin or the connected resistor.

(2) The G/Y (Pin 22), R/R-Y (Pin 23), B/B-Y (Pin 24) and SYNC IN (Pin 25) pin input signals are clamped at the inputs using the capacitors connected to each pin, so these signals should be input at sufficiently low impedance.
(Input at an impedance of 1kΩ (max.) or less.)

(3) The smoothing capacitor of the DC level control feedback circuit in the capacitor block connected to the RGB output pins should have a leak current with a small absolute value and variance. Also, when using the pulse elimination (PAL display) function, the picture quality should be thoroughly evaluated before deciding the capacitance value of the capacitor.

(4) A thorough study of whether the capacitor connected to the COM output pin satisfies the LCD panel specifications should be made before deciding the capacitance value.

(5) If this IC is used in connection with a circuit other than an LCD, it may cause that circuit to malfunction depending on the order in which power is supplied to the circuits. Thoroughly study the consequences of using this IC with other circuits before deciding on its use.

(6) Since this IC utilizes a C-MOS structure, it may latch up due to excessive noise or power surge greater than the maximum rating of the I/O pins, or due to interface with the power supply of another circuit, or due to the order in which power is supplied to circuits. Be sure to take measures against the possibility of latch up.

(7) Be sure to observe the power supply and power saving sequence specifications specified for this IC.

(8) Do not apply a voltage higher than V_{DD} or lower than V_{SS} to I/O pins.

(9) Do not use this IC under operating conditions other than those given.

(10) Absolute maximum rating values should not be exceeded even momentarily. Exceeding ratings may damage the device, leading to eventual breakdown.

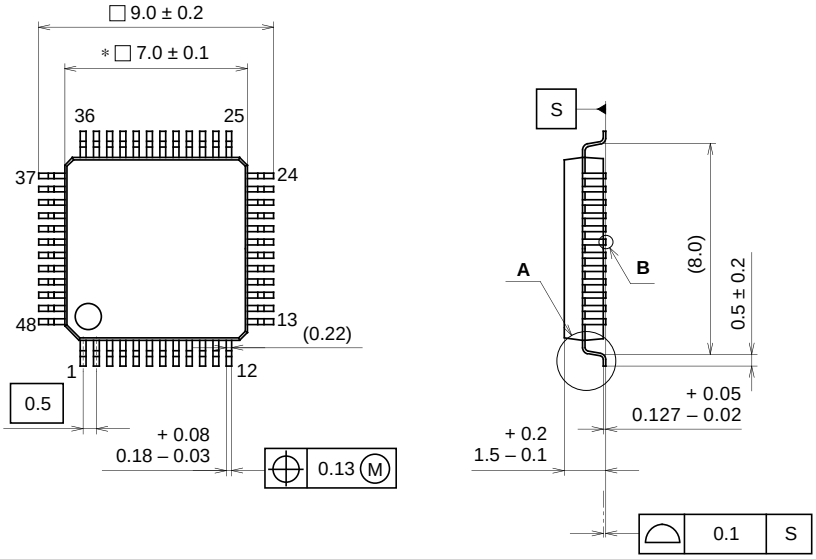
(11) This IC has a MOS structure which is easily damaged by static electricity, so thorough measures should be taken to prevent electrostatic discharge.

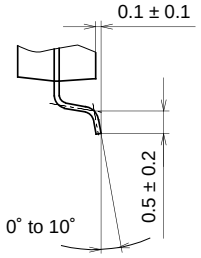
(12) Always connect the V_{SS}, GND1 and GND2 pins to the lowest potential applied to this IC; do not leave these pins open. The voltages applied to the power supply pins should be as follows.
V_{SS} = GND1 = GND2 ≤ V_{DD} = $V_{CC}1$ ≤ $V_{CC}2$.

(13) Be sure to connect the damping resistor of 10Ω to ROUT, GOUT, BOUT, PSIGOUT and COM output.

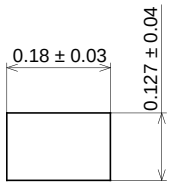
Package Outline Unit: mm

48PIN LQFP (PLASTIC)





DETAIL **A**



DETAIL **B**: PALLADIUM

NOTE: Dimension "∗" does not include mold protrusion.

SONY CODE	LQFP-48P-L01
EIAJ CODE	P-LQFP48-7x7-0.5
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	PALLADIUM PLATING
LEAD MATERIAL	COPPER ALLOY
PACKAGE MASS	0.2g